256 BIT SRAM Memory System Design

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Abstract:
A 256 BIT SRAM system has been designed using 45nm technology such that the parameters like area can be minimized while working at the maximum possible frequency. The individual components are the building blocks of the SRAM so careful consideration of Flip flop, MUX, decoder was given in order to maximize robustness, reduce glitches and area. Read and trip voltages were measured for different pull up, access and pull down sizes. Maximum frequency achieved is 1.5GHz & it works on supply of 780mV.

Keywords: Precharge, Sense amplifier, row and column decoder, Layout.

I. INTRODUCTION

There are multiple types of SRAMs being used now a days like Asynchronous, synchronous, special and non- volatile SRAMs. We have designed a synchronous SRAM. In this the read and write cycles are synchronized with the clock signal so it can be used for fast applications. The address, control and data signals are controlled by the clock signal. Synchronous SRAM is widely used for Cache and other applications requiring burst transfers.

SRAM corresponds with the following components to read, write and store data: Read register, address register, row and column decoder, R/W circuitry.

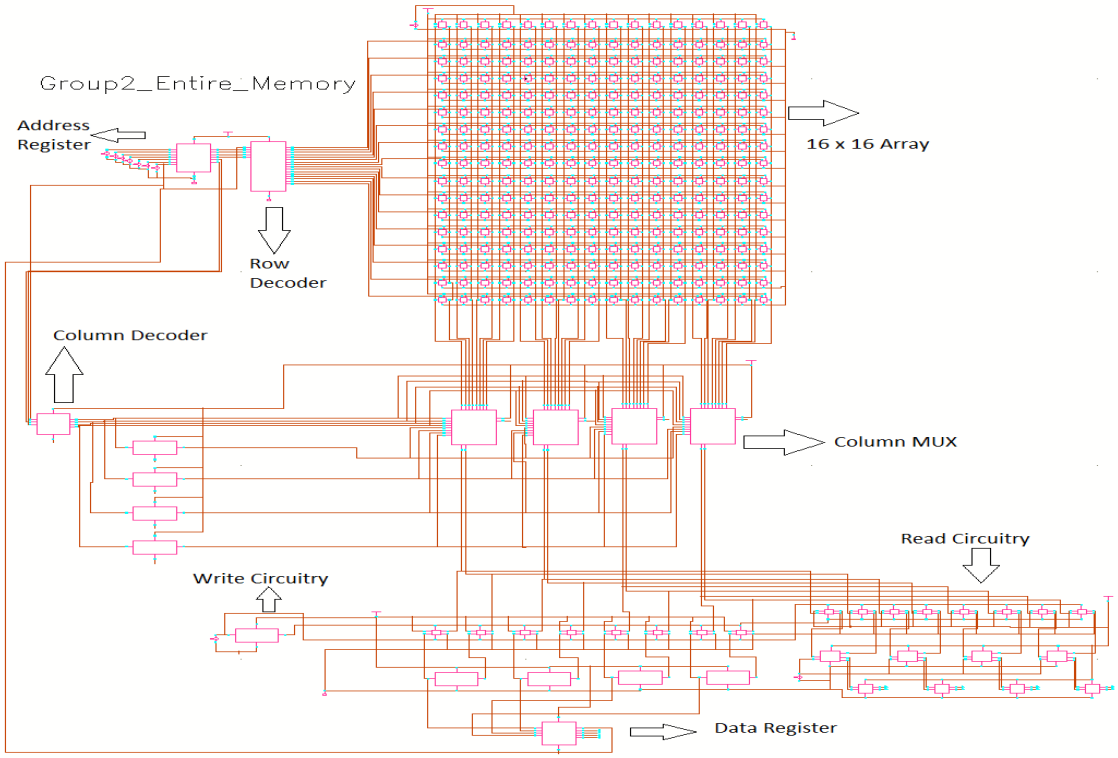

Figure 1: Schematic of SRAM

II. Design components

A. 2:4 Decoder

We used hierarchical approach to design 2 to 4 decoder which forms the building block for 4 to 16 time because only one high output is required at a time. So, in case if NAND gate is used, 4 inverters for 1st stage and 16 inverters for 2nd stage are row decoder. One 2 to 4 decoder is used to drive four 2 to 4 decoders in the second stage. The decoder consists of NOR gate instead of NAND gate as the latter gives logic '1' except when all inputs are logic '1'. So in this the output needs to be inverted every required. This has been reduced by using NOR gate which also leads to less area. Size of PMOS is 550nm and that of NMOS is 400nm in the NOR gate used.

The PMOS and NMOS used in the inverter are of 135nm and 90nm respectively.

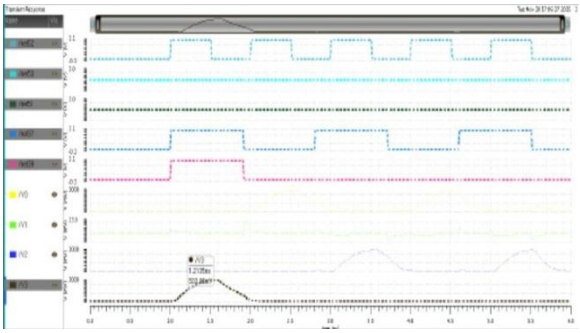

Figure 2: WL generation through decoder (AD0 AD1 AD2 AD3=0011, WL3is 'High')

B. Address & Data Register

A static D flip flop has been designed using C2MOS (NMOS is 450nm and PMOS is 580nm) which has been used has a building block for the address and data registers. It has been chosen over dynamic DFF due to its robustness, given sufficient time, leakage paths may discharge the parasitic capacitance making the flip-flop reach invalid states.

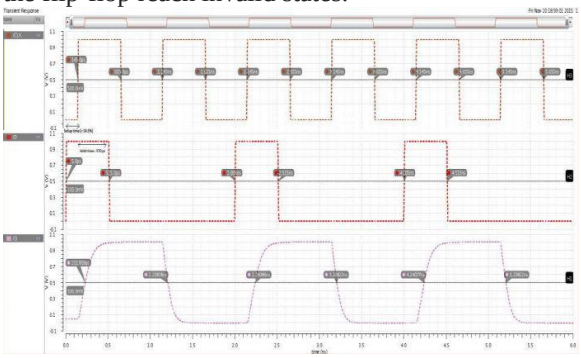

Figure 3: D flip flop waveform

C. Column Multiplexer:

A transmission gate based MUX has been designed due to less number of transistors which reduces the area on chip ultimately. Moreover transmission gate MUX provided us with full swing in the output which reduces the static leakage. Both PMOS and NMOS used are of 90nm.

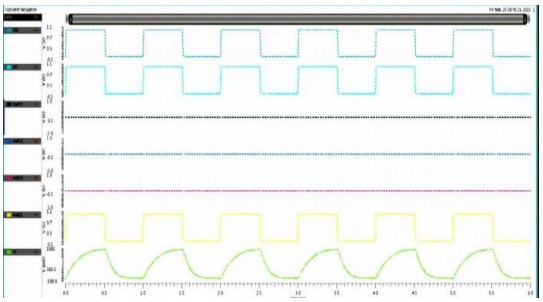

Figure 4: Column Multiplexer

D. Precharge Circuit:

The read operation is done when we precharge both bitlines high, then turn on wordline. One of the bitlines will be pulled down by the cell. All PMOS are 600nm in the precharge circuit.

E. SRAM cell

A 6-T SRAM cell has been used. In this the data is stored in cross coupled inverters. The wordline is raised in order to read and then precharge bit is set. Similarly for write operation, the wordline is raised and then we drive data onto bit. Pull up:Access:Pull down = 90nm:105nm-:05nm.

F. Sense amplifier

This is a part of the read circuitry. It senses the low power signals from a bitline from data bit (0 or 1) stored in a memory cell and amplify the small voltage swing to a level which can be interpreted outside of memory. It has been designed using the cross coupled inverters to produce regenerative feedback. All PMOS and NMOS in this are of 90nm. Output of sense amplifier is fed into the cross coupled NAND latch. The sizing of PMOS for NAND gate is 135nm and that of NMOS is 180nm.

III. SIMULATION RESULT:

The read and write operations of the memory along with the output waveforms can be observed here. The behavior can thus be tested and verified from the waveforms as well.

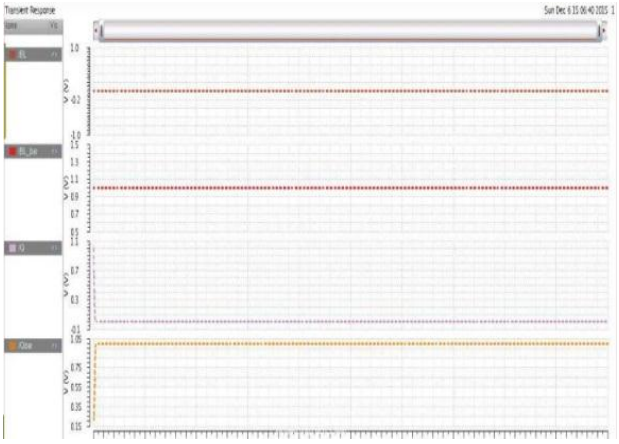

Figure 5: Writing '0' in Memory

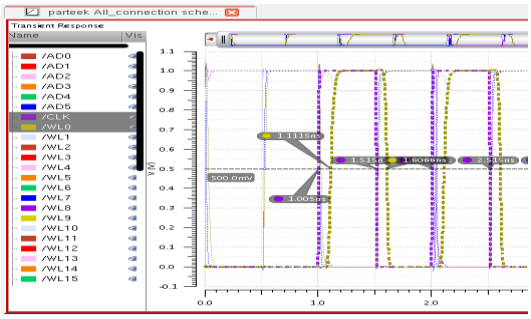

Figure 6: CLK to WL delay

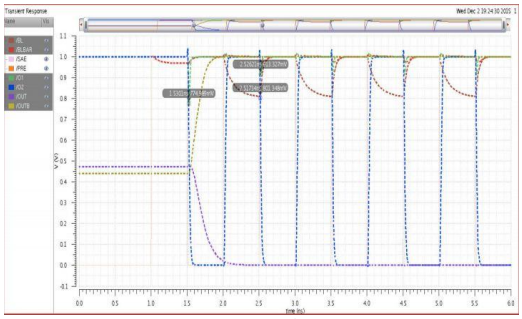

Figure 7: Reading '0' from memory

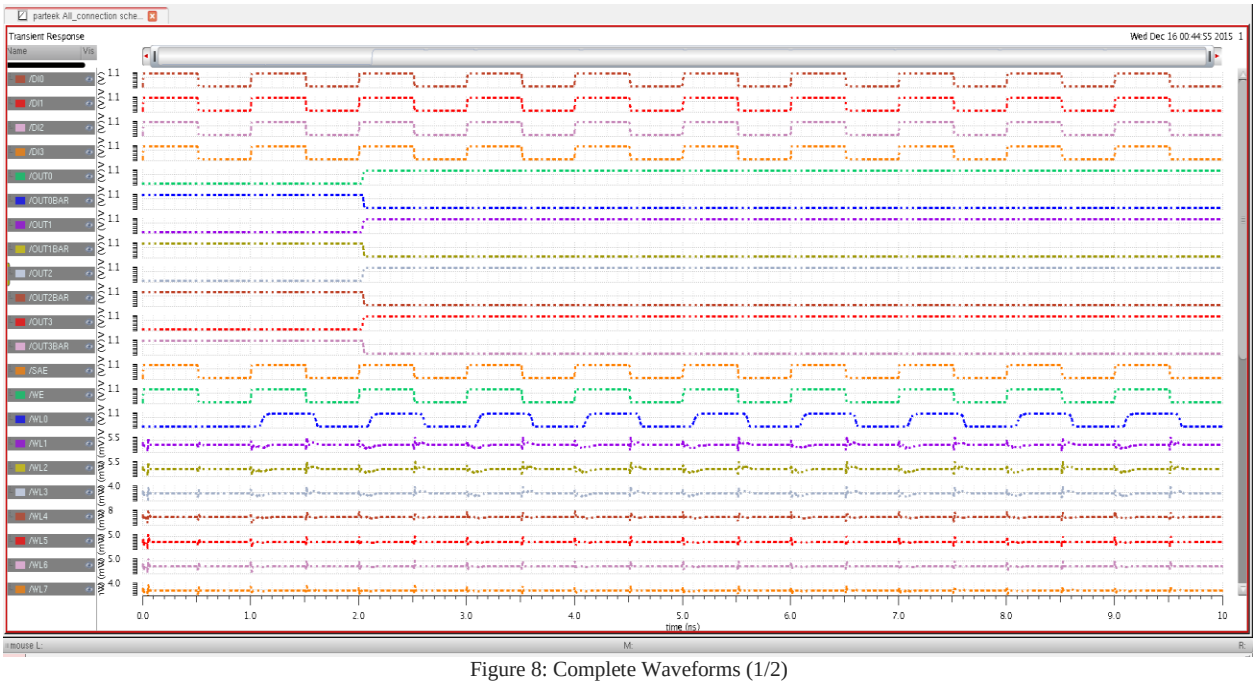

Figure 8: Complete Waveforms (1/2)

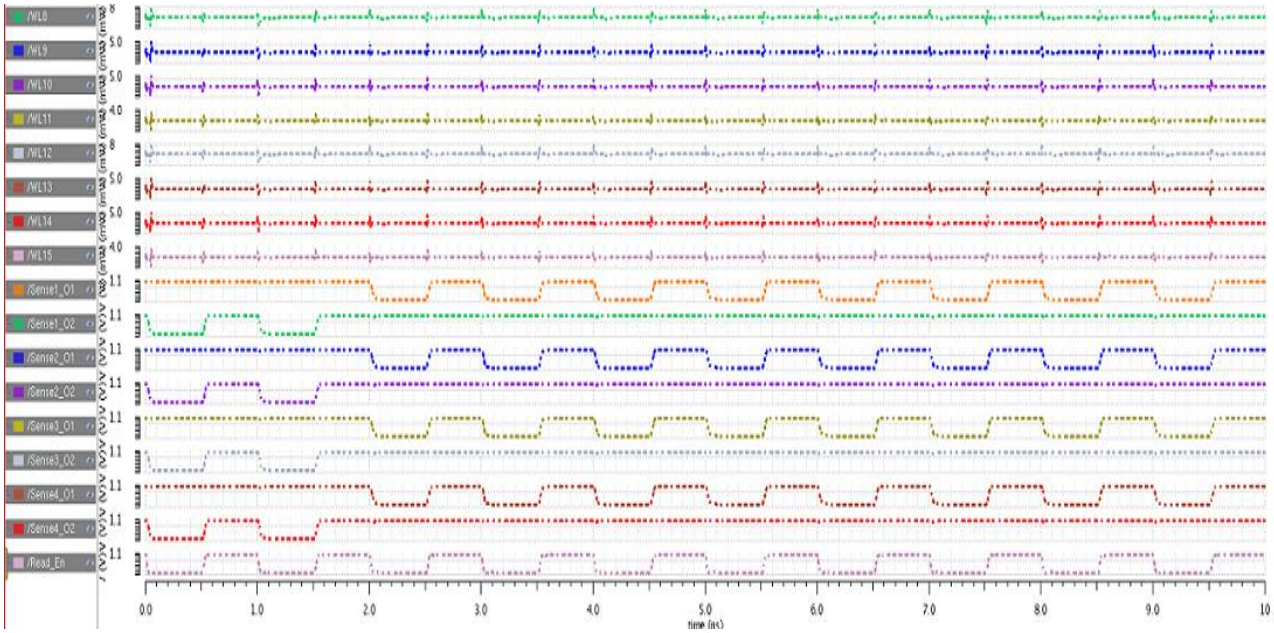

Figure 9: Complete Waveforms (2/2)

IV.LAYOUT

The layout of the SRAM cell has been designed keeping in mind the area. Metal 1 is used to make connections between the cross coupled inverters and word line. Metal 2 is used for connecting access transistors with the inverters. Metal 3 has been used for bitline and bitline bar connections. For vdd and gnd (constant supplies) higher metal (metal 4) has been used due to lower resistivity.

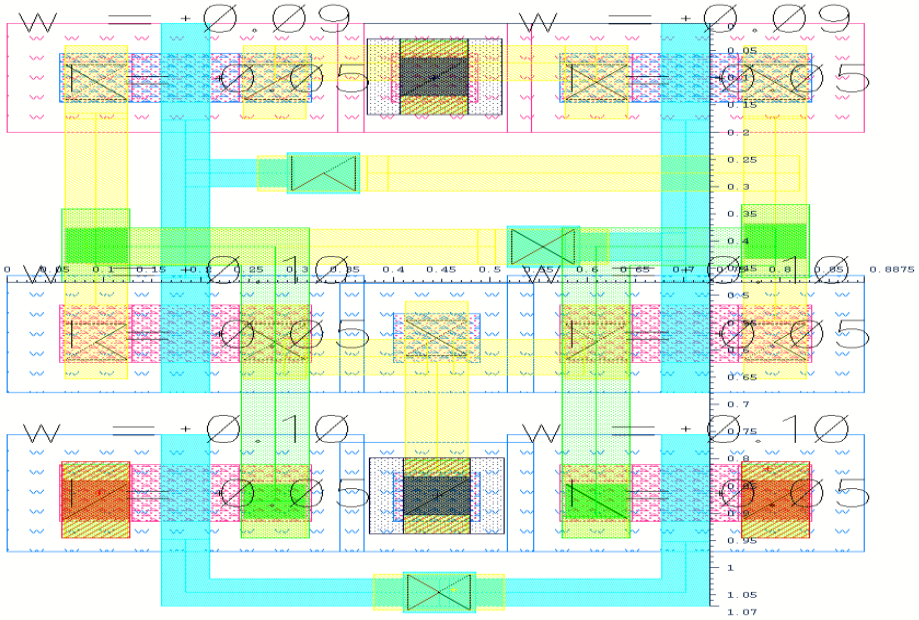

Figure 10: Layout of Cell

Table 1: Performance Metric Table

Read Margin	23%
Write Margin	41.9%
CLK to Q delay	86.9ps (8.69%)
Optimized cell area	0.9496μm^2
Glitches	8mV
CLK to WL delay	160ps (10.6%)
Maximum frequency	1.5GHz
Minimum supply voltage	780mV
Delta bit (bit line- bit line bar)	102.8mV

CONCLUSION

A 256 BIT SRAM has been designed along with the sketch of the layout. The operation has been tested for a clock frequency of 1.5 GHz and supply voltage as low as 780mV but it increases the clock to wl delay from 10.6% to 14% and it works as expected. The glitches are found to be 6mV.

FUTURESCOPE

Post layout simulation after adding the internal capacitances (parasitic) can be done in order to check the variation of the output with respect to internal capacitances. The designed system can be further improved by precise timing of SRAM control signals. Pulse generation building blocks can be implemented for high stability and low power dissipation. Read and Write margins can be further improved by using read and write assistive circuits.

ACKNOWLEDGEMENT

We would like to thank our Professor Shaloo Rakheja for her constant efforts in motivating us in order to accomplish 256bit SRAM, to make us aware of the mistakes and improve upon them. We would also like to thank our fellow classmates to constantly discuss the concepts and to help us stay on the right track.

CADENCE USER CREDENTIALS AND PATH

Varun Sharma Net ID- vs1638 N Number- N15177570
Path: vs1638/cadence/SRAM
All relevant files are in this library

REFERENCES:

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