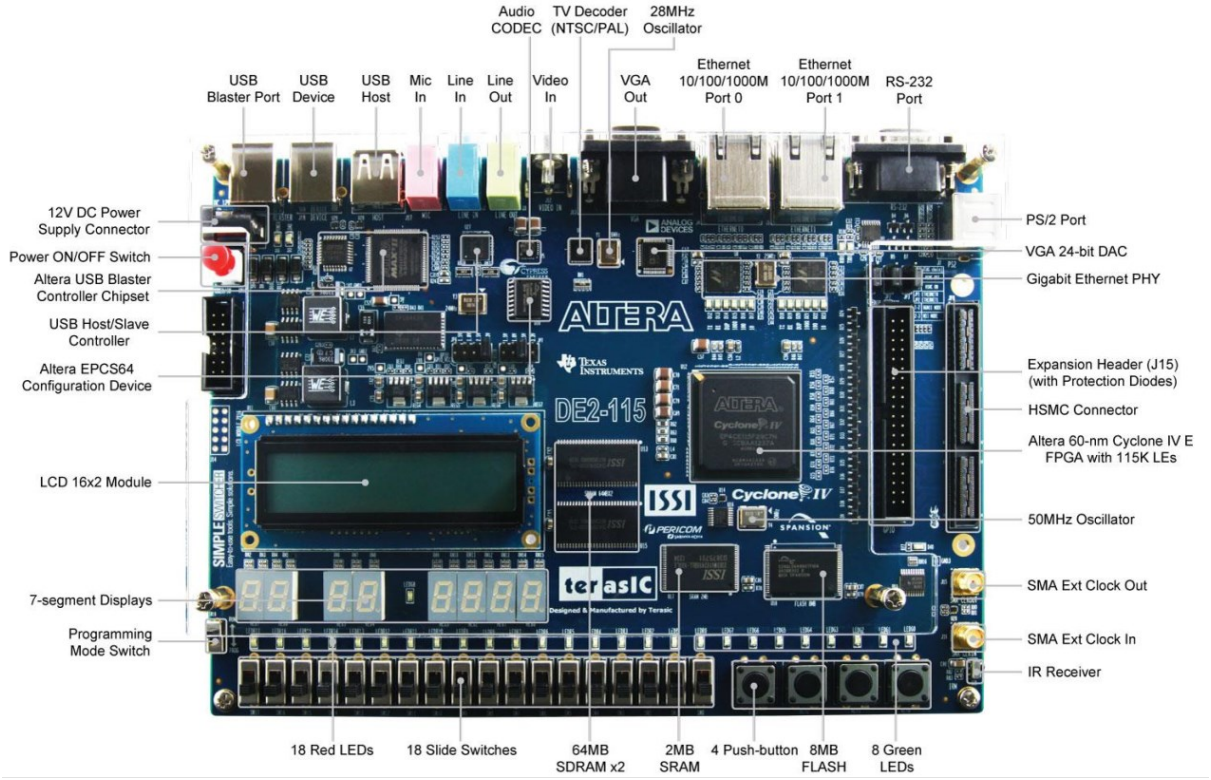
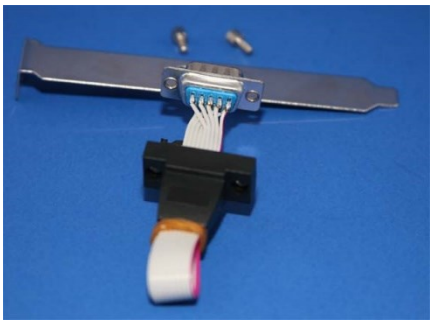
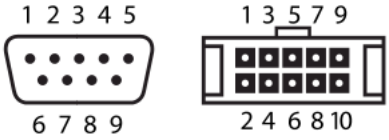
(CLONE) NES GAMEPAD NA DE2-115





Pinout for NES clone (db9) gamepads

```
        +---------> Clock
        | +-------> Latch
        | | +-----> Data
        | | |
   ____________
 5 \ x o o o x / 1
    \ x o x o /
   9 `~~~~~~~' 6
        |   |
        |   +----> Power
        +--------> Ground
```



DB-9		IDC-10
pin 1	⟷	pin 1
pin 2	⟷	pin 2
pin 3	⟷	pin 3
pin 4	⟷	pin 4
pin 5	⟷	pin 5
pin 6	⟷	pin 6
pin 7	⟷	pin 7
pin 8	⟷	pin 8
pin 9	⟷	pin 9
NC	⟷	pin 10

*NC = Not Connected

JOY1

IDC10/DB9 ➔ GPIO @de2-115
2-DATA ➔ GPIO_27 (AE24)
3-LATCH ➔ GPIO_29 (AF26)
4-CLOCK ➔ GPIO_31 (AG23)
6-VCC ➔ 3V3
8-GND ➔ GND

JOY2

IDC10/DB9 ➔ GPIO @de2-115
2-DATA ➔ GPIO_33 (AH26)
3-LATCH ➔ GPIO_35 (AG26)
4-CLOCK ➔ GPIO_34 (AH23)
6-VCC ➔ 3V3
8-GND ➔ GND

ZX KEYB

8-pin con ➔ GPIO_11-GPIO_25 (right/odd)
5-pin con ➔ GPIO_1-GPIO_9 (right/odd)

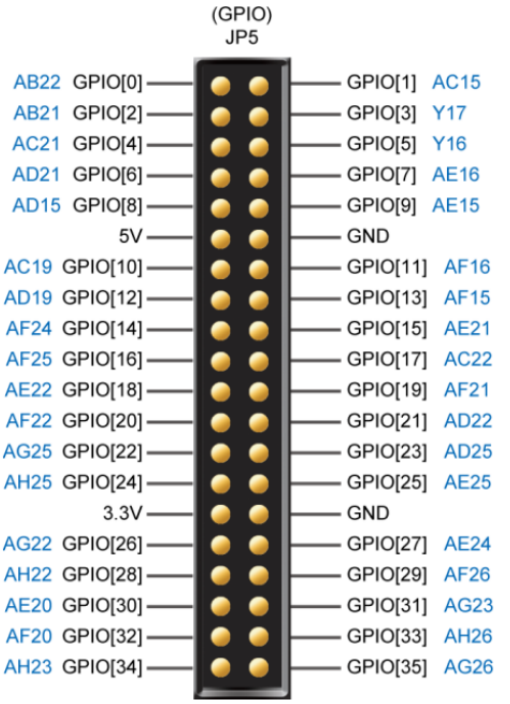
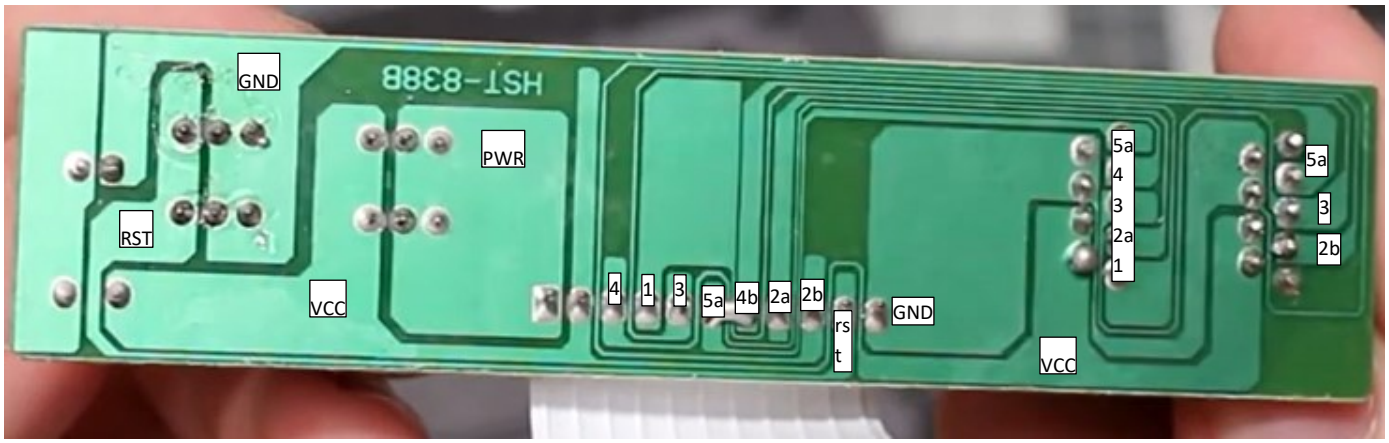
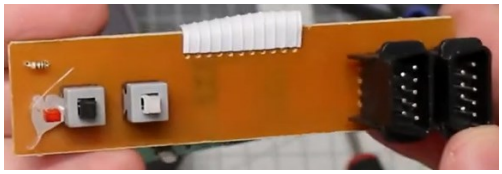


Figure 4-15 GPIO Pin Arrangement

Reverse engineering à placa da consola NES clonada – onde ligam estes comandos





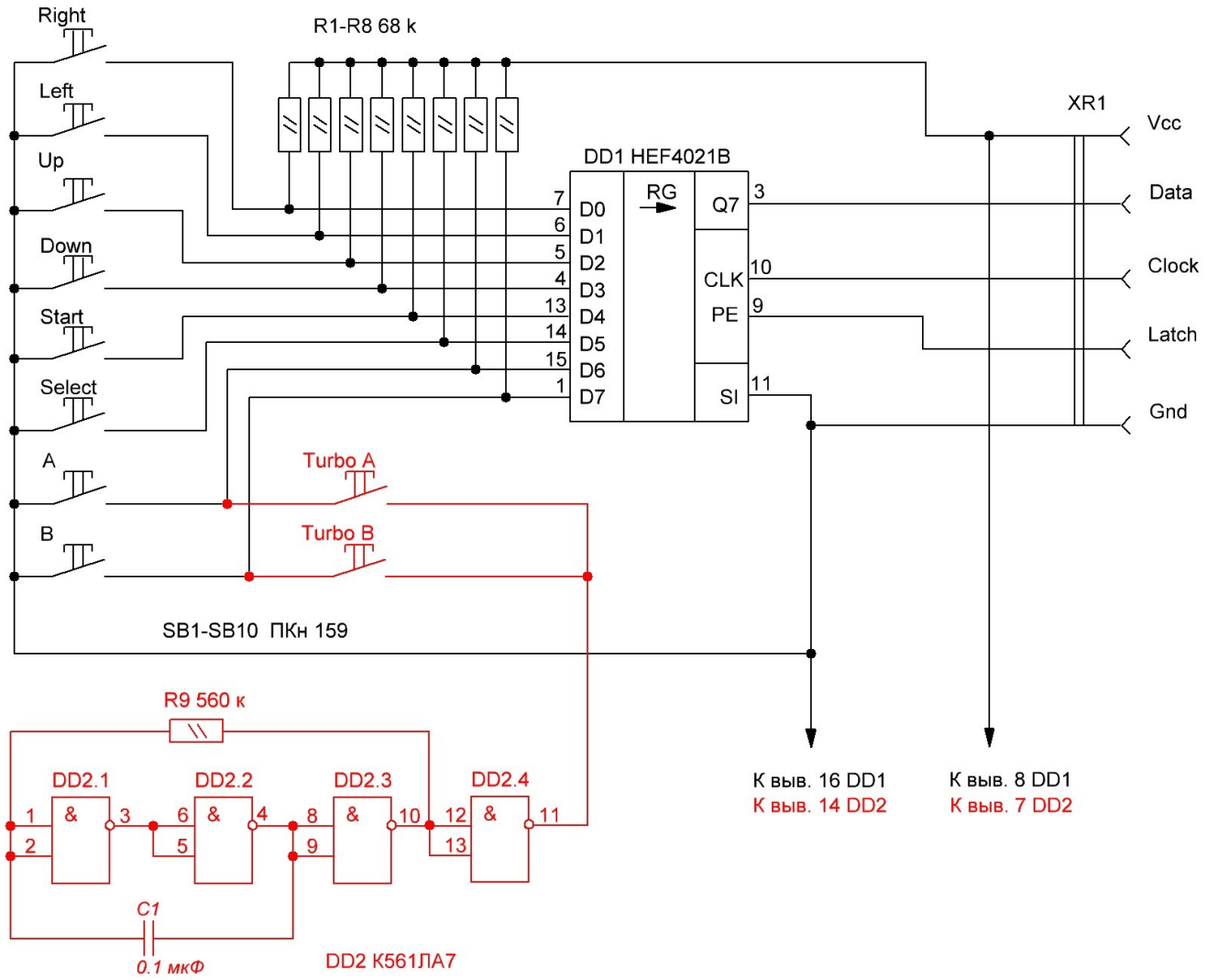
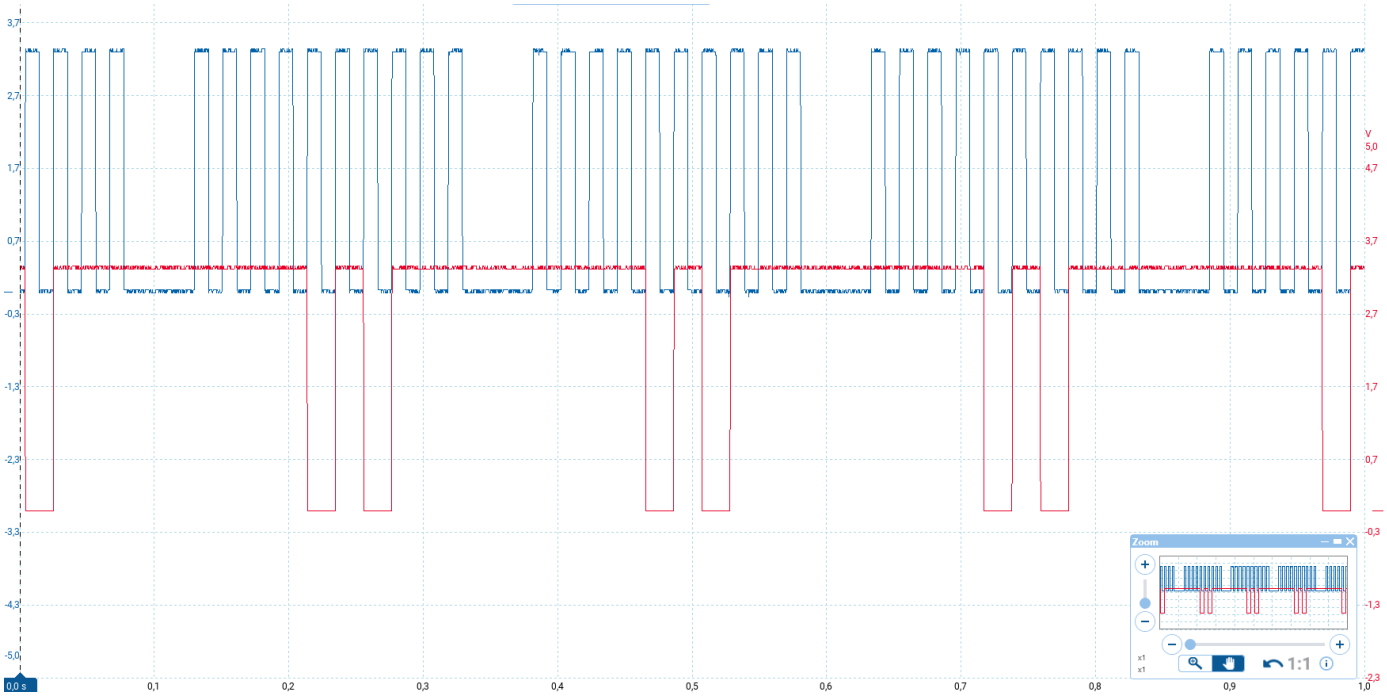


Рис. 6

VCC=3-15V



DOWN + RIGHT pressed (led5 e led7)

tem clocks extra a serem enviados (lê 0s). Atenção que a saída do Shift-register está ligada a Q7 (ver datasheet) o que significa que assim que é feito o parallel-load (latch) a saída de dados fica com o valor do bit 7 (botão A)

```
--
-- clk    _______|  |__|  |__|  |__|  |__|  |__|  |__|  |__|  |__|  |_________|  |__|  |___...
--
-- latch  _|  |_____________________________________________________|  |_______________...
--
-- data   __|  A  |  B  | STR | SEL | UP  |DOWN |LEFT |RIGHT|_____|  A  |  B  | STR ...
--
--    bit: 7  6  5  4  3  2  1  0
-- output: R  L  D  U  E  T  B  A
```

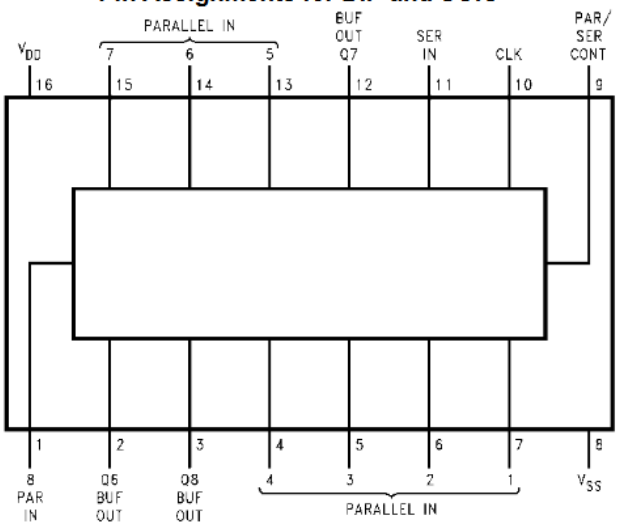
NOTA: recepção dos botões com posição trocada (little-endian) em relação ao circuito (big-endian).

Order Number	Order Code	Package Description
CD4021BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow Body
CD4021BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



Top View

Truth Table

CL (Note 1)	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n (Note 2)
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
⌐	0	0	X	X	0	Q_{n-1}
⌐	1	0	X	X	1	Q_{n-1}
⌙	X	0	X	X	Q1	Q_n

X = Don't care case

Note 1: Level change

Note 2: No change

REFs:

https://pt.aliexpress.com/item/32919127872.html

https://assets.nexperia.com/documents/data-sheet/HEF4021B.pdf