Lab2-1.

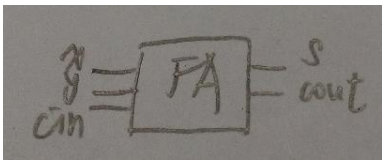
1. Design Specification

1-bit full adder

Input : x, y, cin

Output : s, cout

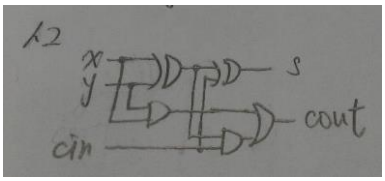
s + cout = x + y + cin



2. Design Implementation

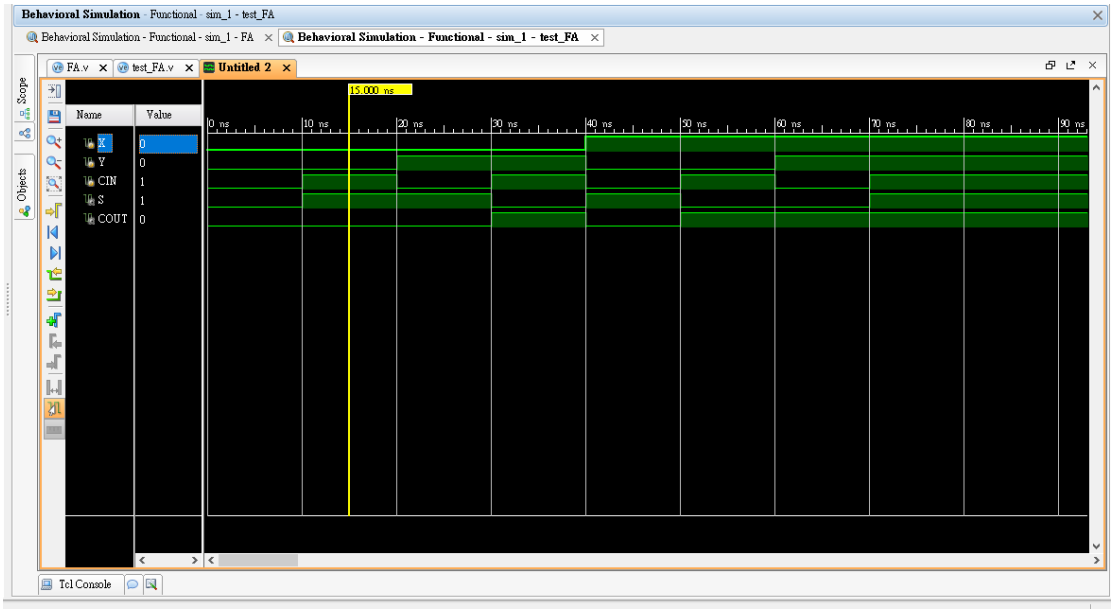
s = x ^ y ^ cin

cout = xy + (x ^ y)cin (xy : carry generate, x^y : carry generate)



I/O	x	y	cin	s	cout
Pin	V17	V16	W16	U16	E19

3. Stimulation



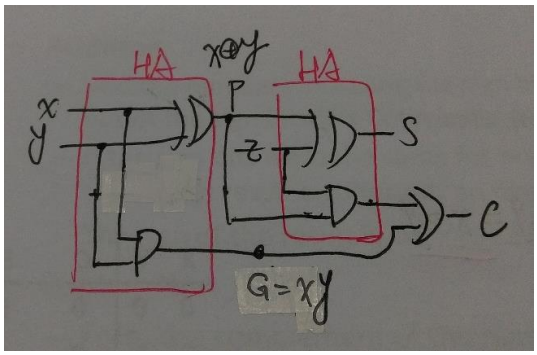
x	y	cin	s	cout
0	0	0	0	0
0	0	1	1	0

0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. References

Logic Design – Lecture 6 Arithmetic Circuits

It can also implement by half adder and other logic gates



Lab2-2

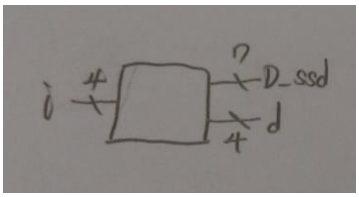
1. **Design Specification**

   7-segment display decoder

   Input : i[3:0]

   Output : D_ssd[7:0], d[3:0]

   i are binary number, D_ssd are 7-segment display, d are four LEDs to monitor the input.



2. **Design Implementation**

   8’b00000011 represent 0

   8’b10011111 represent 1

   8’b00100101 represent 2

   8’b00001101 represent 3

   8’b10011001 represent 4

   8’b01001001 represent 5

   8’b01000001 represent 6

   8’b00011111 represent 7

   8’b00000001 represent 8

   8’b00001001 represent 9

   8’b01110001 represent F

   case(i)

   0: 8’b00000011

   1: 8’b10011111

   2: 8’b00100101

   3: 8’b00001101

   4: 8’b10011001

   5: 8’b01001001

   6: 8’b01000001

   7: 8’b00011111

   8: 8’b00000001

   9: 8’b00001001

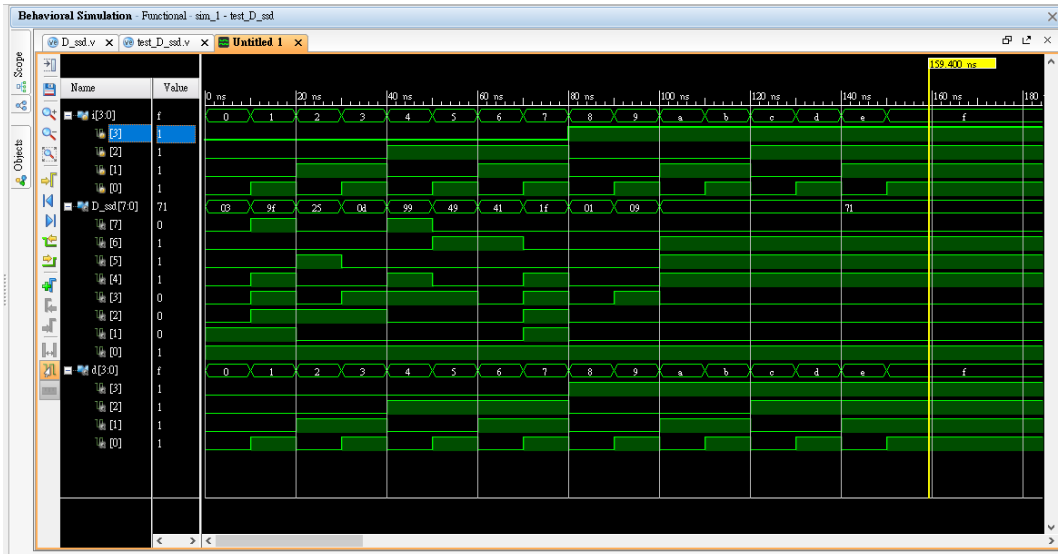
   Default: 8’b01110001

d = i

I/O	I[3]	I[2]	I[1]	I[0]	D[3]	D[2]	D[1]	D[0]
Pin	W17	W16	V16	V17	V19	U19	E19	U16

I/O	D_ssd[7]	D_ssd[6]	D_ssd[5]	D_ssd[4]	D_ssd[3]	D_ssd[2]	D_ssd[1]	D_ssd[0]
Pin	V7	U7	V5	U5	V8	U8	W6	W7

3. Stimulation



i	D_ssd	d
0000(0)	8’b00000011(0)	0000(0)
0001(1)	8’b10011111(1)	0001(1)
0010(2)	8’b00100101(2)	0010(2)
0011(3)	8’b00001101(3)	0011(3)
0100(4)	8’b10011001(4)	0100(4)
0101(5)	8’b01001001(5)	0101(5)
0110(6)	8’b01000001(6)	0110(6)
0111(7)	8’b00011111(7)	0111(7)
1000(8)	8’b00000001(8)	1000(8)
1001(9)	8’b00001001(9)	1001(9)
1010(10)	8’b01110001(F)	1010(10)
1011(11)	8’b01110001(F)	1011(11)
1100(12)	8’b01110001(F)	1100(12)
1101(13)	8’b01110001(F)	1101(13)
1110(14)	8’b01110001(F)	1110(14)
1111(15)	8’b01110001(F)	1111(15)

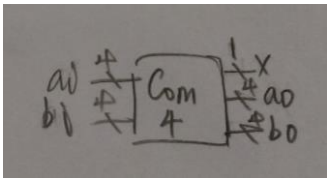
Lab2-3

1. Design Specification

4 bits comparator

If(a≤b), x = 0

If(a>b), x = 1



2. Design Implementation

If(ai≤bi)

x = 0

else

x = 1

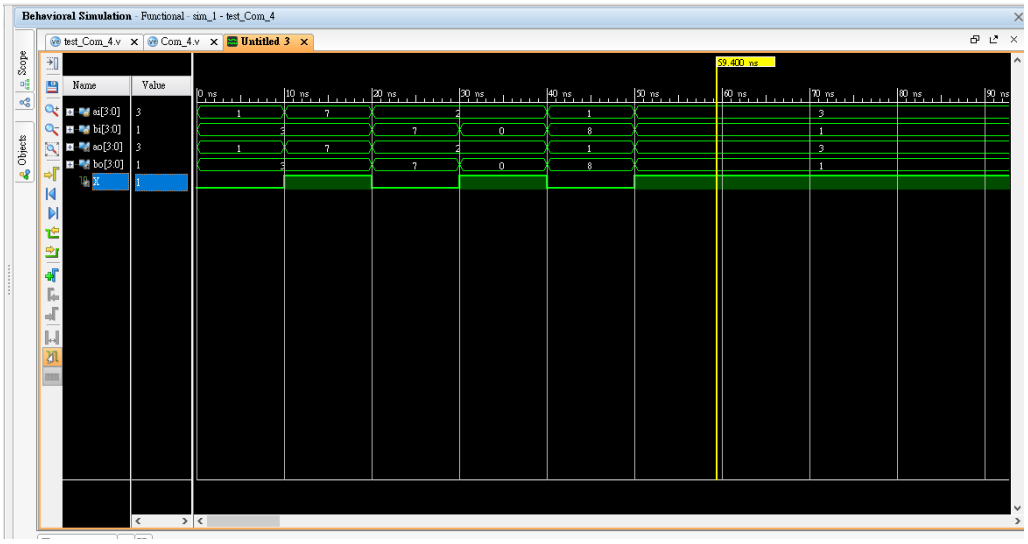
ao = ai

bo = bi

I/O	Ai[3]	Ai[2]	Ai[1]	Ai[0]	Bi[3]	Bi[2]	Bi[1]	Bi[0]
Pin	W13	W14	V15	W15	W17	W16	V16	V17

I/O	Ao[3]	Ai[2]	Ai[1]	Ai[0]	Bi[3]	Bi[2]	Bi[1]	Bi[0]	X
Pin	V14	U14	U15	W18	V19	U19	E19	U16	V13

3. Stimulation



ai	bi	ao	bo	x
0001(1)	0011(3)	0001(1)	0011(3)	0
0111(7)	0011(3)	0111(7)	0011(3)	1
0010(2)	0111(7)	0010(2)	0111(7)	0
0010(2)	0000(0)	0010(2)	0000(0)	1
0001(1)	1000(8)	0001(1)	1000(8)	0
0011(3)	0001(1)	0011(3)	0001(1)	1