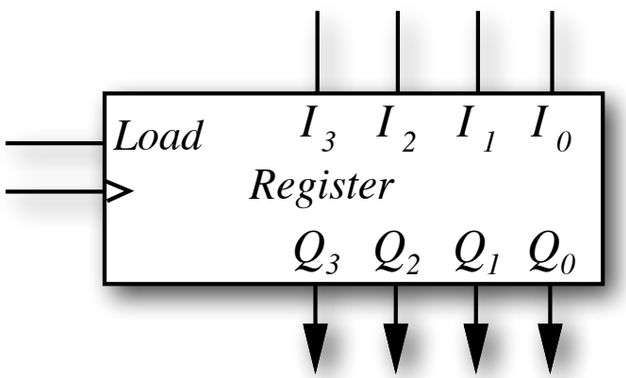
4-bit Register with Parallel Load (1/2)

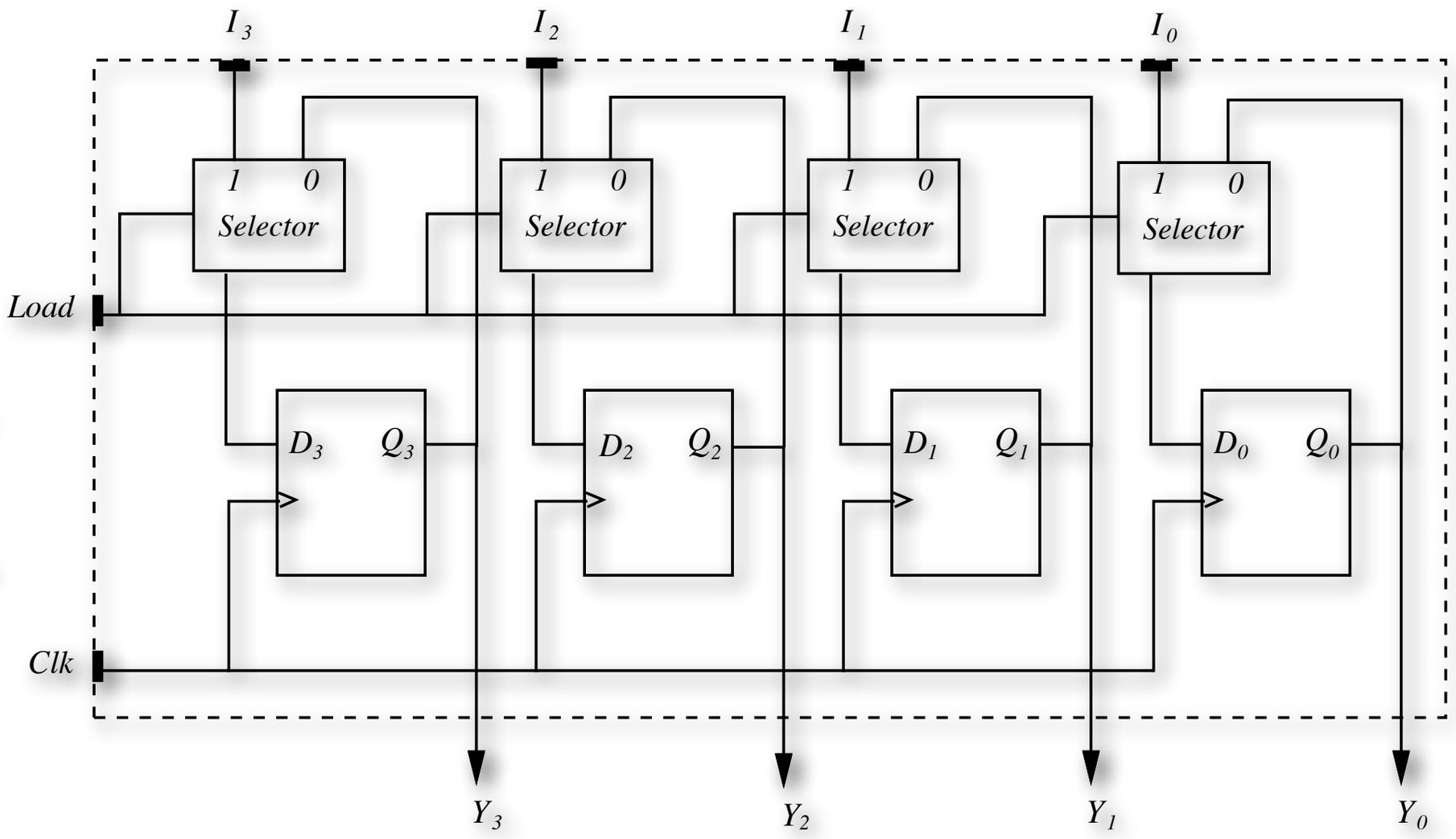
- To control *when* the data will be entered into a register, and for *how long* it will be stored before being sent to the output



graphic symbol

Present state Load	Next state Q_3 Q_2 Q_1 Q_0
0	No change
1	I_3 I_2 I_1 I_0

operation table



register schematic