Prelab3.

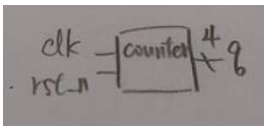
1. **Design Specification**

   4-bit synchronous binary up counter

   Input : clk, ret_n

   Output : q

   Q will count 0 to 15

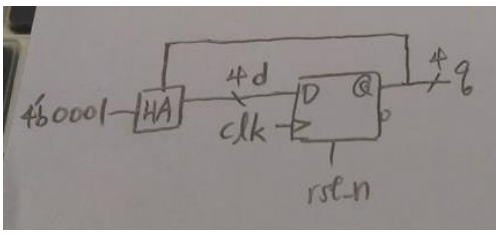


2. **Design Implementation**

   D = q + 1

   @(negedge rst_n), q = 4'b0000

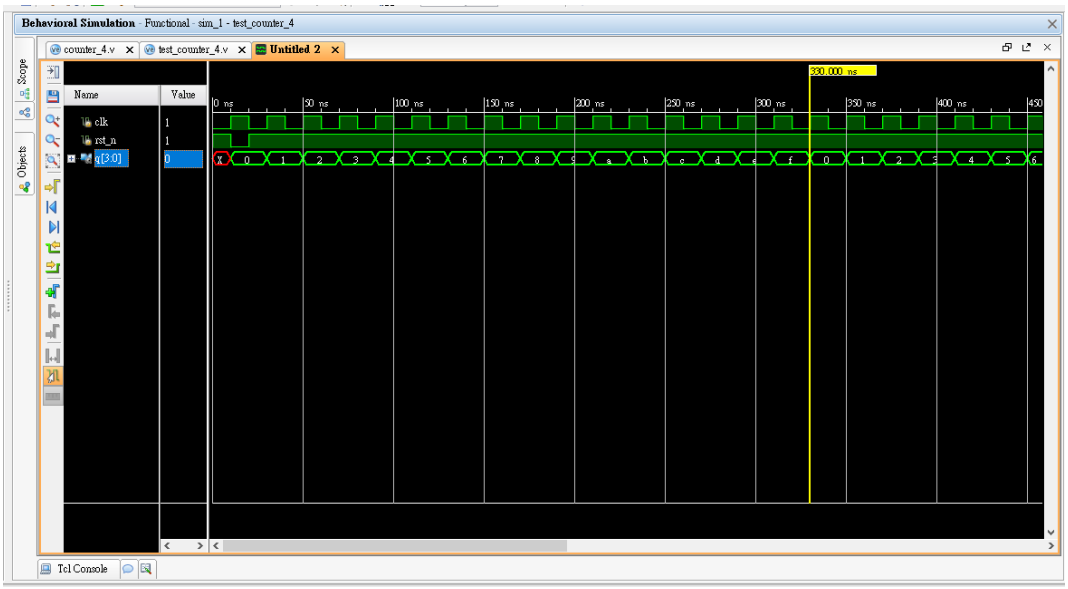
   @(posedge clk), q = d



   D flip-flop with reset

```
always @(posedge clk or negedge rst_n)
    begin
        if(rst_n == 0)
            q <= 4'b0000;
        else
            q <= d;
    end
```

3. **simulation**



clk	Rst_n	q
0	**1**	**X**
1	**0**	**0**
0	**1**	**0**
1	**1**	**1**
0	**1**	**1**
1	**1**	**2**
0	**1**	**2**
1	**1**	**3**
0	**1**	**3**
1	**1**	**4**
0	**1**	**4**
1	**1**	**5**
0	**1**	**5**
1	**1**	**6**
0	**1**	**6**
1	**1**	**7**
0	**1**	**7**
1	**1**	**8**
0	**1**	**8**
1	**1**	**9**
0	**1**	**9**
1	**1**	**10**
0	**1**	**10**
1	**1**	**11**

0	**1**	**11**
1	**1**	**12**
0	**1**	**12**
1	**1**	**13**
0	**1**	**13**
1	**1**	**14**
0	**1**	**14**
1	**1**	**15**
0	**1**	**15**
1	**1**	**0**