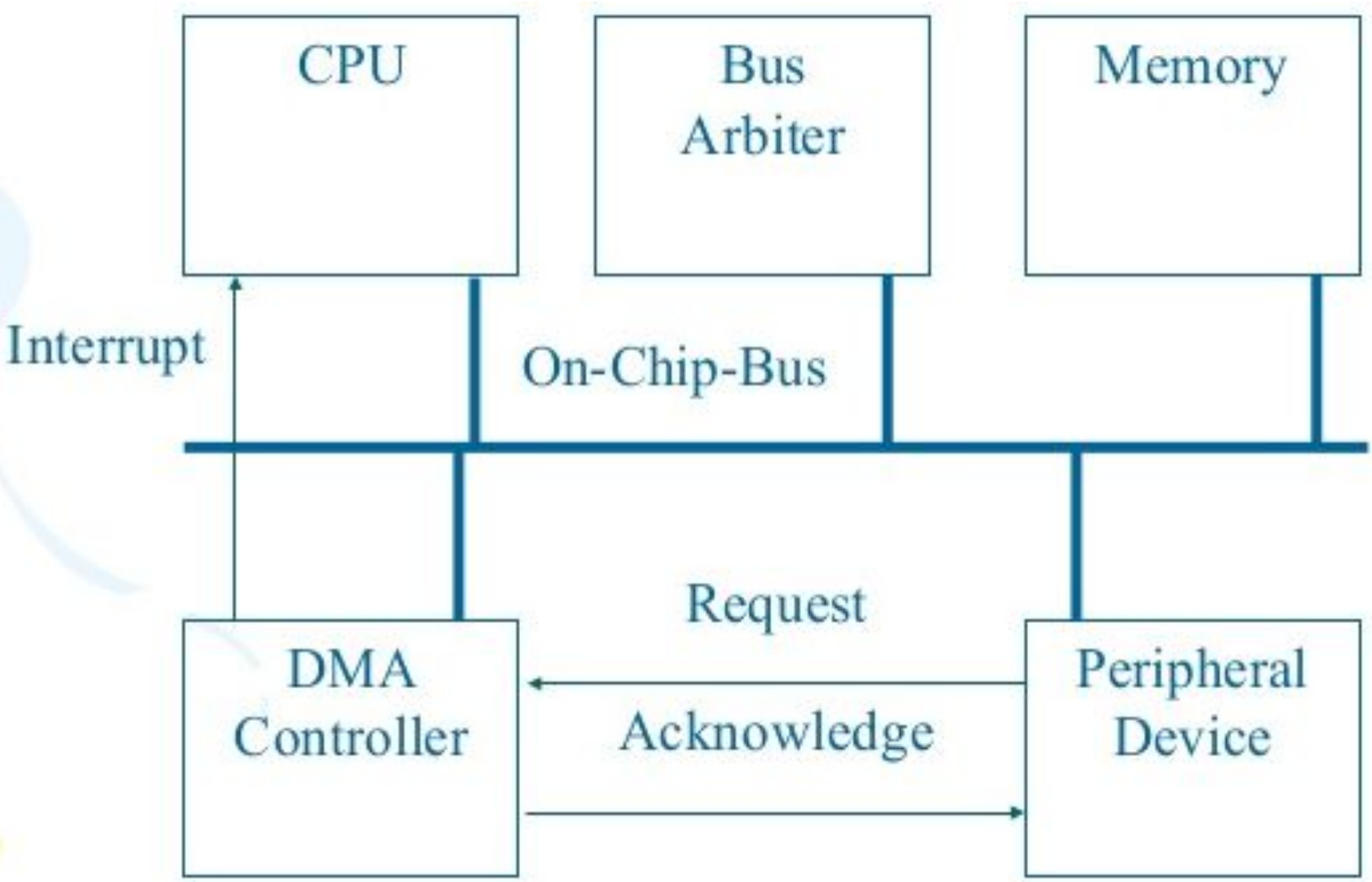
DMA AND 8237 DMA CONTROLLER

DMA CONTROLLER



DMA CONTROLLER

- The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.

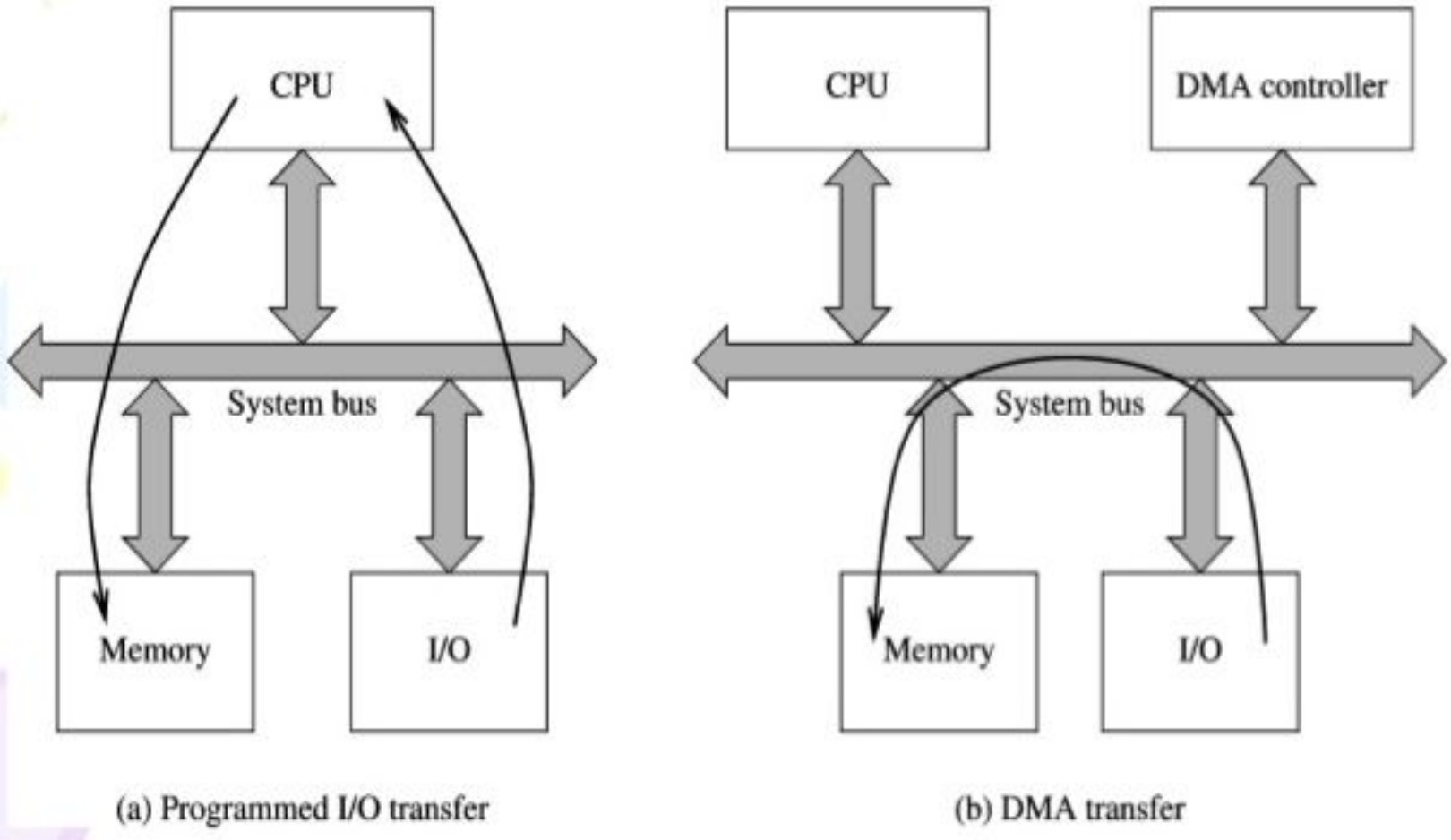
- *DMA controller*: dedicated hardware used for controlling the DMA operation

- A DMA controller temporarily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly between an I/O port and a series of memory locations.

DMA CONTROLLER

- The DMA transfer is also used to do high-speed memory-to memory transfers.
- Two control signals are used to request and acknowledge a DMA transfer in the microprocessor-based system.
- The HOLD signal is a bus request signal which asks the microprocessor to release control of the buses after the current bus cycle.
- The HLDA signal is a bus grant signal which indicates that the microprocessor has indeed released control of its buses by placing the buses at their high-impedance states.

DMA CONTROLLER

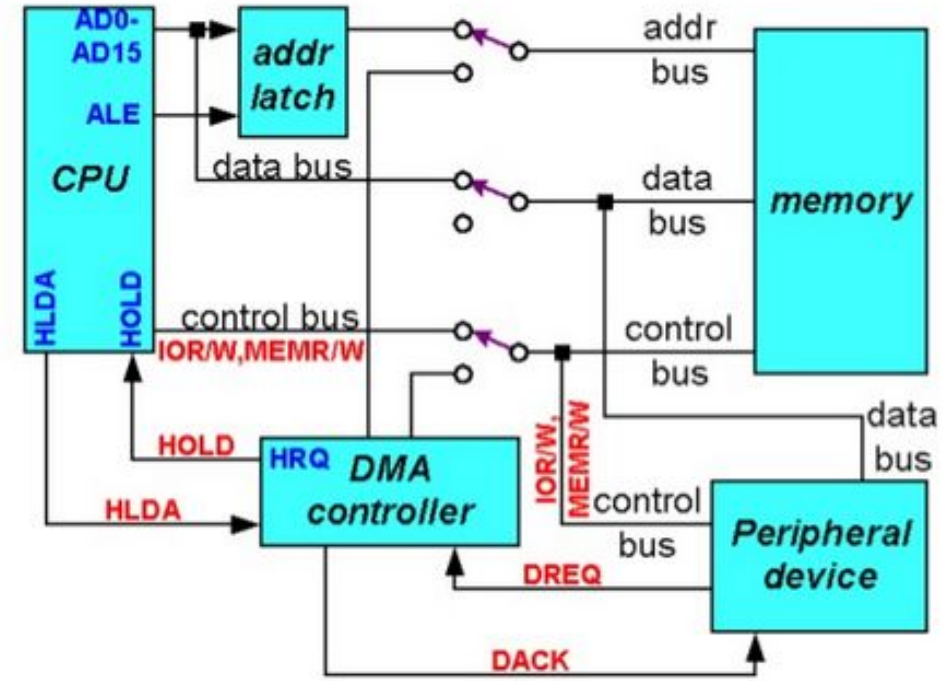


- Direct Memory Address normally occurs between an I/O Device and Memory without use of processor.
- **DMA READ** transfers data from memory to I/O Device
- **DMA WRITE** transfers data from I/O Device

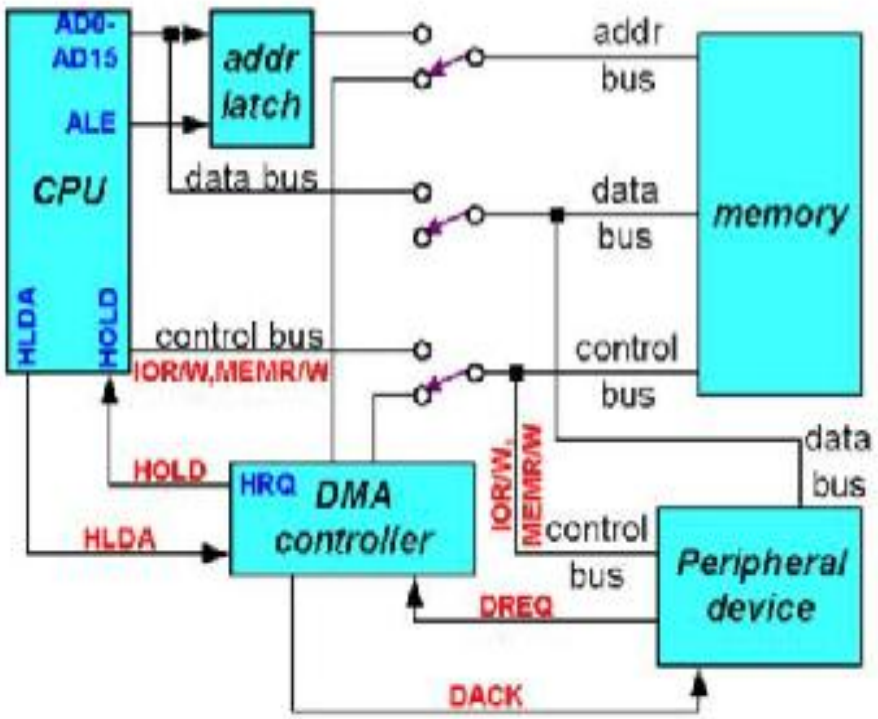
to memory.

- 8237 supplies separate memory and I/O control signals.
- DMA Controller provides memory with its address and controller signals to select the I/O device during DMA transfer

CPU HAVING CONTROL OVER THE BUS



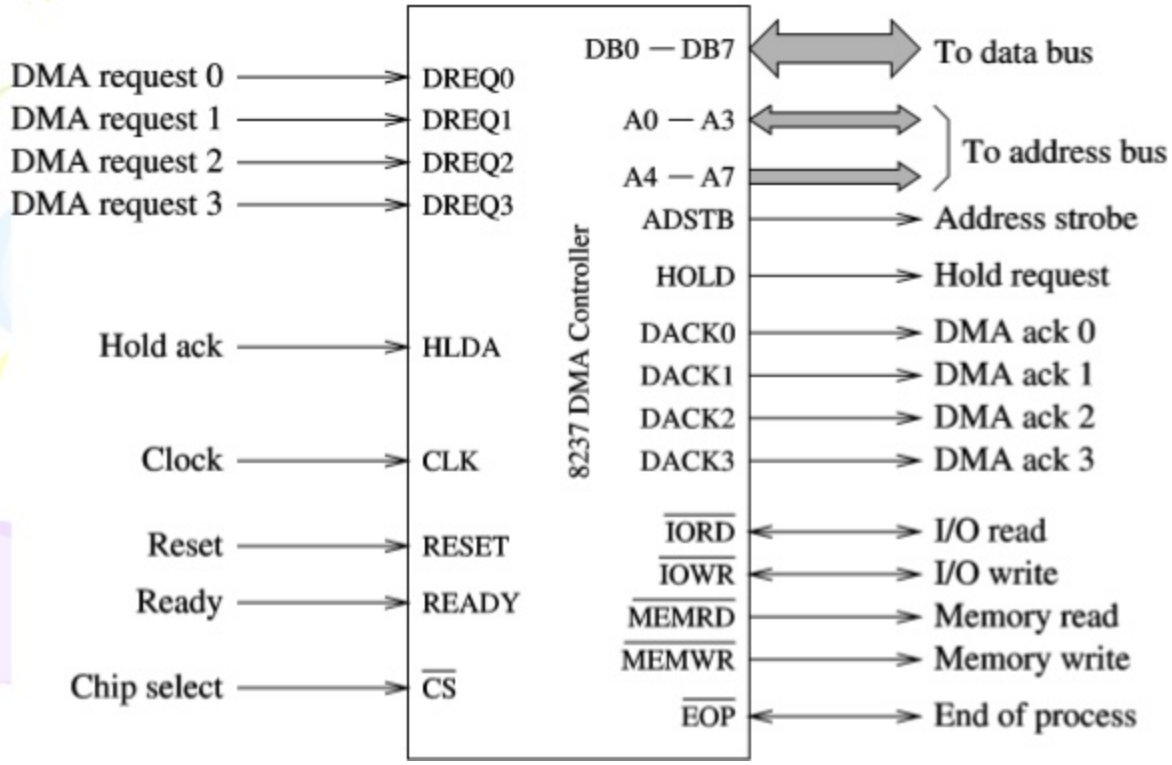
When DMA operates:



PROGRAMMABLE DMA CONTROLLER 8237

- The 8237 is a four-channel device that can be expanded to include any number of DMA channel inputs.
- The 8237 is capable of DMA transfers at rates of up to 1.6 M Byte per second.
- Each channel is capable of addressing a full 64k-byte section of memory and can transfer up to 64k bytes with a single programming.

8237 DMA controller



8237

DACK0–DACK3	O	**DMA ACKNOWLEDGE:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**ADDRESS ENABLE:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**ADDRESS STROBE:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.
$\overline{\text{MEMR}}$	O	**MEMORY READ:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{\text{MEMW}}$	O	**MEMORY WRITE:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
PIN5	I	**PIN5:** This pin should always be at a logic HIGH level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended however, that PIN5 be connected to V_{CC}.

8237

Symbol	Type	Name and Function
V_{CC}		**POWER:** + 5V supply.
V_{SS}		**GROUND:** Ground.
CLK	I	**CLOCK INPUT:** Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 5 MHz for the 8237A-5.
$\overline{CS}$	I	**CHIP SELECT:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	**RESET:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**READY:** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.

8237

HLDA	I	**HOLD ACKNOWLEDGE:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0–DREQ3	I	**DMA REQUEST:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0–DB7	I/O	**DATA BUS:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
$\overline{IOR}$	I/O	**I/O READ:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	I/O	**I/O WRITE:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.

8237

Symbol	Type	Name and Function
$\overline{EOP}$	I/O	**END OF PROCESS:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ line. The reception of $\overline{EOP}$, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
A0–A3	I/O	**ADDRESS:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4–A7	O	**ADDRESS:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**HOLD REQUEST:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.

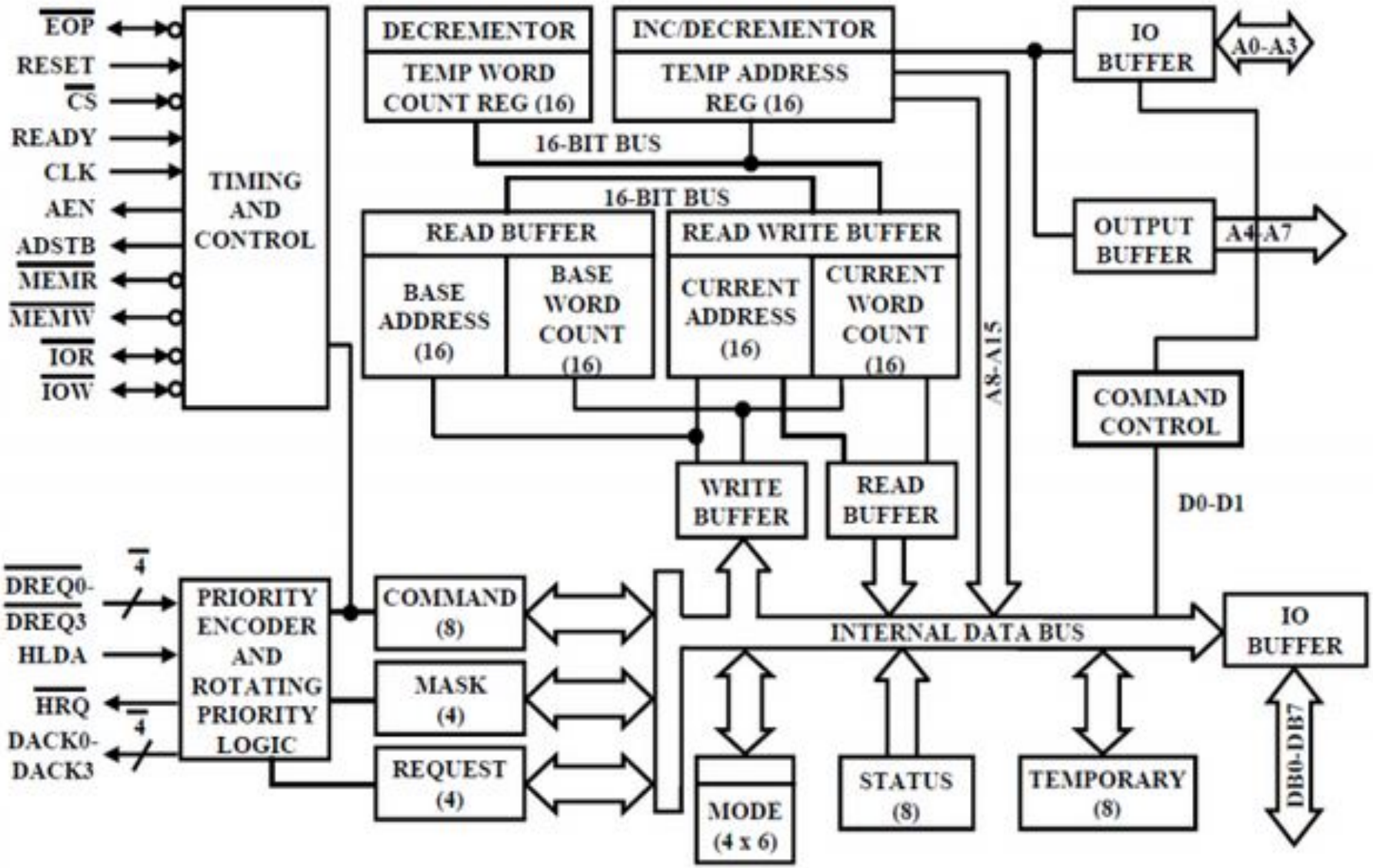
DMA OPERATION

- DMA OPERATION The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles.
- IDLE CYCLE When no channel is requesting service, the 8237A will enter the Idle cycle. In this cycle the 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service
- ACTIVE CYCLE When 8237 is in idle cycle and unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

MODES OF 8237

- The 8237 operates in four different modes, depending upon the number of bytes transferred per cycle and number of ICs used.
- **Single -** The device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer.
- **Block** - Transfer progresses until the word count reaches zero or the EOP signal goes active.
- **Demand** - Transfers continue until TC or EOP goes active or DRQ goes inactive. The CPU is permitted to use the bus when no transfer is requested.
- **Cascade** - Used to cascade additional DMA controllers. DREQ and DACK is matched with HRQ and HLDA from the next chip to establish a priority chain.

BLOCK DIAGRAM OF 8237



BLOCK DIAGRAM OF 8237

- The 8237A block diagram includes three basic blocks of control logic and all of the internal registers.

- **The Timing Control block** generates internal timing and external control signals.
- **The Program Command Control block** decodes the various commands given to the 8237 by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word to select the type of DMA operation during the servicing.
- **The Priority Encoder block** resolves priority contention between DMA channels requesting service simultaneously.

INTERNAL REGISTERS OF 8237

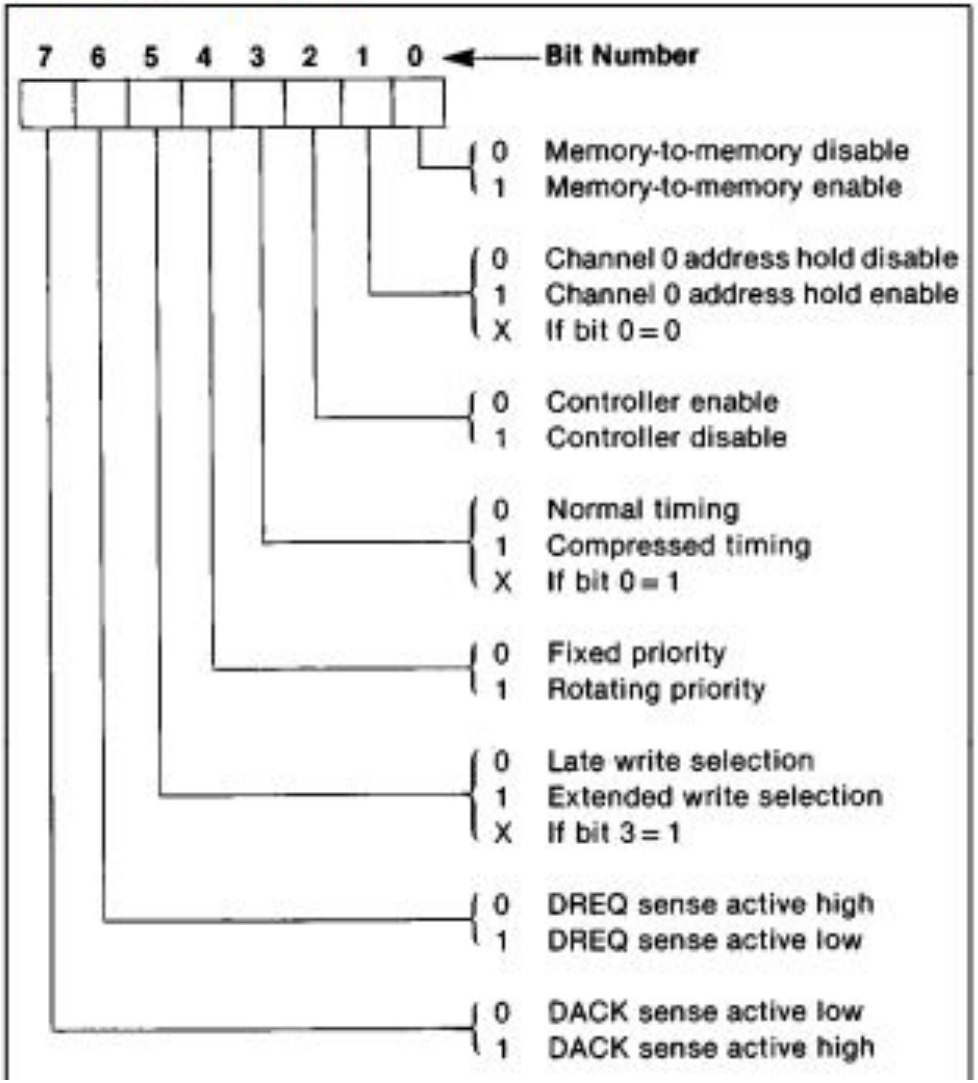
- The 8237A contains 344 bits of internal memory in the form of registers.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1

8237 INTERNAL REGISTERS

- **CAR: Current Address Register:** It holds 16 bit memory address used for DMA transfer. Each channel has its own CAR.
- When byte is transferred during DMA operation CAR is incremented/ decremented as per programming.
- **Current Word Count Register:** It programs a channel for number of bytes to be transferred during DMA operation.
- **Command Register:** This register programs and controls the operation of the 8237. LSB decides memory to memory transfer . Uses DMA Channel 0 to hold the source address and channel 1holds destination address.

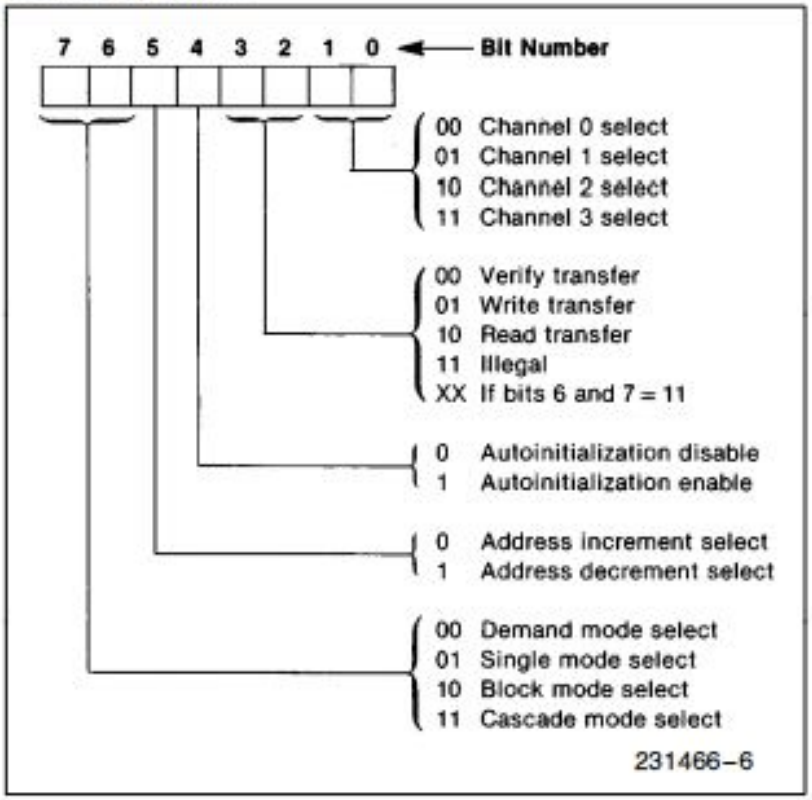
Command Register



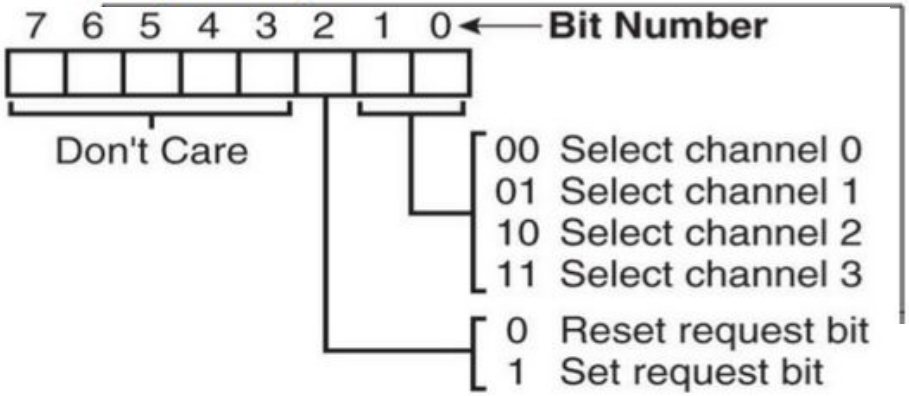
8237 INTERNAL REGISTERS CONTND.

- **BA: Base Address and BWCR:Base word count registers** are used when auto – initialization is seleccted for channel.
- In auto – initilization mode, these registers are used to reload CAR and CWCR after DMA operation is completed.
- **MR: Mode Register: it programs the mode of operation for a channel. Each channel** has own Mode register as selected by bit 0 and bit 1.
- Remaining bits of mode register select operation, auto-initilization, increment / decrement and mode for the channel.

Mode Register



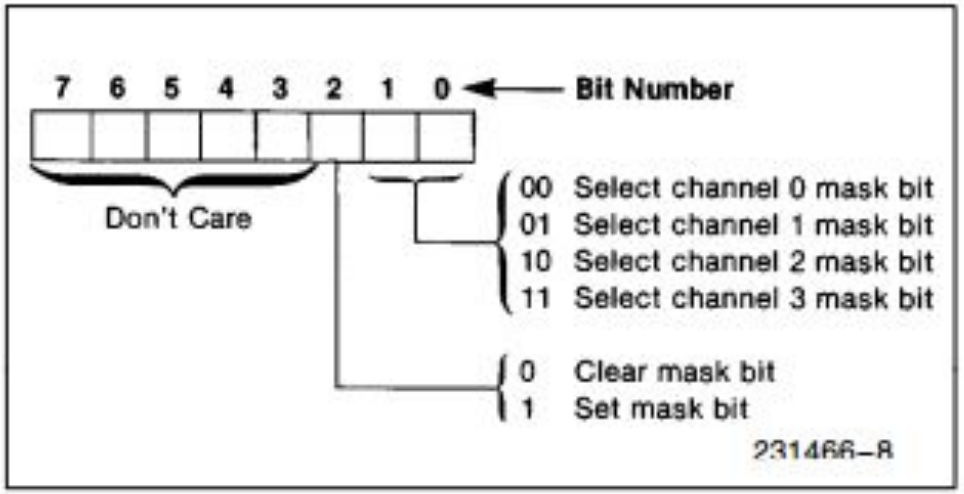
Request Register



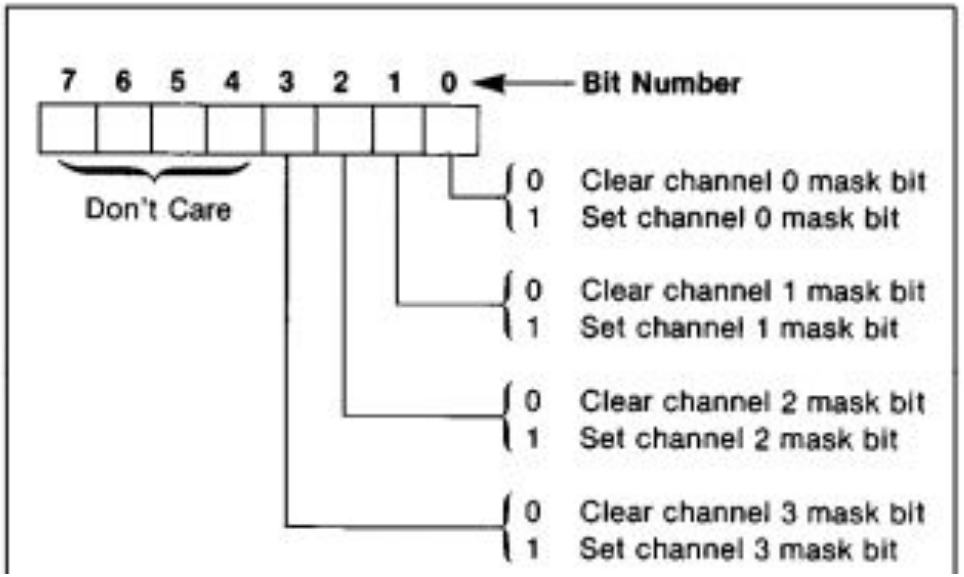
8237 INTERNAL REGISTERS CONTND.

- **RR:Request Register:** is used to request for DMA transfer via software or by DREQ. It is It is very useful in memory to memory transfer when an external signal is not available to begin the DMA transfer. It is non-maskable and subject to prioritization by the Priority Encoder network.
- **MRSR: Mask register set reset:** sets or clears the channel mask. If mask is set channel is disabled.
- **MSR:Mask Set Register:** clears or sets mask for all channels with one command instead of individual channel as with MRSR.
- **SR: Status Register:** shows status of each DMA channel. TC indicates if channel has reached its terminal count. If reached then DMA transfer is terminated. Request bit shows DREQ input from various channels.

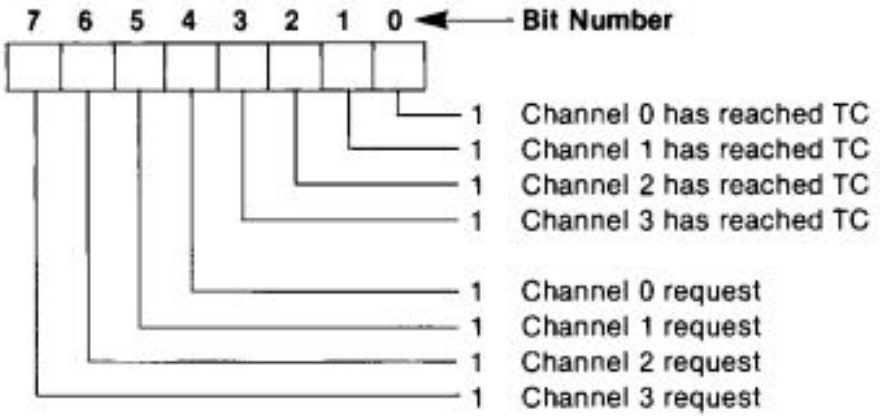
Mask Register



All four bits of the Mask register may also be written with a single command.



STATUS REGISTER



CASCADING OF 8237(FOR REFERENCE ONLY)