# UNIT 1

## NUMERICALS

Q1. 8085 Microprocessor has 16 bit wide data bus and 32 bit wide address bus. Find out how many data bits transferred at a time and how many locations can be addressed.

Ans In 8085 microprocessor there are 16 bit wide data bus so 16 bit data can be transferred at a time.

and size of address bus = 32 bit

So $2^{32}$ locations can be addressed.

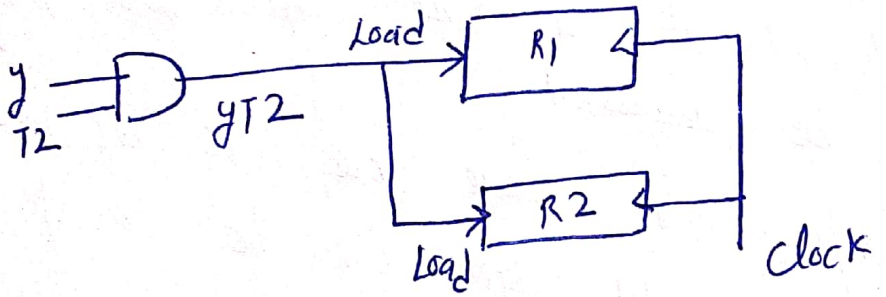
Q2. Show the block diagram of the h/w that implements the following register transfer statement:

yT2: R2 ← R1, R1 ← R2

Sol$^n$ Here two operations are executed at the same time. The given register transfer statement denotes an operation that exchanges the contents of two registers (R1 and R2) during one common clock pulse yT2: 1.

This simultaneous operation is possible with registers that have edge triggered flip flops.

The block diagram of the hardware that implements yT2 is shown below
Here R1 and R2 are n bit registers.




Q3 Represent the following conditional control statement by two register transfer statement with control function:

if (P=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3)

Sol'n The conditional control statement shows that, the contents of Register R2 will be transfer to the register R1 only if P=1. otherwise (i.e if this condition fails P ≠ 1) the contents of register R3 will be transfer to the register R1 only if Q=1.
This can be represted by the following two register transfer statements with control function:

P: R1 ← R2

P'Q: R1 ← R3

Q4. A digital computer has a common bus system for 16 Registers of 32 bits each. The bus is constructed with multiplexers

a) How many selection inputs are there in each multiplexers?

b) What size of multiplexers are needed?

c) How many multiplexers are there in the bus?

Soln

a) for 16 Registers, 4 selection lines are used in each multiplexers.

b) for 16 Registers, 16 x 1 multiplexers are needed.

c) Since each 16 Registers are of 32 bits so 32 multiplexers are needed for each bit.

Q5 Design a 4 bit combinational circuit decrementer using four full adder circuits.

Soln Since decrementer is a circuit which decrements the content of specified register by 1, which will be implemented by adding 2's complement of 1 to the content of specified register i.e.

$R - 1 = R + 2\text{'s complement of } 1$

$= R + (1111)$

↳ (since 2's complement of 0001 is 1111)

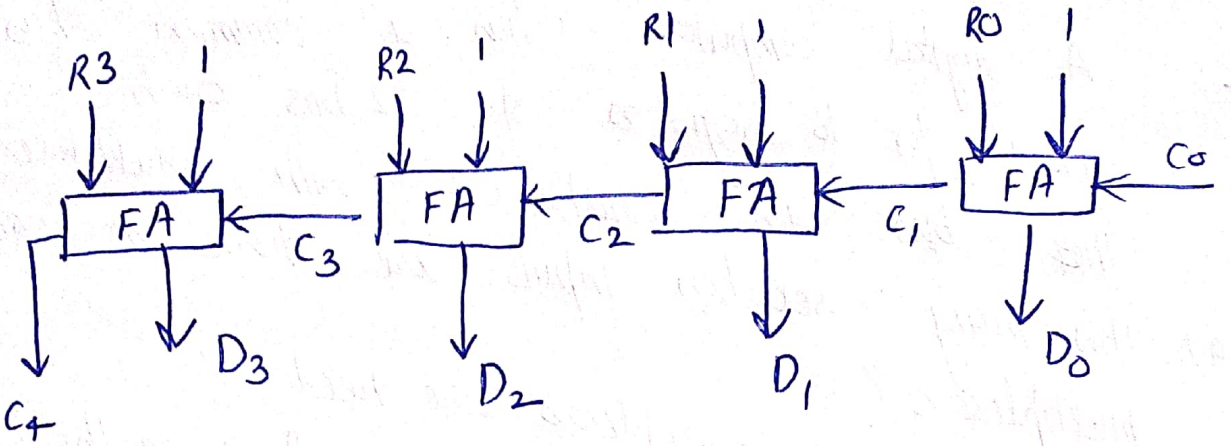



fig: 4 bit binary decrementer

Q6 An 8 bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011100. determine the register value after the arithmetic shift left and state whether there is an overflow.

Sol'n initial content of the register is 10011100

RI → 10011100

ashr RI → 11001110

RI → 10011100

ashl RI → 00111000

The arithmetic shift left inserts a 0 into LSB and shifts all other bits to the left. This cause the sign bit to the lost. also if

Initially (before shift) the MSB and its next bit are not equal, then an overflow occurs. Here MSB (before shifts) is 1 and its next bit is 0 which are not equal. so an overflow occurs. A negative number becomes positive.

Q7. Starting from an inital value of R = 11011101, determine the sequence of binary values in R after a logical shift left, followed by a circular shift right and a circular shift left.

Soln

R = 110 11101

Shl R = 10111010

cir R = 01011101

shr R = 00101110

cil R = 01011100