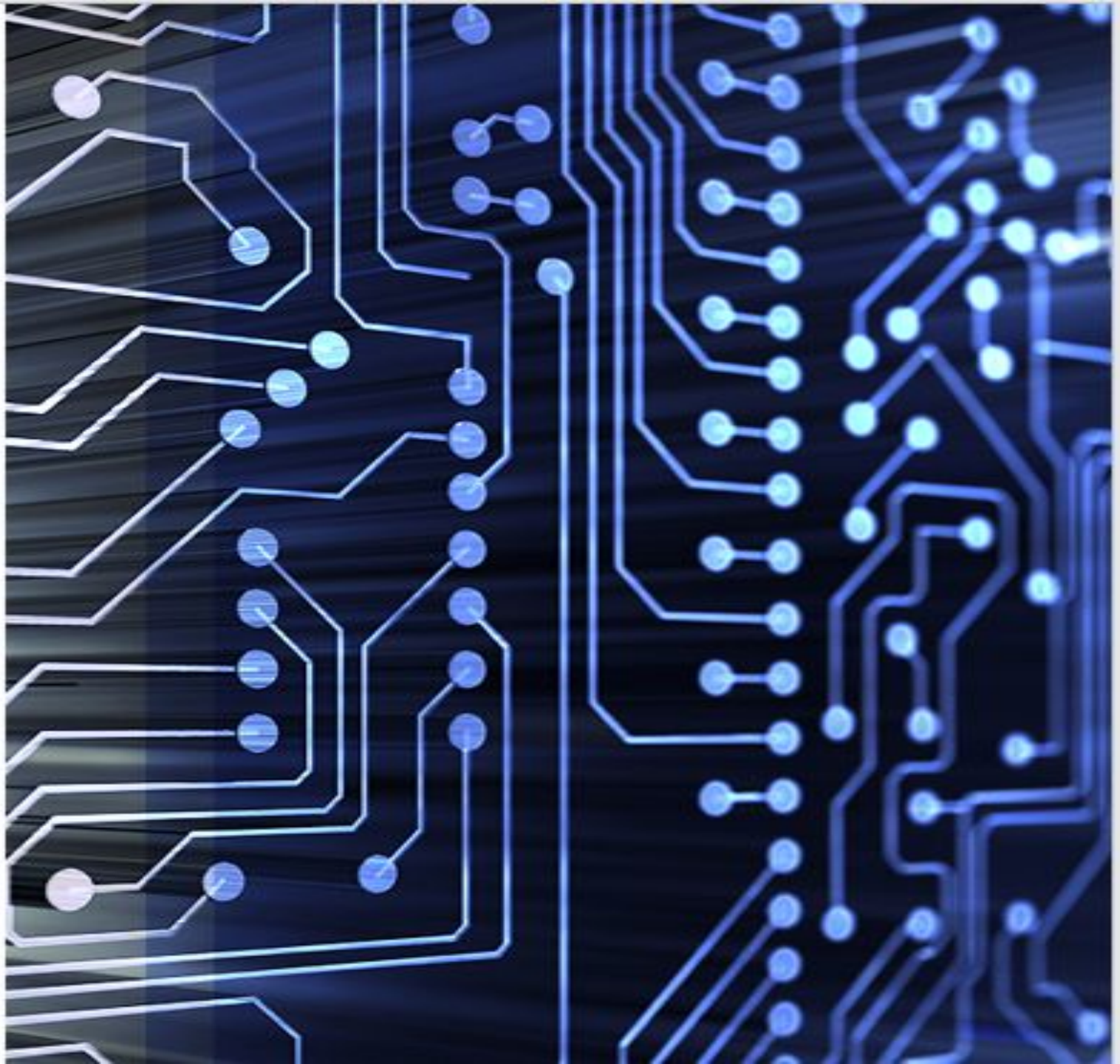


COMPUTER ORGANIZATION & ARCHITECTURE KCS-302

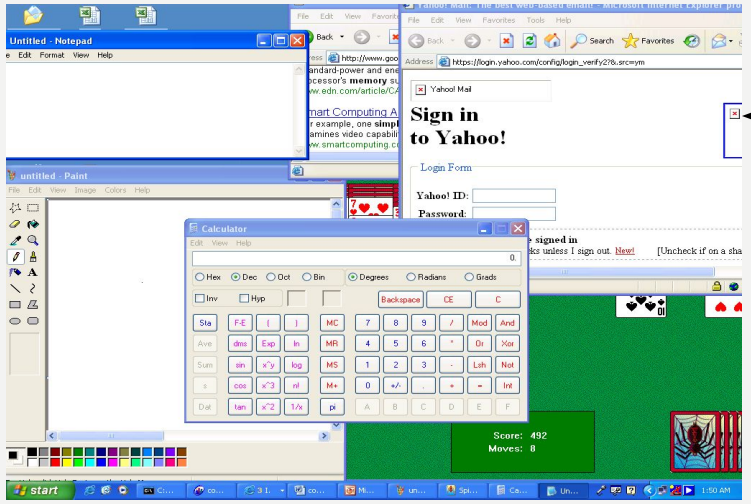
UNIT 1-INTRODUCTION & BUS

BOOK

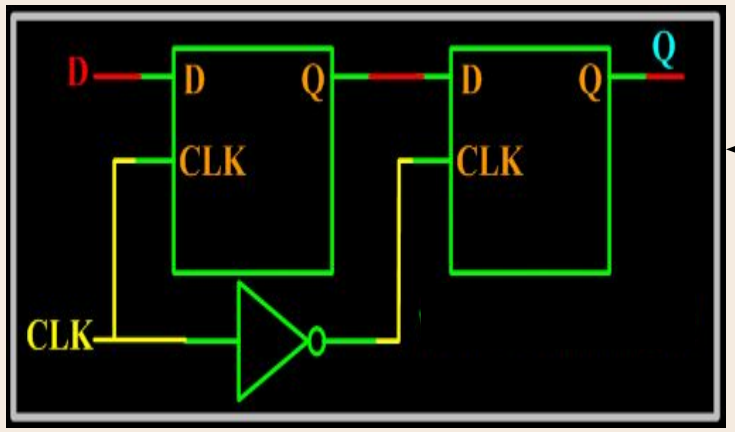
Introduction to computer Architecture

- M. Morris Mano

WHAT WE KNOW ABOUT THE COMPUTER



Software "Runs" on **Hardware**!!!



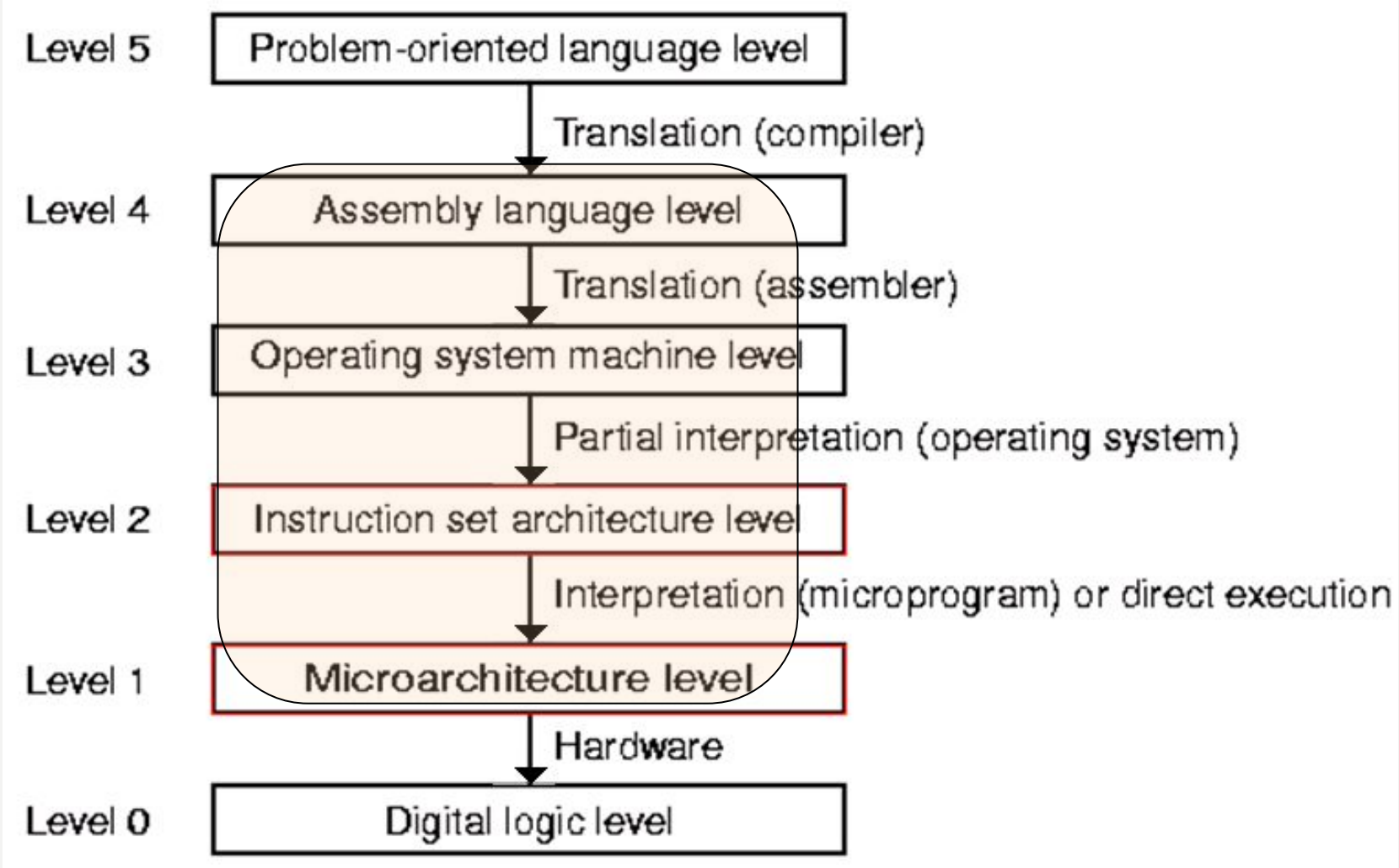
Hardware is composed of
Digital Circuits

WHY IS STUDYING THIS COURSE IS IMPORTANT?

Understanding the computer would help us make efficient code for the computer and understand the behavior of the computer towards various applications

STRUCTURED COMPUTER ORGANIZATION

- The computer is organized as a series of abstractions, each abstraction building on the one below it.



COMPUTER ARCHITECTURE

- Computer Architecture is a functional description of requirements and design implementation for the various parts of computer. It deals with functional behavior of computer system. It comes before the computer organization while designing a computer.
- **Computer Architecture** is concerned with the structure and behaviour of the computer as seen by the user.it includes the information formats, the instruction set and techniques for addressing memory. The architectural design of a computer system is concerned with the specifications of the various functional modules, such as processors and memories, and structuring them together into a computer system.

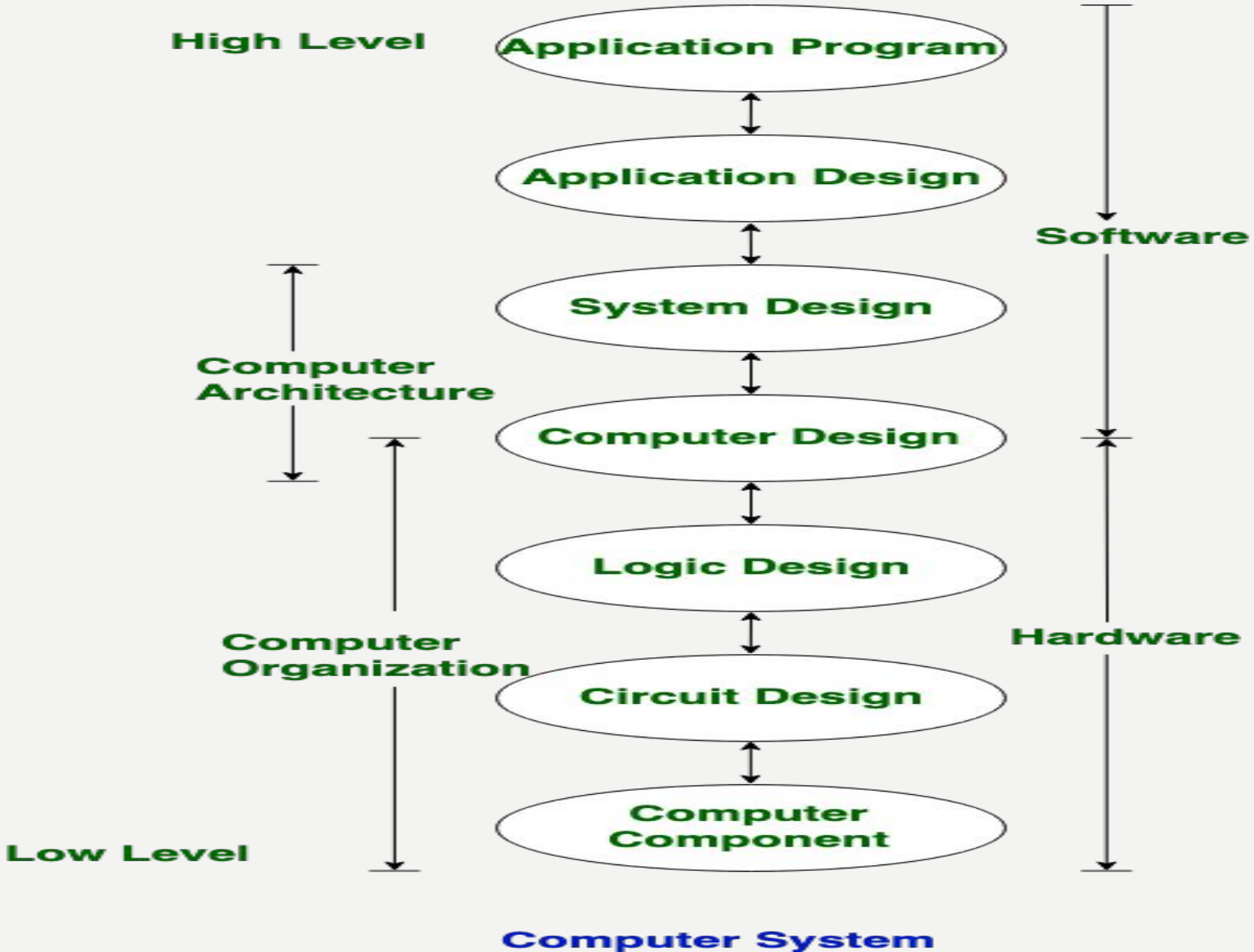
COMPUTER ORGANIZATION

- It is concerned with the way hardware components operate and the way they are connected to form a computer system.
- The various components are assumed to be in place and the task is to investigate the organizational structure to verify that the computer parts operated as intended.
- . **Computer Organization** refers to the level of abstraction above the digital logic level, but below the operating system level.

COMPUTER DESIGN

- Computer design is concerned with the hardware design of the computer.
  - Once the computer specifications are formulated, it is the task of the designer to develop hardware for the system.
  - Computer design is concerned with the determination of what hardware should be used and how the parts should be connected.
  - This aspect of computer hardware is sometimes referred to as computer implementation.

CO ,CA , CD

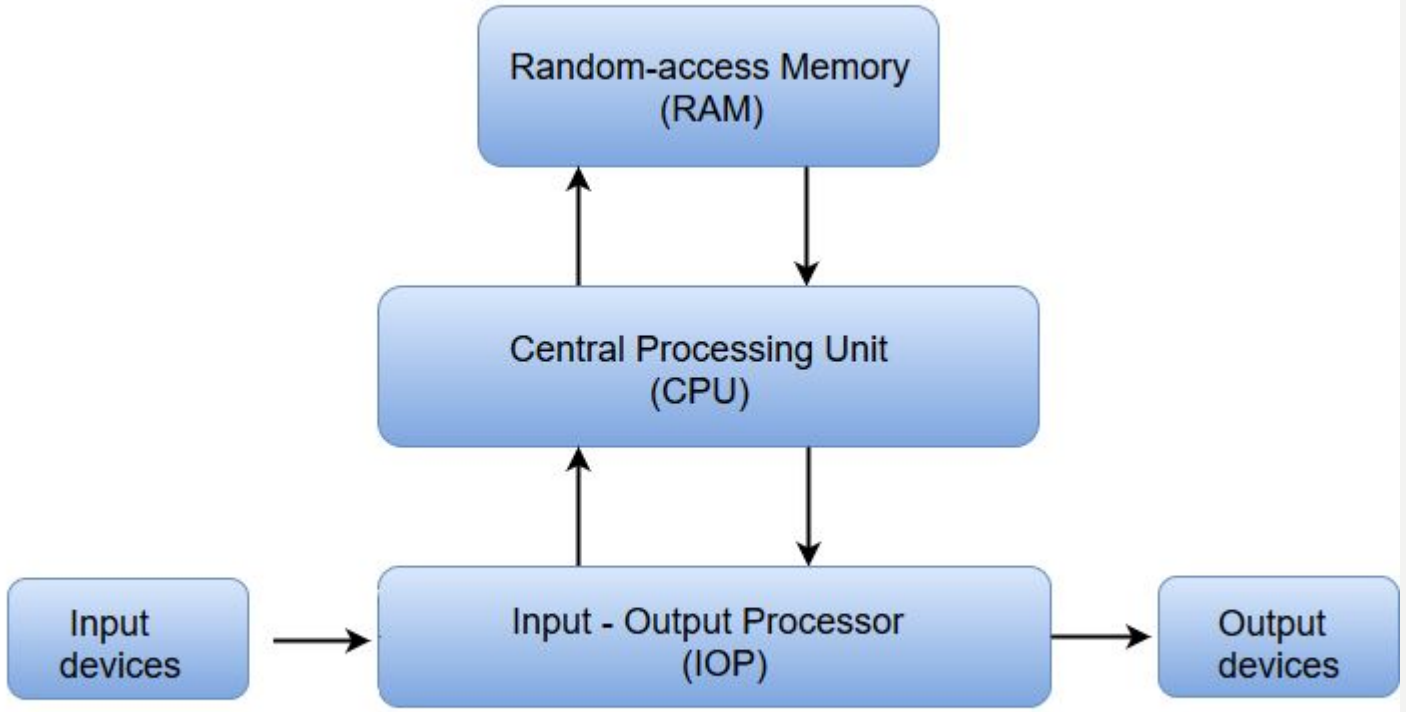

High Level
Application Program
Application Design
System Design
Computer Design
Logic Design
Circuit Design
Computer Component
Low Level
Software
Hardware
Computer Architecture
Computer Organization
Computer System

DIFFERENCE B/W CA & CO

Computer Architecture	Computer Organization
Computer Architecture is concerned with the structure and behaviour of a computer system as seen by the user.	Computer Organization is concerned with the way hardware components are connected together to form a computer system.
It acts as the interface between hardware and software.	It deals with the components of a connection in a system.
Computer Architecture helps us to understand the functionalities of a system.	Computer Organization tells us how exactly all the units in the system are arranged and interconnected.
A programmer can view architecture in terms of instructions, addressing modes and registers.	Whereas Organization expresses the realization of architecture.
While designing a computer system architecture is considered first.	An organization is done on the basis of architecture.
Computer Architecture deals with high-level design issues.	Computer Organization deals with low-level design issues.
Architecture involves Logic (Instruction sets, Addressing modes, Data types, Cache optimization)	Organization involves Physical Components (Circuit design, Adders, Signals, Peripherals)

FUNCTIONAL UNIT & THEIR INTERCONNECTIONS

Block diagram of a digital computer:



FUNCTIONAL UNIT & THEIR INTERCONNECTIONS

- Functional units of a computer system are parts of the CPU (Central Processing Unit) that performs the operations and calculations called for by the computer program. A computer consists of five main components namely, Input unit, Central Processing Unit, Memory unit Arithmetic & logical unit, Control unit and an Output unit.

A typical **digital computer** system has four basic **functional** elements:

- (1) input-output equipment,
- (2) main memory,
- (3) control **unit**, and
- (4) arithmetic-logic **unit**.

CONTD...

- **Control Unit –**A control unit (CU) handles all processor control signals. It directs all input and output flow, fetches the code for instructions and controlling how data moves around the system.
- **Arithmetic and Logic Unit (ALU) –**The arithmetic logic unit is that part of the CPU that handles all the calculations the CPU may need, e.g. Addition, Subtraction, Comparisons. It performs Logical Operations, Bit Shifting Operations, and Arithmetic Operation.
- **Input/Output Devices –** Program or data is read into main memory from the *input device* or secondary storage under the control of CPU input instruction. *Output devices* are used to output the information from a computer.

BUS

Buses – Data is transmitted from one part of a computer to another, connecting all major internal components to the CPU and memory, by the means of Buses. Communication pathway that is connected two or more devices is called BUS. It consists of multiple lines,So a bus can be defined as a group of lines that serves a connecting path for several devices.

Types:

1. **Data Bus:** It carries data among the memory unit, the I/O devices, and the processor.
2. **Address Bus:** It carries the address of data (not the actual data) between memory and processor.
3. **Control Bus:** It carries control commands from the CPU (and status signals from other devices) in order to control and coordinate all the activities within the computer.

BUS WIDTH

- The number of lines present in bus is referred as BUS width. the width of a data bus is a key factor in determining overall system performance..
- The wider the data bus ,the greater the number of bits transferred at a time.
- The width of a address bus has an impact on the system capacity. The wider the address bus ,the greater the range of locations that can be referenced.
- For example, 8085 microprocessor, has 8 bit wide data bus and 16 bit wide address bus, hence 8 bit data can be transferred at a time and there are 2^16=64 MB locations can be addressed.

DATA BUS

- It is a group of conducting wires which carries Data only.Data bus is bidirectional because data flow in both directions, from microprocessor to memory or Input/Output devices and from memory or Input/Output devices to microprocessor.
- If a data bus consists of 32 lines ,it means 32 bit data can be transferred simultaneously (one bit per line),on the other hand ,if each instruction is 16 bit long and 8 bit data bus is available , and the the processor must access the memory module twice during each instruction cycle.

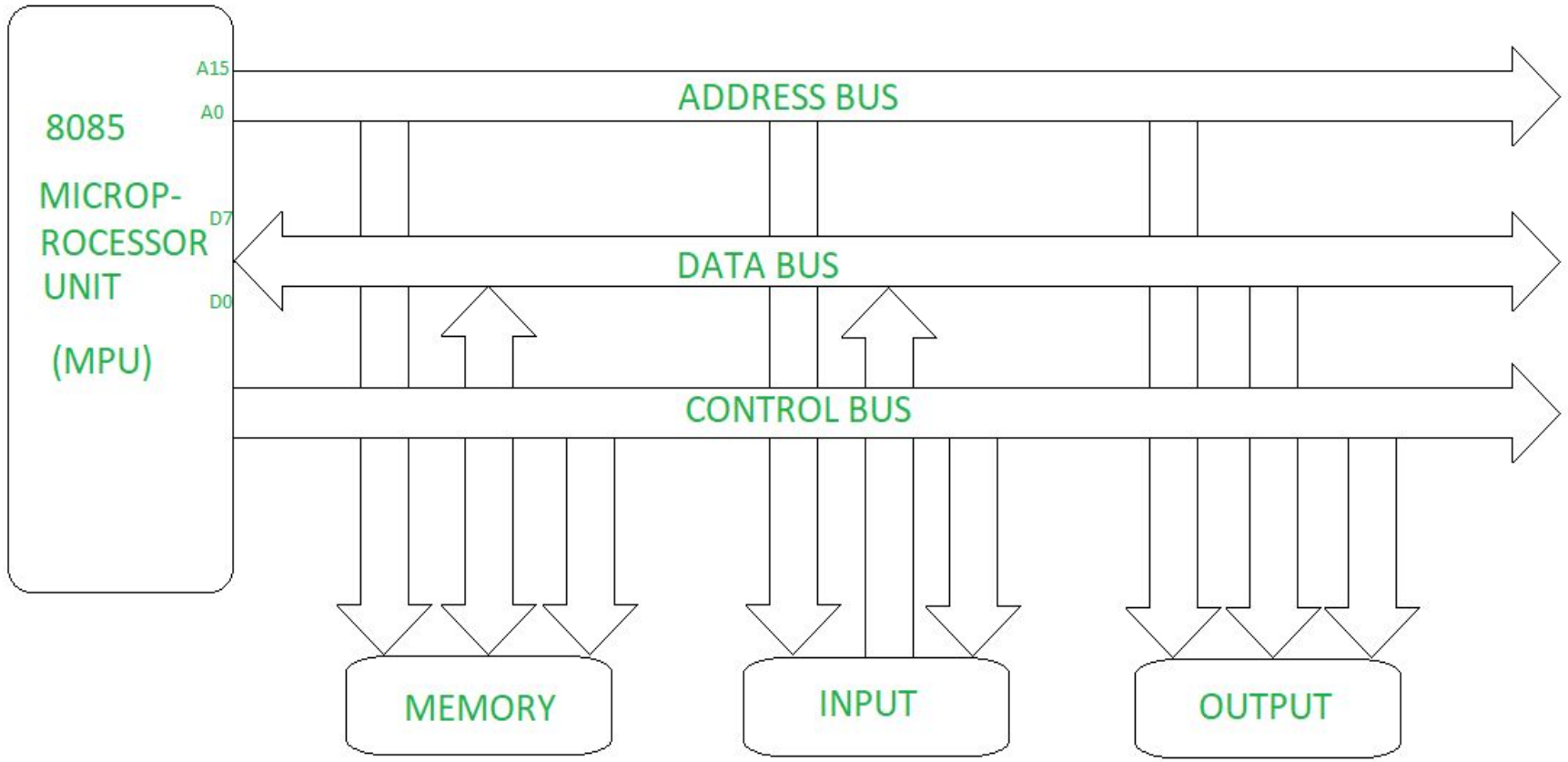
ADDRESS BUS

- **Address lines are used to designate the source or destination of the data on the data bus.** These source or destination may either be memory or I/O devices. Address lines collectively known as address bus. Number of address lines determines the maximum addressing capacity by the processor.
- It is a group of conducting wires which carries address only.Address bus is unidirectional because data flow in one direction, from microprocessor to memory or from microprocessor to Input/output devices

CONTROL BUS

- It is a group of conducting wires, which is used to generate timing and control signals to control all the associated peripherals, microprocessor uses control bus to process data, that is what to do with selected memory location. Some control signals are:
  - Memory read-places data from the address location onto the data bus.
  - Memory write-places data from the data bus into the address locations.
  - I/O read-places data from the addressed I/O port onto the data bus.
  - I/O Write-places data from the data bus as output to the addressed I/O port.
  - Opcode fetch

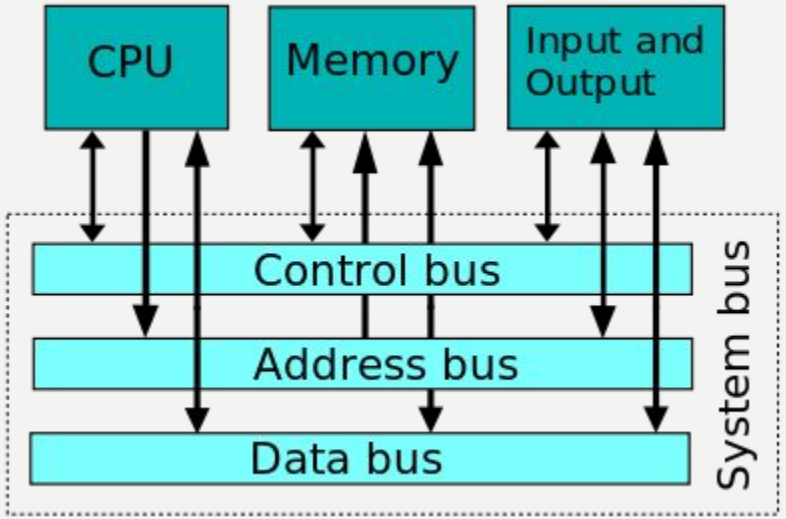
BUS ARCHITECTURE



Bus organization system of 8085 Microprocessor

SYSTEM BUS

The **system bus** is a pathway composed of cables and connectors used to carry data between a computer microprocessor and the main memory. The **bus** provides a communication path for the data and control signals moving between the major components of the computer **system.**



BUS ARBITRATION

- It decides which component will use the BUS among various competing requests.
- The possibility may exist that more than one module may need control of the bus, e.g. an I/O module may require reading reading or writing directly to memory,without sending the data to the processor, because only one unit may at a time be able to transmit successfully over the bus , there is some selection mechanism is required to maintain such transfers.this mechanism is known as BUS arbitration.

TYPES OF BUS ARBITRATION

- There are two approaches to bus arbitration:

1. Centralized Bus Arbitration
    i. Daisy Chaining Method
    ii. Polling Method
    iii. Independent Requesting Method
2. Distributed Bus Arbitration

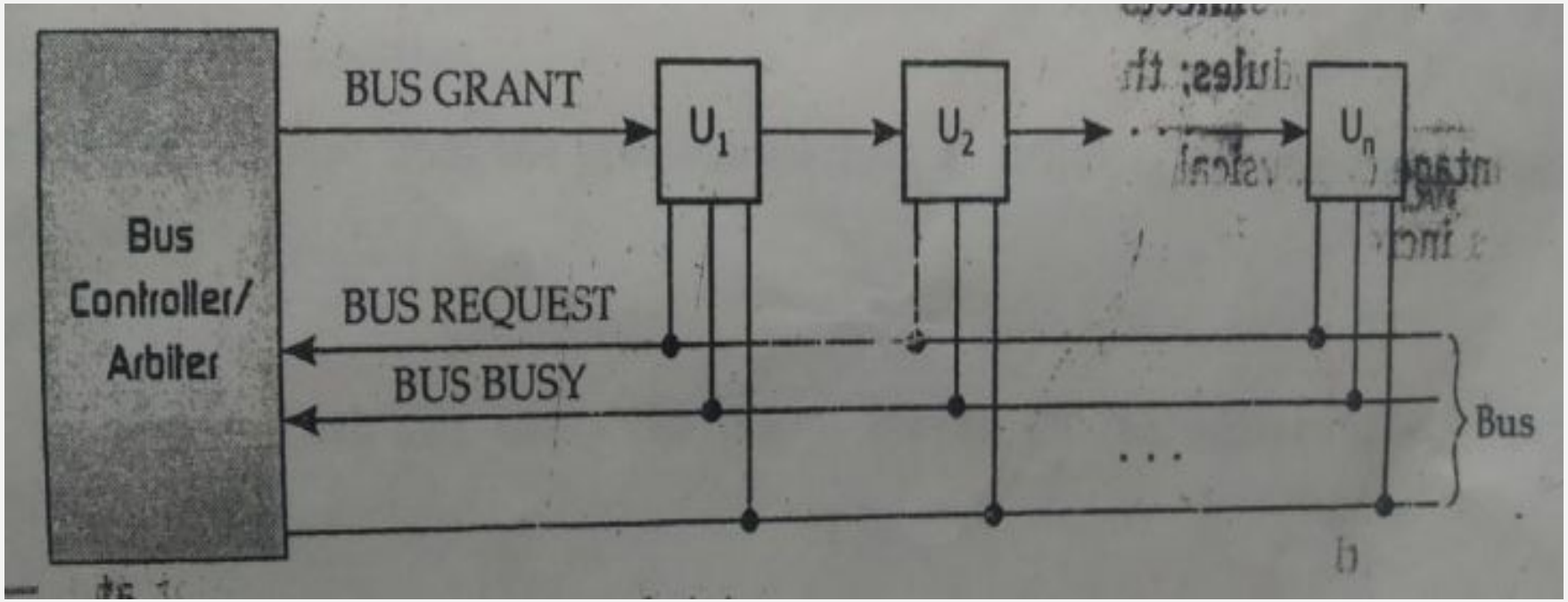
BUS ARBITRATION

1. Centralized Arbitration

- In centralized bus arbitration, a single bus arbiter performs the required arbitration. The bus arbiter may be the processor or a separate controller connected to the bus.
- There are three different arbitration schemes that use the centralized bus arbitration approach. There schemes are:
  - a. Daisy chaining
  - b. Polling method
  - c. Independent request

DAISY CHAINING METHOD

- **a) Daisy chaining**
  - The system connections for Daisy chaining method are shown in fig below.



DAISY CHAINING METHOD

- In this method all the requesting components are attached serially on the BUS. This method involves three control signals assigned as BUS request , BUS GRANT and BUS BUSY. All the bus units are connected to the bus BUS REQUEST line. When activated, it indicates that one or more devices are requesting to use the bus. The bus controller responds to a BUS REQUEST only if BUS BUSY is inactive. When the bus control is given to the requesting device, it enables its physical connection and activates the BUS BUSY.
- When the first requesting device gets control of the bus and receives BUS GRANTsignal,it blocks further propagation of the signals, activates BUS BUSY and begins to use of the BUS.
- When a non requesting device receives BUS GRANT signal, it forwards the signal to the next device.
- Thus if two devices simultaneously request bus access, the device that is closer to the bus controller receives bus grant first., and receives the bus control.
- That is , devices that are closed to the bus controller are of higher priority than those of other devices.

DAISY CHAINING METHOD

Advantages –

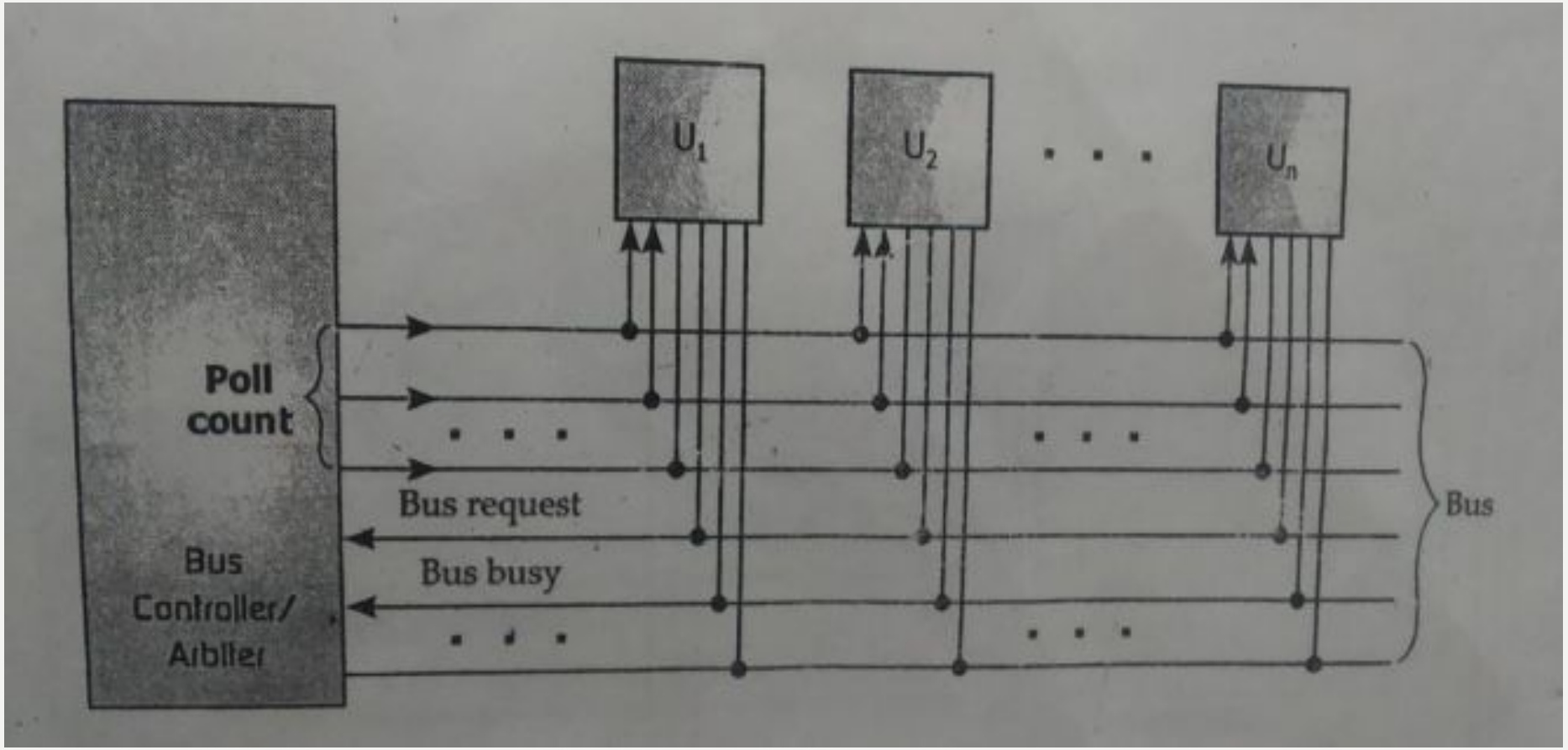
- Simplicity and Scalability.
- The user can add more devices anywhere along the chain, up to a certain maximum value.
- It is a simple method, it requires few control lines, independent of the number of devices connected to the bus.

Disadvantages –

- Priority is fixed, it cannot be changed during program execution.also the chain of devices is susceptible to failure which involves BUS grant line and its associated circuit.
- Propagation delay is arises in this method.
- If one device fails then entire system will stop working.

POLLING METHOD

- The system connections for polling method are shown in figure below.



POLLING METHOD

- This method replaces the BUS GRANT line of Daisy chain method with a set of poll count lines that are connected directly to all devices on the BUS.
- Similar to daisy chain method, devices request access to the bus via a common BUS REQUEST line. In response to a signal on BUS REQUEST,bus controller generates a sequence of numbers on the poll count lines. Each device compares these numbers as their device address already assigned to them, when a requesting device finds that its address matches the number on the poll count lines, the device activates BUS BUSY. The bus controller responds by terminating the polling process and the device connects to the bus.

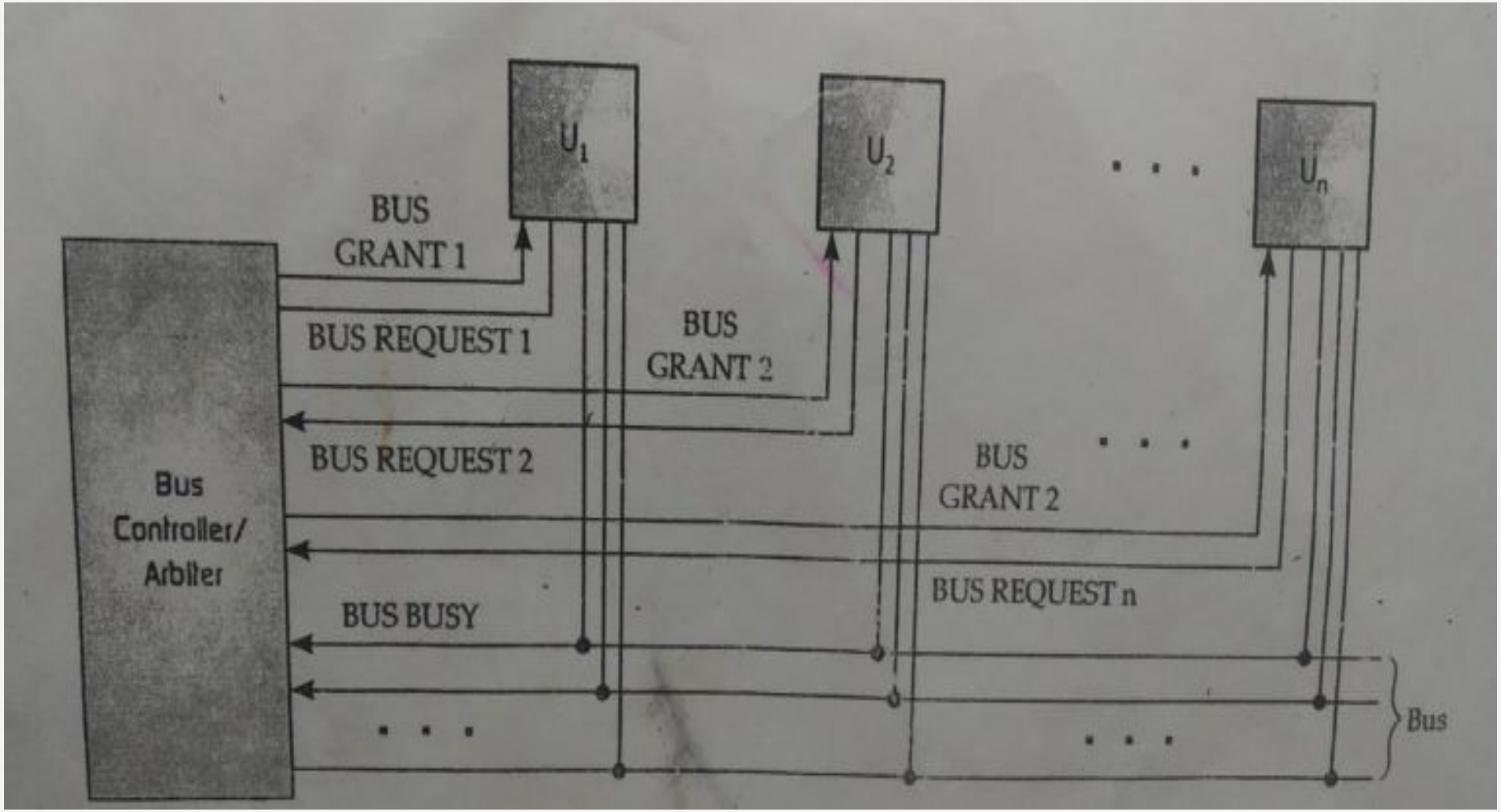
POLLING METHOD

- **Advantages –**
- This method does not favor any particular device and processor.
- The method is also quite simple.
- If one device fails then entire system will not stop working.as failure of a device does not affect other devices.
- The priority of a device is determined by the position of its address in the polling sequence. This sequence can be programmed if the poll lines are connected to a programmble register.
- **Disadvantages –**

Number of devices that can share the bus is limited by the addressing capability of the poll lines.

INDEPENDENT REQUEST METHOD

The figure below shows the system connections for the independent request scheme.



INDEPENDENT REQUEST METHOD

- In this method, there are separate BUS REQUEST and BUS GRANT lines for every device that are sharing the bus. In this approach, the bus controller has the capability of immediate identifying all the requesting devices. The bus controller responds rapidly to the request by determining the highest priority device that has sent the bus request. This priority is programmable and is predetermined. The priority decider internal to the bus controller selects the desired request.

INDEPENDENT REQUEST METHOD

- **Advantages –**
- This method generates fast response.
- Due to separate BUS REQUEST and BUS GRANT lines, the arbitration is fast.
- **Disadvantages –**
- Hardware cost is high as large no. of control lines are required.
- Due to independent requesting, there are 2n control lines for controlling n devices,in contrast,daisy chaining requires two such lines, while polling requires approximately $\log_2 n$ lines.

DISTRIBUTED BUS ARBITRATION

- **Distributed Arbitration**
- In distributed scheme, there is no central controller, each module contains access control logic and the modules act together to share the bus. This means that all modules participate in the selection of bus transfer.