Programmable Interface devices

Programmable Peripheral Interface [8255]

PPI 8255

- It is an **I/O port chip used for interfacing I/O devices** with microprocessor.

- The **parallel input-output port chip 8255** is also called as **programmable *peripheral input-output port.***

- The Intel's **8255 is designed for use with Intel's 8-bit, 16-bit microprocessors.**

PPI 8255

- It has **24 input/output lines** which may be individually programmed in groups.
- The groups of I/O pins are named as **Group A , Group B and Group C upper and Group C lower.**
- Each of these two groups contains a subgroup of eight I/O lines called as **8-bit port** and another subgroup of four lines or a **4-bit port.**

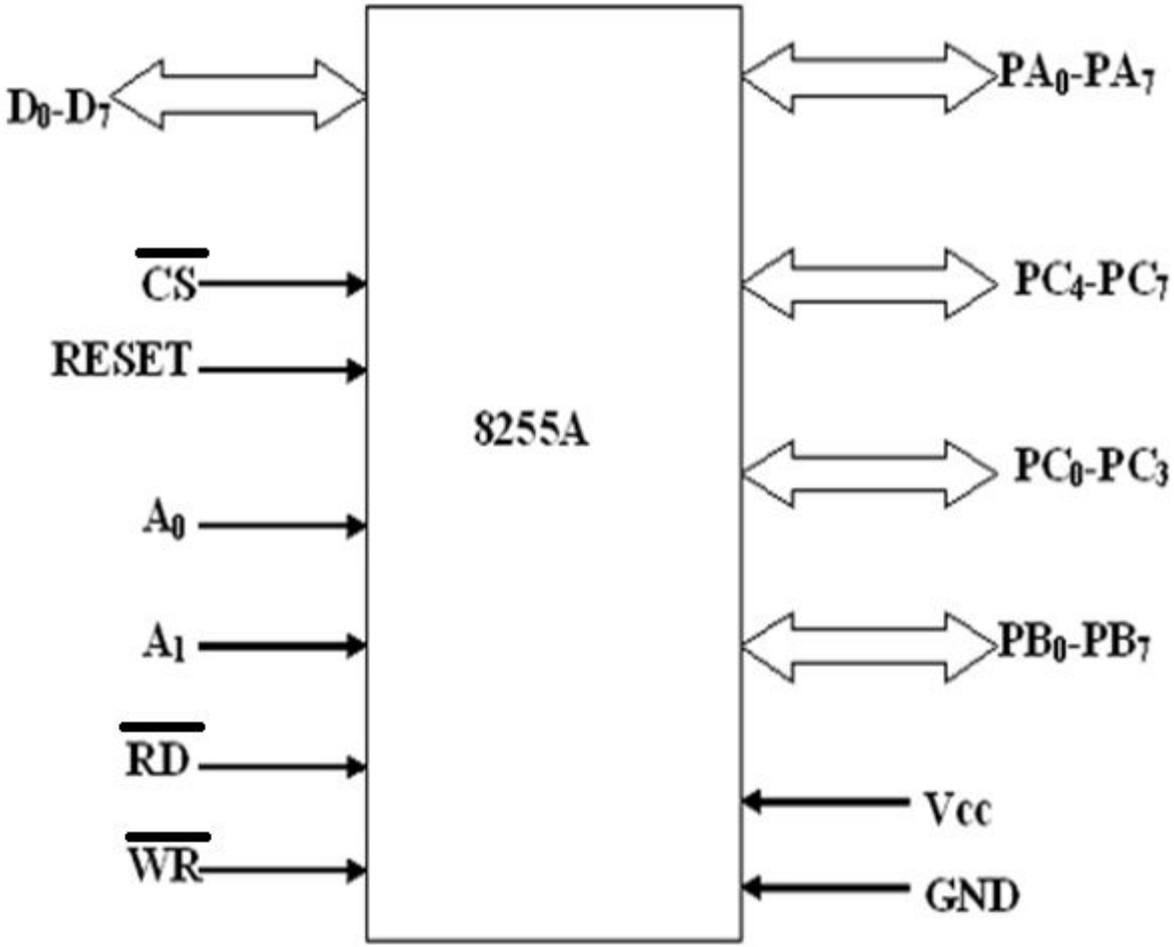
PPI 8255

- Group A contains port A lines identified by symbols **PA_0-PA_7 and** port C lines are identified as **PC_4-PC_7**. Similarly, Group B contains an 8-bit port B, containing lines **PB0-PB7** and a 4-bit port C with lower bits **PC0- PC3.**

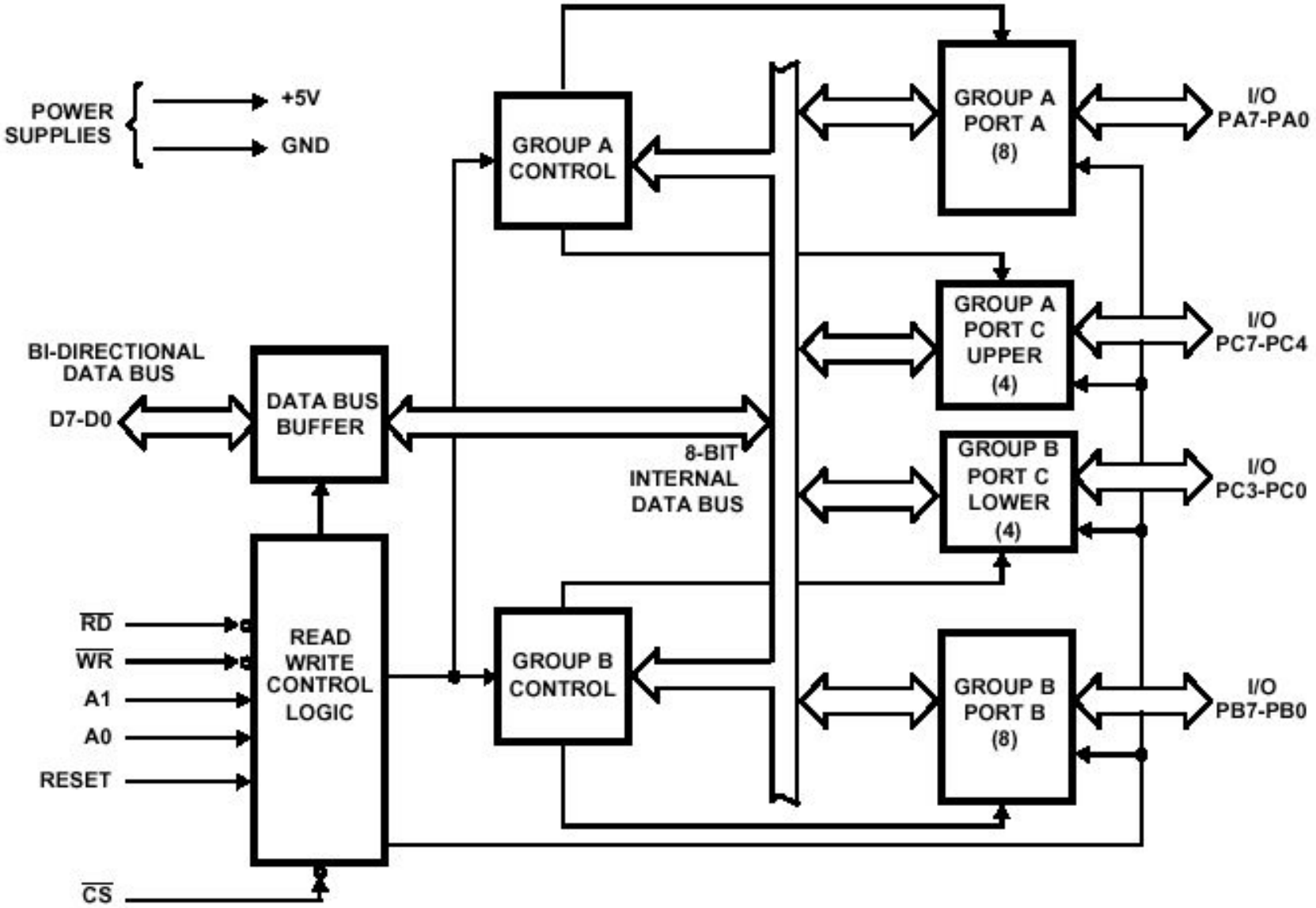
- All of **these ports can function independently either as input or as output ports.**

- This can be achieved by **programming the bits of an internal register of 8255 called as control word register (CWR).**

SIGNALS OF 8255



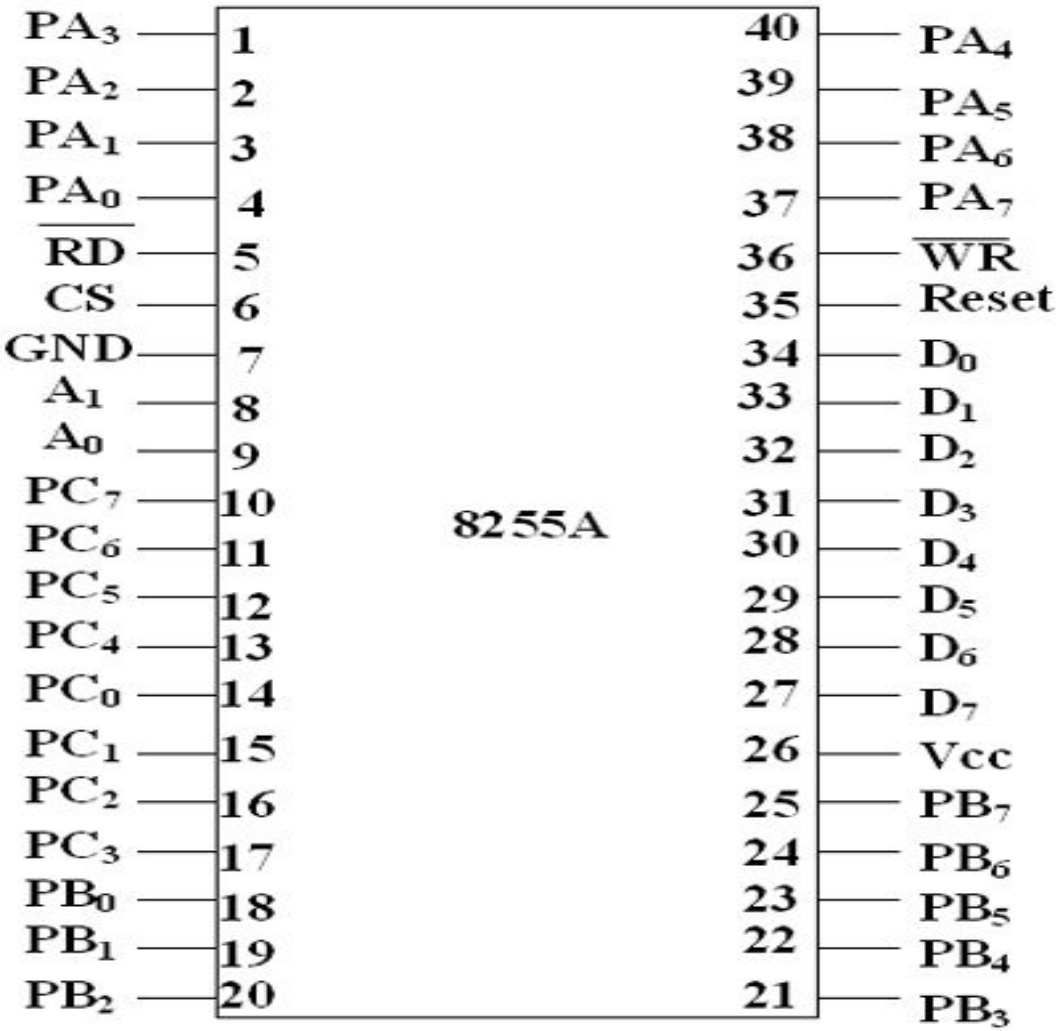
Block Diagram of 8255



Block Diagram of 8255

- Two control groups, labeled group A control and group B control define how the three I/O ports operate.
- The upper 4 bits of port C are associated with group A control while the lower 4 bits of port C are associated with group B control.
- The other logic blocks are read/write control logic and data bus buffer. These blocks provide the electrical interface between the micro processor and 8255.
- The data bus buffer buffers the data I/O lines to/from the microprocessor data bus.
- The read/write control logic routes the data to and from the correct internal registers with the right timing.

Pin Diagram of 8255



8255A Pin Configuration

Pin Diagram of 8255

- The 8255 is a 40 pin integrated circuit (IC).
- **D0 - D7** are the data input/output lines for the device. All information read from and written to the 8255 occurs via these 8 data lines.
- **CS (*Chip Select Input*):** If this line is a logical 0, the microprocessor can read and write to the 8255.
- **RD (*Read Input*):** Whenever this input line is a logical 0 and the CS input is a logical 0, the 8255 data outputs are enabled onto the system data bus.

Pin Diagram of 8255

- **WR (*Write Input*)** Whenever this input line is a logical 0 and the CS input is a logical 0, data is written to the 8255 from the system data bus

- **A0 - A1** (*Address Inputs*) The logical combination of these two input lines determines which internal register of the 8255 data is written to or read from.

- **RESET** The 8255 is placed into its reset state if this input line is a **logical 1**. All peripheral ports are set to the **input mode.**

Pin Diagram of 8255

- **PA0 - PA7**, **PB0 - PB7**, **PC0 - PC7** These signal lines are used as 8-bit I/O ports.
- They can be connected to peripheral devices.
- The 8255 has three 8 bit I/O ports and each one can be connected to the physical lines of an external device.
- These lines are labeled PA0-PA7, PB0-PB7, and PC0-PC7.
- The groups of the signals are divided into three different I/O ports labeled port A (PA), port B (PB), and port C (PC).

Pin Diagram of 8255

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to Data bus
0	1	0	0	1	Port B to Data bus
0	1	0	1	0	Port C to Data bus
0	1	0	1	1	CWR to Data bus

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

Control Word Register

- Write a program for IC 8255, PPI (Programmable peripheral Interface) to read DIP switches from port C and display the reading to port B.

Solution:

- 1**. Control Word**= 1 0 0 0 1 0 0 1=89H

2. **Port Address**

A7A6A5A4A3A2A1A0

1 0 0 1 0 0 0 0-90H-PA

1 0 0 1 0 0 0 1-91H-PB

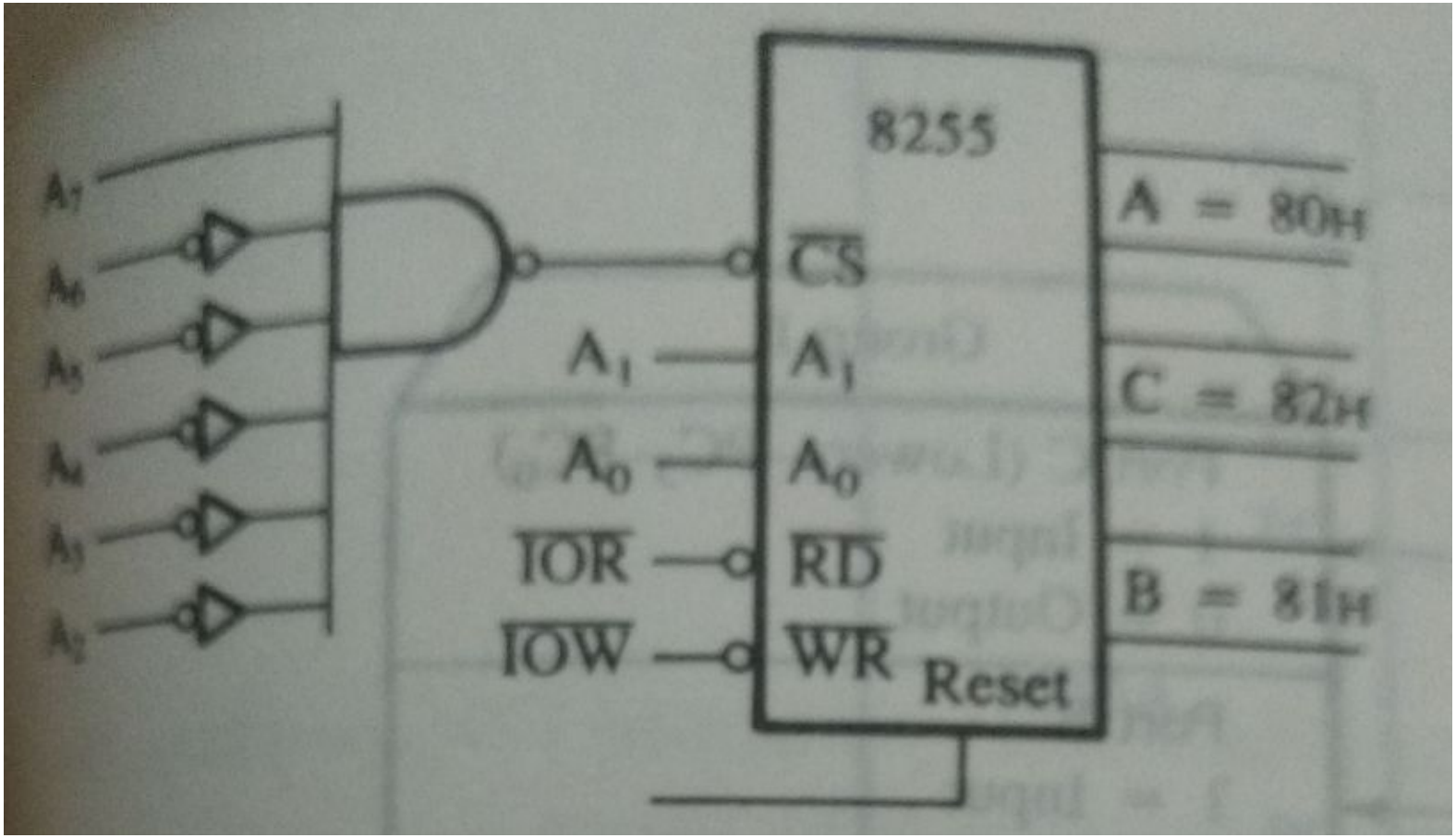
1 0 0 1 0 0 1 0-92H-PC

1 0 0 1 0 0 1 1-93H-CWR

3. Program:

```
MVI A,89H
OUT 93H
IN 92H
OUT 91H
HLT
```

Write a program for IC 8255, PPI (Programmable peripheral Interface) to read DIP switches from port A and display the reading to port B. Determine Port addresses as pr the circuit given below:



- Write a program for IC 8255, PPI (Programmable peripheral Interface) to read DIP switches from port A and display the reading to port B.

Solution:

- 1**. Control Word**= 1 0 0 1 0 0 0 0=90H

2. **Port Address**

A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	0	0	0	0	0-80H-PA
1	0	0	0	0	0	0	1	1-81H-PB
1	0	0	0	0	0	1	0	0-82H-PC
1	0	0	0	0	0	1	1	1-83H-CWR

3. Program:

```
MVI A,90H
OUT 83H
IN 80H
OUT 81H
HLT
```

Modes of 8255

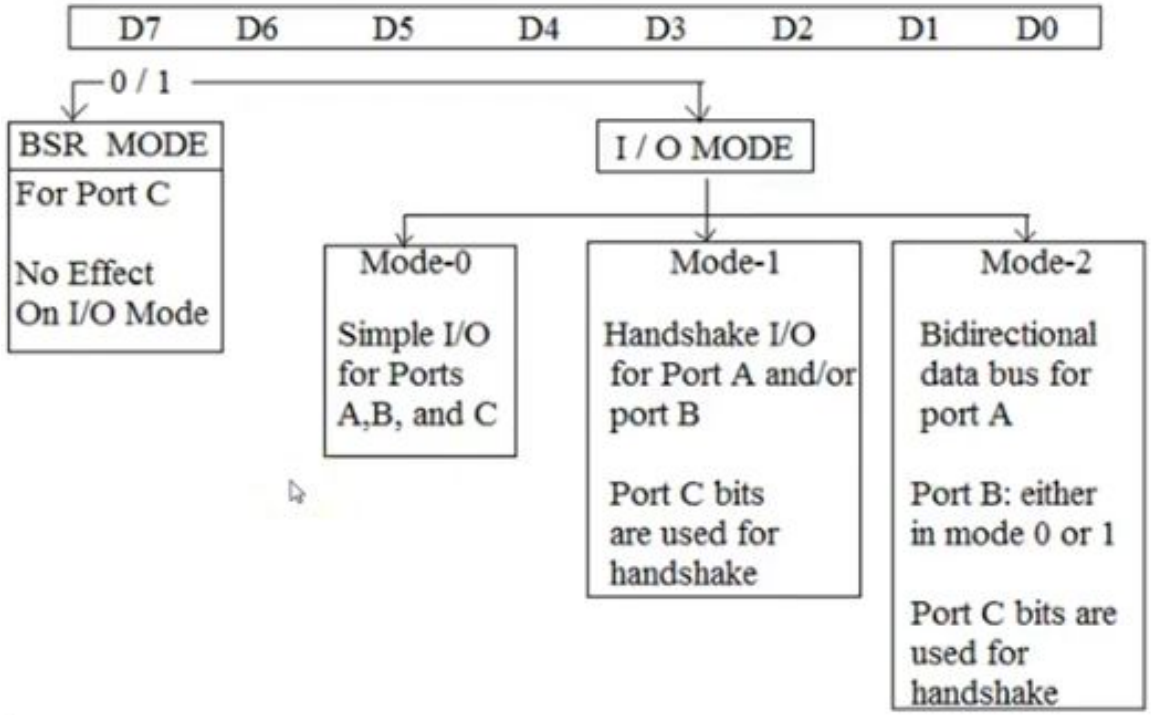
- There are two basic modes of operation of 8255, They are:
- **1. I/O mode.**
- **2. BSR mode.**

- **In I/O mode, the 8255 ports work as programmable I/O ports**, while

- **In BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.**

8255 PPI MODES OF OPERATION

Control Word Format



Modes of 8255

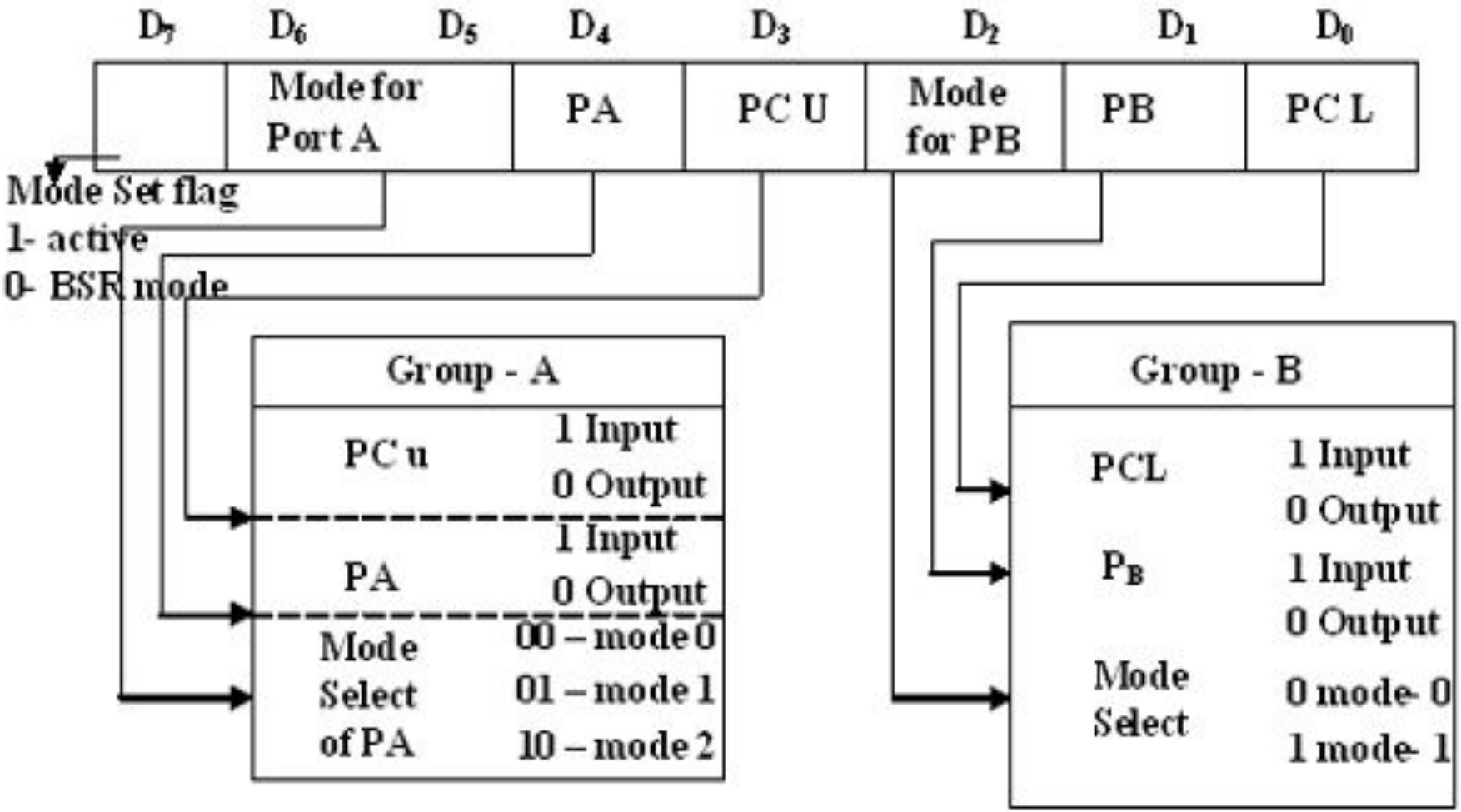
- There are 3 I/O modes of operation for the ports of 8255.
- **Mode 0, Mode 1, and Mode 2**

1) Mode 0 - Basic I/O mode

2) Mode 1 - Strobed I/O mode

3) Mode 2 - Strobed bi-directional I/O

Control word Format of 8255 - I/O mode



Control Word Format of 8255

Modes of 8255

Mode 0 Operation

- It is Basic or **Simple I/O.**
- It **does not use any handshake signals**.
- It is **used for interfacing an i/p device or an o/p device.**
- **It is used when timing characteristics of I/O devices is well known**

Modes of 8255

Mode 1 Operation

- It uses handshake I/O.
- 3 lines are used for handshaking.
- It is used for interfacing an i/p device or an o/p device.
- Mode 1 operation is used when timing characteristics of I/O devices is not well known, or used when I/O devices supply or receive data at irregular intervals.

Modes of 8255

- Handshake signals of the port inform the processor that the data is available, data transfer complete etc.

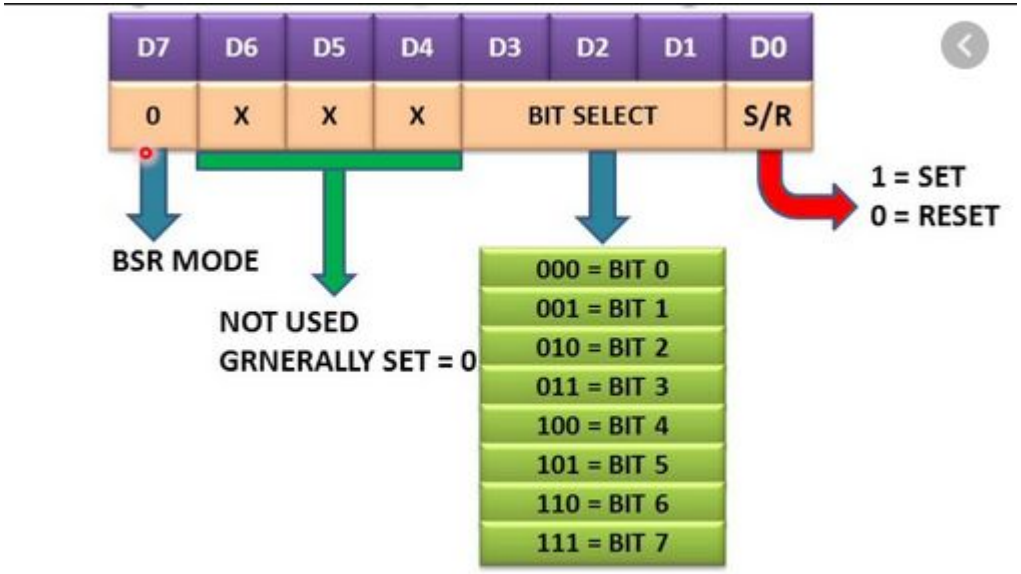
Mode 2 Operation

- It is bi-directional handshake I/O.
- Mode 2 operation uses 5 lines for handshaking.
- It is used with an I/O device that receives data some times and sends data sometimes.
- Mode 2 operation is useful when timing characteristics of I/O devices is not well known, or when I/O devices supply or receive data at irregular intervals.

Modes of 8255

- Port A, Port B and Port C can work in Mode 0
- Port A and Port B can work in Mode 1
- Only Port A can work in Mode 2

BSR MODE{ BIT SET RESET MODE



- Initialize Control word register to set PC7

CONTROL WORD FOR SETTING PC7-0 0 0 0 1 1 1 1

MVI A,0F

OUT 93H

- Initialize Control word register to reset PC3
- CONTROL WORD FOR RESETTING PC4-0 0 0 0 0 1 1 0

MVI A,08

OUT 93H

BSR MODE

- WAP for Initializing Control word register to set PC7 & PC3 and then reset these after certain delay.Assume Port address 93H for CWR

CONTROL WORD FOR SETTING PC7-0 0 0 0 1 1 1 1=0FH
CONTROL WORD FOR SETTING PC3-0 0 0 0 0 1 1 1=07H
CONTROL WORD FOR RESETTING PC7-0 0 0 0 1 1 1 0=0EH
CONTROL WORD FOR RESETTING PC3-0 0 0 0 0 1 1 0=06H

```
MVI A,0FH
OUT 93H
MVI A,07H
OUT 93H
CALL DELAY
MVI A,0EH
OUT 93H
MVI A,06H
OUT 93H
```

```
DELAY: MVI C.10H
L1: DCR C
    JNZ L1
    RET
```

Programmable Interval Timer[8254/8253]

PIT 8254/8253

- The **Intel 8253** and **8254** are Programmable Interval Timers (PITs), which perform timing and counting functions.
- After the desired delay, the 8254 will interrupt the CPU.
- It is 24 pin IC requires +5 V
- It consists of 3 16 bit counters operates in 6 modes.

8253/8254

The 8254 is a superset of 8253. The functioning of these two ICs are almost similar along with the pin.

Features of 8254

1) Three independent 16-bit down counters.

2) 8254 can handle inputs upto clk frequency 10 MHz where as 8253 can operate upto 2.6 MHz.

3) Three counters are identical presettable, and can be programmed for either binary or BCD count.

4) Counter can be programmed in six different modes.

5) Compatible with all Intel and most other microprocessors.

6) 8254 has powerful command called READ BACK command which allows the user to check the count value, , programmed mode and current mode and current status of the counter

Difference between 8253 and 8254

	8253	8254
1	Maximum input clock frequency is 2.6 MHz	Maximum input clock frequency is 8 MHz
2	It does not have read-back feature	It has read-back feature

PIT 8254

- It generates accurate time delays under software control.
- Instead of setting up timing loops in software, the programmer configures the interval timer to match system requirements and programs the counter for the desired delay or for the desired output.
- Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are

Real time clock
Event-counter
Digital one-shot

PIT 8254

Programmable rate generator

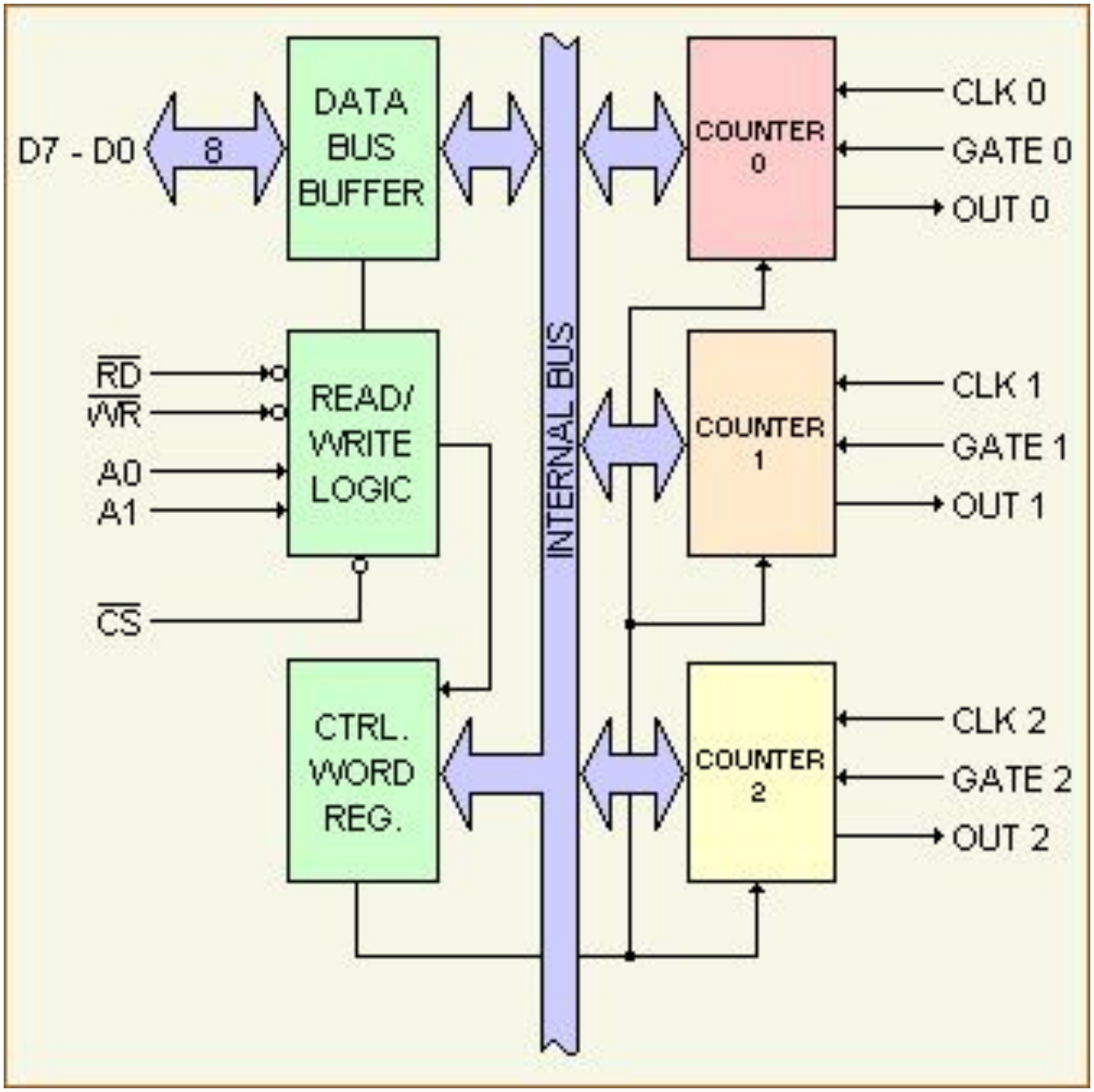
Square wave generator

Binary rate multiplier

Complex waveform generator

Complex motor controller

Block Diagram of 8254/8253



Block Diagram of 8254/8253

- **Data/Bus Buffer**

- This block contains the logic to buffer the data bus to / from the microprocessor, and to the internal registers.

- It has 8 input pins, usually labeled as D7..D0, where D7 is the MSB

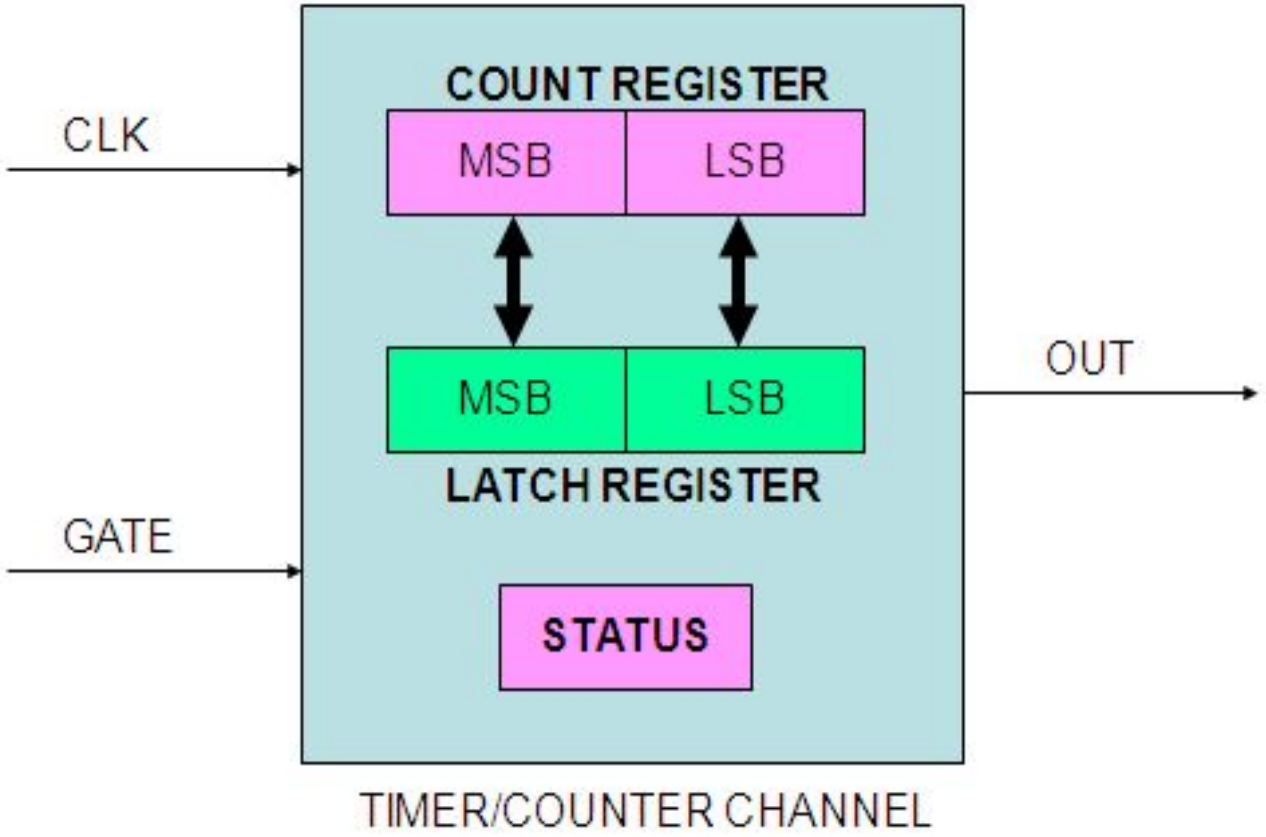
Block Diagram of 8254/8253

- **Read/Write Logic**
- $\overline{RD}$: read signal
- WR': write signal
- CS': chip select signal
- A0, A1: address lines
- Operation mode of the PIT is changed by setting the above hardware signals.
- For example, to write to the Control Word Register, one needs to set CS'=0, RD'=1, WR'=0, A1=A0=1.

Block Diagram of 8254/8253

- The timer has three counters, called channels.
- Each channel can be programmed to operate in one of six modes.
- Once programmed, the channels can perform their tasks independently.

Block Diagram of 8254/8253



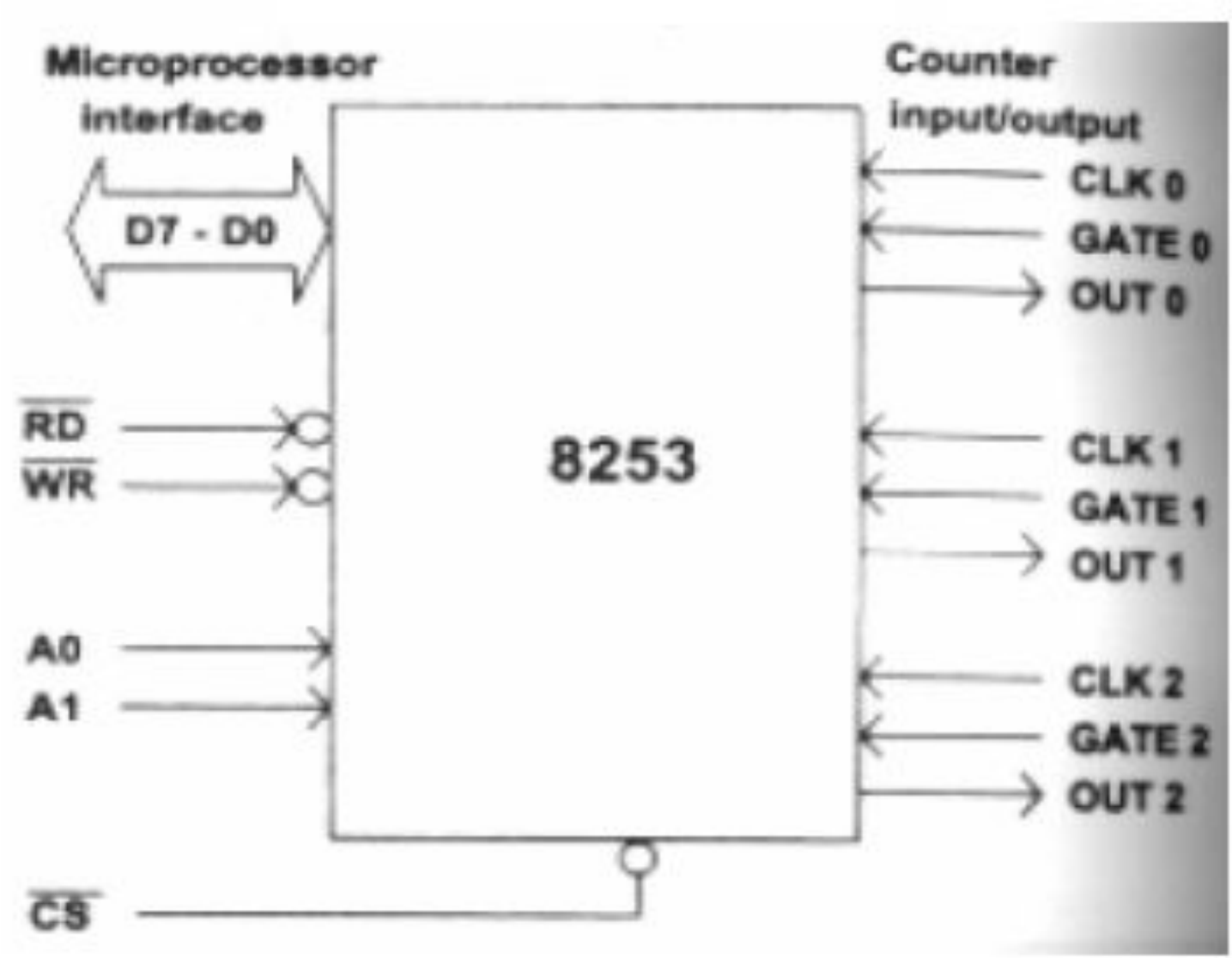
Block Diagram of 8254/8253

- **Counters**
- There are 3 counters (or timers), which are labeled as "Counter 0", "Counter 1" and "Counter 2.
- Each counter has 2 input pins – "CLK" (clock input) and "GATE" and 1-pin, "OUT", for data output.
- The 3 counters are 16-bit down counters independent of each other, and can be easily read by the CPU.

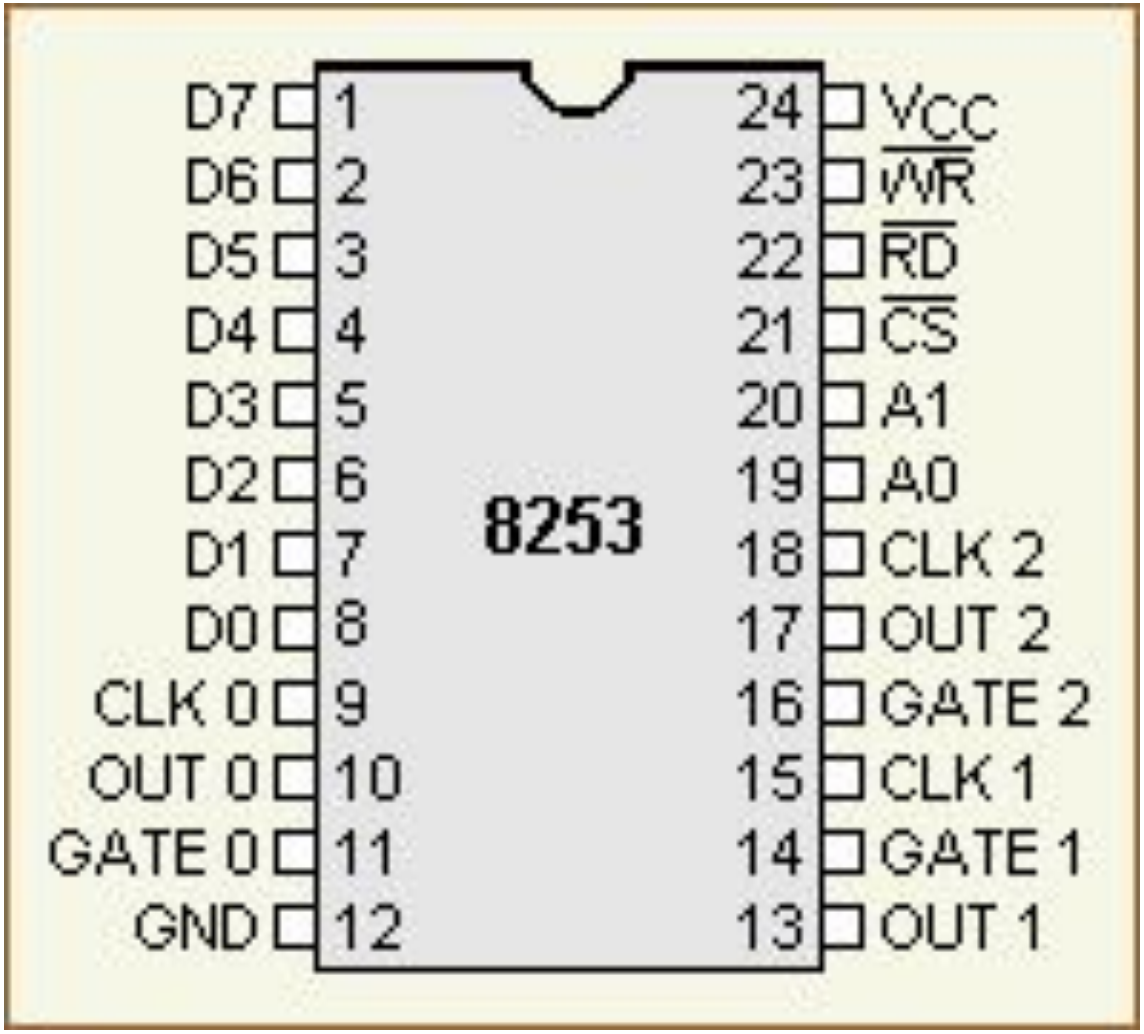
Block Diagram of 8254/8253

- Counters are programmed by writing a Control Word and then an initial count.
- GATE=1 enables counting, GATE=0 disables counting.
- All 3 counters are 16-bits.
- PIT has only an 8-bit data bus and can read or write only one byte at a time.
- Thus to read or write a 16-bit value, you must do so one byte at a time.

SIGNALS OF 8254/8253



Pin Diagram of 8254/8253



Pin Diagram of 8254/8253

Symbol	Pin No.	Type	Name and Function
D7-D0	1 - 8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUTPUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
VCC	24		POWER: A 5V power supply connection.
$\overline{WR}$	23	I	WRITE CONTROL: This input is low during CPU write operations.
RD	22	I	READ CONTROL: This input is low during CPU read operations.

Pin Diagram of 8254/8253

<table>
<tr><td>CS</td><td>21</td><td>I</td><td>CHIP SELECT: A low on this input enables the 8254 to respond to RD and WR signals. RD and WR are ignored otherwise.</td></tr>
<tr><td>A1, A0</td><td>20 – 9</td><td>I</td><td>ADDRESS: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
<table>
<tr><th>A1</th><th>A0</th><th>Selects</th></tr>
<tr><td>0</td><td>0</td><td>Counter 0</td></tr>
<tr><td>0</td><td>1</td><td>Counter 1</td></tr>
<tr><td>1</td><td>0</td><td>Counter 2</td></tr>
<tr><td>1</td><td>1</td><td>Control Word Register</td></tr>
</table></td></tr>
<tr><td>CLK 2</td><td>18</td><td>I</td><td>CLOCK 2: Clock input of Counter 2.</td></tr>
<tr><td>OUT 2</td><td>17</td><td>O</td><td>OUT 2: Output of Counter 2.</td></tr>
</table>

Pin Diagram of 8254/8253

GATE 2	16	I	GATE 2: Gate input of Counter 2.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
OUT 1	OUT 1	O	OUT 1: Output of Counter 1.

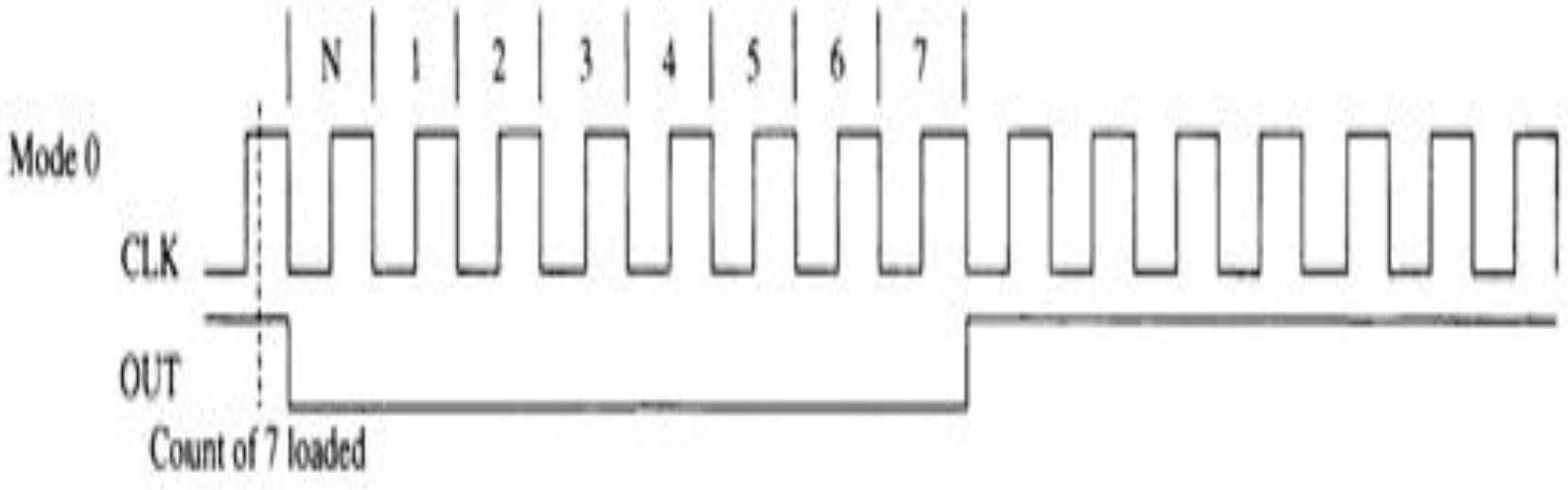
Operating Modes PIT 8254

- There are **six modes of operation for the counters.**
- In all modes the **counters operate as down counters.**
- They are defined as follows:
- Mode 0: Interrupt on Terminal Count/ Event counter
- Mode 1: Hardware Re triggerable One-Shot
- Mode 2: Rate Generator
- Mode 3: Square Wave Mode
- Mode 4: Software Triggered Strobe
- Mode 5: Hardware Triggered Strobe (Re triggerable)

Operating Modes PIT 8254

- **MODE 0: Interrupt on terminal count**

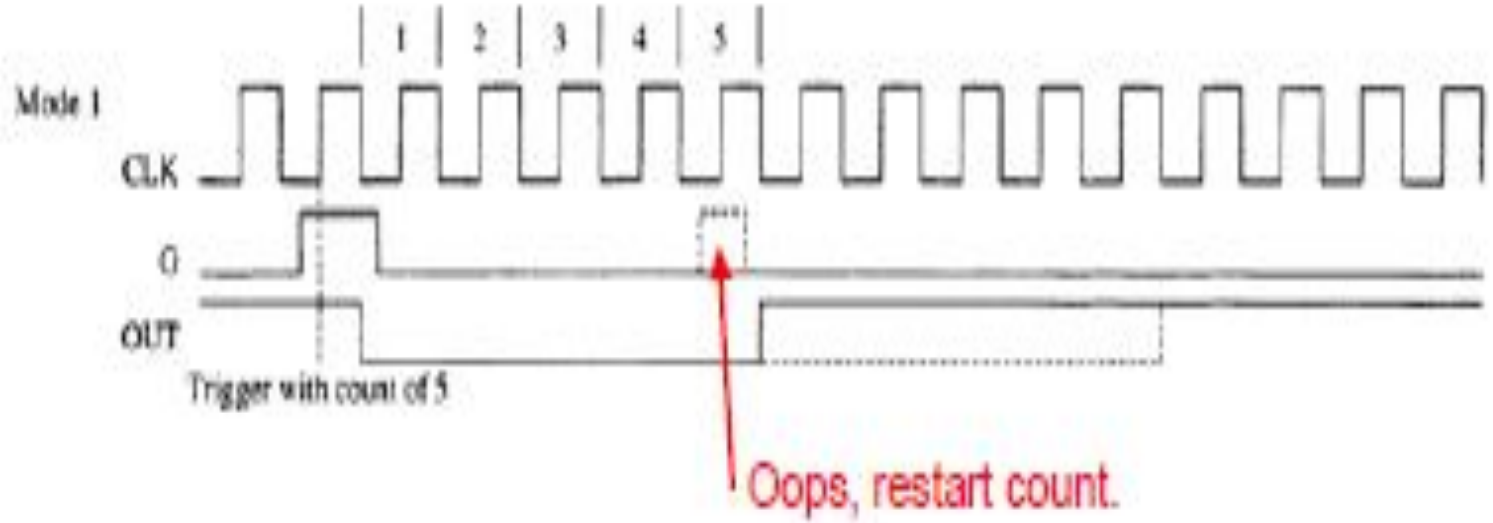
  1. Event counting.
  2. After the Control Word is written, OUT is initially low and remains low.
  3. When the counter reaches zero. OUT then goes high and remains high until a new count.



Operating Modes PIT 8254

- **MODE 1: Hardware retriggerable one-shot**

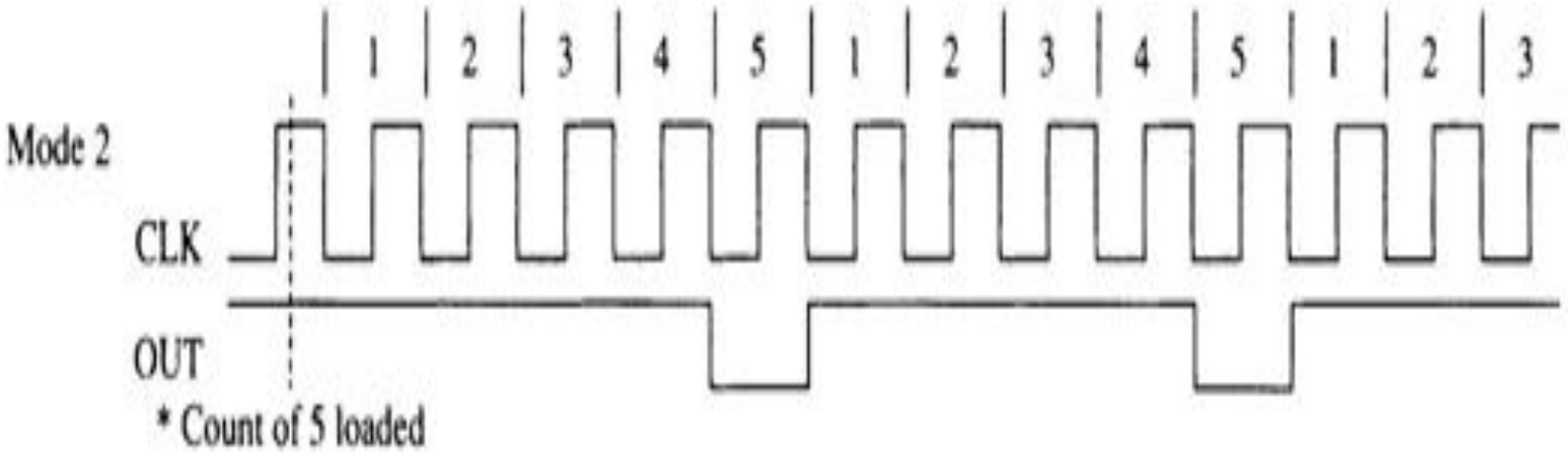
  1. OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and remain low until the Counter reaches zero.
  2. OUT will then go high and remain high until the CLK pulse after the next trigger.



Operating Modes PIT 8254

- **MODE 2: Rate generator**

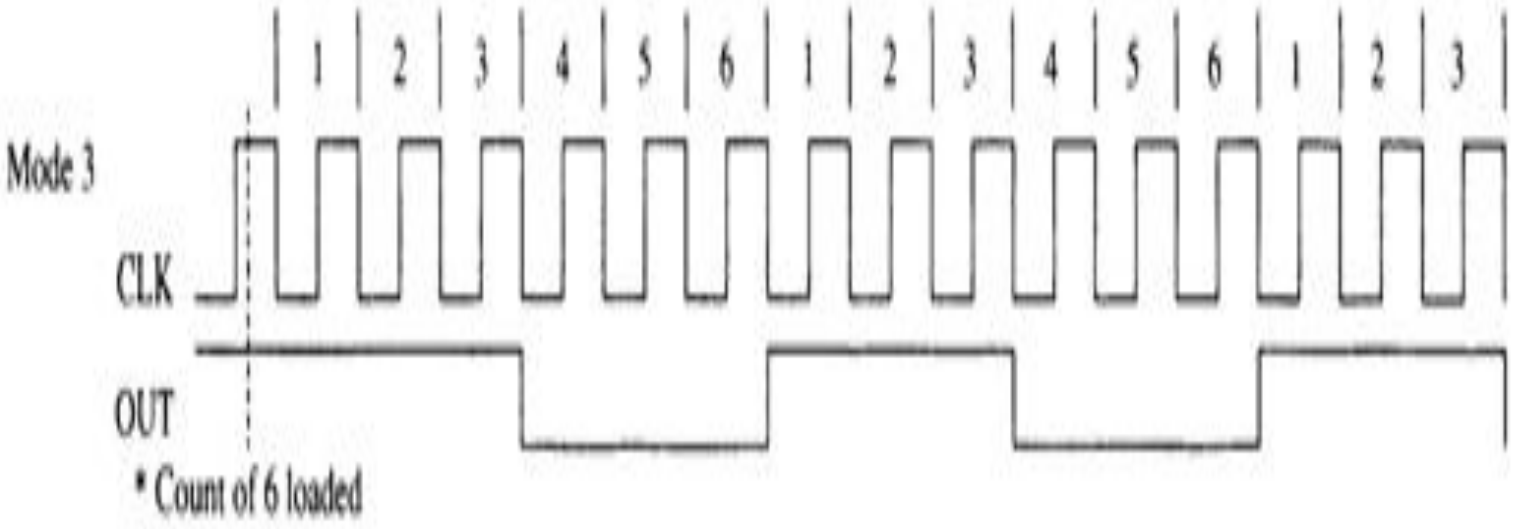
  1. Functions like a divide-by-N counter and used to generate a Real Time Clock interrupt.
  2. OUT will initially be high.
  3. When the initial count has expired, OUT goes low for one CLK pulse.
  4. Out then goes high again, the Counter reloads the initial count and the process is repeated.
  5. MODE 2 is periodic. The same sequence is repeated indefinitely.



Operating Modes PIT 8254

- **MODE 3: Square wave mode**

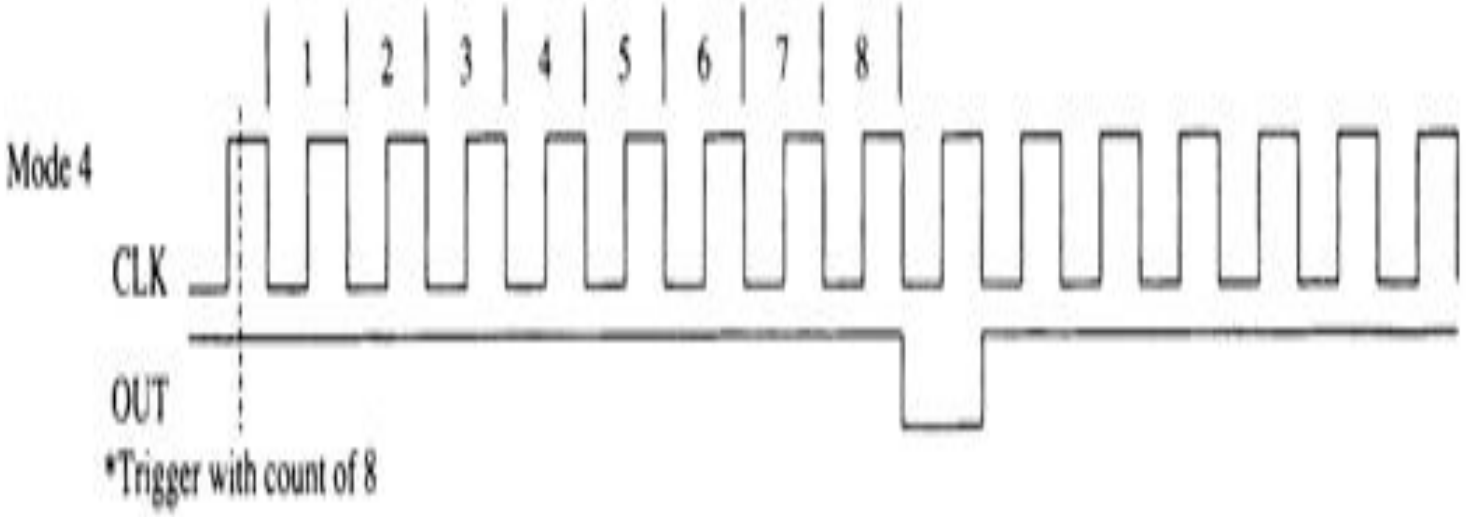
  1. Typically used for baud rate generation.
  2. Out will initially be high.
  3. When half the initial count is expired, OUT goes low for the remainder of the count.
  4. MODE 3 is periodic. The same sequence is repeated indefinitely.



Operating Modes PIT 8254

- **MODE 4: Software triggered strobe**

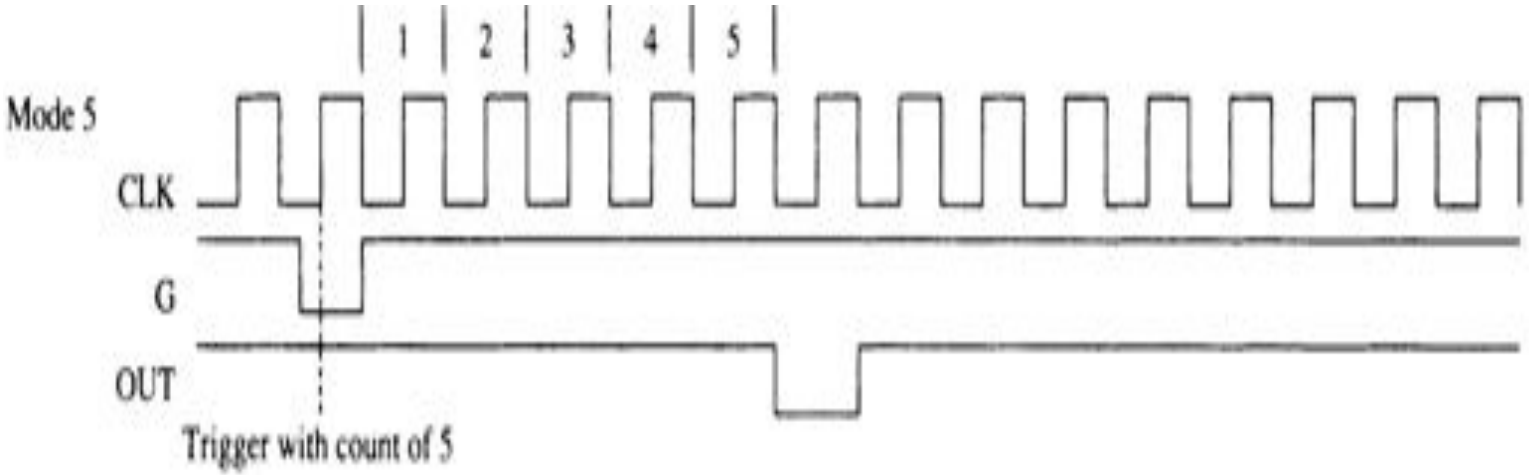
  1. OUT will initially be high.
  2. When the initial count expires, OUT will go low for one CLK pulse and then go high again.
  3. The counting sequence is "triggered" by writing the initial count.
  4. The Counter is loaded on the next CLK pulse following writing a Control Word and initial count.



Operating Modes PIT 8254

- **MODE 5: Hardware triggered strobe (retriggerable)**

  1. OUT will initially be high.
  2. Counting is triggered by a rising edge of GATE.
  3. When the initial count expires, OUT will go low for one CLK pulse and then go high again.
  4. The difference between MODE 4 and MODE 5 is that in MODE 5 the count will not be loaded until the CLK pulse after a trigger.



Programming of 8254

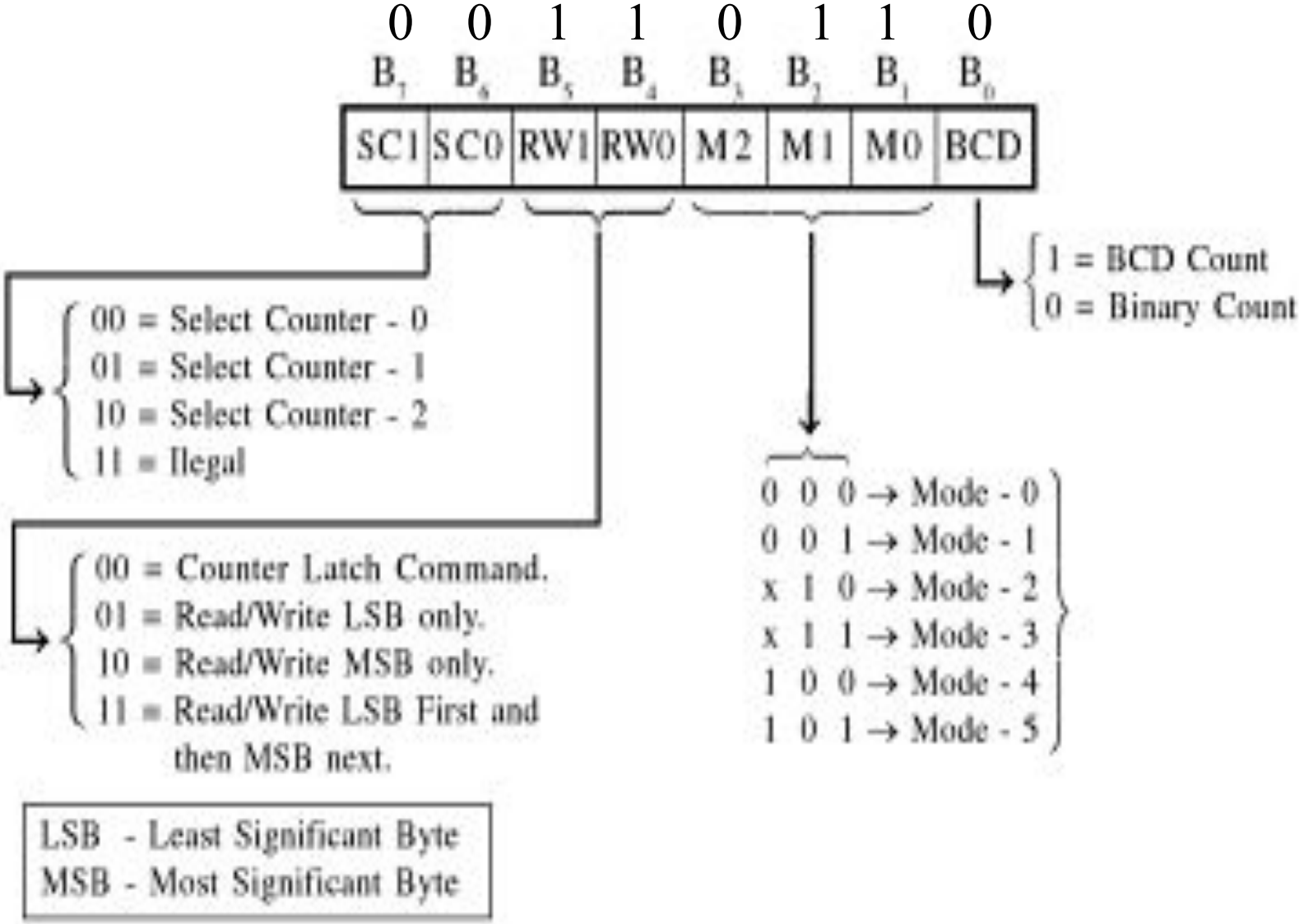
1. Counters are programmed by writing a Control Word and then an initial count.

2. Control Words are written into the Control Word Register, which is selected when A0,A1=11. The Control Word itself specifies which Counter is being programmed.

3. Initial counts are written into the Counters, not the Control Word Register. The A0,A1 inputs are used to select the Counter to be written into.

4. The format of the initial count is determined by the Control Word used.

Control Word of PIT 8254



Control Word of PIT 8254

- There are 5 steps to calculate the proper control word number:

- Step 1: Chose one counter (SC1 and SC0)
- Step 2: Chose method to load (RW1 and RW0)
- Step 3: Chose programming mode (M2, M1 and M0)
- Step 4: Chose binary or BCD number (BCD).
- Step 5: Convert the final binary word into decimal

Control Word of PIT 8254

- **Example** Suppose you want to make counter 0 a binary counter that generates square waves, and uses LSB and MSB read/write loading. What is the proper control word? Assuming COUNT = 2500H, Write a program for square wave generation if Port addresses are 90H,91H, 92H,93H for Counter0, Counter 1, Counter 2 & CWR

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	0

Example has the 8-bit control word = 00110110 binary which in decimal is equal to 54

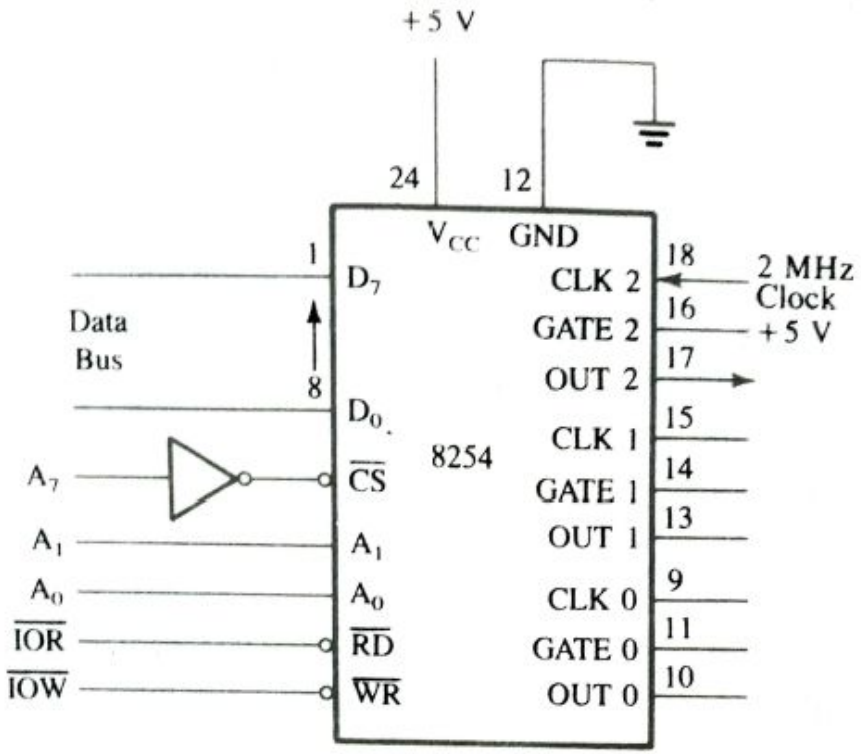
Control Word of PIT 8254

- A0 and A1 select one of the three counters or the control word register to be read from/written into as specified in the following table.

A1	A0	Selected Block
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Reg.

- MVI A, 36H
- OUT 93H
- MVI A,00H
- OUT 90H
- MVI A,25H
- OUT 90H

IDENTIFY PORT ADDRESS FOR GIVEN CIRCUIT AND WRITE A PROGRAM FOR INITIALIZING COUNTER 1 WITH 50000 COUNT VALUE.

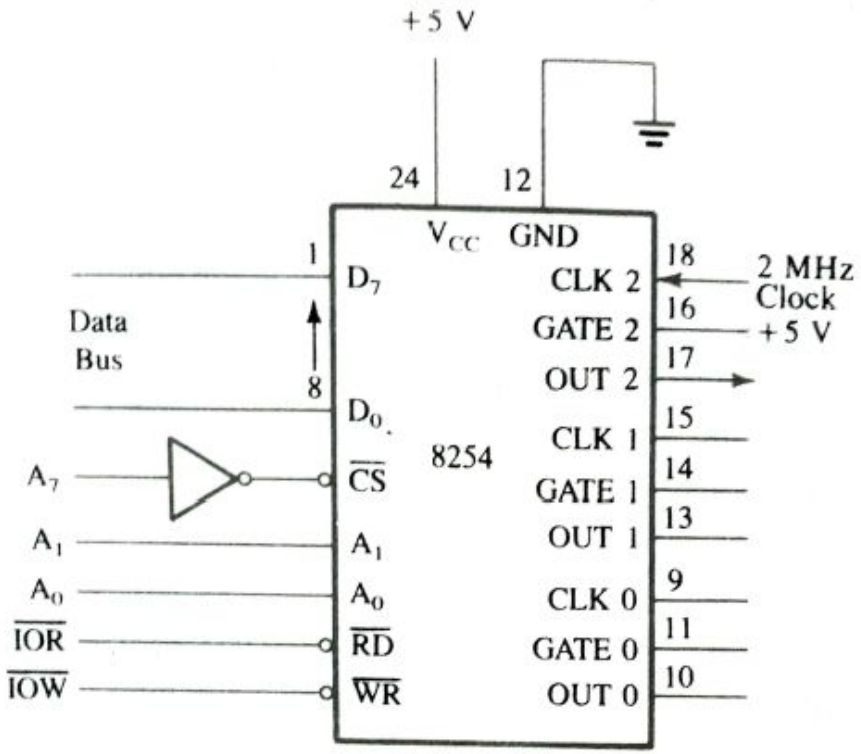


Solution: COUNT=50000 = C350H

*MAXIMUM COUNT VALUE IN BCD IN 4 DIGITS CAN BE 9999 AND IN HEX FFFF equal to 65535.

- **Port Address**
- A7A6A5A4A3 A2A1A0
- 1 0 0 0 0 0 0 0-80H-COUNTER0
- 1 0 0 0 0 0 0 1-81H-COUNTER1
- 1 0 0 0 0 0 1 0-82H-COUNTER2
- 1 0 0 0 0 0 1 1-83H-CWR
- MVI A, 0111 0000B (70H)
- OUT 83H
- MVI A, 50H
- OUT 81H
- MVI A, C3H
- OUT 81H
- HLT

Identify port address for given circuit and Write a program for generating a pulse after every 50us



Solution: Clock frequency = 2 MHz , Clock Time=1 / 2MHz = 0.5 us

Frequency of Pulse=1/T = 1 / 50us

Count = 2MHz / 20KHz or 50us/0.5us

Count=100 = 64H

- **Port Address**
- A7A6A5A4A3 A2A1A0
- 1 0 0 0 0 0 0 0-80H-COUNTER0
- 1 0 0 0 0 0 0 1-81H-COUNTER1
- 1 0 0 0 0 0 1 0-82H-COUNTER2
- 1 0 0 0 0 0 1 1-83H-CWR
- MVI A, 1001 0100B (94H)
- OUT 83H
- MVI A, 64H
- OUT 82H
- HLT

Q. WAP for generation of square wave with 1KHz frequency using counter1 if CLK= 1MHz.

Solution

1.

Control Word Counter1 is selected in mode3 used for square wave generation. **Control Word = 01110111=77 H**

2.

Port Address for Counter0 is 80H
Port Address for Counter1 is 81H
Port Address for Counter2 is 82H
Port Address for Control word register is 83H

3.

Count=Given frequency/Required frequency=1 MHz/ 1 KHz =1000

4.

Program

```
MVI A, 77H
OUT 83H
MVI A, 00       ;TO LOAD NO. OF COUNTS LOW BYTE FIRST i.e. 00
OUT 81H           ; to port address 81H
MVI A, 10       ;TO LOAD NO. OF COUNTS HIGH BYTE NEXT i.e. 10
OUT 81H          ; to port address 81H
```

Q. WAP for generation of 1ms square wave with counter1 if CLK Period= 0.5us.

Solution

1.

Control Word Counter1 is selected in mode3 used for square wave generation.

Control Word = 01110110=76 H

2.

Port Address for Counter0 is 80H
Port Address for Counter1 is 81H
Port Address for Counter2 is 82H
Port Address for Control word register is 83H

3.

Count= Required time/ Given clock time period=1 ms/ 0.5 us =2000= 07D0H

4.

Program

```
MVI A, 76H
OUT 83H
MVI A, D0H    ;TO LOAD NO. OF COUNTS LOW BYTE FIRST i.e. 00
OUT 81H         ; to port address 81H
MVI A, 07H    ;TO LOAD NO. OF COUNTS HIGH BYTE NEXT i.e. 10
OUT 81H        ; to port address 81H
```