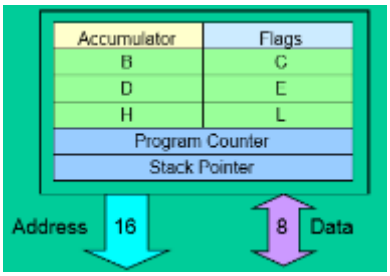
MICROPROCESSOR

Q1 Draw the programming model of 8085 microprocessor.

Solution:



Q2 What is address bus, data bus and control bus in microprocessor based systems?

Solution:

System Bus –wires connecting memory & I/O to microprocessor**.**

Address Bus
- Unidirectional
- Identifying peripheral or memory location

Data Bus
- Bidirectional
- Transferring data

Control Bus
- Synchronization signals
- Timing signals
- Control signal

Q3 What is ISR (Interrupt Service Routine)? List down pins on 8085 microprocessor for interrupt. How many interrupts are there in 8085 microprocessor? State highest priority interrupt and least priority interrupt.

Solution: ISR (Interrupt Service Routine): When microprocessor is executing a program it is called as main program and if it is interrupted, it will execute current instruction and branch from main program to sub-program called as Interrupt Service Routine. Afte execution of ISR it will return back to main program.

Interrupt Pins

TRAP, RST7.5, RST 6.5, RST 5.5, INTR, $\overline{INTA}$

There are 5 interrupts in 8085 microprocessor.

TRAP, RST7.5, RST 6.5, RST 5.5, INTR.

***TRAP is the highest priority interrupt*. INTR is the least priority interrupt.**

Q4 How many address lines, data lines are available on memory chip having size of 16Kx8?

Solution:

16K x 8= 2^{14}x8

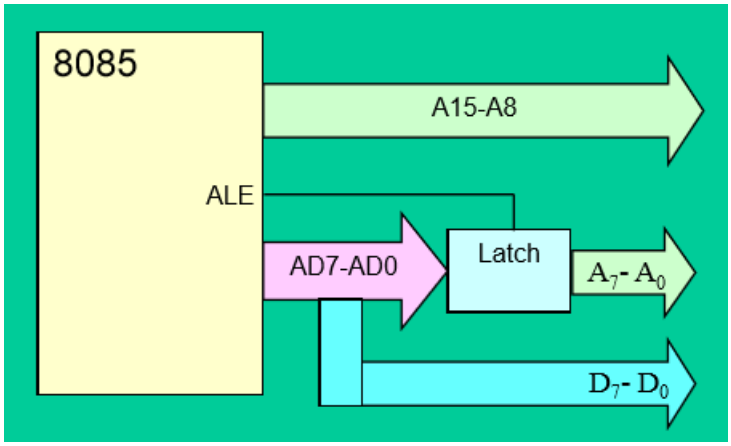
Address lines-14

Data lines-8

Q5 Why multiplexing is done in microprocessor? How multiplexing of address/data bus is done?

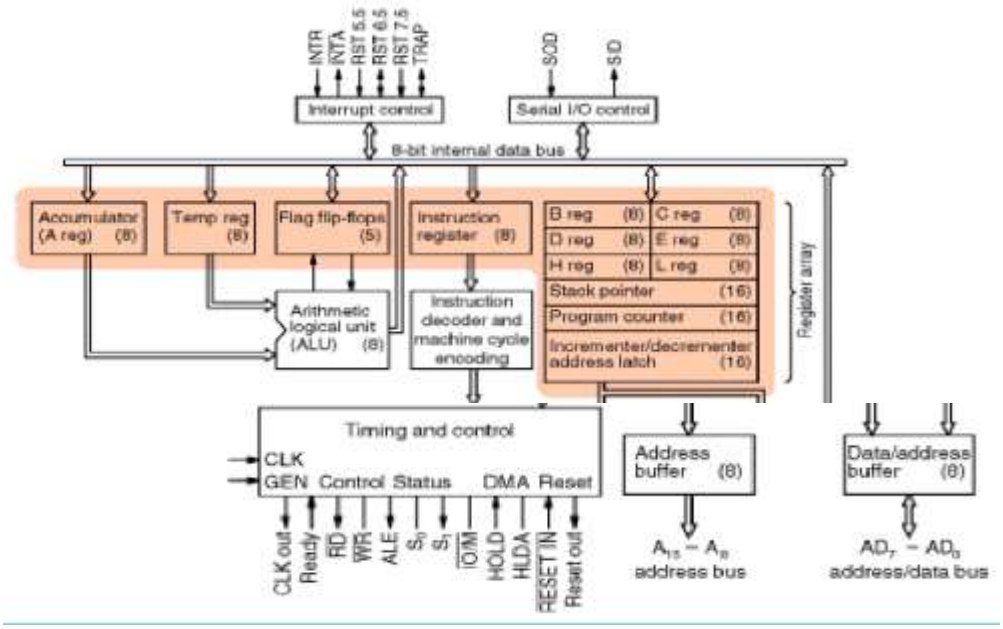
Solution:

- Multiplexing is used to reduce the number of pins and to reduce chip area.
- The address bus has 8 signal lines A8-A15 which are unidirectional and other eight address lines are multiplexed(Time shared) with 8 data lines So the bits AD0 –AD7 In 8085 microprocessor are bi-directional and serve as A0 –A7and D0 –D7at the same time.
- During the execution of the instruction, these lines carry the address bits during the early part, then during the late parts of the execution, they carry the 8 data bits.
- In order to separate the address from the data, we can use a latch to save the value before the function of the bits changes and using ALE to enable the latch.
- The higher order bits of the address remain on the bus for three clock cycles however lower order bits remain only for one clock cycle.
- To make sure we have the entire address for first three clock cycles, we will use an external latch 74LS373 to save the value of AD0-AD7 when it is carrying the address. ALE signal is used to enable the latch.



Q6Explain the architecture of 8085 microprocessor with block diagram.

Solution:



- 8-bit general purpose µp
- Capable of addressing 64 k of memory
- Has 40 pins • Requires +5 v power supply
- Can operate with 3 MHz clock
- 8085 upward compatible

Microprocessor consists of: –

- **ALU:** Arithmetic Logic Unit: It performs data processing function. It includes Accumulator,,temperorary register, arithmetic and logical circuits and five flags.Temporary register is used for holding data temporarily during the execution of the operation. This temporary register is not accessible by the programmer.Accumulator, is 8 bit register which is part of every arithmetic & logic operation. It holds 8 bit data and also stores the result. After every ALU operation flag will be affectrd.
- **General Purpose Registers**(six in number)that provide storage internal to CPU. These are B, C, D, E, H& L(8 bit registers) Can be used singly Or can be used as 16 bit register pairs – BC, DE, HL • H & L can be used as a memory pointer (holds memory address). It includes W and Z temperory registers to hold the data internally and not accessible by user.
- **Flag Register** – 8 bit register –shows the status of the microprocessor before/after an operation – S (sign flag), Z (zero flag), AC (auxiliary carry flag), P (parity flag) & CY (carry flag)
- **The Program Counter (PC)** – This is a register that is used to control the sequencing of the execution of instructions. – This register always holds the address of the next instruction. – Since it holds an address, it must be 16 bits wide.
- **The Stack pointer** – The stack pointer is also a 16-bit register that is used to point into memory. – The memory this register points to is a special area called the stack. – The stack is an area of memory used to hold data that

will be retrieved soon. – The stack is usually accessed in a Last in First out (LIFO) fashion.

- **Non Programmable Registers(Instruction Register)& Decoder** – Instruction is stored in IR after fetched by processor – Decoder decodes instruction in IR
- **Timing and Control unit:**This unit synchronizes all the microprocessor operations with the clock and generates control signals necessary for communication between the microprocessor and peripherals.
- **Interrupt Control Unit** accepts interrupt request fom*TRAP, RST7.5, RST 6.5, RST 5.5, INTR* pins and generates $\overline{INTA}$ Interrupt acknowledgement signal after getting INTR interrupt request.
- **Serial I/O Control unit** is used for serial (bit by bit) input output operation.SID for serial input line and SOD for serial output line.

Q7 Explain with an example various types of addressing modes supported by 8085 microprocessor.

Solution:

There are five addressing modes in 8085.

1. Immediate Addressing Mode: - An immediate is transferred directly to the register.

E.g.: - MVI A, 30H (30H is copied into the register A)

MVI B,40H(40H is copied into the register B).

2. Register Addressing Mode: - Data is copied from one register to another register.

E.g.: - MOV B, A (the content of A is copied into the register B)

MOV A, C (the content of C is copied into the register A).

3. Direct Addressing Mode: - Data is directly copied from the given address to the register.

E.g.: - LDA 3000H (The content at the location 3000H is copied to the register A).ndirect Addressing Mode: - The data is transferred from the address pointed by the data in a register to other register.

E.g.: - MOV A, M (data is transferred from the memory location pointed by the register to the accumulator).

5. Implied Addressing Mode: - This mode doesn't require any operand. The data is specified by opcode itself.e.g: - RAL, CMA

Q8 Describe register organization of 8085 microprocessor listing all 8-bit and 16-bit registers.

Solution: Registers –

- General Purpose Registers B, C, D, E, H& L(8 bit registers) Can be used singly Or can be used as 16 bit register pairs BC, DE, HL • H & L can be used as a data pointer (holds memory address)

Special Purpose Registers

- Accumulator(8 bit register) – Store 8 bit data – Store the result of an operation – Store 8 bit data during I/O transfer
- Flag Register – 8 bit register –shows the status of the microprocessor before/after an operation – S (sign flag), Z (zero flag), AC (auxiliary carry flag), P (parity flag) & CY (carry flag)
- The Program Counter (PC) – This is a register that is used to control the sequencing of the execution of instructions. – This register always holds the address of the next instruction. – Since it holds an address, it must be 16 bits wide.
- The Stack pointer – The stack pointer is also a 16-bit register that is used to point into memory. – The memory this register points to is a special area called the stack. – The stack is an area of memory used to hold data that will be retrieved soon. – The stack is usually accessed in a Last in First out (LIFO) fashion.
- Non Programmable Registers
  • Instruction Register & Decoder – Instruction is stored in IR after fetched by processor – Decoder decodes instruction in IR

Q9 Explain and draw pin diagram of 8085 microprocessor with classification of signals and directions.

Solution

Microprocessor - 8085 Pin Configuration

- **Address bus**. A15-A8, it carries the higher **8-bits** of memory/IO address and is unidirectional
- **Multiplexed Address/Data bus**. **AD7-AD0**, it carries the lower 8-bit address and data bus . During execution of instruction, in earlier part of the cycle it carries the lower order address and in later cycle it carries the data
- **Control and status signals**.

  - $IO/\overline{M}$: This is a status signal used to differentiate between I/O and memory operation. When it is high it indicates I/O operation and when it is low it indicates memory operations.
  - S1 & S0: These signals are the status signals and identify various operations:

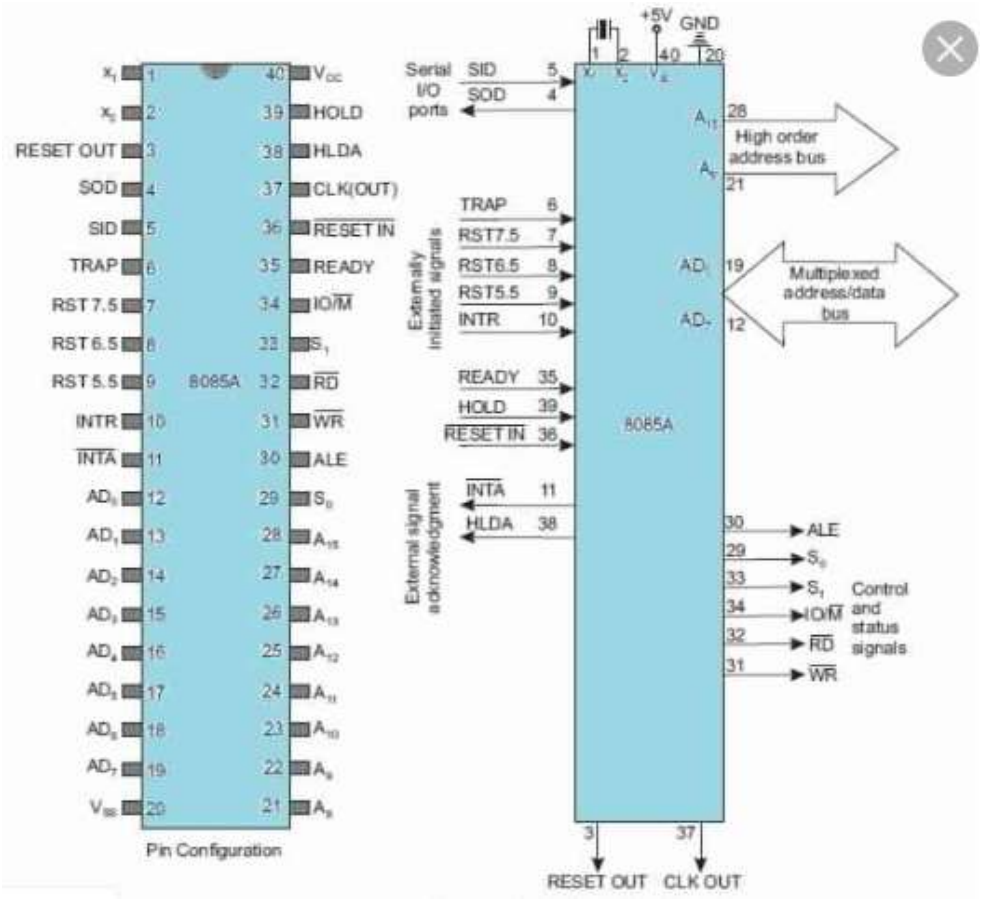
Machine Cycle	Status $IO/\overline{M}$	S_1	S_0	Control Signals
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	

- $\overline{RD}$: Active low read control signal: This signal indicates selected memory or I/O device is to be read and data is available on data bus.
- $\overline{WR}$: Active low write control signal: This signal indicates data on data bus is to be written to selected memory or I/O device.
- ALE: Address Latch Enable: This signal is used to demultiplex Address/ Data bus.When microprocessor starts an operation it makes ALE signal high to indicate address is available on address bus and then ALE gets low to indicate this bus is used as data bus.

- Power and frequency signal:
- VCC: +5V Power supply
- Vss: Ground
- X1 X2 :A crystal of frequency 6MHz is connected cross X1, X2 pins and it is divided by microprocessor internally to be operated at 3MHz frequency.
- CLK(OUT): This can be used as system clock for other devices.

- Externally Initiated **Signals**
  There are five interrupt signals that can be used to interrupt a program *TRAP, RST7.5, RST 6.5, RST 5.5, INTR*.
- TRAP : Non-maskable interrupt and has highest priority
- INTR: General purpose interrupt and least priority interrupt.
- RST 7.5, RST 6.5, RST 5.5 : Restart interrupt: vectored interrupt that transfers the control to specific memory location. Priority of RST 7.5 is highest then RST 6.5 and then RST 5.5.
- Hold: This pin is used by DMA (Direct Memory Access)Controller to request microprocessor to release their buses.
- Ready:This pin is used to synchronize microprocessor with slow peripherals. When READY is low microprocessor is in wait state and waits for slow peripheral to accept or receive data.
- $\overline{RESETIN}$: When low signal is applied across this pin it resets the microprocessor . When microprocessor is reset it suspends all operations and Program Counter is initialized to Zero.

- Acknowledgement Signals:
- $\overline{INTA}$: Interrupt Acknowledgement Signal:This signal is used to acknowledge the interrupt.
- HLDA: This signal is used to acknowledge the hold request.



Q10 Write the format for flag register and explain each flag bit. Determine the final status of flag register and contents of accumulator register after execution of following program:

MVI A, 28H
INR A
XRA A
ADI 48H
ADD A
HLT

Solution:FlagRegister:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		CY

ZERO FLAG (Z): This flag is set to a 1 by the instruction just ending if the A Register contains a result of all 0's. Besides the obvious mathematical applications, this is useful in determining equality in a compare operation (a value subtracted from a second value with an answer of 0), or in logical AND or OR operations where the result left the A Register with no bit set to a 1 (the AND was not satisfied). If any bits were left set to a 1 in the A Register, the flag will be reset to a 0 condition.

SIGN FLAG(S): This flag is set to a 1 by the instruction just ending if the leftmost, or highest order, bit of the A Register is set to a 1. The leftmost bit of a byte in signed arithmetic is the sign bit, and will be 0 if the value in the lower seven bits is positive, and 1 if the value is negative.

PARITY FLAG(P): This flag is set to a 1 by the instruction just ending if the A Register is left with an even number of bits set on, i.e., in even parity. If the number of bits in the A Register is odd, the bit is left off. This may be useful in I/O operations with serial devices, or anyplace that error checking is to be done.

CARRY FLAG (CY): This flag is set to a 1 by the instruction just ending if a carry out of the leftmost bit occurred during the execution of the instruction. An example would be the addition of two 8-bit numbers whose sum was 9 bits long. The 9th bit would be lost, yielding an erroneous answer if the carry bit was not captured and held by this flag. This flag is also set if a borrow occurred during a subtraction or a compare operation.

AUXILIARY CARRY FLAG (AC): This flag is set to a 1 by the instruction just ending if a carry occurred from bit 3 to bit 4 of the A Register during the instruction's execution. Because of the relationships of decimal in pure BCD to hexadecimal coding, it is possible to bring BCD values directly into the A Register and perform mathematical operations on them. The result, however, will be as if two hex characters are being processed. If the result must be returned to the program as BCD rather than as hex, the Decimal Adjust Accumulator (DAA) instruction can make that translation; the Auxiliary Carry Flag is provided to assist in this operation.

MVI A, 28H
INR A
XRA A
ADI 48H
ADD A
HLT
Status of Accregister : 90H

Flag register: S = 1, Z = 0, AC = 1, P = 1, CY = 0

Q11 What do you mean by instruction cycle, machine cycle and T-state?
(a)Draw the timing diagram for MVI B,49H of 8085 microprocessor.
(b) Draw timing diagram for MOV A,B
(c)Draw the timing diagram for IN C0H of 8085 microprocessor.
(d)Draw the timing diagram for OUT C0H of 8085 microprocessor.

Solution:

Instruction Cycle:

The time required to execute an instruction

Machine Cycle:

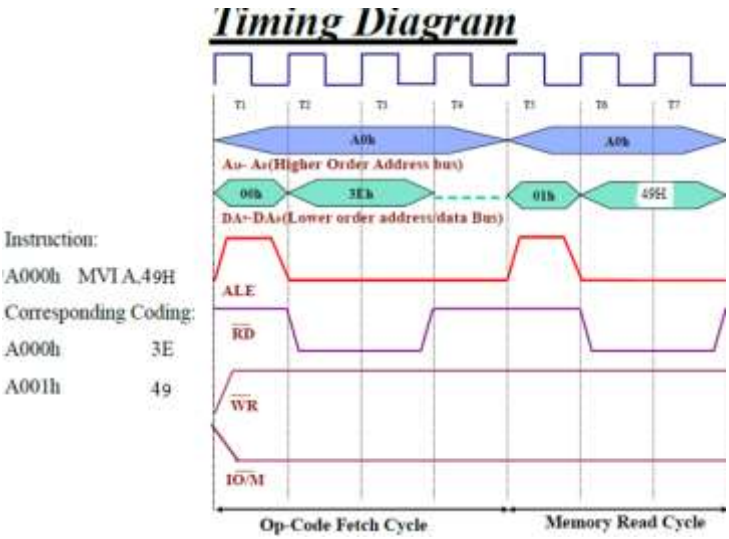
The time required to access the memory or input/output devices .

T-State:

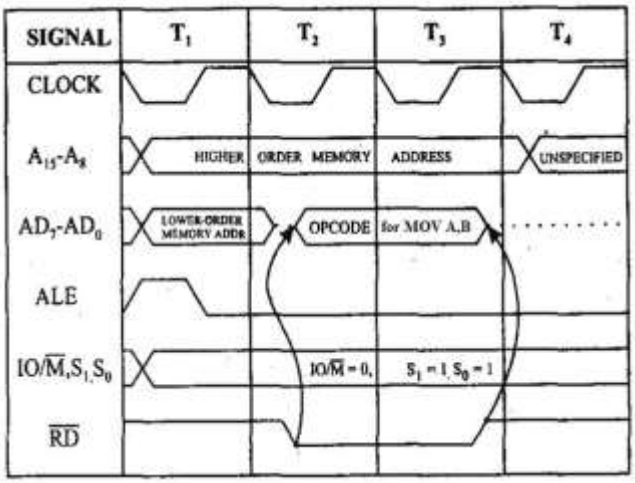
•The machine cycle and instruction cycle takes multiple clock periods.

•A portion of an operation carried out in one system clock period is called as T-state.

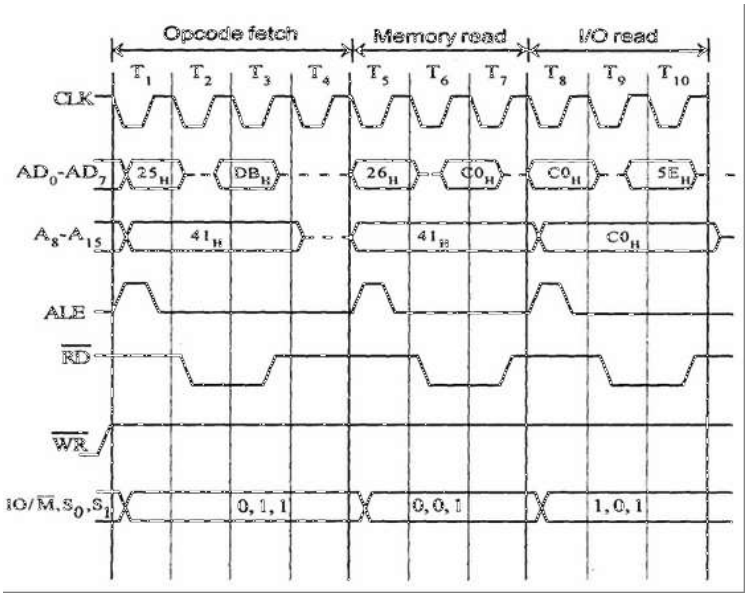
(a) Timing Diagram MVI A, 49H



(B) TIMING DIAGRAM MOV A,B

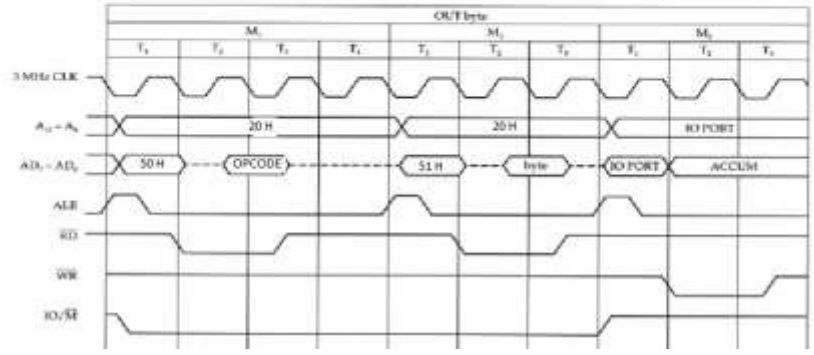


(C) Timing Diagram of IN C0 H

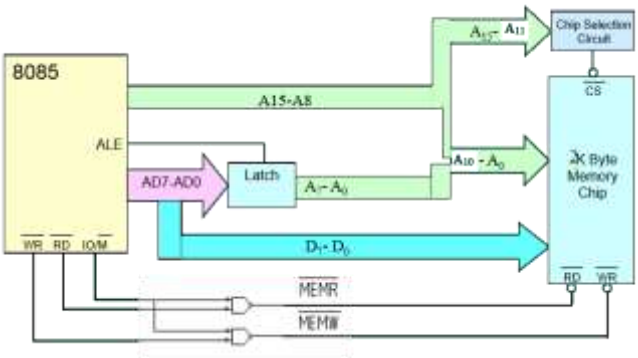


(D) TIMING DISAGRAM OF OUT 85 H

Intel 8085 OUT Instruction Timing Diagram



Q12. **Explain interfacing of 8085 microprocessor with 2K x 8 memory using diagrams. Give its address range illustrating address decoding table if the starting address is 8800H.**



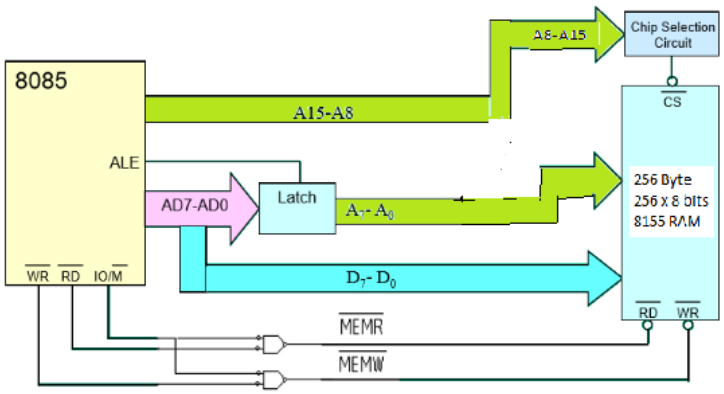
Solution:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

NOTE: ** 8155/8156 (RAM) is 256 X 8
8355/8755 (ROM) is 2K X 8

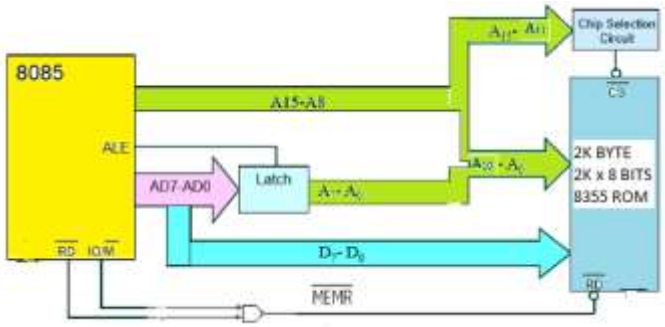
Q13 Draw interfacing of 8085 microprocessor with 256 Byte RAM memory in 8155 RAM . Give its address range illustrating address decoding table.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	MEMORY ADDRESS
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	8800 H
1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	88FF H



Q14 Draw interfacing of 8085 microprocessor with 2KB ROM memory in 8355 CHIP. Give its address range illustrating address decoding table.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	MEMORY ADDRESS
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	8800 H
1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	8FFF H



Q15 Explain the following pins of 8085 microprocessor

$$(i)\overline{RD}\&\overline{WR}(ii)ALE(iii)HOLD(iv)\ IO/\overline{M}(v)\overline{INTA}\ \ (vi)\overline{RESETIN}$$

Solution:

(i) RD* and WR*:

RD*(output 3-state, active low)

- Read memory or IO device.
- This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device

WR*(output 3-state, active low)

- Write memory or IO device.

- This indicates that the data on the data bus is to be written into the selected memory location or I/O device.

(ii) ALE (Address Latch Enable)

- It is an output signal used to give information of AD0-AD7 contents.
- It is a positive going pulse generated when a new operation is started by uP.
- When pulse goes high it indicates that AD0-AD7 are address.
- When it is low it indicates that the contents are data.

(iii) HOLD: HOLD signal is generated by the DMA controller circuit. On receipt of this signal, the microprocessor acknowledges the request by sending out HLDA signal and leaves out the control of the buses. After the HLDA signal the DMA controller starts the direct transfer of data.

(iv) IO/M* : Select memory or an IO device.

- This status signal indicates that the read / write operation relates to whether the memory or I/O device.
- It goes high to indicate an I/O operation.
- It goes low for memory operations.

(v) INTA*: On receipt of an interrupt, the microprocessor acknowledges the interrupt by the active low INTA (Interrupt Acknowledge) signal.

(vi) RESETIN* (input, active low)

- This signal is used to reset the microprocessor.
- The program counter inside the microprocessor is set to zero.
- The buses are tri-stated.

Q16. Explain Instruction set of 8085 microprocessor.

Solution It is classified into 5 categories:

1. Data Transfer Instruction Set
2. Arithmetic Instruction Set
3. Logical Instruction Set
4. Branching Instruction Set
5. Machine Control Instruction

1. Data Transfer Instruction Set

S.No.	Instruction and Operation	Example	No. of Bytes	Machine Cycle	T-State	Addressing Mode
1	MOV Rd, Rs Data is copied from one register to other	MOV C,A	1	1	4	Register
2	MVI R, DATA Data is copied to one register directly	MVI A,45 H	2	2	7	Immediate
3	LXI Rp, 16 bit data Data is loaded to register pair	LXI H, 4200 h	3	3	10	Immediate
4	LDA 16 BIT ADDRESS Data is transferred from memory address specified to register	LDA 4200	3	4	13	Direct
5	STA 16 BIT ADDRESS Data is copied from register to memory address specified	STA 2500 H	3	4	13	Direct
6	IN 8 BIT PORT ADDRESS Data is copied from I/O Device to Accumulator Register	IN C0 H	2	3	10	Direct
7	OUT 8 BIT PORT ADDRESS Data is copied from accumulator to I/O device	OUT 85 H	2	3	10	Direct
8	MOV R,M Data is copied from memory to registrer where M is the address held by HL Register pair	MOV A,M	1	2	7	Indirect

2. Arithmetic Instruction Set

S.No.	Operation	Example	No. of Bytes	Machine Cycle	T-State	Addressing Mode

1	ADD R - Register content is added with Accumulator content	ADD C	1	1	4	Register
2	ADI 8BIT -Accumulator is added with 8 bit data	ADI 45 H	2	2	7	Immediate
3	ACI 8 BIT- ADD IMMEDIATE DATA TO ACCUMULATOR WITH CARRY	ACI 28 H	2	2	7	Immediate
4	ADC R -ADD Accumulator data with register	ADC B	1	1	4	Register
5	SUB R - Register content is subtracted from accumulator	SUB C	1	1	4	Register
6	SUI 8BIT - 8 bit data is subtracted from accumulator	SUI 80 H	2	2	7	Immediate
7	SBI 8BIT- Subtract 8 bit data and borrow from accumulator	SBI 50 H	2	2	7	Immediate
8	SBB R -Subtract register content with borrow from accumulator	SBB D	1	1	4	Register
9	INR R -Increment the content of Register	INR C	1	1	4	Register
10	DCR R- Decrement the content of register	DCR D	1	1	4	Register
11	INX Rp -Increment the content of register pair	INX H	1	3	10	Register
12	DCX Rp -Decrement the content of register pair	DCX H	1	3	10	Register
13	ADD M- Add contents of accumulator with M where M is the address held by HL Register pair	ADD M	1	2	7	Indirect

3. Logical Instruction Set

S.No.	Operation	Example	No. of Bytes	Machine Cycle	T-State	Addressing Mode
1	ANA R - Register content is anded with Accumulator content	ANA C	1	1	4	Register
2	ANI 8BIT -Accumulator content is anded with 8 bit data	ANI 45 H	2	2	7	Immediate
3	ORA R - Register content is ORed with Accumulator content	ORA C	1	1	4	Register
4	ORI 8BIT -Accumulator content is ORed with 8 bit data	ORI 45 H	2	2	7	Immediate
5	XRA R - Register content is Ex-ored with Accumulator content	XRA C	1	1	4	Register
6	XRI 8BIT -Accumulator is EX-ored with 8 bit data	XRI 45 H	2	2	7	Immediate

7	CMA- complement the contents of accumulator	CMA	1	1	4	Impicit
8	RAL- Rotate each bit in Accumulator to left one position including carry	RAL	1	1	4	Impicit
9	RLC- Rotate each bit in accumulator to left and MSB to carry	RLC	1	1	4	Impicit
10	RAR-Rotate each bit in Accumulator to right one position including carry	RAR	1	1	4	Impicit
11	RRC- Rotate each bit in accumulator to right and LSB to carry	RRC	1	1	4	Impicit
12	CMP R- Compare contents of accumulatotor with register and contents do not change only flags are affected-if A<R, CY=1, Z=0 IF A> R, CY=0,Z=0 IF A=R CY=0,Z=1	CMP D	1	1	4	Register
13	CPI 8BIT- Compare 8 bit data with accumulator- if A<8bit, CY=1, Z=0 IF A> 8 bit, CY=0,Z=0 IF A=8bit CY=0,Z=1	CPI 84 H	2	2	7	Immediate

4. Branching Instruction Set:

S.No.	Operation	Example	No. of Bytes	Machine Cycle	T-State	Addressing Mode
1	JMP-jump unconditionally	JMP 2050	3	3	10	Direct
2	JC- Jump conditionally, checks the condition, if condition is true means carry =1, then goes to specified address else goes to next instruction	JC 4000	3	2/3	7/10	Direct
3	JNC- Jump conditionally, checks the condition, if condition is true means carry =0, then goes to specified address else goes to next instruction	JNC 4500	3	2/3	7/10	Direct
4	JP- Jump conditionally, checks the condition, if condition is true i.e. S=0 means positive, then goes to specified address else goes to next instruction	JP 2050	3	2/3	7/10	Direct
5	JM- Jump conditionally, checks the condition, if condition is true i.e. S=1 means negative, then goes to specified address else goes to next instruction	JM 2600	3	2/3	7/10	Direct
6	JZ= Jump conditionally, checks the condition, if condition is true means Z =1, then goes to specified address else goes to next instruction	JZ 2100	3	2/3	7/10	Direct

7	JNZ- Jump conditionally, checks the condition, if condition is true means Z =0, then goes to specified address else goes to next instruction	JNZ 3500	3	2/3	7/10	Direct
8	JPE= Jump conditionally, checks the condition, if condition is true i.e. parity is even means P=1, then goes to specified address else goes to next instruction	JPE 4800	3	2/3	7/10	Direct
9	JPO- Jump conditionally, checks the condition, if condition is true i.e. prity is odd means P=0, then goes to specified address else goes to next instruction	JPO 4600	3	2/3	7/10	Direct
10	CALL – Call unconditionally- program sequence is transferred to subroutine with 16 bit address specified .	CALL 6500	3	8	18	Direct
11	RET-After executing interrupt service routine, program sequence is transferred from subroutine to calling program	RET	1	3	10	Implicit

5. Machine Contol Instruction Set

S.No.	Operation	Example	No. of Bytes	Machine Cycle	T- State	Addressing Mode
1	EI-Enable interrupt	EI	1	1	4	IMPLICIT
2	DI-Disble interrupt	DI	1	1	4	Implicit
3	NOP- No operation	NOP	1	1	4	Implicit
4	HALT	HALT	1	1	4	Implicit

Q17. What is an Interrupt? Solution: Interrupt is a process where an external device can get the attention of the microprocessor.

–The process starts from the I/O device

–The process is asynchronous.

Q18. Classify interrupts.

Classification of Interrupts

–>Interrupts can be classified into two types:

•Maskable Interrupts are the Interrupts that can be delayed or Rejected or ignored.

•Non-Maskable Interrupts are the interrupts that can not be delayed or Rejected or ignored.

→Interrupts can also be classified into:

•Vectored interrupts are the interrupts in which the address of the service routine is hard-wired.

•Non-vectored interrupts are the interrupts in which the address of the service routine needs to be supplied externally by the device.

→Interrupts can also be classified as

1.Software Interrupts: The software interrupts are program instructions. These instructions are inserted at desired locations in a program.

The 8085 has eight software interrupts from RST 0 to RST 7 The vector address for these interrupts can be calculated as follows.

Interrupt number * 8 = vector address for RST 5.5 = 5.5* 8 = 40 = 28H

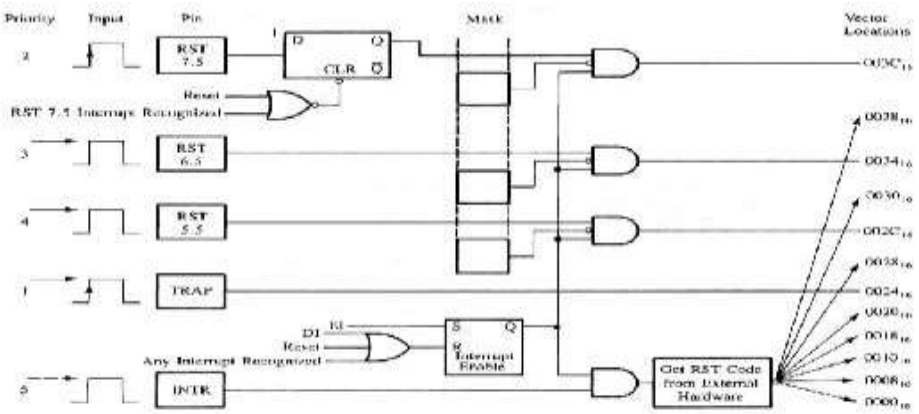
Vector address for interrupt RST 5 is 0028H

•Hardware interrupts: An external device initiates the hardware interrupts and placing an appropriate signal at the interrupt pin of the processor. If the interrupt is accepted then the processor executes an interrupt service routine.

The 8085 has five hardware interrupts

(1)TRAP (2) RST 7.5 (3) RST 6.5 (4) RST 5.5
(5)INTR

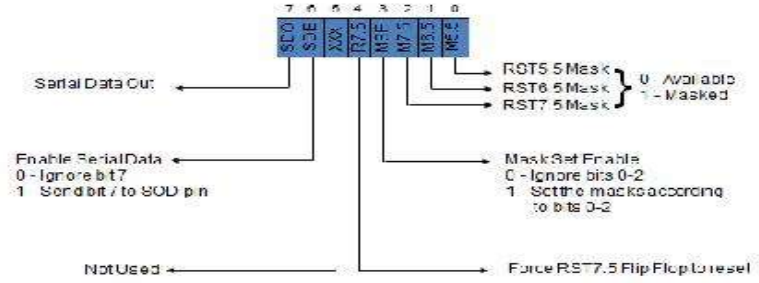
Q19. Illustrate Interrupt structure of 8085 microprocessor. Also differentiate among all interrupts of 8085 microprocessor.
Solution:

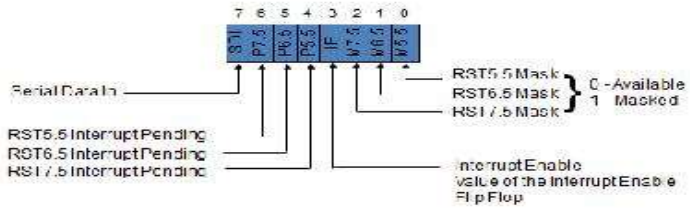


Interrupt Name	Maskable	Masking Method	Vectored	Memory	Triggering Method
INTR	Yes	DI / EI	No	No	Level Sensitive
RST 5.5 / RST 6.5	Yes	DI / EI SIM	Yes	No	Level Sensitive
RST 7.5	Yes	DI / EI SIM	Yes	Yes	Edge Sensitive
TRAP	No	None	Yes	No	Level & Edge Sensitive

Q20.Explain SIM and RIM instructions with their Control Word Format. Also write a program to enable RST 6.5 Interrupt and disable 5.5 and 7.5 interrupt.

Solution:





SIM:Set Interrupt Mask: This instruction takes the bit pattern in the Accumulator and applies it to the interrupt mask for enabling and disabling the specific interrupts.

To reset RST7.5

Serially data out

RIM: Read Interrupt Mask:

Loads the accumulator with an 8-bit pattern showing the status of each interrupt pin and mask. Also it is used for serial data input.