Interrupts in 8086

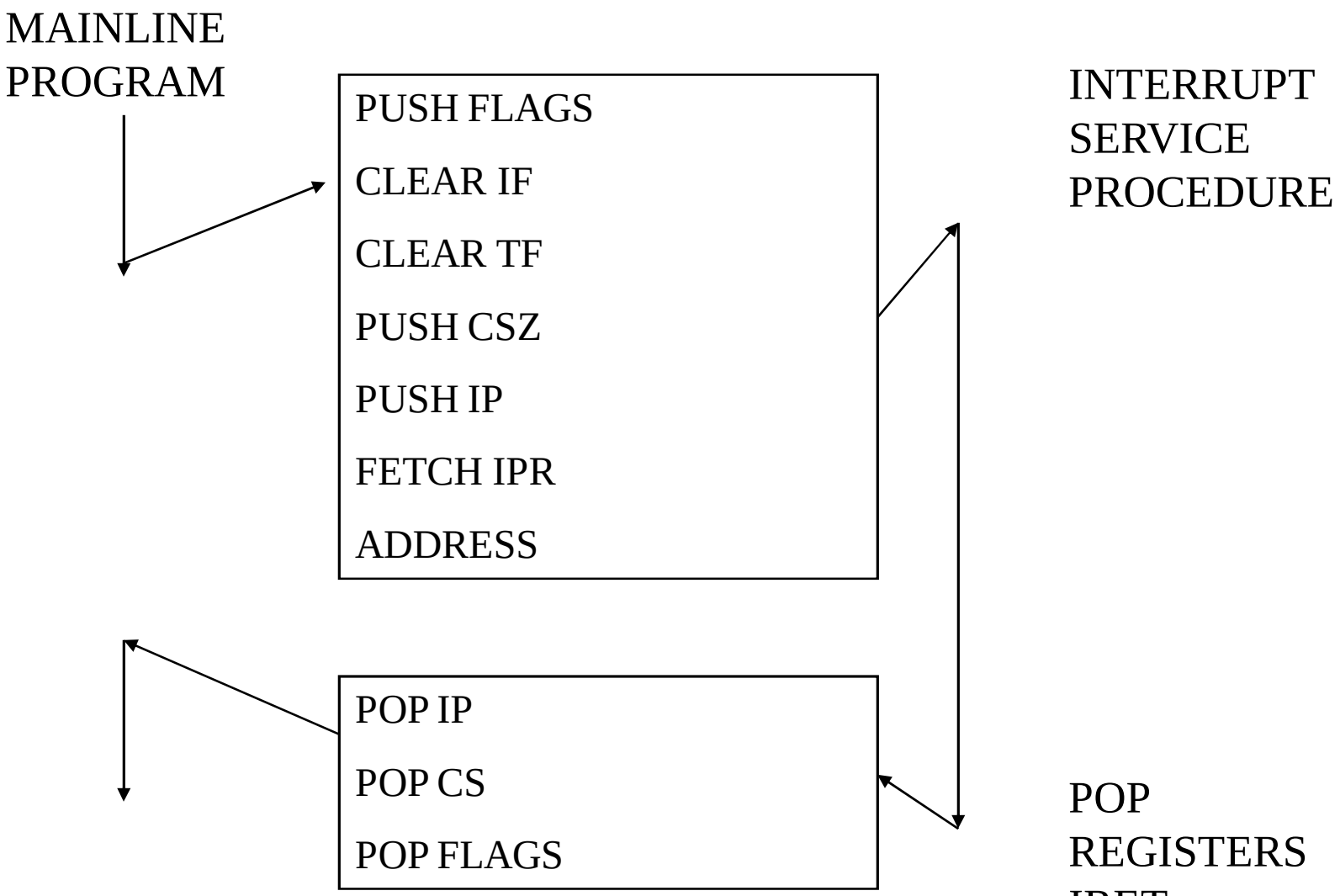
Most microprocessor allows normal program execution to be trerminated by some external signal or by a special instruction in the program. In response to this the processor stops the execution of current program and calls the procedure which services the interrupt.

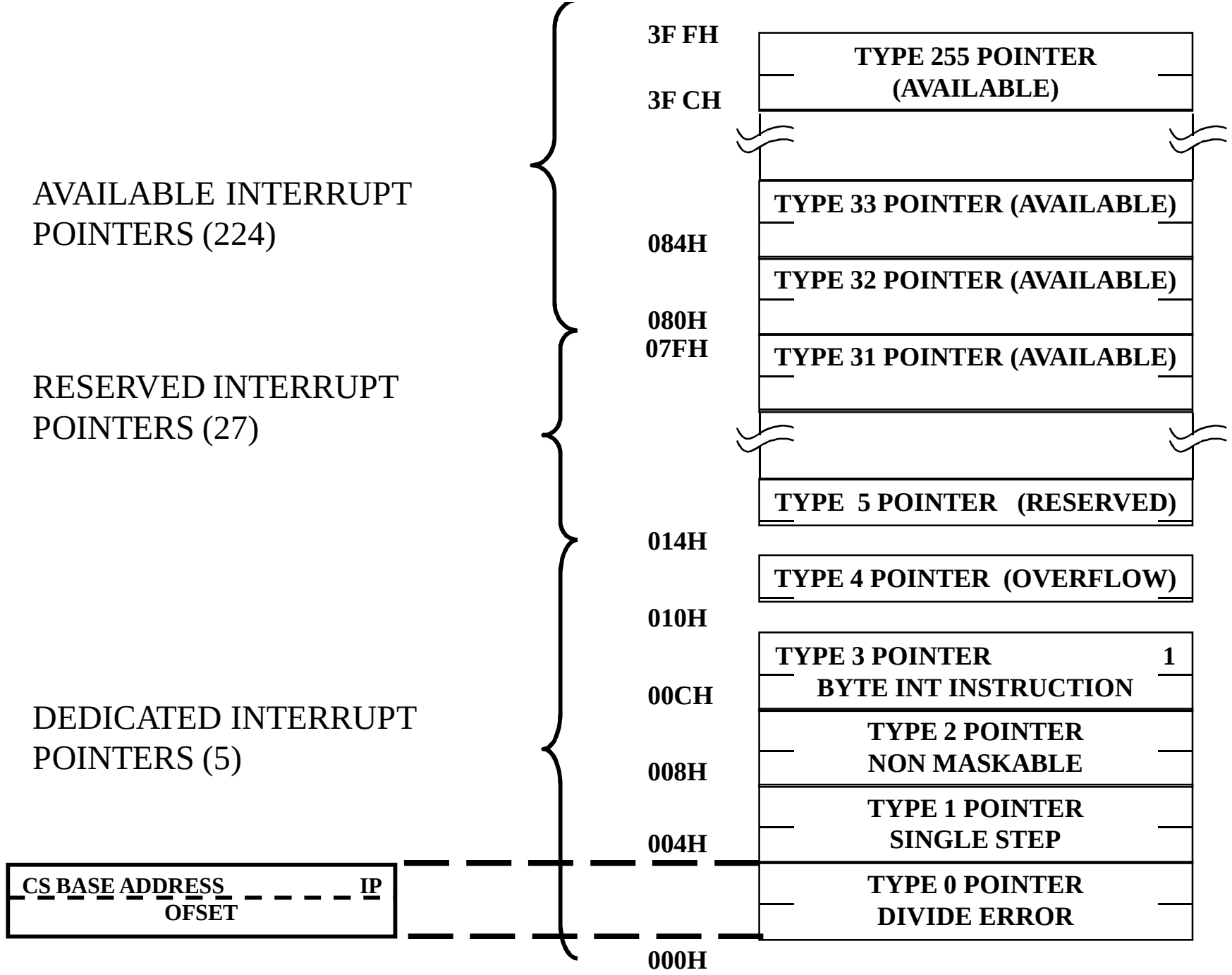
An interrupt can come from any three sources:

1. an external signal applied to the nonmaskable interrupt (NMI) input pin or to the interrupt (INTR) input pin. It is also known as hardware interrupt.
2. Execution of the interrupt instruction(INT). Also known as Software interrupt.
3. Some error condition produced by the execution of an instruction. Ex. Divide by zero.

At the end of each instruction cycle, the 8086 checks to see if any interrupts have been requested, the 8086 responds to the interrupt by stepping through the following series of major actions.

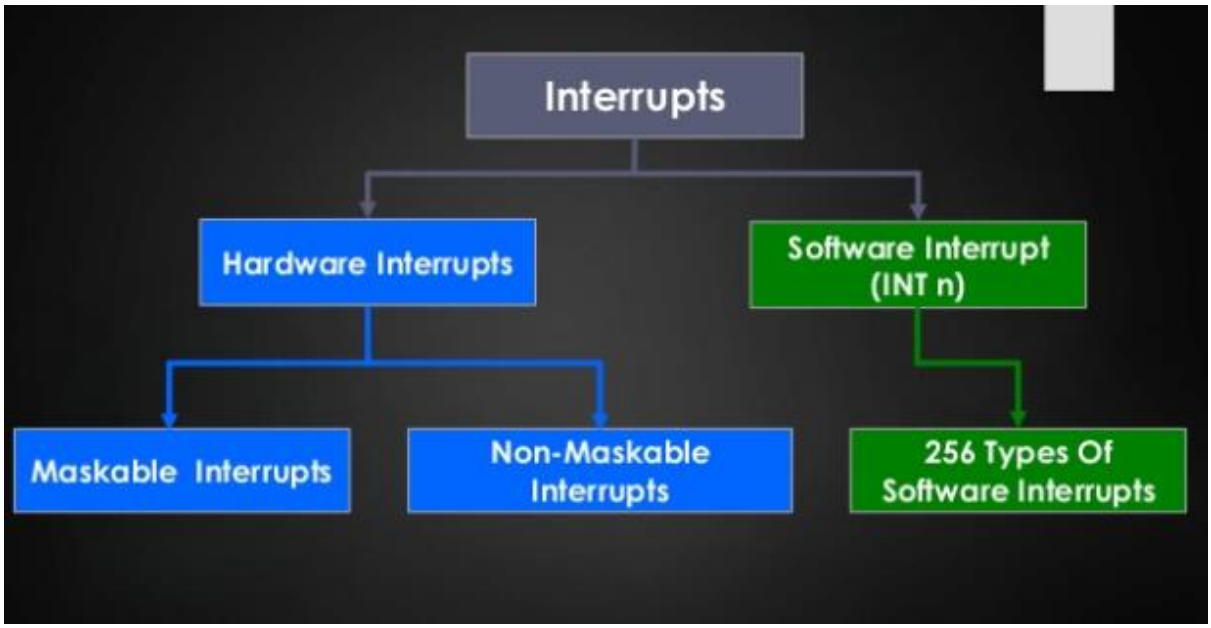
1. It decrements the stack pointer by 2 and pushes the flag register on the stack.
2. It disables the 8086 INTR interupt input by clearing the interrupt flag(IF) in the flag register.
3. It resets tha trap flag (TF) in the flag register.
4. It decrements the stack pointer by 2 and pushes the current code segment register contents on the stack..
5. It decrements the stack pointer by 2 and pushes the current instruction pointer contents on the stack.
6. It does an indirect far jump to the start of the procedure the user has written to response to the interrupt.


MAINLINE
PROGRAM
PUSH FLAGS
CLEAR IF
CLEAR TF
PUSH CSZ
PUSH IP
FETCH IPR
ADDRESS
INTERRUPT
SERVICE
PROCEDURE
POP IP
POP CS
POP FLAGS
POP
REGISTERS
IRET



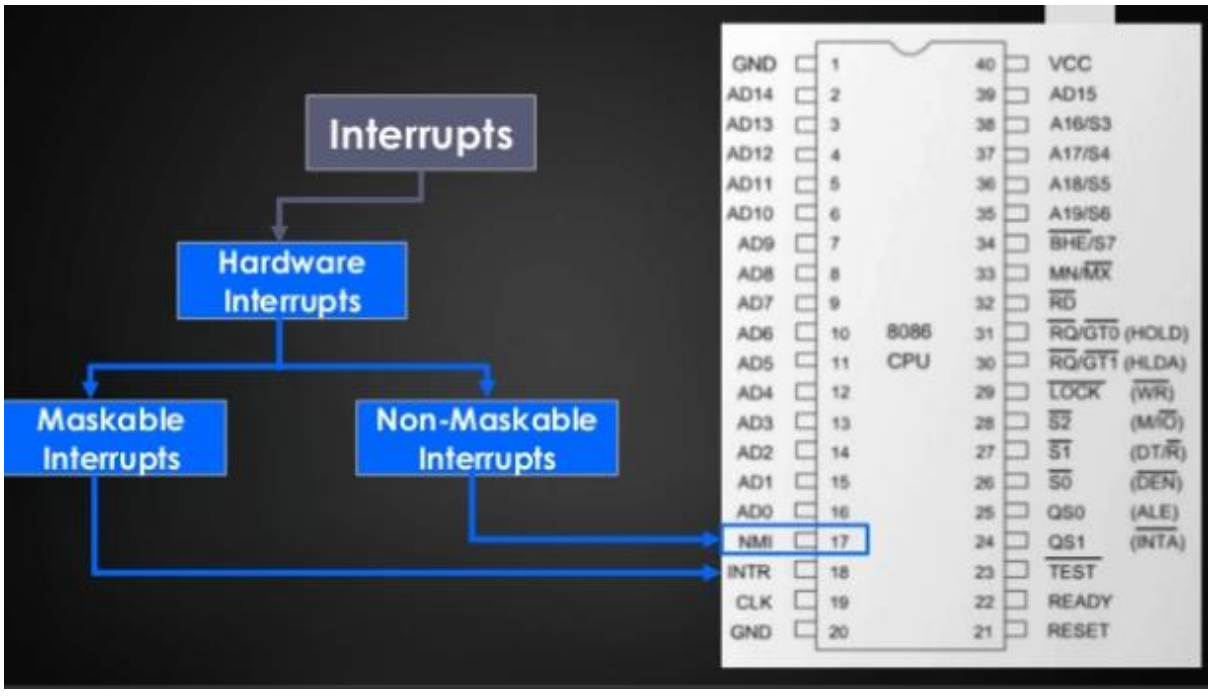
VECTOR INTERRUPT TABLE O 8086

Contents



Hardware Interrupts

The interrupts initiated by external hardware by sending an appropriate signal to the interrupt pin of the processor is called hardware interrupt. The 8086 processor has two interrupt pins INTR and NMI. The interrupts initiated by applying appropriate signal to these pins are called hardware interrupts of 8086.



Hardware Interrupts

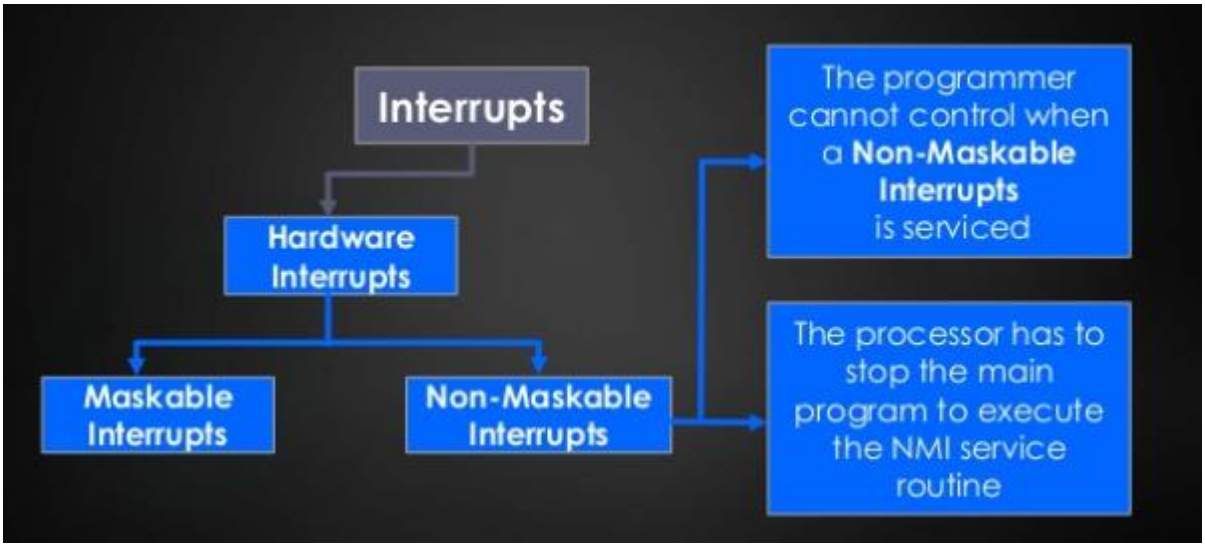
Used to handle external hardware peripherals , such as key boards , mouse , hard disks , floppy disks , DVD drivers, and printers.

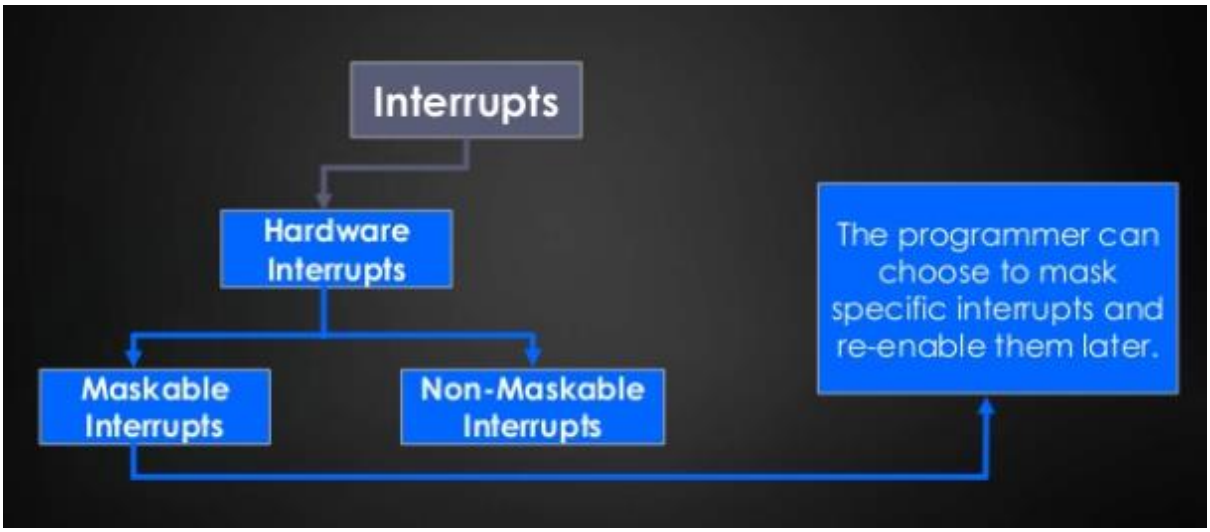
key boards | mouse | hard disks | floppy disks | DVD drivers

Maskable & Non-Maskable Interrupts

The processor has the facility for accepting or rejecting hardware interrupts. Programming the processor to reject an interrupt is referred to as masking or disabling and programming the processor to accept an interrupt is referred to as unmasking or enabling. In 8086 the interrupt flag (IF) can be set to one to unmask or enable all hardware interrupts and IF is cleared to zero to mask or disable a hardware interrupts except NMI. The interrupts whose request can be either accepted or rejected by the processor are called maskable interrupts.

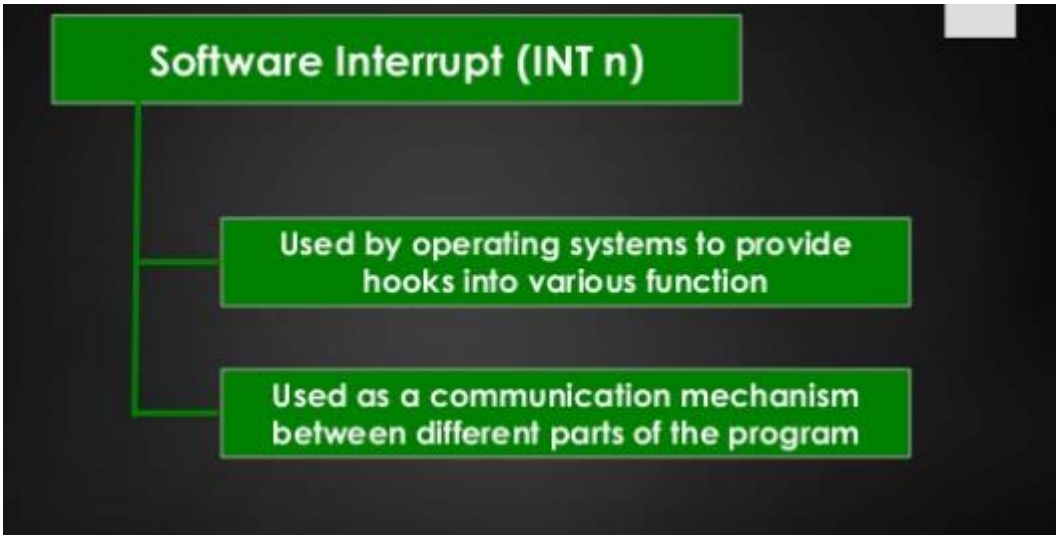
The interrupts whose request has to be definitely accepted (or cannot be rejected) by the processor are called non-maskable interrupts. Whenever a request is made by non-maskable interrupt, the processor has to definitely accept that request and service that interrupt by suspending its current program and executing an ISR. In 8086 processor all the hardware interrupts initiated through INTR pin are maskable by clearing interrupt flag (IF). The interrupt initiated through NMI pin and all software interrupts are non-maskable.





Software Interrupts

The software interrupts are program instructions. These instructions are inserted at desired locations in a program. While running a program, if software interrupt instruction is encountered then the processor initiates an interrupt. The 8086 processor has 256 types of software interrupts. The software interrupt instruction is INT n, where n is the type number in the range 0 to 255.



8086 INTERRUPT TYPES
256 INTERRUPTS OF 8086 ARE DIVIDED IN TO 3 GROUPS

1. **TYPE 0 TO TYPE 4 INTERRUPTS-**
   These Are Used For Fixed Operations And Hence Are Called Dedicated Interrupts

2. **TYPE 5 TO TYPE 31 INTERRUPTS**
   Not Used By 8086,reserved For Higher Processors Like 80286
   80386 Etc

3. **TYPE 32 TO 255 INTERRUPTS**
   Available For User, called User Defined Interrupts These Can Be H/W Interrupts And Activated Through Intr Line Or Can Be S/W Interrupts.

- **Type – 0 Divide Error Interrupt**
  Quotient Is Large Cant Be Fit In Al/Ax Or Divide By Zero
- **Type –1 Single Step Interrupt**
  Used For Executing The Program In Single Step Mode By Setting Trap Flag
- **Type – 2 Non Maskable Interrupt**
  This Interrupt Is Used For Execution Of NMI Pin.
- **Type – 3 Break Point Interrupt**
  Used For Providing Break Points In The Program
- **Type – 4 Over Flow Interrupt**
  Used To Handle Any Overflow Error.

Conclusion

The CPU executes program, as soon as a key is pressed, the Keyboard generates an interrupt. The CPU will response to the interrupt – read the data. After that returns to the original program. So by proper use of interrupt, the CPU can serve many devices at the "same time"