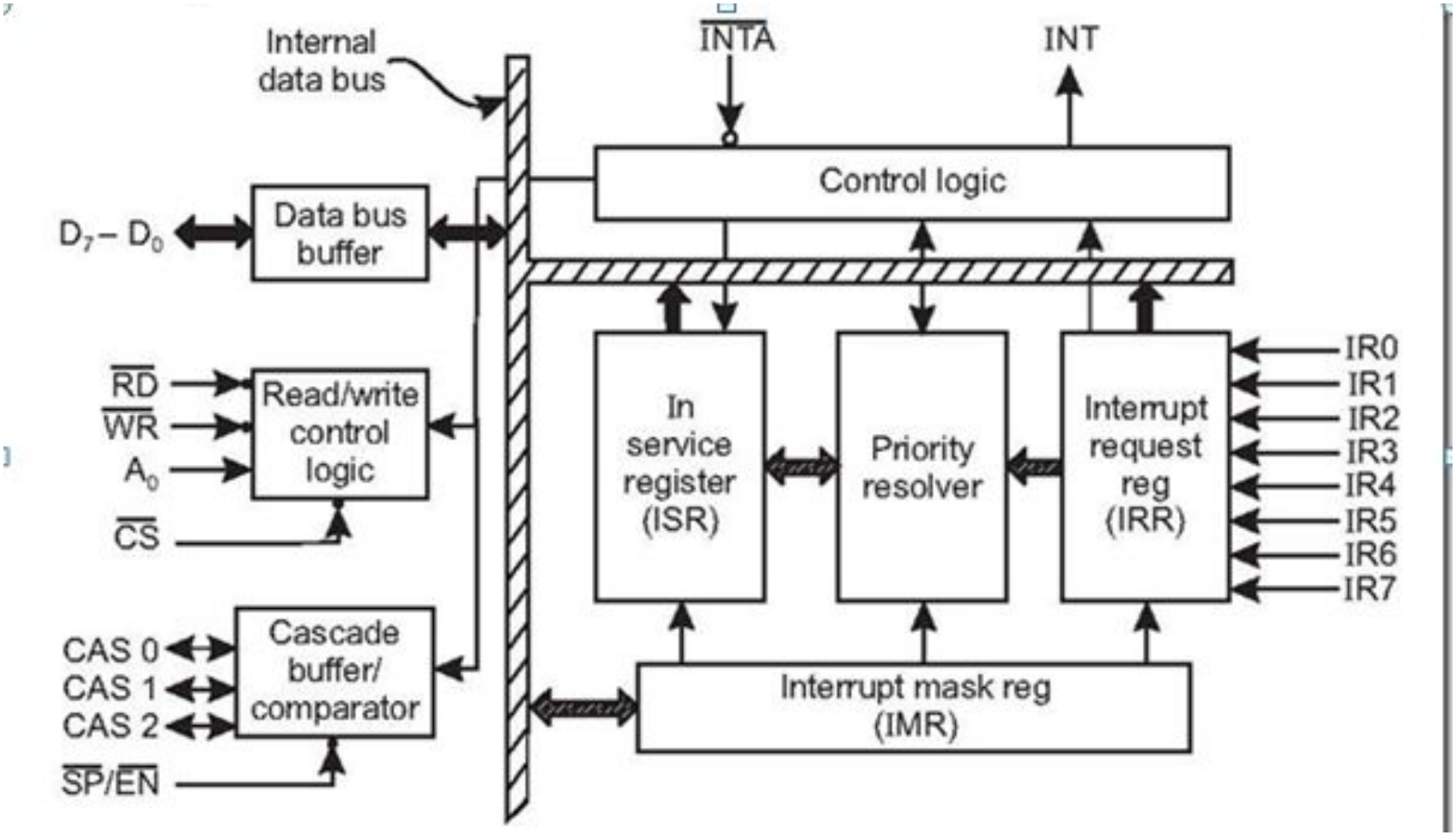
8259 Programmable Interrupt Controller



Features of 8259 Programmable Interrupt Controller

1)It can handle eight interrupt inputs. This is equivalent to providing eight interrupt pins on the processor in place of one INTR in 8085

2)The chip can vector an interrupt request anywhere in the memory map from 0000H to FFFFH in 8085A microprocessor. However, all the eight interrupts are spaced at an interval of either four or eight locations.

3)It can resolve eight levels of interrupt priorities in a variety of modes. The priorities of interrupts can be changed under running condition.

4)Each of the interrupt requests can be masked individually.

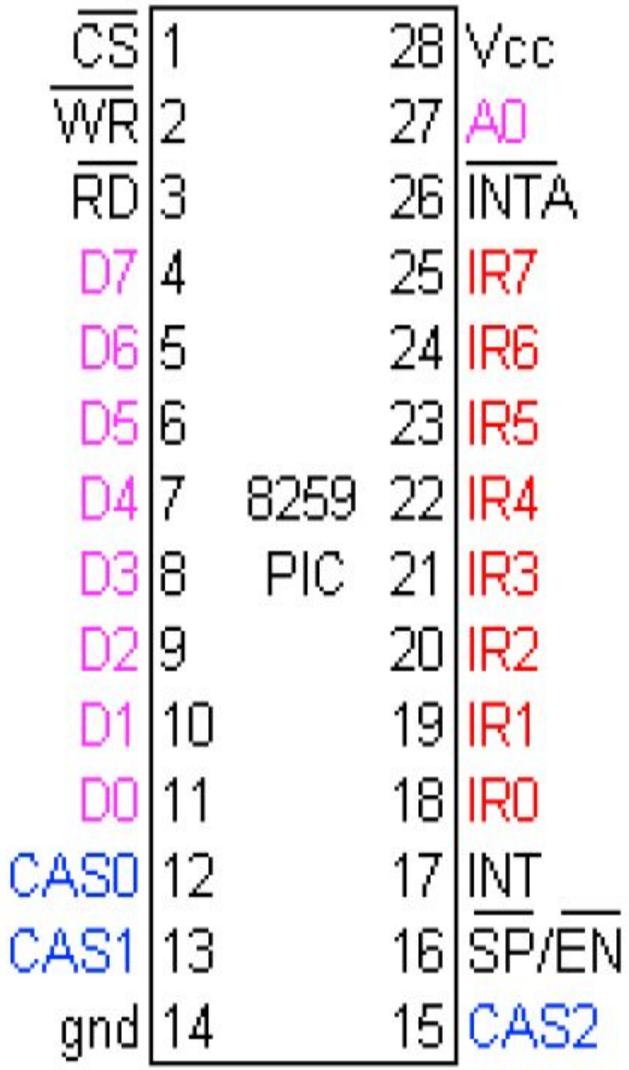
Features of 8259 Programmable Interrupt Controller continued

5)The status of pending interrupts, in service interrupts, and masked interrupts can be read at any time.

6)The chip can be programmed to accept interrupt requests either as level triggered or edge triggered interrupt request

7)If required, nine 8259As can be cascaded in a master-slave configuration mode to handle 64 interrupt inputs.

PIN DIAGRAM OF 8259



D0-D7	Bi-directional, tristated, buffered data lines. Connected to data bus directly or through buffers.
RD-bar	Active low read control
WR-bar	Active low write control
A0	Address input line, used to select control register.
CS-bar	Active low chip select
CAS0-2	Bi-directional, 3 bit cascade lines. In master mode, PIC places slave ID no. on these lines. In slave mode, the PIC reads slave ID no. from master on these lines. It may be regarded as slave-select.
SP-bar / EN-bar	Slave program / enable. In non-buffered mode, it is SP-bar input, used to distinguish master/slave PIC. In buffered mode, it is output line used to enable buffers.
INT	Interrupt line, connected to INTR of microprocessor.
INTA-bar	Interrupt ack, received active low from microprocessor.
IR0-7	Asynchronous IRQ input lines, generated by peripherals.

Sequence of steps followed when 8259 is to be connected with 8085 microprocessor:

1. One or more of the IR lines goes high.
2.Corresponding IRR bit is set.
3. 8259'priority resolver checks three registers INR, IRR, IMR and sends INT to CPU.
4.CPU sends an acknowledgement INTA' to 8259 and ISR is set. IRR is reset.
5. 8259 releases Opcode for CALL instruction on data bus.
6.CALL initiates two more Interrupt acknowledgement cycles (low pulses).
7.8259 releases the subroutine address, first low byte on first acknowledgement pulse then high byte on next pulse.
8.When Interrupt cycle is completed, an EOI command is issued by processor, ISR bit is reset depending upon mode.

Working OVERVIEW

- The interrupt requests are accepted by 8259 from many interrupting devices IR0 to IR7 pins.
- After that, it identifies the highest priority interrupt request from those inputs that are already active.
- To configure the 8259 for fixed priority mode of operation, among them IR0 has the highest and IR7 has the lowest priority.
- If the inputs IR2, IR4, and IR6 are active, then IR2 has the highest priority interrupt request among the active requests than the other. The details of the interrupt requests those are active are stored in the Interrupt Request Register (IRR).
- By loading the Interrupt Mask Register (IMR), it is possible to mask the interrupt request. If the interrupt requests IR2 and IR3 are masked, then IR4 will get the highest priority interrupt request among the active requests that are not masked.
- It is possible that the processor is already servicing IR5 interrupt request. All the information about the interrupt requests that are presently services is kept in In-Service Register in short abbreviation (ISR).

- A priority resolver unit exists in 8259 which receives inputs requests from IRR, ISR, and IMR and identifies the highest priority interrupt request.
- Since the priority of IR4 is much greater than IR5 which is currently being serviced, the INT (Interrupt Request) of the output is activated. At the same time, bit no 4 of ISR is set to 1 by the8259. The output of INT of 8259 is connected to INTR input of 8085 as shown in the figure below. The INT output of 8259 should not get connected to any other interrupt pin of 8085.
- Hence the priority resolver decides to activate the INT output only when the following conditions are satisfied otherwise not.

•Activation to IR input is done
•When the masking of the IR input is not done
•When the processor is currently not servicing an IR request with a higher priority.

Functional Description:

- The 8259A (PIC) has eight interrupt request inputs – IR7 - IR0.

- The 8259A uses its INT output to interrupt the 8085A via INTR pin.
- The 8259A receives interrupt acknowledge pulses from the microprocessor at its INTA' input. Vector address, used by the 8085A to transfer control to the service subroutine of the interrupting device, is provided by the 8259A on the data bus.
- The 8259A is a programmable device that must be initialized by command words sent by the microprocessor. After initialization the 8259A mode of operation can be changed by operation command words from the microprocessor

Block Diagram/Architecture description

- **Data Bus Buffer:** This 3- state, bidirectional 8-bit buffer is used to interface the 8259A to the system data bus.
- Control words and status information from the microprocessor to PIC and from PIC to microprocessor respectively, are transferred through the data bus buffer.
- **Read/Write Control Logic** : The function of this block is to accept output commands sent from the CPU.
- It contains the initialization command word (ICW) registers and operation command word (OCW) registers which store the various control formats for device operation.
- This function block also allows the status of 8259A to be transferred to the data bus.

- **Interrupt Request Register (IRR):**It is an 8-bit register – one bit for each interrupt request.
- It stores all the interrupt inputs that are requesting service. If an interrupt input is unmasked, and has an interrupt signal on it, then the corresponding bit in the IRR will be set.
- The content of this register can be read to know the status of pending interrupts.
- **Interrupt Mask Register (IMR):** The IMR is used to disable (Mask) or enable (Unmask) individual interrupt request inputs.
- This is also an 8-bit register. Each bit in this register corresponds to the interrupt input with the same number. To unmask any interrupt the corresponding bit is set ‘0’.

- **<u>In-service Register</u> (ISR):** The in-service register keeps track of which interrupt inputs are currently being serviced.
- For each input that is currently being serviced the corresponding bit of in-service register (ISR) will be set.
- In 8259A, during the service of an interrupt request, if another higher priority interrupt becomes active, it will be acknowledged and the control will be transferred from lower priority interrupt service subroutine (ISS) to higher priority ISS.

- **<u>Priority Resolver</u>**: This logic block determines the priorities of the interrupts set in the IRR.
- It takes the information from IRR, IMR and ISR to determine whether the new interrupt request is having highest priority or not.
- If the new interrupt request is having the highest priority, it is selected and processed. The corresponding bit of ISR will be set during interrupt acknowledge machine cycle.

- **Cascade Buffer/Comparator:** This function block stores and compares the IDs of all 8259A's in the system.
- The associated 3-I/O lines (CAS2-CAS0) are outputs when 8259A is used as a master and are inputs when 8259A is used as a slave.
- As a master, the 8259A sends the ID of the interrupting slave device onto the CAS2-0 lines. The slave 8259As compare this ID with their own programmed ID.
- Thus selected 8259A will send its pre-programmed subroutine address on to the data bus during the next one or two successive INTA pulses.

(For Reference Only)

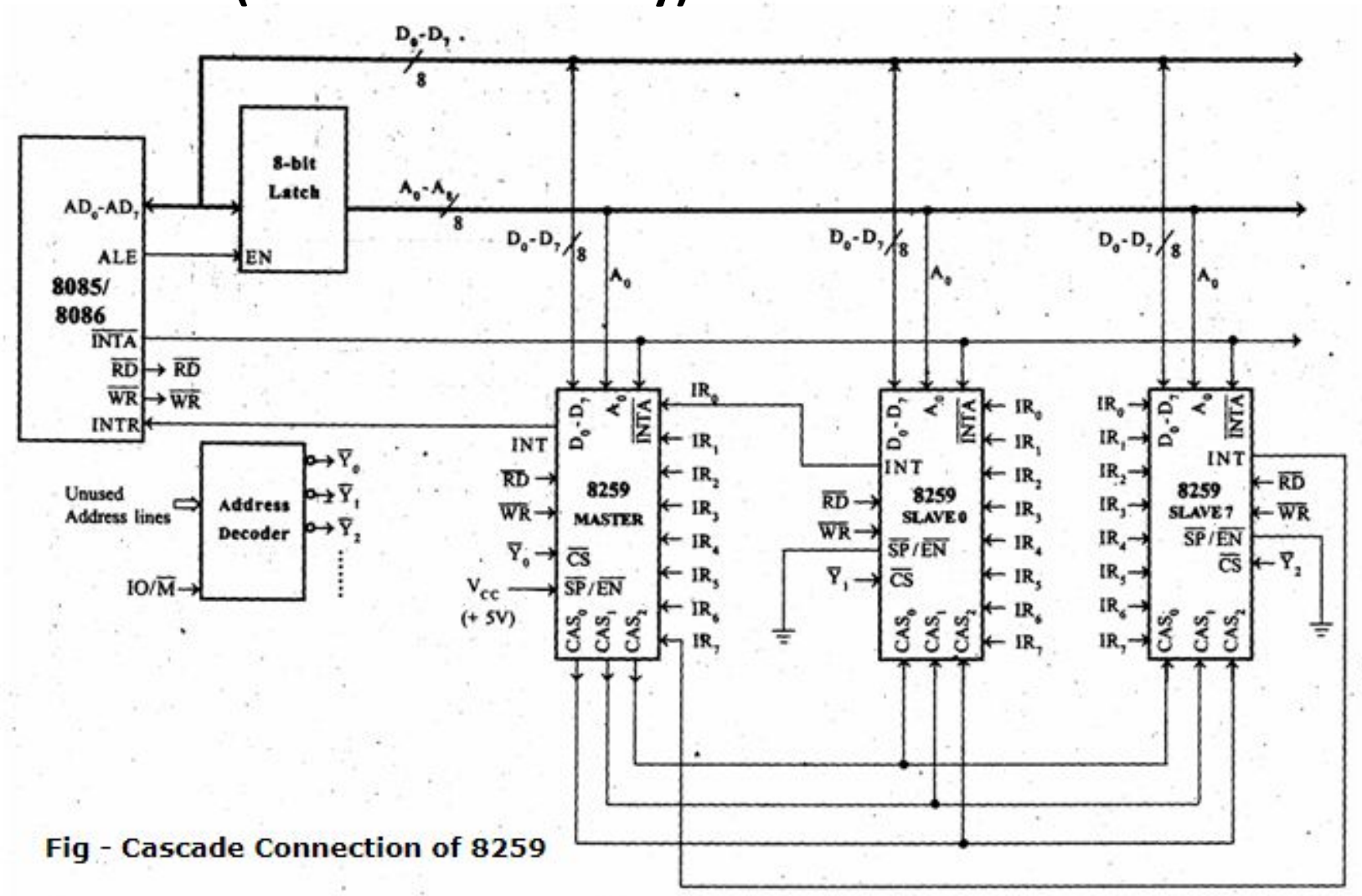


Fig - Cascade Connection of 8259

ICW1:INITIALIZATION CONTROL WORD1

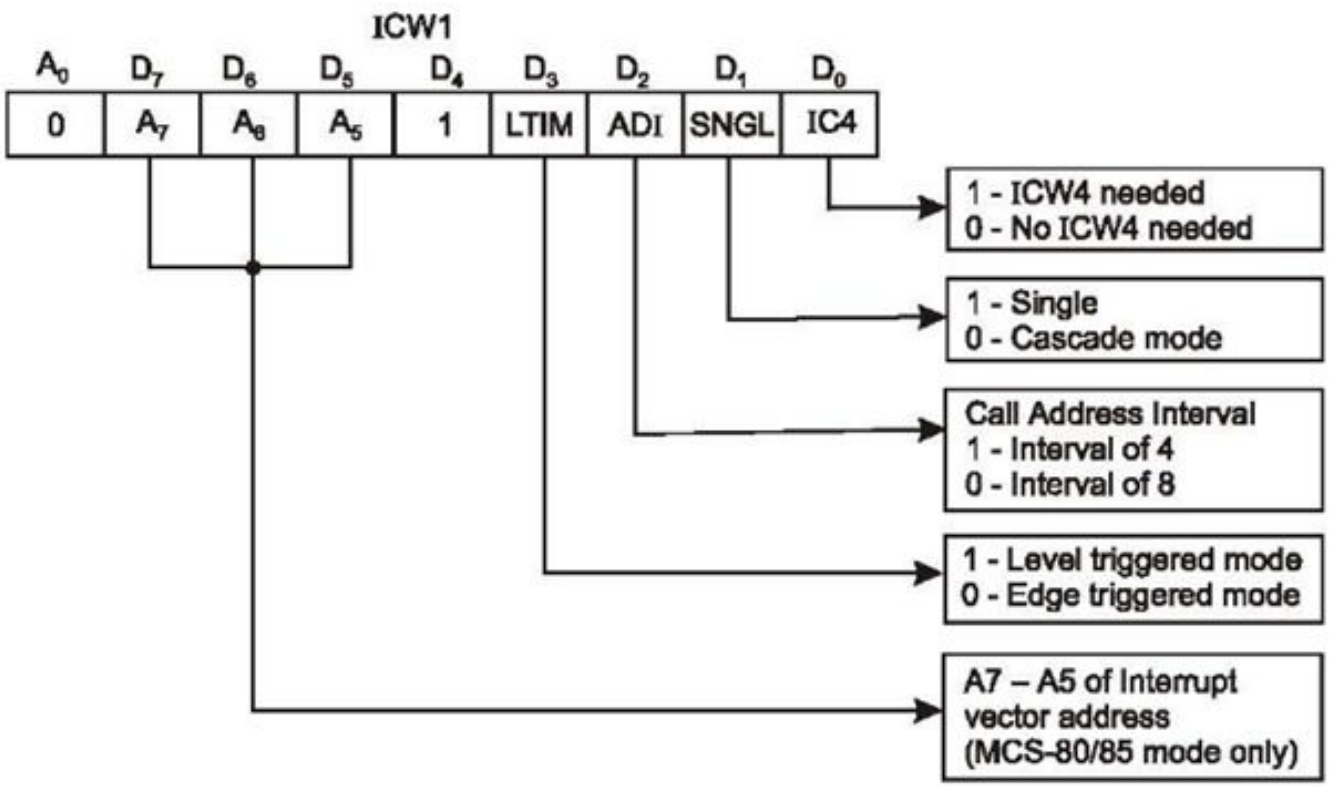
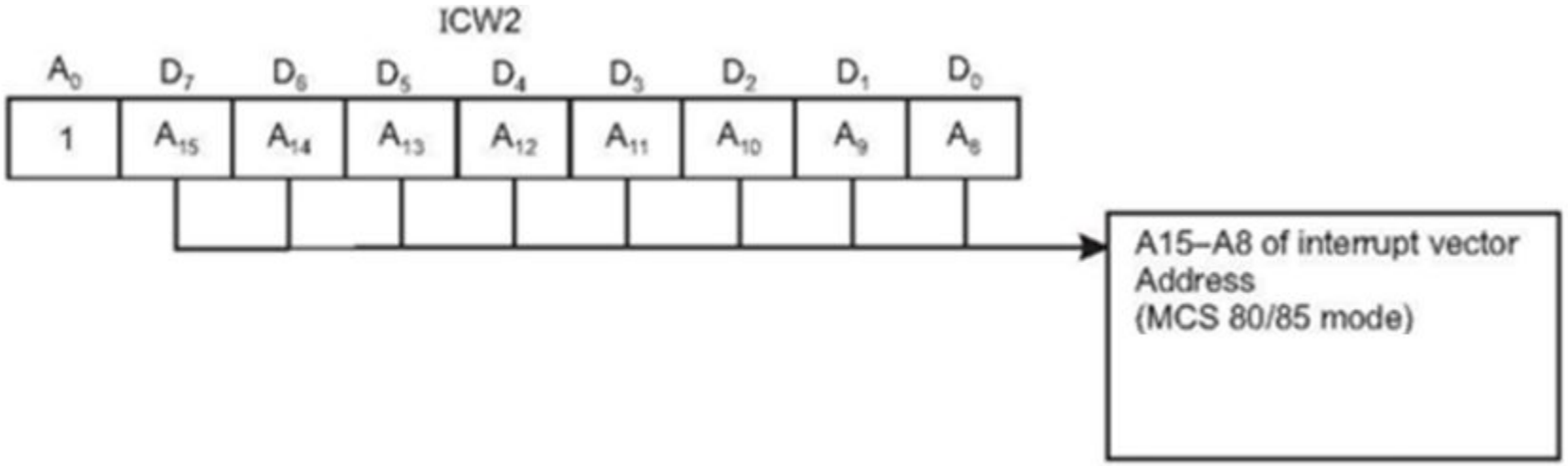
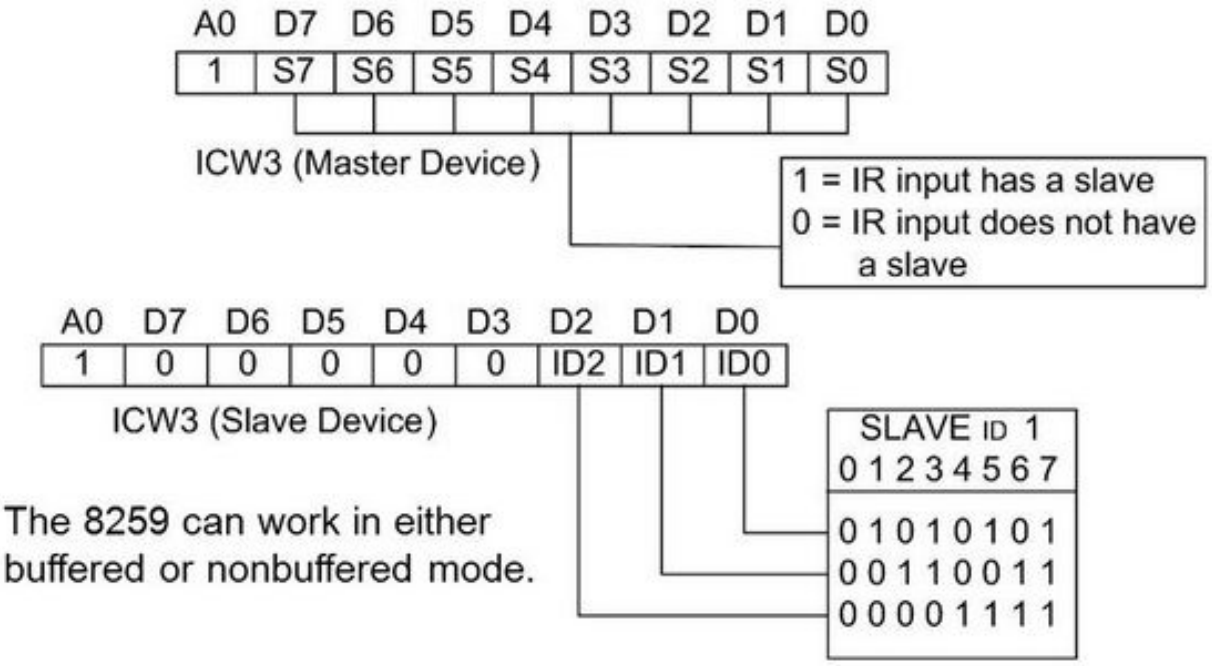


Fig. 9e.8: Initialisation command word 1 (*Source:* Intel Corporation)

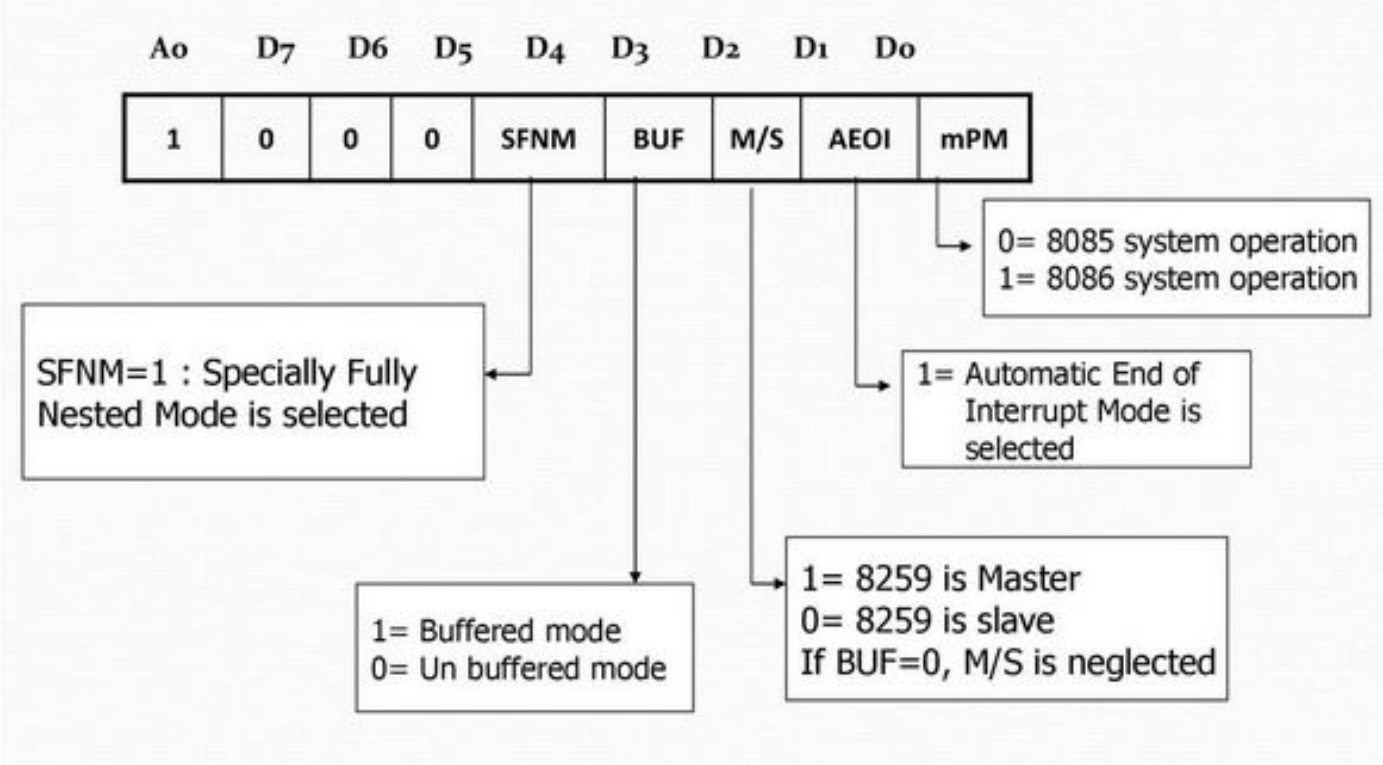
ICW2-Higher Byte of ISR



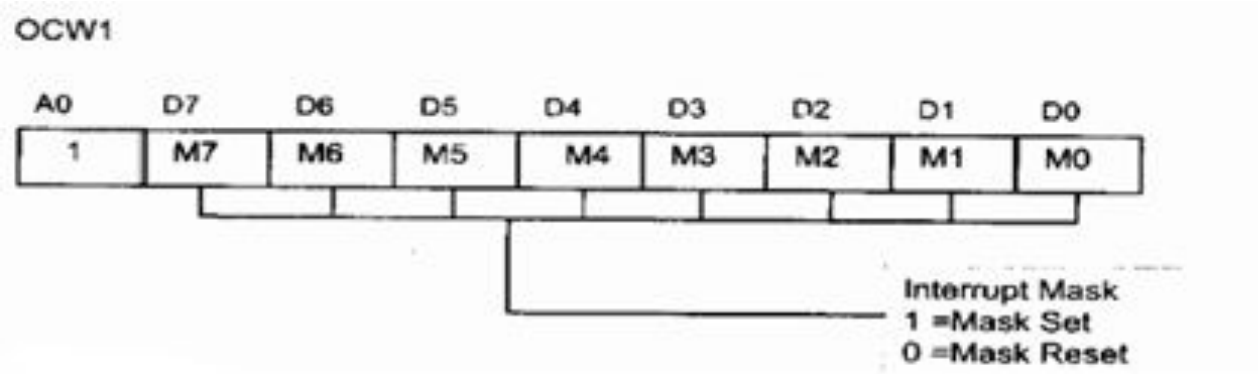
ICW3


A0 D7 D6 D5 D4 D3 D2 D1 D0
1 S7 S6 S5 S4 S3 S2 S1 S0
ICW3 (Master Device)
1 = IR input has a slave
0 = IR input does not have a slave
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 ID2 ID1 ID0
ICW3 (Slave Device)
SLAVE ID 1
0 1 2 3 4 5 6 7
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1
The 8259 can work in either buffered or nonbuffered mode.

ICW4


A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 SFNM BUF M/S AEOI mPM
0= 8085 system operation
1= 8086 system operation
SFNM=1 : Specially Fully Nested Mode is selected
1= Automatic End of Interrupt Mode is selected
1= Buffered mode
0= Un buffered mode
1= 8259 is Master
0= 8259 is slave
If BUF=0, M/S is neglected

OCW1:OUTPUT CONTROL WORD1



8259A- OPERATING MODES

FULLY NESTED MODE:

- General purpose mode / default mode.
- IR0 to IR7 are arranged from highest to lowest.
- IR0→ Highest IR7→Lowest

AUTOMATIC ROTATION MODE:

- In this mode, a device after being serviced, receives the lowest priority.

SPECIFIC ROTATION MODE:

- Similar to automatic rotation mode, except that the user can select any IR for the lowest priority, thus fixing all other priorities.

8259A- OPERATING MODES

END OF INTERRUPT (EOI):

- After the completion of an interrupt service, the corresponding ISR bits needs to be reset to update the information in the ISR. This is called EOI command.

It can be issued in three formats:

NON SPECIFIC EOI COMMAND:(manually)

- When this command is sent to 8259A, it resets the highest priority ISR bit.

SPECIFIC EOI COMMAND:(manually)

- This command specifies which ISR bit is to reset.

SPECIFIC EOI COMMAND FORMAT

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	L2	L1	L0

ISR Bit is to be reset

0	0	0 → 0th Bit
0	0	1 → 1st Bit

Etc…

8259A- OPERATING MODES

AUTOMATIC EOI:

- In this mode, no command is necessary.
- During the end of interrupt acknowledge cycle, the ISR bit is reset.
- Used for master only