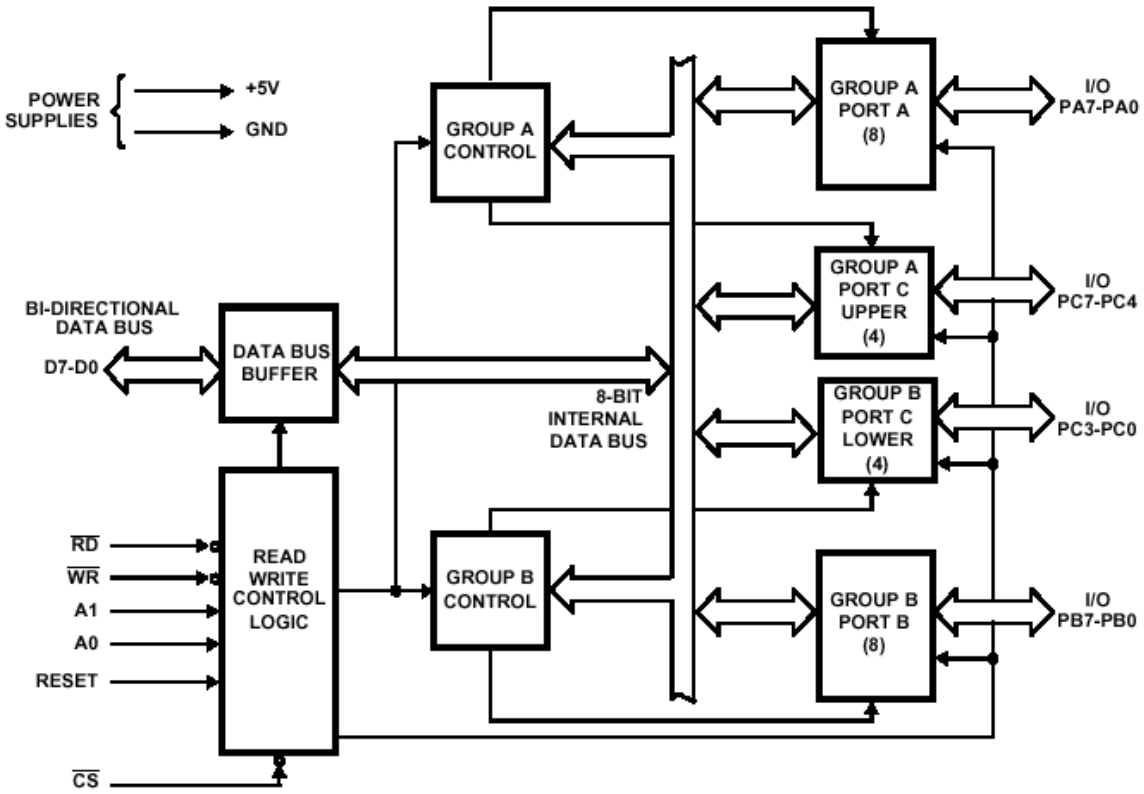
UNIT-IV

Q1. Draw and explain block diagram of 8255 PPI. Write its control words and explain its all modes of operation.
Ans-



- It is an **I/O port chip used for interfacing I/O devices** with microprocessor.
- The **parallel input-output port chip 8255** is also called as **programmable *peripheral input-output port.***
- The Intel's **8255 is designed for use with Intel's 8-bit, 16-bit microprocessors.**
- It has **24 input/output lines** which may be individually programmed in groups.
- The groups of I/O pins are named as **Group A , Group B and Group C upper and Group C lower.**
- Each of these two groups contains a subgroup of eight I/O lines called as **8-bit port** and another subgroup of four lines or a **4-bit port.**

- The port A lines are identified by symbols **PA0-PA7** while the port C lines are identified as **PC4-PC7**. Similarly, Group B contains an 8-bit port B, containing lines **PB0-PB7** and a 4-bit port C with lower bits **PC0- PC3.**
- All of **these ports can function independently either as input or as output ports.**
- This can be achieved by **programming the bits of an internal register of 8255 called as control word register (CWR).**
- Two control groups, labeled group A control and group B control define how the three I/O ports operate.
- The upper 4 bits of port C are associated with group A control while the lower 4 bits are associated with group B control.
- The other logic blocks are read/write control logic and data bus buffer. These blocks provide the electrical interface between the micro processor and 8255.
- The data bus buffer buffers the data I/O lines to/from the microprocessor data bus.
- The read/write control logic routes the data to and from the correct internal registers with the right timing.

There are two basic modes of operation of 8255, They are:

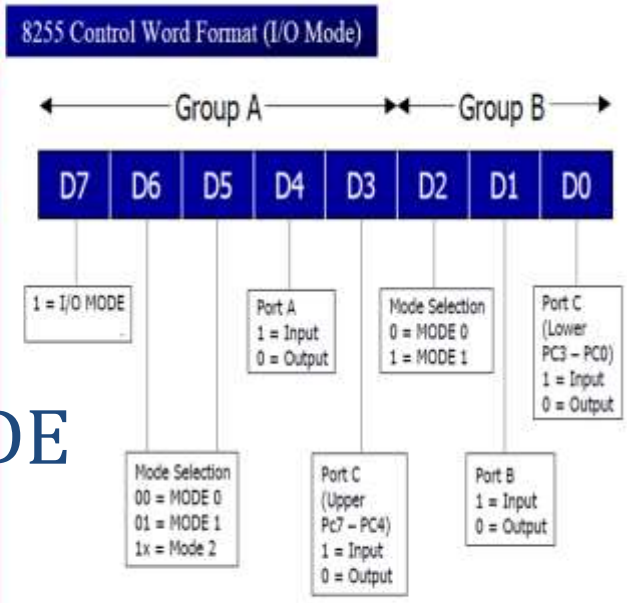
1. I/O mode.

2. BSR mode.

- **In I/O mode, the 8255 ports work as programmable I/O ports**, while
- **In BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.**

PROGRAMMING THE 8255

Mode Selection of 8255 (cont')



BSR MODE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	x	x	x	Bit Select			S/R

Not Used

Set=1
Reset=0

BSR Mode

0	0	0	bit 0
0	0	1	bit 1
0	1	0	bit 2
0	1	1	bit 3
1	0	0	bit 4
1	0	1	bit 5
1	1	0	bit 6
1	1	1	bit 7

Modes of 8255

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

0/1

There are 3 I/O modes of operation for the ports of 8255.

Mode 0, Mode 1, and Mode 2

1) Mode 0 - Basic I/O mode

2) Mode 1 - Strobed I/O mode

3) Mode 2 - Strobed bi-directional I/O

<u>Mode 0 Operation</u>

- It is Basic or **Simple I/O.**
- It **does not use any handshake signals**.
- It is **used for interfacing an i/p device or an o/p device.**
- **It is used when timing characteristics of I/O devices is well known**

<u>Mode 1 Operation</u>

- It uses handshake I/O.
- 3 lines are used for handshaking.

- It is used for interfacing an i/p device or an o/p device.
- Mode 1 operation is used when timing characteristics of I/O devices is not well known, or used when I/O devices supply or receive data at irregular intervals.

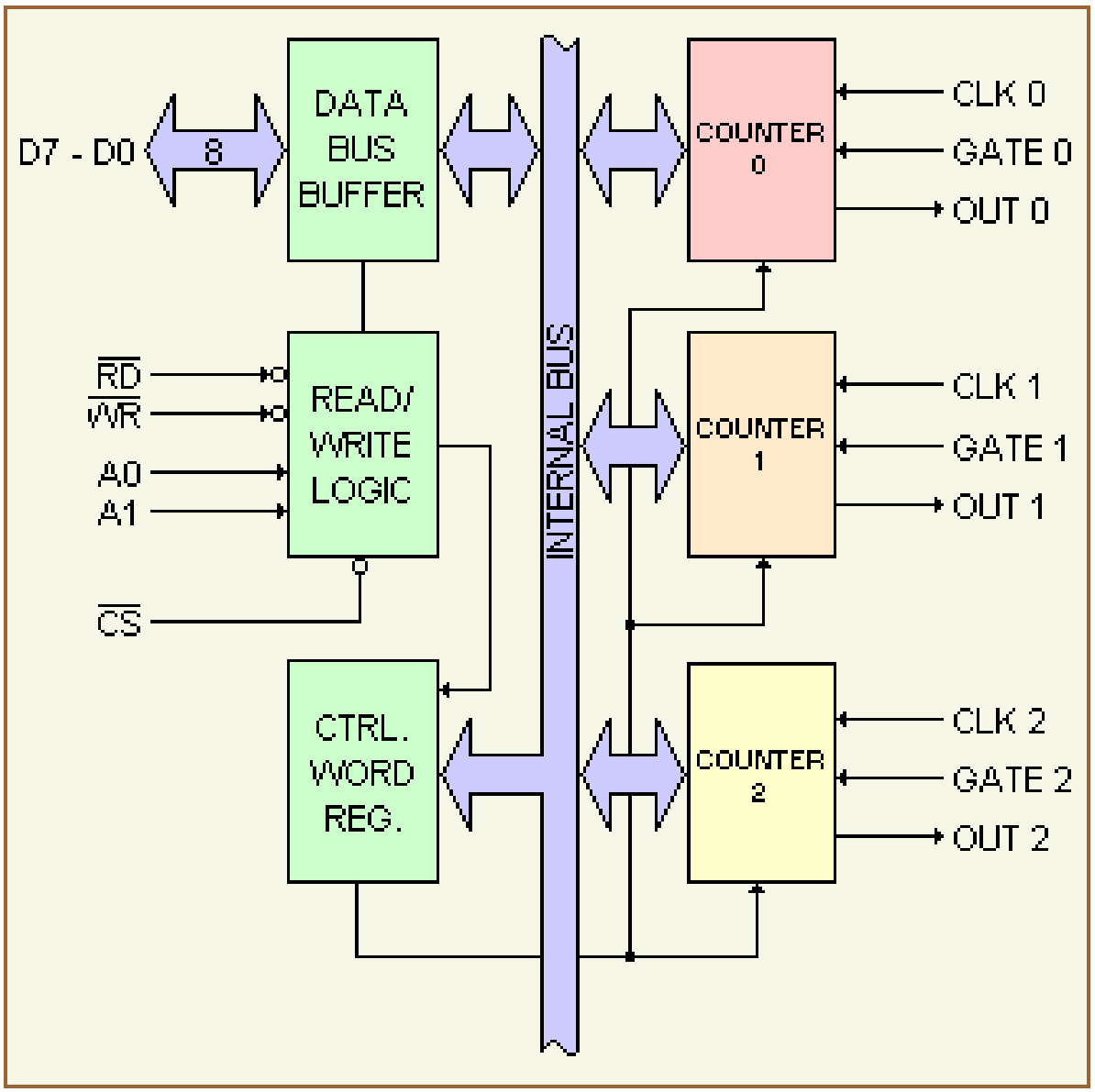
Mode 2 Operation

- It is bi-directional handshake I/O.
- Mode 2 operation uses 5 lines for handshaking.
- It is used with an I/O device that receives data some times and sends data sometimes.
- Mode 2 operation is useful when timing characteristics of I/O devices is not well known, or when I/O devices supply or receive data at irregular intervals.

Q2. Draw and explain block diagram of 8253 PIT. Write its control words and explain its all modes of operation.

Ans-

- The Intel 8253 and 8254 are Programmable Interval Timers (PITs), which perform timing and counting functions.
- After the desired delay, the 8254 will interrupt the CPU.
- It is 24 pin IC requires +5 V
- It consists of 3 16 bit counters operates in 6 modes.
- It generates accurate time delays under software control.
- Instead of setting up timing loops in software, the programmer configures the interval timer to match system requirements and programs the counter for the desired delay or for the desired output.
- Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are

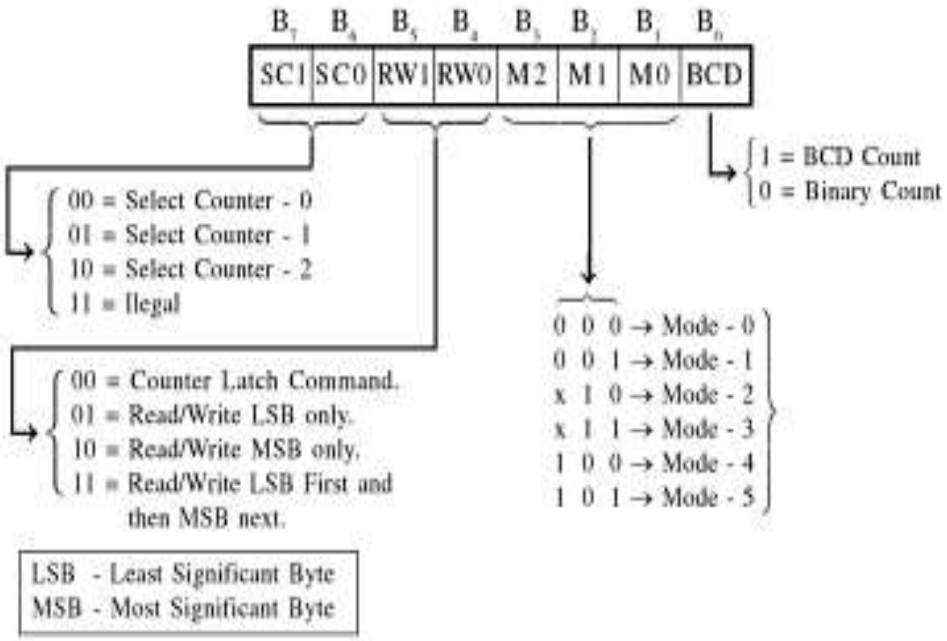


- **Data/Bus Buffer**
- This block contains the logic to buffer the data bus to / from the microprocessor, and to the internal registers.
- It has 8 input pins, usually labeled as D7..D0, where D7 is the MSB
- **Read/Write Logic**
- /RD: read signal
- /WR: write signal
- /CS: chip select signal
- A0, A1: address lines
- Operation mode of the PIT is changed by setting the above hardware signals.

- For example, to write to the Control Word Register, one needs to set /CS=0, /RD=1, /WR=0, A1=A0=1.

  - The timer has three counters, called channels.
  - Each channel can be programmed to operate in one of six modes.
  - Once programmed, the channels can perform their tasks independently.
  - The timer is usually assigned to IRQ-0 (highest priority hardware interrupt) because of the critical function it performs and because so many devices depend on it.
  - **Counters**
  - There are 3 counters (or timers), which are labeled as "Counter 0", "Counter 1" and "Counter 2.
  - Each counter has 2 input pins – "CLK" (clock input) and "GATE" and 1-pin, "OUT", for data output.
  - The 3 counters are 16-bit down counters independent of each other, and can be easily read by the CPU.
  - Counters are programmed by writing a Control Word and then an initial count.
  - GATE=1 enables counting, GATE=0 disables counting.
  - All 3 counters are 16-bits.
  - PIT has only an 8-bit data bus and can read or write only one byte at a time.
  - Thus to read or write a 16-bit value, you must do so one byte at a time.

CONTROL WORD OF PIT 8254



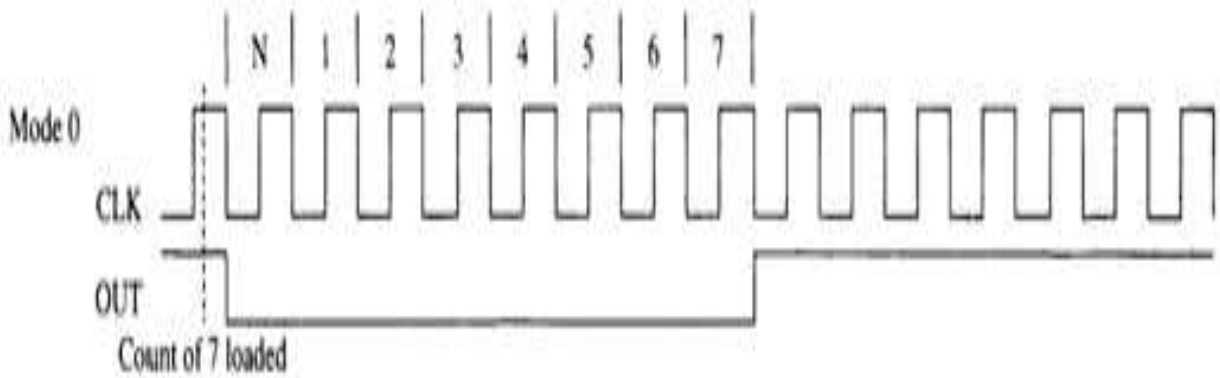
- There are **six modes of operation for the counters.**
- In all modes the **counters operate as down counters.**
- They are defined as follows:
- Mode 0: Interrupt on Terminal Count/ Event counter
- Mode 1: Hardware Re triggerable One-Shot
- Mode 2: Rate Generator
- Mode 3: Square Wave Mode
- Mode 4: Software Triggered Strobe
- Mode 5: Hardware Triggered Strobe (Re triggerable)

OPERATING MODES PIT 8254

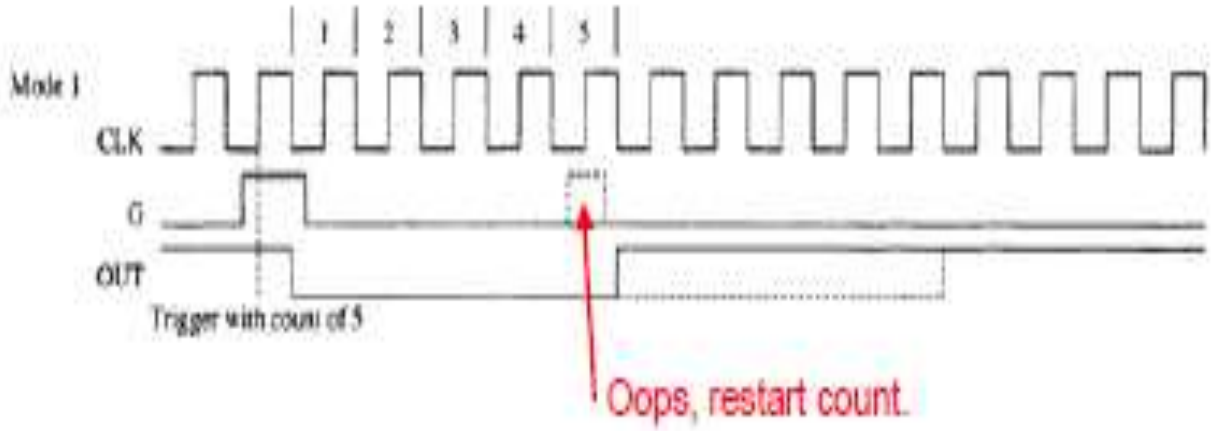
MODE 0: Interrupt on terminal count

1. Event counting.

2. After the Control Word is written, OUT is initially low and rema
3. When the counter reaches zero. OUT then goes high and remains hi
or a new Mode 0 Control Word is written into the Counter.

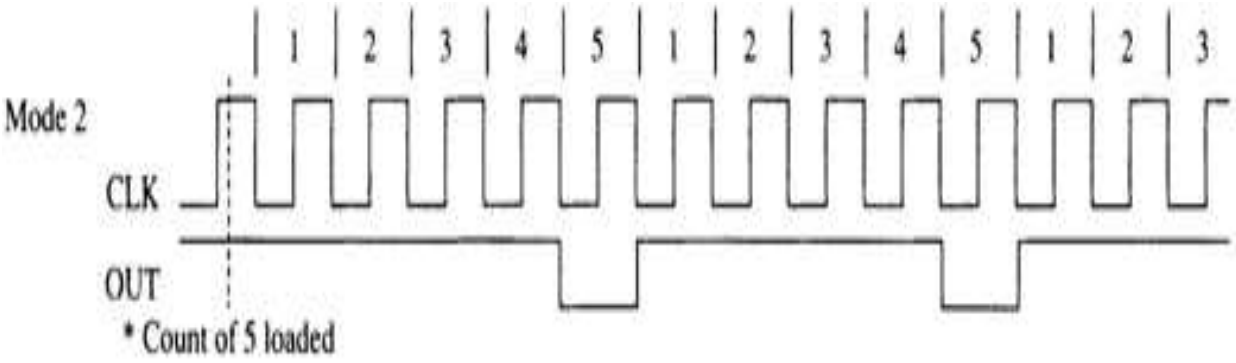


- **MODE 1: Hardware retriggerable one-shot**
  1. OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and remain low until the Counter reaches zero.
  2. OUT will then go high and remain high until the CLK pulse after the next trigger.



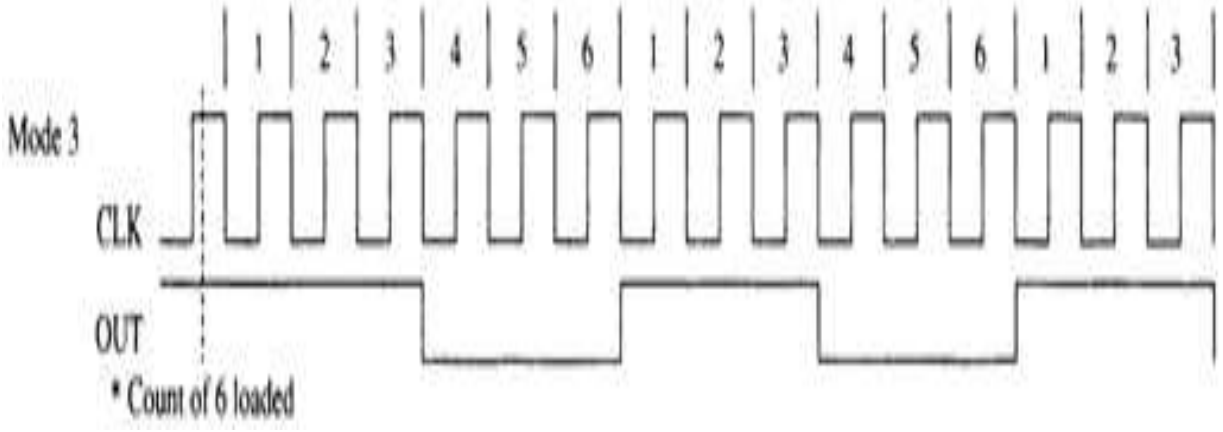
MODE 2: Rate generator

1. Functions like a divide-by-N counter and used to generate a Real Time Clock interrupt.
2. OUT will initially be high.
3. When the initial count has decremented to one, OUT goes low for one CLK pulse.
4. Out then goes high again, the Counter reloads the initial count and the process is repeated.
5. MODE 2 is periodic. The same sequence is repeated indefinitely.



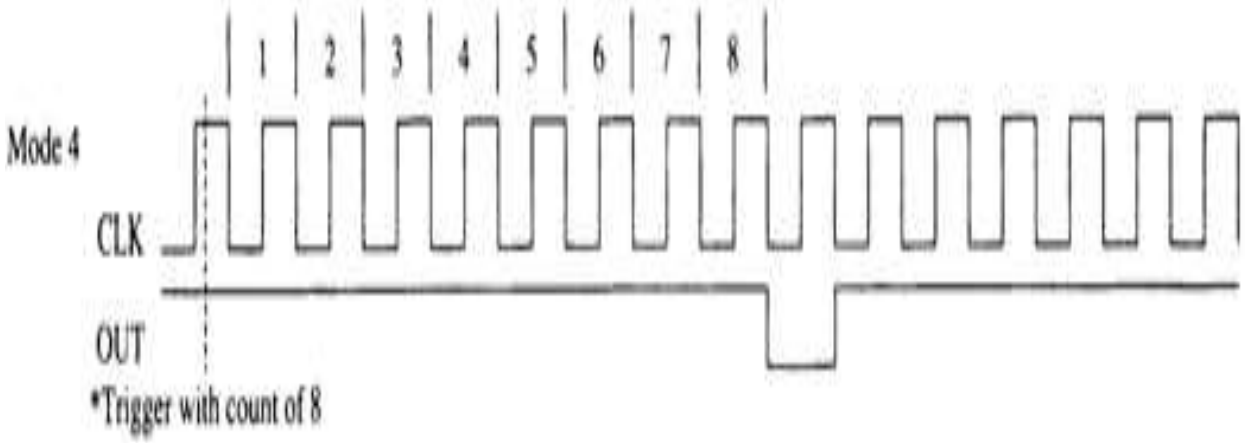
MODE 3: Square wave mode

1. Typically used for baud rate generation.
2. Out will initially be high.
3. When half the initial count is expired, OUT goes low for the remainder of the count.
4. MODE 3 is periodic. The same sequence is repeated indefinitely.



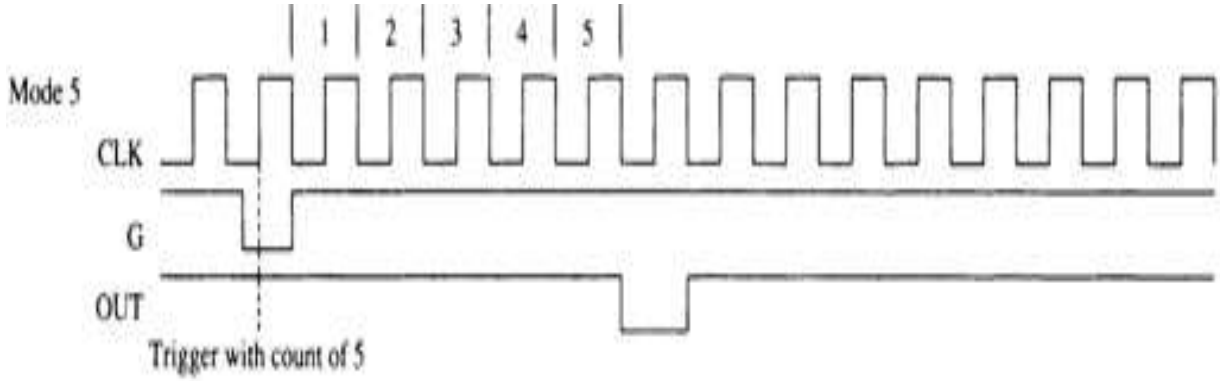
- **MODE 4: Software triggered strobe**

1. OUT will initially be high.
2. When the initial count expires, OUT will go low for one CLK pulse and then go high again.
3. The counting sequence is "triggered" by writing the initial count.
4. The Counter is loaded on the next CLK pulse following writing a Control Word and initial count.



MODE 5: Hardware triggered strobe (retriggerable)

1. OUT will initially be high.
2. Counting is triggered by a rising edge of GATE.
3. When the initial count expires, OUT will go low for one CLK pulse and then go high again.
4. The difference between MODE 4 and MODE 5 is that in MODE 5 the count will not be loaded until the CLK pulse after a trigger.



Q3 WAP for generation of 1KHz square wave with counter0 if CLK= 1MHz.

Solution

<u>Control Word</u>

Counter0 is selected in mode3 used for square wave generation.

Control Word = 36 H (54D)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	0

Example has the 8-bit control word = 00110110 binary which in decimal is equal to 54

No. of counts = CLK FREQUENCY/ REQUIRED FREQUENCY

= 1 MHz/ 1 KHz

=1000

Assume Port Address for Counter0 is 80H

Port Address for Counter1 is 82H

Port Address for Counter2 is 84H

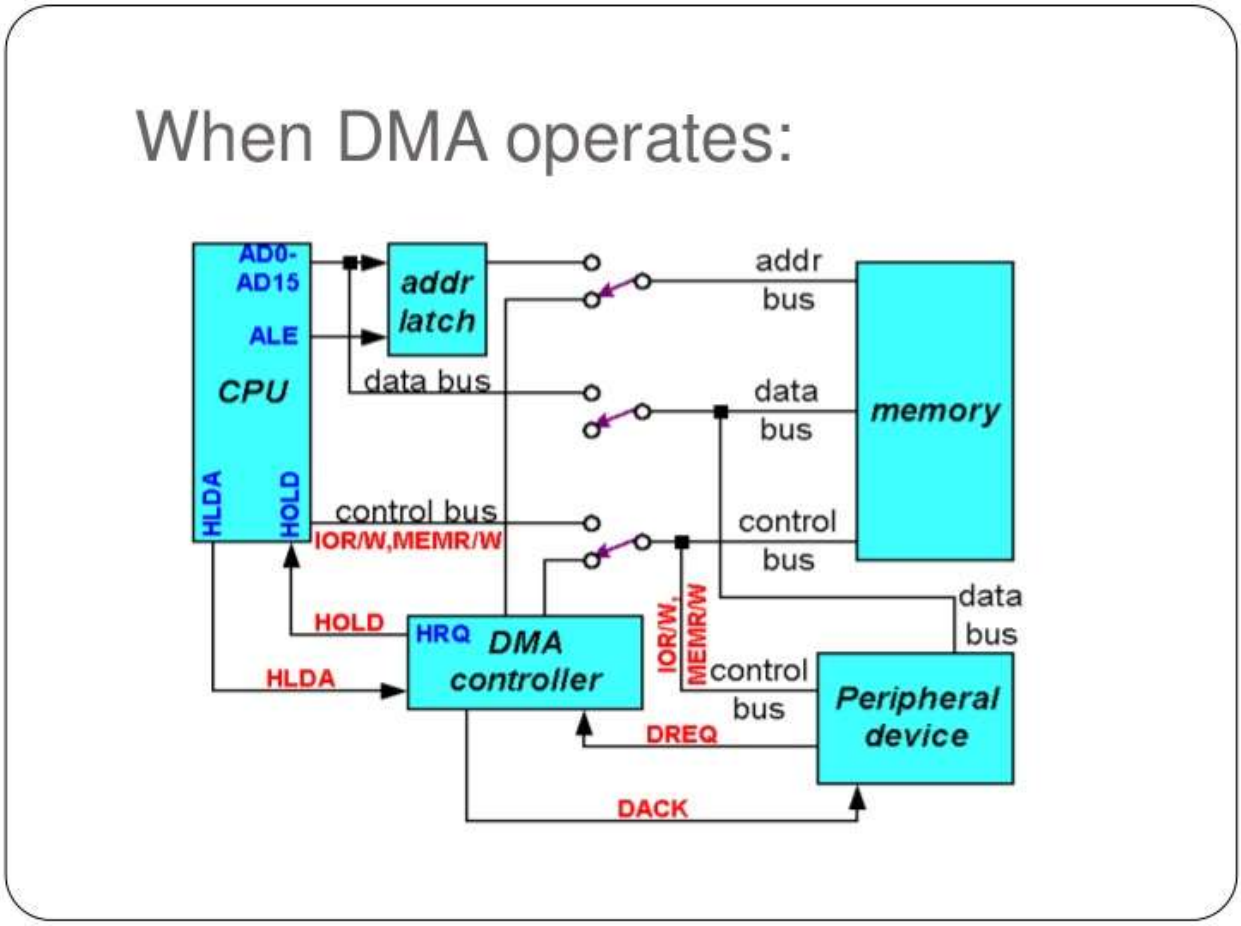
Port Address for Control word register is 86H

Program

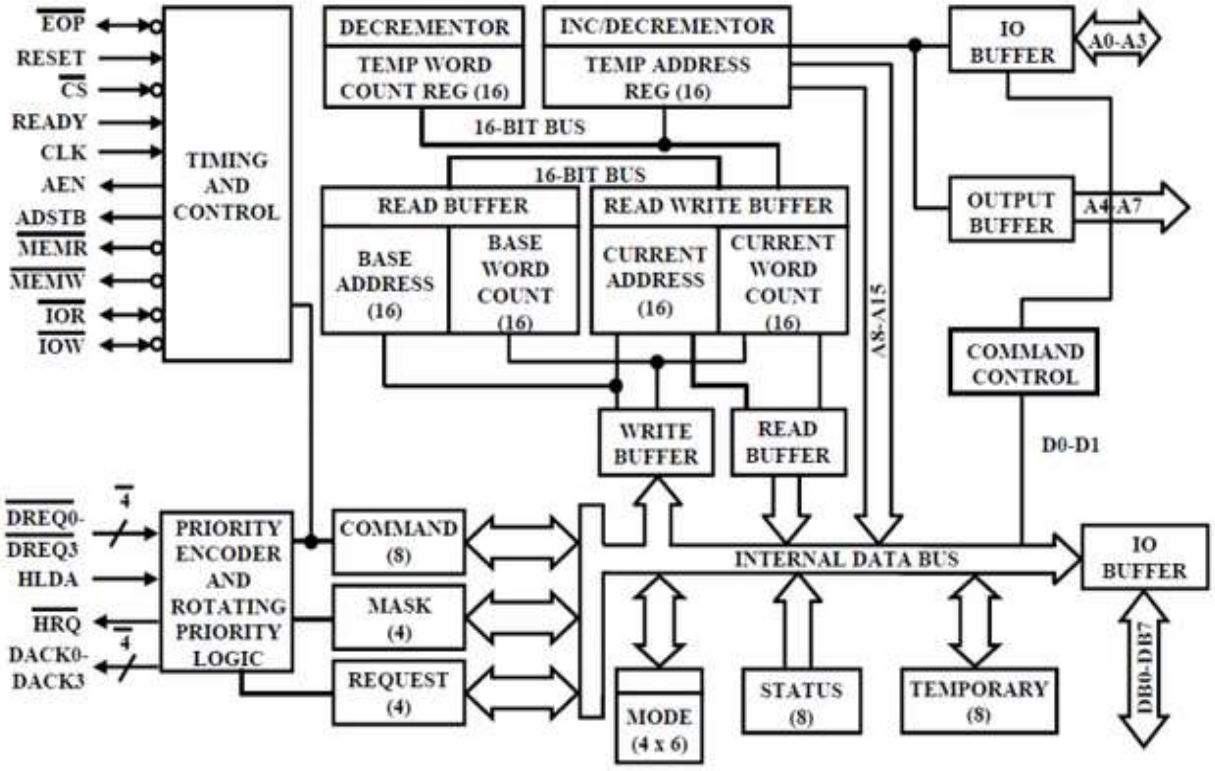
```
MOV AL, 36H; LOAD CONTROL WORD TO AL
OUT 86H, AL; TO LOAD CONTROL WORD TO CWR AT PORT ADDRESS 86H
MOV AL, 00  ; TO LOAD NO. OF COUNTS LOW BYTE FIRST i.e. 00
OUT 80H, AL  ; to port address 80H
MOV AL, 10;TO LOAD NO. OF COUNTS HIGH BYTE NEXT i.e. 10
OUT 80H, AL  ; to port address 80H
```

Q4. What is DMA ? Explain its operation. Draw and explain block diagram of DMA Controller. Explain its modes of operation.

- **Ans-** The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.
- *DMA controller*: dedicated hardware used for controlling the DMA operation
- A DMA controller temporarily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly between an I/O port and a series of memory locations.
- The DMA transfer is also used to do high-speed memory-to memory transfers.
- Two control signals are used to request and acknowledge a DMA transfer in the microprocessor-based system.
- The HOLD signal is a bus request signal which asks the microprocessor to release control of the buses after the current bus cycle.
- The HLDA signal is a bus grant signal which indicates that the microprocessor has indeed released control of its buses by placing the buses at their high-impedance states.



- **DMA OPERATION The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles.**
- **IDLE CYCLE When no channel is requesting service, the 8237A will enter the Idle cycle. In this cycle the 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service**
- **ACTIVE CYCLE When 8237 is in idle cycle and unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:**



- **The 8237A block diagram includes the major logic blocks and all of the internal registers.**
- **The 8237A contains three basic blocks of control logic.**
- **The Timing Control block generates internal timing and external control signals for the 8237A.**
- **The Program Command Control block decodes the various commands given to the 8237A by the micro-processor prior to servicing a DMA Request.**

- **It also decodes the Mode Control word used to select the type of DMA during the servicing.**
- **The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously**
- **The 8237A is designed to operate in two major cycles.**
- **These are called Idle and Active cycles.**

MODES OF OPERATION OF 8237 DMA CONTROLLER

The 8237 operates in four different modes, depending upon the number of bytes transferred per cycle and number of ICs used.

- **Single - The device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.**
- **Block - Transfer progresses until the word count reaches zero or the EOP signal goes active.**
- **Demand - Transfers continue until TC or EOP goes active or DRQ goes inactive. The CPU is permitted to use the bus when no transfer is requested.**
- **Cascade - Used to cascade additional DMA controllers. DREQ and DACK is matched with HRQ and HLDA from the next chip to establish a priority chain. Actual bus signals is executed by cascaded chip.**

Q5. Draw and explain block diagram of 8259 Programmable Interrupt Controller. Write its Control Word.

Solution:

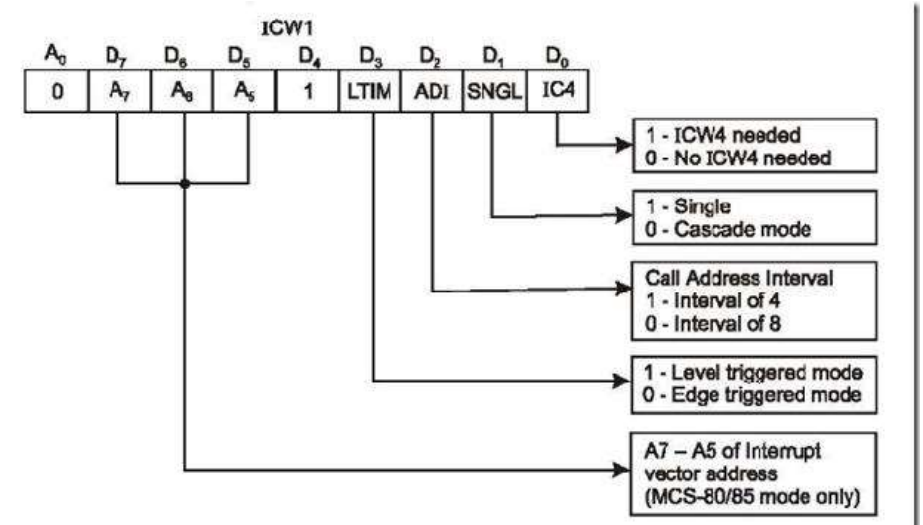


Fig. 9e.8: Initialisation command word 1 (*Source:* Intel Corporation)

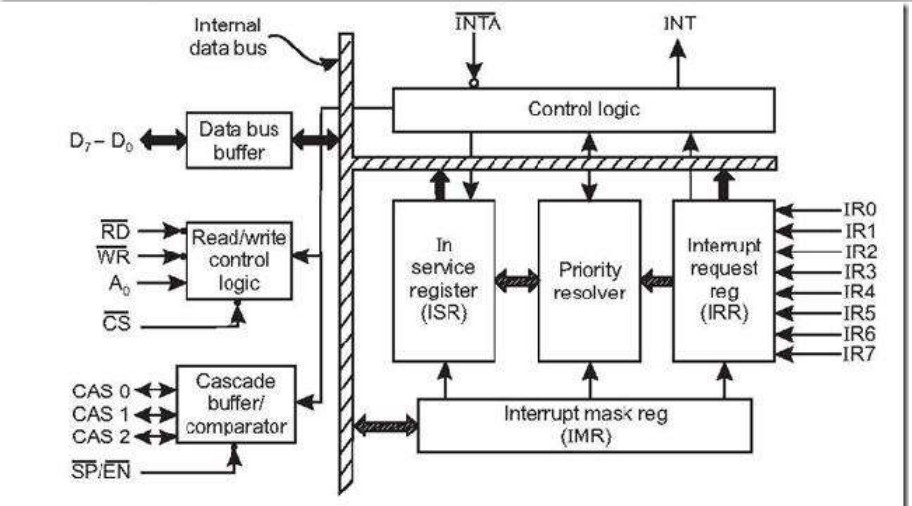


Fig. 9e.2: 8259 Functional block diagram (*Source:* Intel Corporation)

- **Interrupt Sequence:**

1.One or more of the IR lines goes high.
2.Corresponding IRR bit is set.

3.8259 evaluates the request and sends INT to CPU.
4.CPU sends .
5.Highest priority ISR is set. IRR is reset.
6.8259 releases CALL instruction on data bus.
7.CALL causes CPU to initiate two more pulses.
8.8259 releases the subroutine address, first lowbyte then highbyte.
9.ISR bit is reset depending upon mode.

The main features of 8259A programmable interrupt controller are:

1)It can handle eight interrupt inputs. This is equivalent to providing eight interrupt pins on the processor in place of one INTR in 8085

2)The chip can vector an interrupt request anywhere in the memory map from 0000H to FFFFH in 8085A microprocessor. However, all the eight interrupts are spaced at an interval of either four or eight locations.

3)It can resolve eight levels of interrupt priorities in a variety of modes. The priorities of interrupts can be changed under running condition.

4)Each of the interrupt requests can be masked individually.

5)The status of pending interrupts, in service interrupts, and masked interrupts can be read at any time.

6)The chip can be programmed to accept interrupt requests either as level triggered or edge triggered interrupt request

7)If required, nine 8259As can be cascaded in a master-slave configuration mode to handle 64 interrupt inputs.

Functional Description: The 8259A (PIC) has eight interrupt request inputs – IR7 - IR0. The 8259A uses its INT output to interrupt the 8085A via INTR pin. The 8259A receives interrupt acknowledge pulses from the ���� at its INTA input. Vector address, used by the 8085A to transfer control to the service subroutine of the interrupting device, is provided by the 8259A on the data bus. The 8259A is a programmable device that must be initialized by command words sent by the microprocessor. After initialization the 8259A mode of operation can be changed by operation command words from the microprocessor

The descriptions of various blocks are given below:

Data bus buffer: This 3- state, bidirectional 8-bit buffer is used to interface the 8259A to the system data bus. Control words and status information from the microprocessor to PIC and from PIC to microprocessor respectively, are transferred through the data bus buffer.

Read/Write Control Logic : The function of this block is to accept output commands sent from the CPU. It contains the initialization command word (ICW) registers and operation command word (OCW) registers which store the various control formats for device operation. This function block also allows the status of 8259A to be transferred to the data bus.

Interrupt Request Register (IRR):It is an 8-bit register – one bit for each interrupt request. It stores all the interrupt inputs that are requesting service. If an interrupt input is unmasked, and has an interrupt signal on it, then the corresponding bit in the IRR will be set. The content of this register can be read to know the status of pending interrupts.

Interrupt Mask Register (IMR): The IMR is used to disable (Mask) or enable (Unmask) individual interrupt request inputs. This is also an 8-bit register. Each bit in this register corresponds to the interrupt input with the same number. To unmask any interrupt the corresponding bit is set ‘0’.

In-service Register (ISR): The in-service register keeps track of which interrupt inputs are currently being serviced. For each input that is currently being serviced the corresponding bit of in-serviceregister (ISR) will be set. In 8259A, during the service of an interrupt request, if another higher priority interrupt becomes active, it will be acknowledged and the control will be transferred from lower priority interrupt service subroutine (ISS) to higher priority ISS.

Priority Resolver: This logic block determines the priorities of the interrupts set in the IRR. It takes the information from IRR, IMR and ISR to determine whether the new interrupt request is having highest priority or not. If the new interrupt request is having the highest priority, it is selected and processed. The corresponding bit of ISR will be set during interrupt acknowledge machine cycle.

Cascade Buffer/Comparator: This function block stores and compares the IDs of all 8259A's in the system. The associated 3-I/O lines (CAS2-CAS0) are outputs when 8259A is used as a master and are inputs when 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS2-0 lines. The slave 8259As compare this ID with their own programmed ID. Thus selected 8259A will send its pre-programmed subroutine address on to the data bus during the next one or two successive INTA pulses.