DISCRETE OPERATIONAL AMPLIFIER

AIM OF THE PROJECT:

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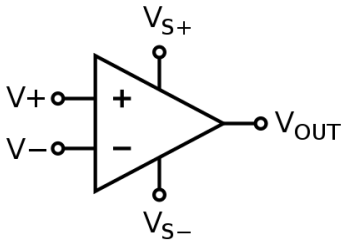
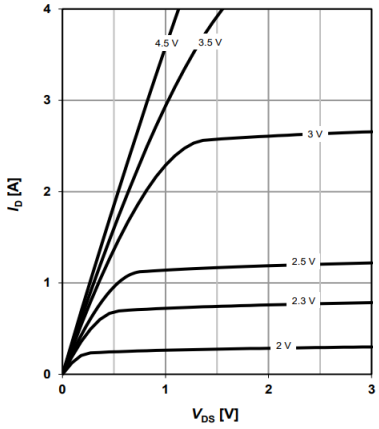
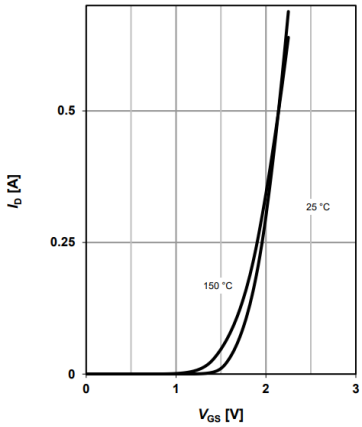


Figura 1: Circuit symbol of an Op.Amp

1. CHOICE OF TECHNOLOGY:

We decided to start the project using only discrete transistors made of MOSFET technology because it was the one we used more in those 2 years. Also, we know the benefits: the gate of mosfet has higher impedance than a BJT's base. This process started when we were still attending Analog Electronics class, so at first we wanted to make also the output stage out of MOSFETs. Then we were introduced to BJTs (or bipolar transistors) and we thought it could be better to change our initial idea. In fact, bipolar transistors can be used to obtain output stages with lower impedance than mosfet ones, their signal amplification is obviously more linear than a mosfet one (so a lower distortion is possible) and they're better as current generators.





MOSFET choice is on two small signals models, an N-channel BSD235N and a P-channel BSD223P made by Infineon.

Here are some data we got from respective datasheet.

IMPORTANT: we are fully aware that commercial transistors are produced with very different characteristics. Even on datasheets, a single parameter can be found on a wide range of values, thus assuming this devices will just have the same behaviour is not realistic. Collecting data and simulate the circuit is made just to get ideas on how the final product could work.

	N-channel BSD235N	P-channel BSD223P
V_{th}	0.95 V	- 0.9 V
V_{BD}	+20 V	- 20V
C_{GS}	45.8 pF	28 pF
C_{GD}	3.2 pF	17 pF
K_P	2.4 A/V^2	0.51 A/V^2
W/L	0.39	0.82
PACK	SOT 363-6 (dual N)	SOT 363-6 (dual P)
λ	0.02	0.01

BJT choice is on two small signals models, an NPN BC847BS and a PNP BC857BS made by Nexperia. Fortunately, they are complementary transistors and have maximum ratings of V_{CE} = 45V , I_C = 100 mA and h_{fe} = 450.

2. THE DIFFERENTIAL PAIR AND GAIN STAGE:

The core of the project is obviously the Differential Pair which is able to amplify the difference of two electric signals.

$$Vo = G_{diff}\,(V1 - V2) + G_{cm}\,(\frac{V1+V2}{2})$$

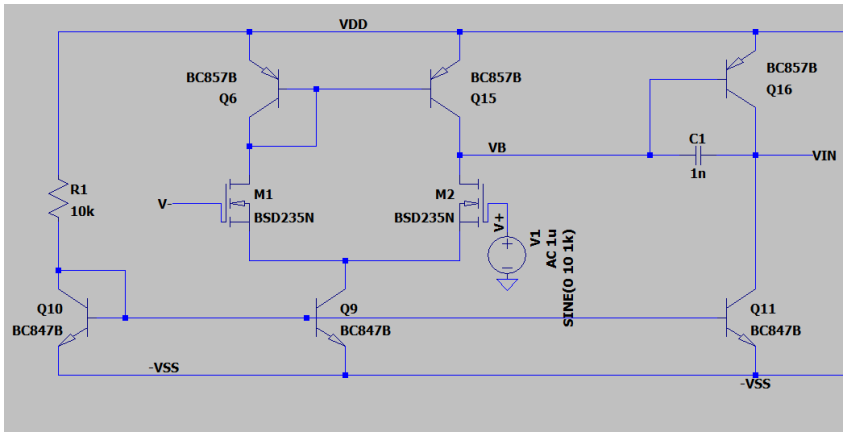


Figura 2: Differential Pair and Common Emitter amplifier

2.1. BIASING POINT

It is important to set Working Point of the circuit. In this case, we have decided to use current generators, in particular Current Mirrors. There is just one of them, and it provides the same amount of current to both amplifier stages: it is made of NPN BJTs (Q10, Q9 and Q11. Usually it's not easy to realize Current Mirrors out of discrete transistors, but our plan to minimize differences is to use equal bjts out of Dual NPN/PNP packages.
The main problem here is that the circuit is not provided of current generators whose values are independent of supply voltage, so biasing current will change from 2mA @ ±10V and 0.5mA @ ±3V. It is important to remember that Q10 will always remain in saturation region because it's in a Transdiode configuration.

2.2. SMALL SIGNAL AND FREQUENCY BEHAVIOUR

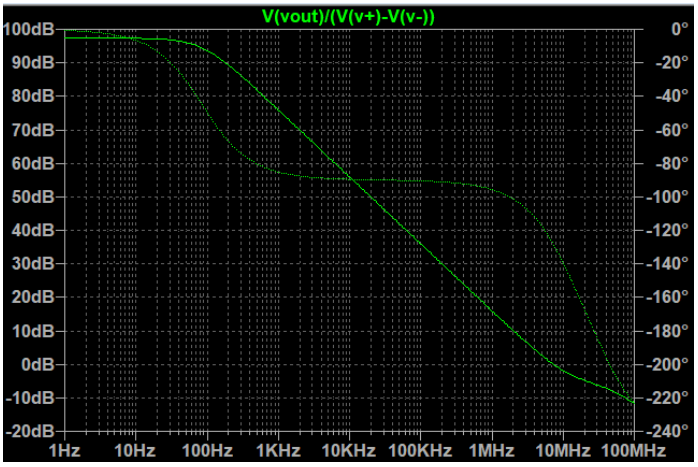


Figura 3: Gain Stage Bode diagram

Small signal gain is a lot influenced by Early Mosfet's Voltage, but again, this parameter was just guessed to run the simulation because we haven't been able to calculate it from datasheet. The value of *r0* (which is the output resistance) is dependent to Early Voltage.

BJTs r0 is lower than a MOSFET one (keeping current constant), but they significally improve input signal range.

In this case, we get a Low Frequency gain of over 100dB (~10^5), so OpAmp will work in linear region with a 10µV input, and a dominant pole at around 30 Hz. Note there's a zero at 10MHz.

We decided to use a 1nF capacitor between Q16 Base and Collector to get Miller Effect advantages. Because there's a gain between these two nodes, equivalent resistance is amplified: $R_{EQ} = R_{SX}(1 + G) + R_{DX}$

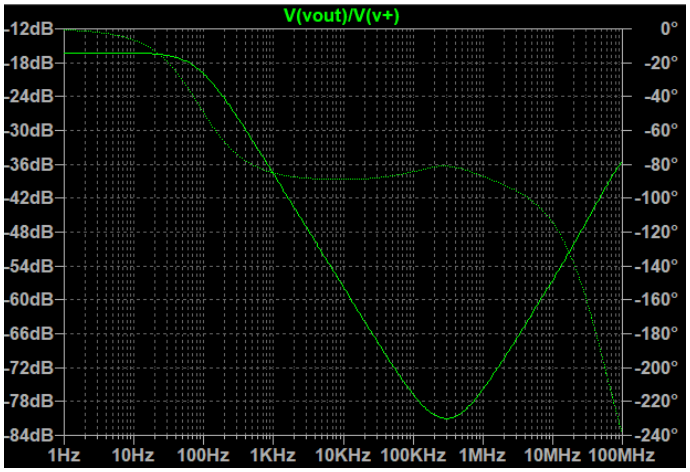


Figura 4: Common Mode Gain

It's important to measure Common Mode gain. An ideal operational amplifier has an infinite Common Mode Rejection Ration (CMRR), so it is provided of a very low Common Mode gain.

2.3. NOISE OUTPUT EFFECT

Figura 5: Noise of differential stages

2.4. HARMONIC DISTORTION

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component
1	1.000e+03	6.231e-03	1.000e+00
2	2.000e+03	3.350e-06	5.376e-04
3	3.000e+03	2.250e-06	3.610e-04

Total Harmonic Distortion: 0.064754%(0.099526%)

Figura 5: Differential Stage HD in Linear Region

When this amplifier is working in Linear Region, so the input is 1μV and the output is not saturated, total Harmonic distortion (which is a direct consequence of quadratic current formula for mosfet current $I = K(V_{GS} - V_T)^2$) is just 0.065%. Obviously, this value increases a lot when input increase, but when this happen, output is already saturated.

3. OUTPUT STAGE

The ideal output stage is a voltage Buffer: its features are High (infinite) Input Impedance and Low (zero) Output Impedance. We made one out of BJTs as we mentioned before, it's a complementary BJTs stage, also known as a Push-Pull amplifier stage.

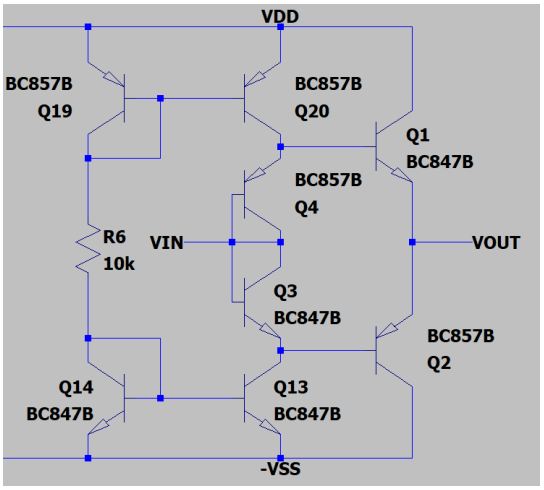


Figura 6: Output Push-Pull Stage

3.1. WORKING POINT

Even in the out stage, Biasing point is set by two Current Mirrors (NPN/PNP generators, Q14 and Q19). We used them both to maintain symmetry. In a push-pull stage, it is really important to hold Q1 and Q2 in a correct working region, so base-emitter voltage must be V_{BE} =0.7V. When discrete components are used, it is very common to see two diodes in series to achieve this goal. We wanted to keep a clean design and decided to use BJTs in a transdiode configuration (so their emitter-collector voltage is 0.7V).

3.2. OUTPUT IMPEDANCE

Thanks to BJTs, Output Impedance can be low. Note that, decreasing R6 would increase current absorption by output stage, so a lower Load can be driven by the output. In fact:

$$R_{OUT} = \frac{1}{2g_m} = {}^{25mV}/_{2I_{OUT}}$$

Figura 7: Input – Output FdT with Load from 10Ω to 100Ω

According to this chart, a minimum Load value could be 50Ω as Open Loop gain is decreased less than 3dB (70% of the original).

3.3. POWER CONSIDERATIONS

Maximum BJTs power dissipation is 0.5W for the NPN model and 0.25W for the PNP one.

A comparator configurations made with this amplifier consume around 13mA @ ±10V, so a total power consumption of 260mW. This mean that, without any load attached, output transistor will dissipate 25mW.

However, it is not secure to connect a low impedance load. A 50Ω resistor will draw a 180mA when output is saturated at 9V. This mean a total output power of 1.6W.

3.4. FdT, NOISE AND HARMONIC DISTORTION OF OUTPUT STAGE

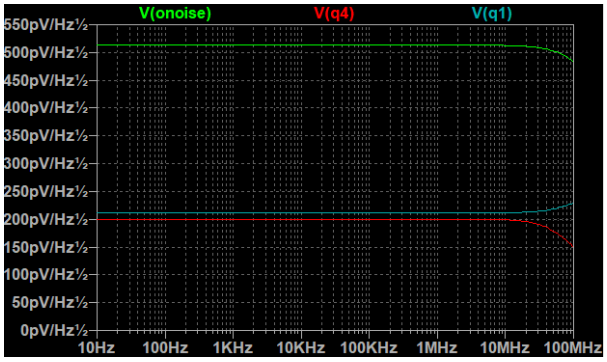


Figura 8: Push-Pull stage noise on the output

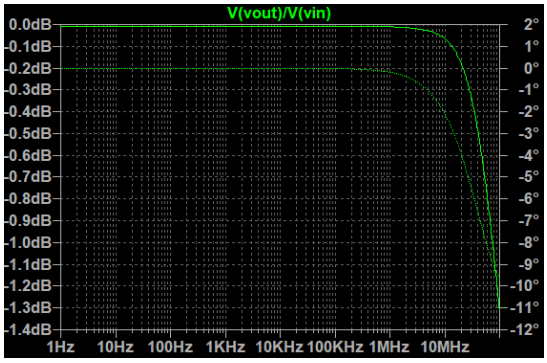


Figura 9: Push-Pull stage FdT

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	8.880e-07	1.000e+00	-0.00°	0.00°
2	2.000e+03	9.019e-15	1.016e-08	-13.90°	-13.90°
3	3.000e+03	1.313e-14	1.479e-08	-4.70°	-4.70°

Total Harmonic Distortion: 0.000002% (0.000000%)

Figura 10: Push-Pull stage HD in linear region (1uV op.amp input)