RTL8720CM-VH2-CG
RTL8720CF-VH2-CG

Ameba ZII
802.11b/g/n 1T1R WLAN + Bluetooth SoC

DATASHEET
(CONFIDENTIAL: Development Partners Only)

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This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.9	2020/06/10	Initial Version
0.91	2020/08/11	Modify 9.5.1/9.5.3 diagram and spec table.
0.92	2020/11/18	Add 9.5 Absolute Maximum Ratings
0.93	2020/11/19	Add 9.6 ESD characteristics
0.94	2021/3/22	Modify Pin8 from VA11_SYN to NC.

Revision	Release Date	Summary
1.0	2023/2/24	Remove RLT8720CN-VH2-CG part number Add VD11_CORE/VD1833_LPC/IDD33 to Table 22 Added note to Table 25 Timing Specification for Power on Sequence, page 35. Added note to Table 26 Timing Specification for Resume from Standby Mode Sequence, page 36. Revised Figure 23 Timing Sequence of Shutdown, page 37. Revised and added note to Table 27 Timing Specification for Shutdown Sequence, page 37. Added section 9.6.4 BOR Sequence, page 38. Revised section 10 Mechanical Dimensions.

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1. General Description

Realtek Ameba ZII series is a highly integrated single-chip with a low power 802.11n Wireless LAN (WLAN) network controller. It combines a Real-M300 (KM4) CPU which is based on ARMv8-M architecture, WLAN MAC, a 1T1R capable WLAN baseband, RF circuit, and Bluetooth Low Energy (BLE) in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

Ameba ZII series integrates internal memory for the full Wi-Fi protocol functions. The embedded memory configuration also provides simple application developments.

2. Features

MCU Feature

- Real-M300 KM4 clock frequency up to 100MHz
- Cache 32KB/D-Cache 16KB
- Support DMA
- eXecute In Place (XIP) on flash

Internal Memory

- Support 384KB ROM
- Support 256KB RAM
- Support external flash interface
- Support MCM embedded 4MB pSRAM (Option, RTL87x0C**M**-Vx2-CG)
- Support MCM embedded 2MB Flash (Option, RTL87x0C**F**-Vx2-CG)

Wi-Fi Feature

- 802.11 b/g/n 1x1, 2.4GHz
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- Support low power Tx/Rx for short-range application
- Support Antenna diversity
- Support Wi-Fi WPS
- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- Integrated balun, PA/LNA

Bluetooth Low Energy

- Bluetooth Low Energy (BLE) 4.2
- Support LE secure connections
- Support LE scatternet
- Support 1 Master/1 Slave.

Secure

- Support ARM TrustZone-M
- Support secure boot
- Wi-Fi WEP, WPA, WPA2, WPS
- Crypto engine: MD5, SHA-1, SHA2-224, SHA2-256, HMAC, AES

Peripheral Interfaces

- 3 x UART interface, baud rate up to 4MHz and all of them can configurable as log UART
- 1 x I2C, Max clock 400Kbps
- 1 x SDIO 2.0 Device, up to 50MHz
- 1 x SPI, Master clock up to 25Mbps/Slave clock up to 5Mbps
- 8 x PWM with configurable duration and duty cycle from 0 ~ 100%
- 16 x programmable GPIOs (RTL8720CF support 20pins GPIO)
- 1 GDMA with 2 channels

Clock source

- 40MHz crystal oscillator

Package Type

- 5mm x 5mm x 0.85mm
- QFN40 pins

3. Block Diagram

Ameba ZII diagram is shown below which contains a general application scenario. External devices could connected with the plenty of peripheral interfaces. The PMU and related blocks for low power application are also elaborate on this diagram.

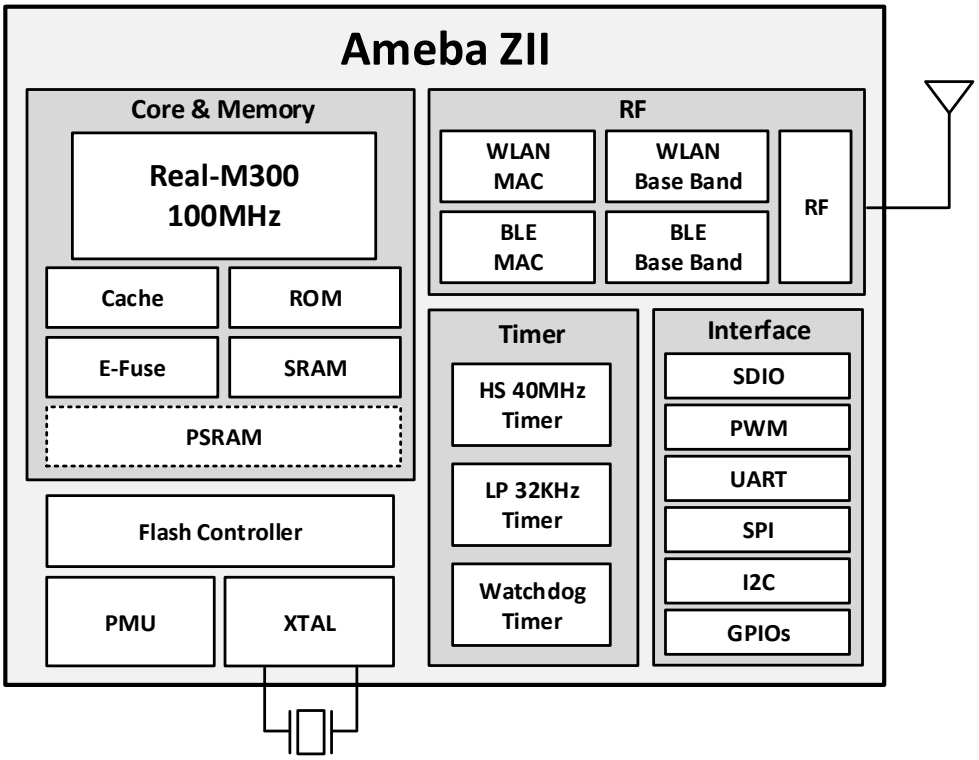


Figure 1. Block Diagram of Ameba ZII

3.1. Power Architectonics

Below figure shows the Ameba ZII power management control unit architecture.

The PMU provides the following functions:

- SWR 1.1V output from 3.3V (optional for LDO mode).
- LDO 2.5V output for writing E-fuse from 3.3V.
- Wakeup system detector to resume from low power state

3.1.1. Regulators Architectonics

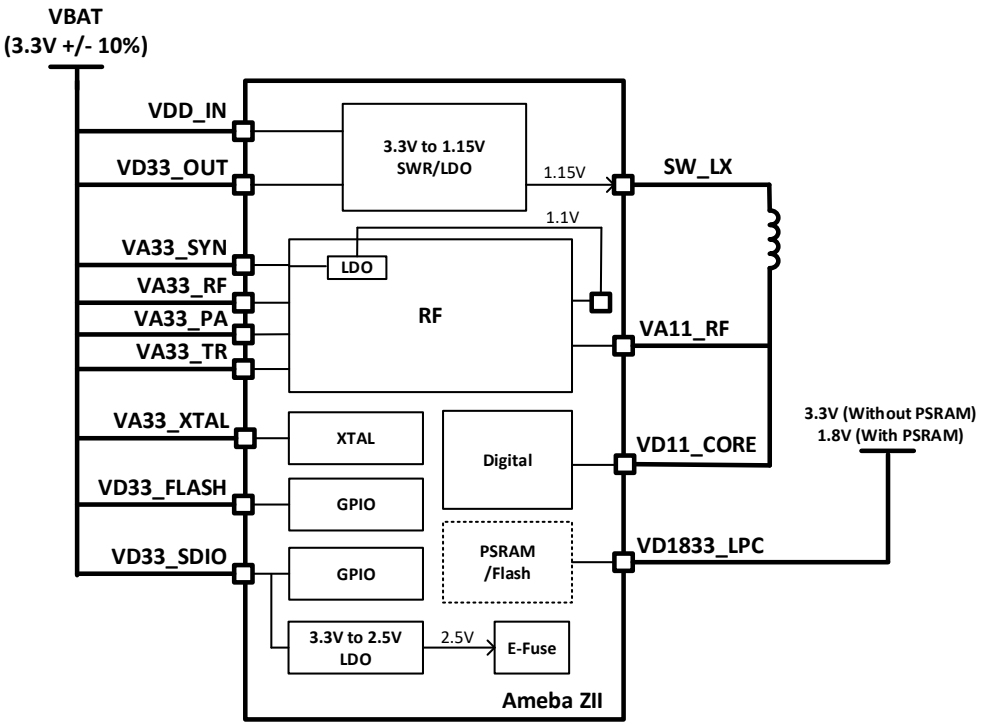


Figure 2. Regulators Architectonics of Ameba ZII

3.1.2. Shutdown Mode

CHIP_EN de-asserts to shutdown whole chip without external power cut components required.
CHIP_EN pull high trigger system into active mode.

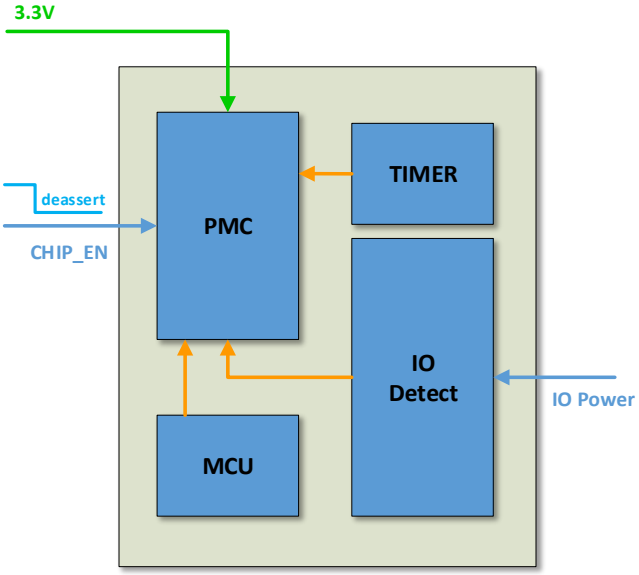


Figure 3. Power Diagram of Shutdown Mode

3.1.3. Deep Sleep Mode

CHIP_EN remains high. Users can invoke Deep Sleep API to enter deep sleep mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Reboot flow

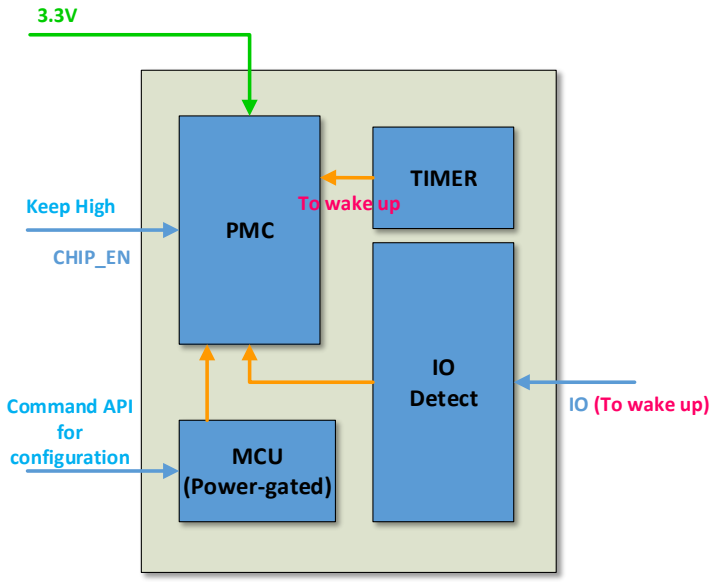


Figure 4. Power Diagram of Deep Sleep Mode

Table 1. Deep Sleep Mode Wakeup Source

Wakeup Source	Note
Low Precision Timer	N/A
Wake pin	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depend on package) , GPIOA_8 (depend on package) ,GPIOA_9 (depend on package) , GPIOA_10 (depend on package) , GPIOA_11 (depend on package) , GPIOA_12 (depend on package) , GPIOA_13 GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18,GPIOA_19, GPIOA_20, GPIOA_23

3.1.4. Standby Mode

CHIP_EN remains high. Users can invoke Standby API to enter standby mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Fast reboot flow

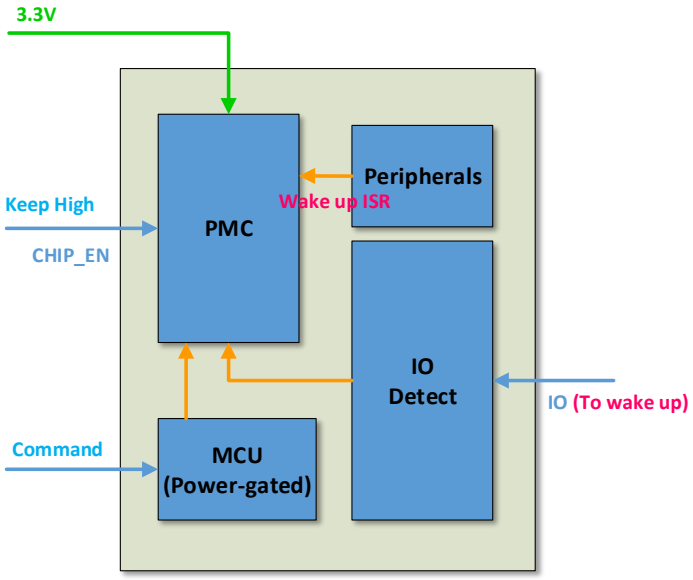


Figure 5. Power Diagram of Standby Mode

Table 2. Standby Mode Wakeup Source

Wakeup Source	Note
Low Precision Timer	N/A
Wake pin	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depend on package) , GPIOA_8 (depend on package) ,GPIOA_9 (depend on package) , GPIOA_10 (depend on package) , GPIOA_11 (depend on package) , GPIOA_12 (depend on package) , GPIOA_13 GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18,GPIOA_19, GPIOA_20, GPIOA_23
UART0	N/A
WLAN	N/A
PWM	N/A
HS Timer	N/A

3.1.5. Sleep Mode

CHIP_EN remains high. Users can invoke Sleep API to enter sleep mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Execution of instructions continues

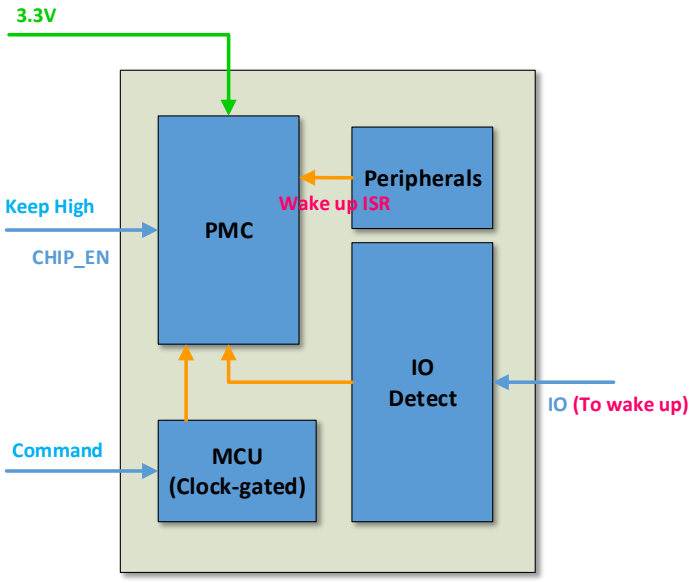


Figure 6. Power Diagram of Sleep Mode

Table 3. Sleep Mode Wakeup Source

Wakeup Source	Note
Low Precision Timer	N/A
Wake pin	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depend on package) , GPIOA_8 (depend on package) ,GPIOA_9 (depend on package) , GPIOA_10 (depend on package) , GPIOA_11 (depend on package) , GPIOA_12 (depend on package) , GPIOA_13 GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18,GPIOA_19, GPIOA_20, GPIOA_23
UART0	N/A
WLAN	N/A
PWM	N/A
HS Timer	N/A
SDIO Device	N/A

3.1.6. Snooze Mode

CHIP_EN remains high. Specified interrupts can wake up the system.

The wake flow is:

1. WLAN power on request
2. Receive particular beacon
3. Wake up ISR is high
4. PMC
5. Enable CPU
6. Execution of instructions continues or fast reboot occurs

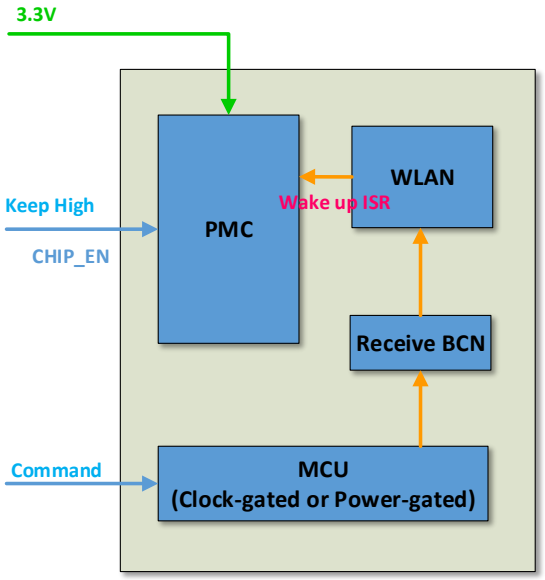


Figure 7. Power Diagram of Snooze Mode

4. Pin Assignments

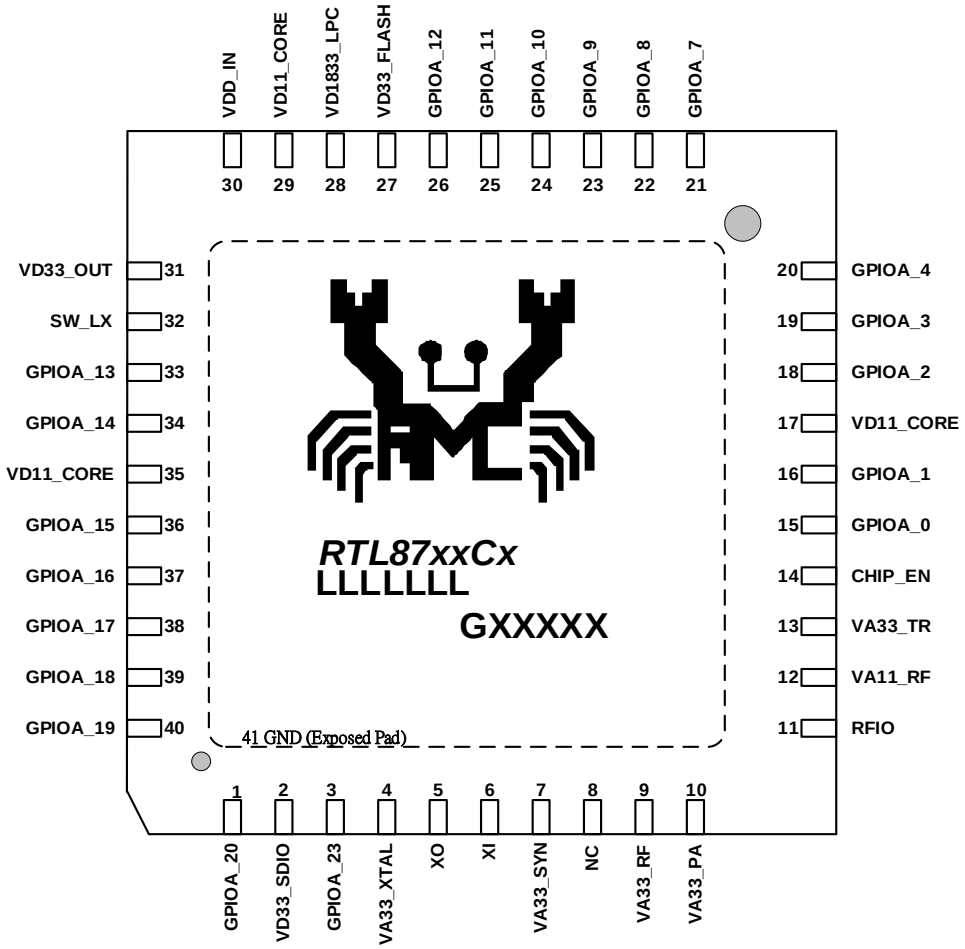


Figure 8. Pin Assignments

4.1. Package Identification

Green package is indicated by the 'G' in GXXXXX.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input O: Output

PI: Power Input PO: Power Output

5.1. Power On Trap Pin

Table 4. Power On Trap Pins

Symbol	Type	Pin No	Description
GPIOA_0 (TEST_MODE_SEL)	I	15	● 1: Enter into test/debug mode ● 0: Normal operation mode
GPIOA_1 (Autoload_Fail)	I	16	● 1 : eFUSE settings are not loaded ● 0: eFUSE settings are loaded
GPIOA_23 (SPS_LDO_SEL)	I	3	● 1: LDO ● 0: SWR

5.2. RF Pins

Table 5. RF and NFC Pins

Symbol	Type	Pin No	Description
RF_IO	IO	11	WL RF signal

5.3. Power Pins

Table 6. Power Pins

Symbol	Type	Pin No	Description
VD33_SDIO	PI	2	3.3V power for SDIO
VA33_XTAL	PI	4	3.3V power for XTAL
VA33_SYN	PI	7	3.3V power for Synthesizer
VA33_RF	PI	9	3.3V power for RF
VA33_PA	PI	10	3.3V power for RF PA
VA11_RF	PI	12	1.15V power for RF
VA33_TR	PI	13	3.3V power for RF
VD11_CORE	PI	17	1.15V power for digital core
VD33_FLASH	PI	27	3.3V power for flash
VD1833_LPC	PI	28	1.8V power for PSRAM if part number embedded MCM PSRAM 3.3V power for Flash if part number embedded MCM Flash 3.3V power for IO if part number without PSRAM/Flash
VD11_CORE	PI	29	1.15V power for digital core
VDD_IN	PI	30	3.3V power input
VD33_OUT	PI	31	3.3V power for SWR/LDO
SW_LX	PO	32	1.15V output power from SWR/LDO
VD11_CORE	PI	35	1.15V power for digital core

5.4. Clock Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	6	Input of 40MHz Crystal Clock Reference
XO	O	5	Output of 40MHz Crystal Clock Reference

5.5. Chip Enable Pins

Table 8. Chip Enable Pin

Symbol	Type	Pin No	Description
CHIP_EN	I	14	● 1: Enable chip. ● 0: Shutdown chip.

5.6. Digital IO Pins

Ameba ZII supports max. 20 GPIO pins and all of them are configurable. Refer to 錯誤! 找不到參照來源。 for detailed information and pin mux rules.

Table 9. GPIO Pins Table

Symbol	Type	Pin No	Description
GPIOA_20	IO	1	GPIO pins. The GPIO Pin Function Table could elaborate more detail.
GPIOA_23	IO	3	
GPIOA_0	IO	15	
GPIOA_1	IO	16	
GPIOA_2	IO	18	
GPIOA_3	IO	19	
GPIOA_4	IO	20	
GPIOA_7	IO	21	
GPIOA_8	IO	22	
GPIOA_9	IO	23	
GPIOA_10	IO	24	
GPIOA_11	IO	25	
GPIOA_12	IO	26	
GPIOA_13	IO	33	
GPIOA_14	IO	34	
GPIOA_15	IO	36	
GPIOA_16	IO	37	
GPIOA_17	IO	38	
GPIOA_18	IO	39	
GPIOA_19	IO	40	

Note: Default states of all pins are High-impedance; Unused pins should be kept floating.

5.6.1. GPIO Pin Function Table

Table 10. Pin Function Group Table

Pin Name	SPIC-Flash/SDIO	JTAG	UART	SPI/WL_LED	I2C	PWM
GPIOA_0		JTAG_CLK	UART1_IN			PWM[0]
GPIOA_1		JTAG_TMS	UART1_OUT	BT_LED		PWM[1]
GPIOA_2		JTAG_TDO	UART1_IN	SPI_CSn	I2C_SCL	PWM[2]
GPIOA_3		JTAG_TDI	UART1_OUT	SPI_SCL	I2C_SDA	PWM[3]
GPIOA_4		JTAG_TRST	UART1_CTS	SPI_MOSI		PWM[4]
GPIOA_7	SPI_M_CS			SPI_CSn		
GPIOA_8	SPI_M_CLK			SPI_SCL		
GPIOA_9	SPI_M_DATA[2]		UART0_RTS	SPI_MOSI		
GPIOA_10	SPI_M_DATA[1]		UART0_CTS	SPI_MISO		
GPIOA_11	SPI_M_DATA[0]		UART0_OUT		I2C_SCL	PWM[0]
GPIOA_12	SPI_M_DATA[3]		UART0_IN		I2C_SDA	PWM[1]
GPIOA_13			UART0_IN			PWM[7]
GPIOA_14	SDIO_INT		UART0_OUT			PWM[2]
GPIOA_15	SD_D[2]		UART2_IN	SPI_CSn	I2C_SCL	PWM[3]
GPIOA_16	SD_D[3]		UART2_OUT	SPI_SCL	I2C_SDA	PWM[4]
GPIOA_17	SD_CMD					PWM[5]
GPIOA_18	SD_CLK					PWM[6]
GPIOA_19	SD_D[0]		UART2_CTS	SPI_MOSI	I2C_SCL	PWM[7]
GPIOA_20	SD_D[1]		UART2_RTS	SPI_MISO	I2C_SDA	PWM[0]
GPIOA_23				LED_0		PWM[7]

6. Memory Organization

6.1. Memory Architecture

Ameba ZII integrates ROM, internal SRAM, extended NOR flash to provide applications with a variety of memory requirements.

6.1.1. Internal ROM

The internal integration of 384KB ROM provides high access speed and low memory leak. The ROM memory clock speed is up to 100MHz.

The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Peripheral Drivers & API
- Non-flash booting functions and drivers
- Security function libs

6.1.2. Internal SRAM

The maximum internal integration of 256KB SRAM provides instruction, data, and buffer usage. The maximum clock speed is up to 100MHz.

6.2. Memory Mapping

Memory map includes all available memory and register offset in Ameba ZII.

6.2.1. Programming Space

Table 11. Programming Space Majorly Design for Software Instruction Storage.

Start Address	Size	Secure	Cache Support	IP Function
0x0000_0000	384KB	Configurable	-	ITCM ROM
0x1000_0000	256KB	Configurable	-	TCM SRAM
0x2000_0000	32KB	Non-Secure	V	Additional SRAM for BT

6.2.2. IO Space

The address map of each peripheral hardware shown below:

Table 12. Address Map of Each Peripheral Hardware Table.

Start Address	Size	Secure	Cache Support	IP Function
0x2000_0000	32KB	Non-secure	V	Additional SRAM for BT
0x4000_0000	2KB	Non-secure	-	SYS Control (SYSON)
0x4000_1000	2KB	Non-secure	-	GPIO
0x4000_1C00	1KB	Non-secure	-	PWM
0x4000_2000	4KB	Non-secure	-	HS Timer

Start Address	Size	Secure	Cache Support	IP Function
0x4000_3000	1KB	Non-secure	-	UART0
0x4000_3800	2KB	Non-secure	-	LP Timer
0x4002_0000	4KB	Non-secure	-	SPI Flash Controller
0x4004_0000	1KB	Non-secure	-	UART1
0x4004_0400	1KB	Non-secure	-	UART2
0x4004_2000	1KB	Non-secure	-	SPI
0x4004_4000	1KB	Non-secure	-	I2C
0x4005_0000	16KB	Non-secure	-	SDIO Device
0x4006_0000	2KB	Non-secure	-	GDMA
0x4007_0000	16KB	Non-secure	-	Crypto Engine
0x4008_0000	256KB	Non-secure	-	WLAN
0x4060_0000	4KB	Non-secure	-	pSRAM Controller
0x5000_0800	2KB	Secure	-	SYS Control (SYSON)
0x5000_2000	4KB	Secure	-	HS Timer
0x5006_0000	2KB	Secure	-	GDMA
0x5007_0000	16KB	Secure	-	Crypto Engine

6.2.3. Extension Memory Space

The external flash memory address base is from 0x9800_0000 to 0x9BFF_FFFF.

Table 13. Address map of Extension Memory Hardware Table.

Name	Physical Address	Size	IP Function
Flash	0x9800_0000 0x9BFF_FFFF	64MB	External flash memory

6.3. SPI NOR Flash

Ameba ZII support NOR flash via SPI interface.

Features of SPI NOR Flash:

- SPI baud rate support 50/33/25/20MHz.
- Support eXecute In Place (XIP).
- Support a memory-mapped I/O interface for read operation
- Support 32K I/D read cache, 2-way associative
- Support decryption on the fly
- Support SPI mode (SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI)

7. Peripherals Interface

7.1. General Purpose DMA Controller

Realtek Direct Memory Access Controller (RTK-DMAC) is a DMA controller with AXI interface. Usually, CPU sends sequential read/write commands controlling data transfer. However, CPU cannot execute instructions when it is handling the transfer. To release CPU resource, DMAC can manage the data transfer completely. CPU configures DMAC registers to setup a transfer and then enable the channel to start the transfer. CPU does not have to take care of the transfer until DMAC trigger interrupts. The DMAC interrupts are generated when the transfer is done or the transfer encounters errors.

Features of GDMA:

- Advanced eXtensible Interface 4 (AXI4) master interface and Advanced Peripheral Bus 3 (APB3) slave interface.
- 32 bits data bus width
- Two channels. Each channel can configure independent source address and destination address to initiate a transfer. The channel has a proprietary FIFO to push or pop data.
- The maximum transfer length per transfer is up to 4095 data items. Each data item can be configured to 1 byte, 2 bytes or 4 bytes width.
- DMA hardware request interface
  - Handshake interface with peripherals to control data flow
- Transfer abort feature
  - The transfer can be stopped safely. DMAC reports the correct data length already received or transmitted after the termination.
- Secure mode access
  - Secure access control for master interface. Non-authorized access cannot access correct data.

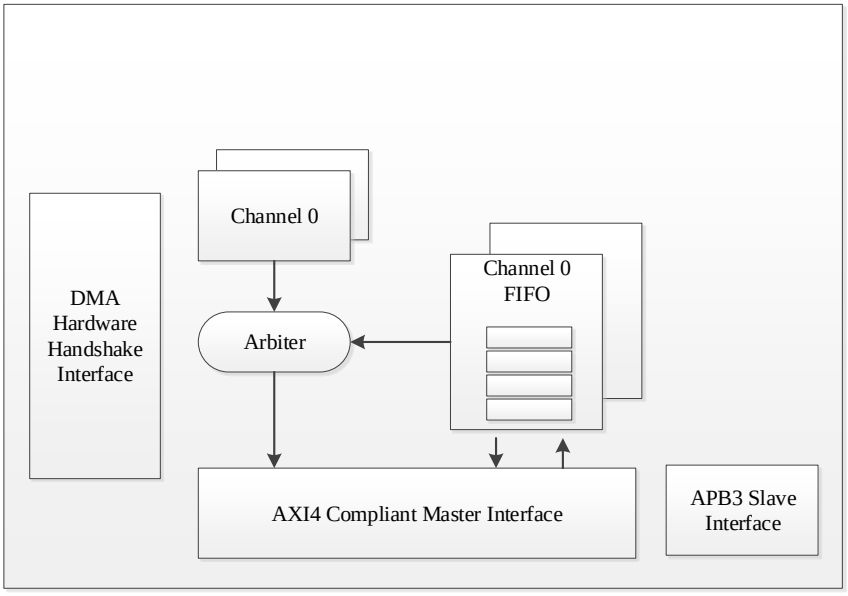


Figure 9. RTL8710C RTK-DMAC Block Diagram

7.2. General Purpose Timer (GTimer)

For various system timing or flow control usage, general purpose timer provides counter and timer mode that could be used for

any kinds of time related event generation or timing measurement.

Features of GTIMER:

- 8 Gtimers supported at HS domain and the source clock is from 40MHz.
- 1 Gtimer supported at LP domain and the source clock is from 32KHz.
- Support counter mode and timer mode.
- Each Gtimer support 4 match events.

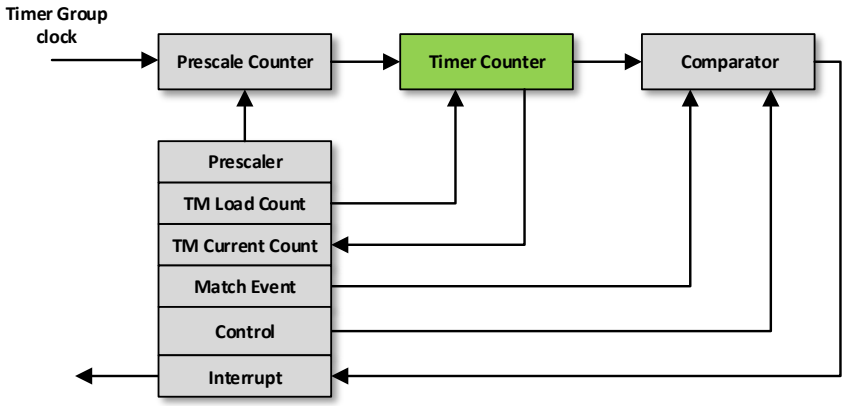


Figure 10. GTimer Functional Diagram

7.3. GPIO Functions

Each of the General Purpose Input/Output (GPIO) pins are software configurable as an output or as an input. In embedded system design, integration and control between different devices and SOC chip is a significant part when planning a new architecture system. For SOC chip, the most essential approach for interfacing external devices of SOC chip is by GPIO interface that could provide simple digital input/output IO control. A simple IO pad architecture given in below figure.

Features of GPIO:

- GPO and GPI functions.
- Support interrupt detection with configurable polarity per GPIO.
- Internal weak pull up and pull low per GPIO.
- Multiplexed with other specific digital functions.

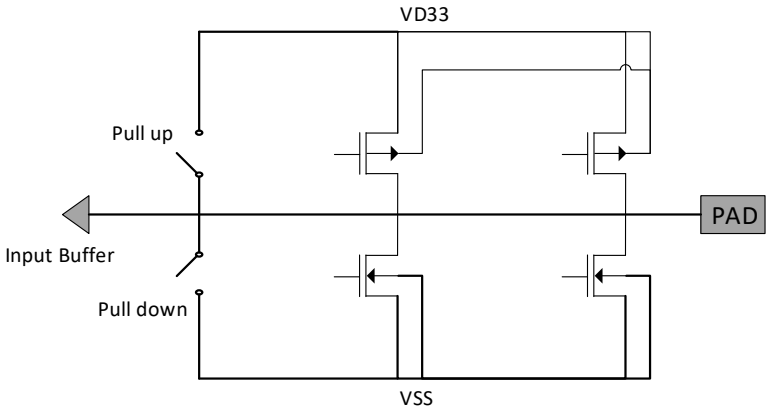


Figure 11. IO Pad Architecture

7.4. UART Interface

Nowadays UART has been a most popular serial interface for system information, debug log and device information exchange. UART supports plenty of hardware acceleration such as transmit/receive data FIFO, DMA transfer etc, which make UART easier to use.

The UART signal level is 3.3V. The host provides the power source with the targeted power level to the UART interface via the IO power.

Features of UART:

- Support 3xUART (max baud rate 4MHz and DMA mode)
- UART (RS232 Standard) Serial Data Format
- Programmable Asynchronous Clock Support
- 16 bytes Transmit Data FIFO and 32 bytes Receive Data FIFO
- Programmable Receive Data FIFO Trigger Level
- Auto Flow Control
- DMA data moving support to save CPU loading

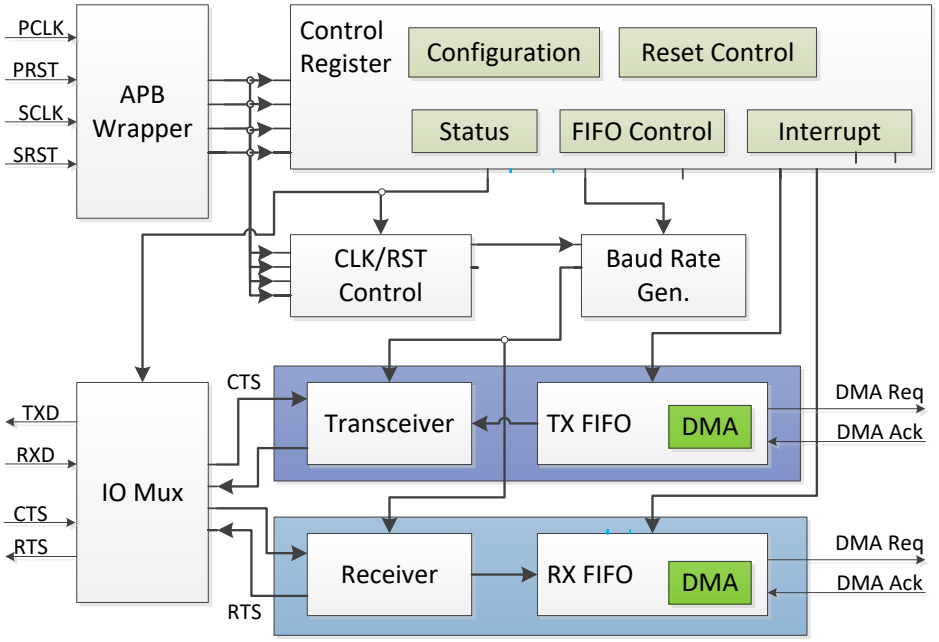


Figure 12. UART Functional Diagram

7.4.1. UART Specification

UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k bit/s. Here is a table to show a baud-rate error calculation.

Table 14. UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)	Desired Baud Rate	Actual Baud Rate	Error (%)
110	110.0533759	0.048523534	380400	380952.381	0.145210555
300	300.120048	0.040016006	460800	460732.9843	0.014543339
600	600.240096	0.040016006	500000	500000	0
1200	1200.480192	0.040016006	921600	922431.8658	0.090263219
2400	2400.960384	0.040016006	1000000	1000000	0
4800	4801.920768	0.040016006	1382400	1383647.799	0.090263219
9600	9603.841537	0.040016006	1444400	1452145.215	0.536223658
14400	14414.41441	0.1001001	1500000	1506849.315	0.456621005
19200	19230.76923	0.16025641	1843200	1856540.084	0.723745898
28800	28860.02886	0.208433542	2000000	2000000	0
38400	38461.53846	0.16025641	2100000	2105263.158	0.250626566
57600	57720.05772	0.208433542	2764800	2784810.127	0.723745898
76800	76923.07692	0.16025641	3000000	3013698.63	0.456621005
115200	115243.583	0.037832489	3250000	3283582.09	1.033295063
128000	128205.1282	0.16025641	3692300	3728813.559	0.988910959
153600	153846.1538	0.16025641	3750000	3793103.448	1.149425287
230400	231092.437	0.300536881	4000000	4000000	0

7.5. SDIO Device Mode Interface

The SDIO (Secure Digital Input Output) is an extension of the SD specification to cover I/O functions.

Features of SDIO:

- Support SDIO 2.0 High Speed mode.
- CIS can be configured with internal non-volatile memory for fast card detection.
- RTK SPI provides high efficiency SPI interface with interrupt and full duplex mode.
- Support high performance Ethernet to Wi-Fi transformation.
- Support non-flash booting in the use of Ethernet to Wi-Fi transformation card.

7.5.1. Bus Timing Specification

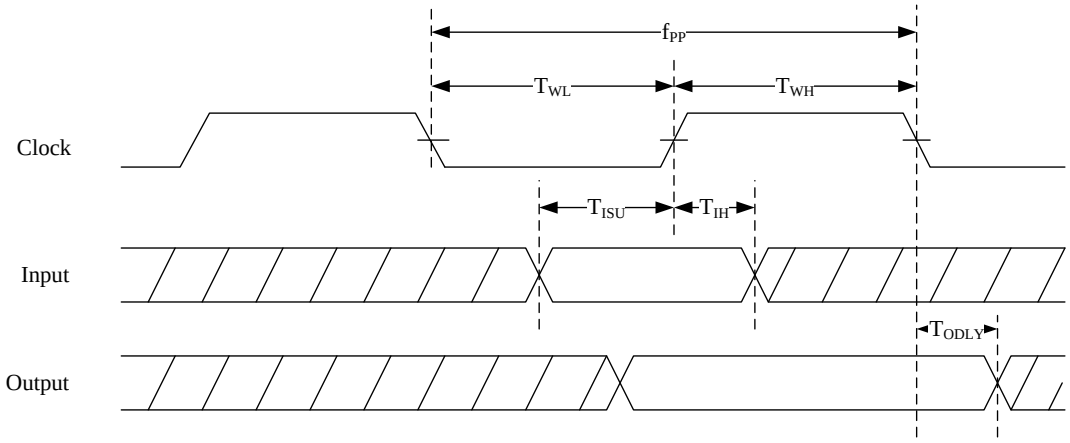


Figure 13. SDIO Interface Timing sequence.

Table 15. SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

7.6. SPI Interface

Serial Peripheral Interface (SPI) is a serial interface that enables data communication between microcontrollers and other peripherals. High throughput and the full-duplex capability with simple hardware interface makes SPI very efficient for various application. SPI is widely adopted to communicate with variety of peripherals including sensors, control devices, memory, LCD, SD card etc.

Features of SPI:

- Support 1 SPI port.
- Support Master/Slave mode.
- Multiple Serial Interface Operations support:
  - Motorola – SPI.
  - Texas Instruments – SSI.
  - National Semiconductor – Microwire.
- Support DMA to offload CPU bandwidth.
- Maximum speed support for each SPI interface:
  - Support baud rate up to 25MHz (Master mode).
  - Support baud rate up to 6.25MHz (Slave mode Rx only).
  - Support baud rate up to 5MHz (Slave mode TRx).
- Programmable clock bit-rate.
- Programmable clock polarity (SCPOL) and phase (SCPH) for SPI protocol.
- Support 8 bit and 16 bit data frame size
- Support bit swapping and byte swapping features
- The depth of transmit FIFO and receive FIFO are 1024 bit (up to 64 data frames)

7.6.1. SPI Protocol

SPI protocol mode can control by 2 parameters, SCPOL and SCPH. Both SCPOL and SCPH and configure as 0 or 1 (SCPOL = 0/1, SCPH = 0/1) and total 4 modes shown in below:

- SCPOL define inactive state of serial clock status:
  - 0: low
  - 1: High
- SCPH define serial clock toggles timning of the first data bit:
  - 0: Middle of the first data
  - 1: Start of the first data

1. SCPOL=0/SCPH=0:

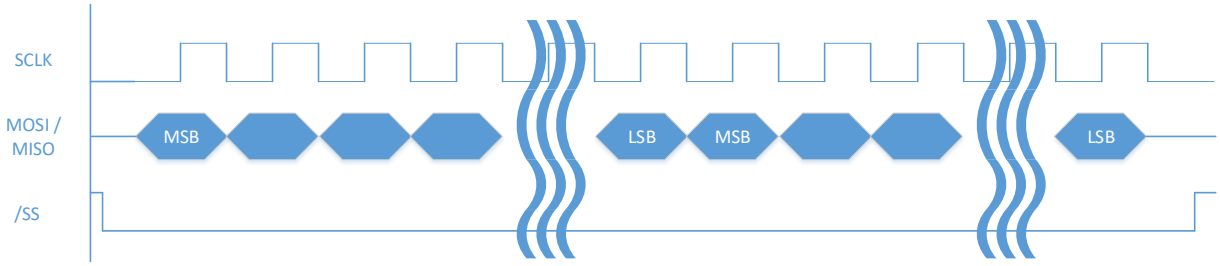


Figure 14. SPI Protocol : Mode 0 (SCPOL=0/SCPH=0)

2. **SCPOL=0/SCPH=1:**

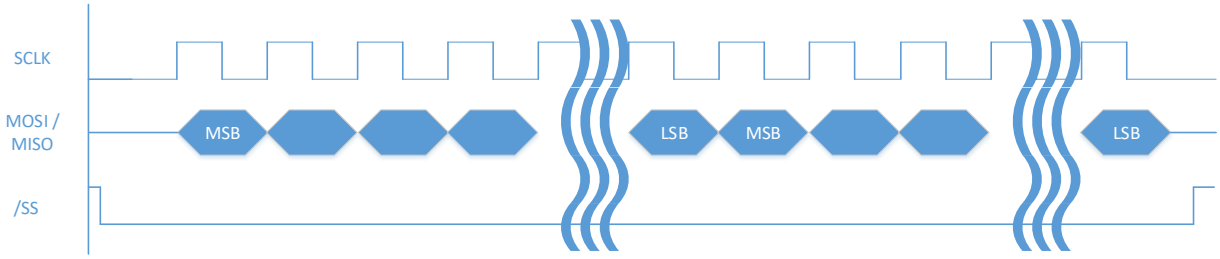


Figure 15. SPI Mode Protocol : Mode 1 (SCPOL=0/SCPH=1)

3. **SCPOL=1/SCPH=0:**

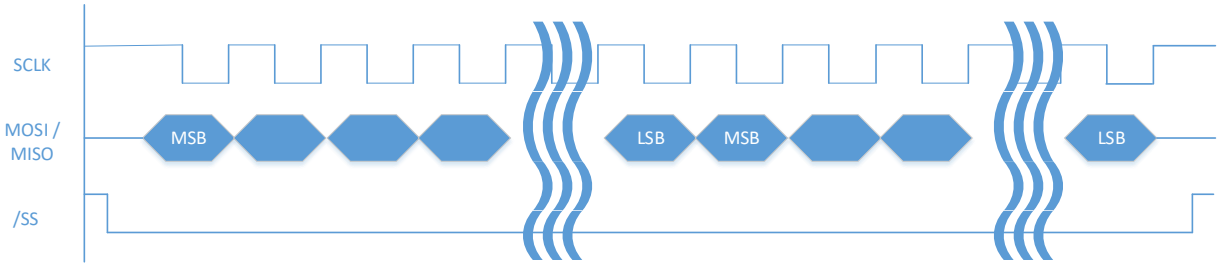


Figure 16. SPI Mode Protocol : Mode 2 (SCPOL=1/SCPH=0)

4. **SCPOL=0/SCPH=1:**

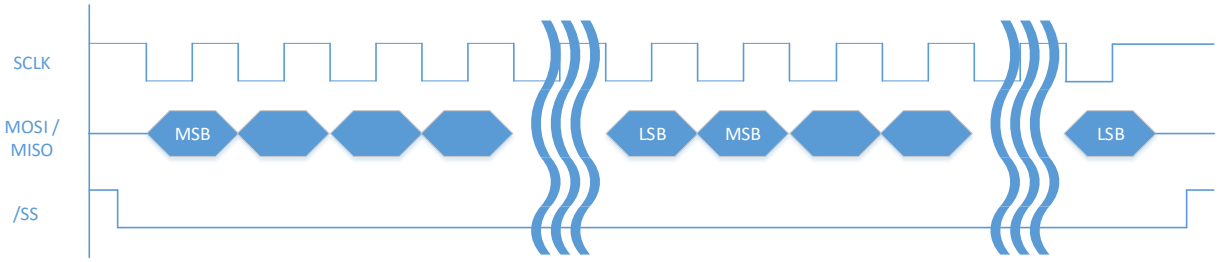


Figure 17. SPI Mode Protocol : Mode 3 (SCPOL=1/SCPH=1)

7.7. I2C Interface

For external device connection, I^2C is another popular serial interface since all I^2C device could be connected together and only two wires (data and clock pin) are required for I^2C protocol. In a pin limited system, I^2C would be ideal interface to integrate different external elements together.

Features of I^2C:

- Support maximum 1x I2C ports.
- Support 3 different speeds:
  - Standard mode (0 to 100 Kb/s).
  - Fast mode (<400 Kb/s).
  - High-speed mode (<3.4 Mb/s) (with appropriate bus loading).
- Master or slave I2C operations.
- 7-bit/10-bit addressing.
- Support Interrupt or polled mode operation.
- Support TX and RX DMA.
- Transmit and receive buffers.

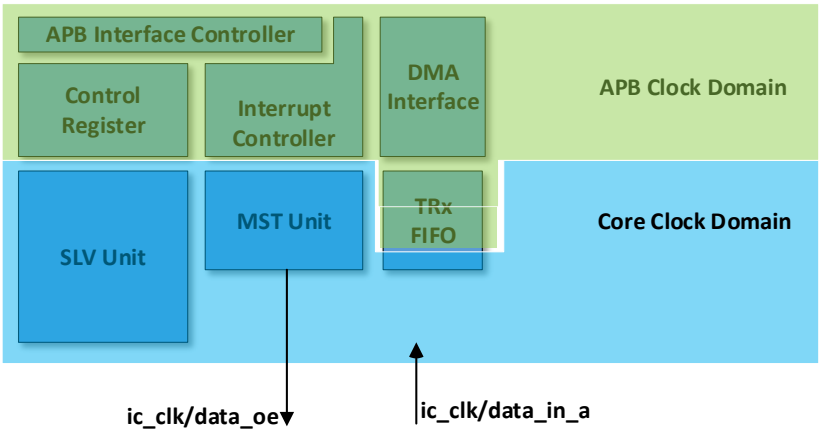


Figure 18. I2C Functional Diagram

7.8. PWM Interface

Pulse-Width Modulation (PWM) controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals are programmable. In some particular application, especially for LED and motor unit control, PWM is one of the most used interfaces. PWM interfaces could cooperate with GTimer therefore PWM could work without involving CPU.

Features of PWM:

- Support maximum 8 PWM functions.
- 0~100% duty can be configurable.
- Use selected HS Gtimer interrupt as counter source.
- Minimum resolution is 50ns.
- The period could be configured up to 8 seconds.

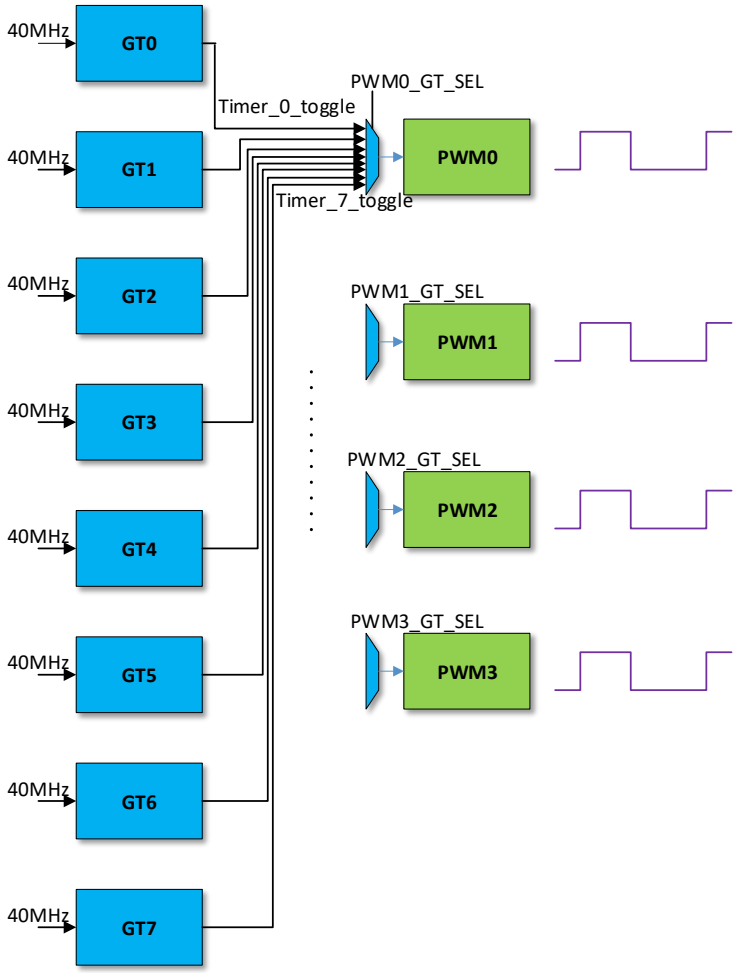


Figure 19. PWM Functional Diagram

7.9. Security Engine

In order to enhance security level in embedded system, security engine offers various authentication and encryption/decryption functions to meet different state security usage. Crypto engine provides low SW computing and high performance cryptographic operation (such as authentication, encryption and decryption).

Features of Security Engine:

5. Provide low SW computing and high performance encryption.
6. Supported authentication algorithms:
7. General cryptographic hash function
   - MD5
   - SAH1
   - SHA2-224
   - SHA2-256
   - Sequential hash
8. HMAC(Hash-based message authentication code)
   - HMAC_MD5
   - HMAC_SHA1
   - HMAC_SHA2-224
   - HMAC_SHA2-256
9. Cipher(Encryption/Decryption) algorithms
   - AES-128/192/256
     - ECB (Electronic Codebook) mode
     - CBC (Cipher Block Chaining) mode
     - CTR (Counter) mode
     - CFB (Cipher Feedback) mode
     - OFB (Output Feedback) mode
     - GCTR (Galois CTR) mode
     - GMAC (Galois MAC) mode
     - GHASH (Galois HASH) mode
     - GCM (Galois/Counter Mode) mode
10. CRC

8. RF Characteristic

Ameba ZII includes an integrated WLAN RF transceiver architecture and operating in 2.4 GHz WLAN and Bluetooth systems.

8.1. RF Block Diagram

This section describes Ameba ZII RF diagram. Ameba ZII includes a Wi-Fi/BT subsystem that integrates a Wi-Fi/BT modem which sharing front-end RF (ADC, TRSW, LPF, PA, LNA, etc.) and this chip is compliant with the IEEE 802.11b/g/n protocol.

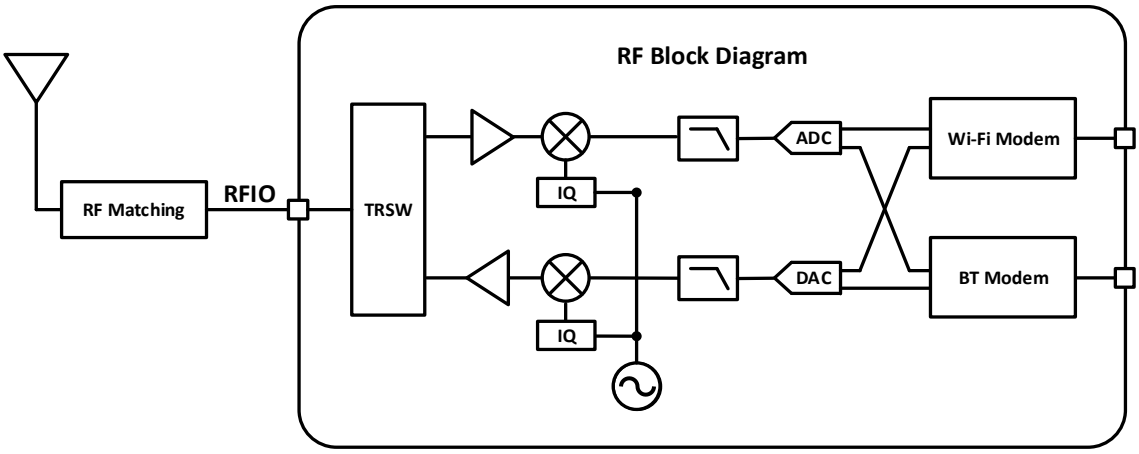


Figure 20. RF Block Diagram.

8.2. Wi-Fi Radio Characteristic

Values in below table are typical value and reference point is antenna port include front-end loss. It might slightly change depend on different RF front-end design or PCB design.

8.2.1. Wi-Fi 2.4GHz Band RF Receiver Specification

Table 16. WLAN 2.4 GHz Receiver Performance Specifications.

Parameter	Description	Minimum	Typical	Maximum	Units
Frequency Range	-	2400	-	2500	MHz
802.11b RX Sensitivity (8% PER)	1 Mbps DSSS	-	-99.0	-	dBm
	2 Mbps DSSS	-	-95.5	-	dBm
	5.5 Mbps DSSS	-	-93.5	-	dBm
	11 Mbps DSSS	-	-90.0	-	dBm
802.11g RX Sensitivity (10% PER)	6 Mbps OFDM	-	-94.0	-	dBm
	9 Mbps OFDM	-	-93.0	-	dBm
	12 Mbps OFDM	-	-91.5	-	dBm
	18 Mbps OFDM	-	-89.0	-	dBm
	24 Mbps OFDM	-	-86.0	-	dBm
	36 Mbps OFDM	-	-82.5	-	dBm
	48 Mbps OFDM	-	-78.0	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
802.11n RX Sensitivity (10% PER)	HT20 MCS0	-	-93.5	-	dBm
	HT20 MCS1	-	-91.0	-	dBm
	HT20 MCS2	-	-88.5	-	dBm
	HT20 MCS3	-	-85.5	-	dBm
	HT20 MCS4	-	-82.5	-	dBm
	HT20 MCS5	-	-77.0	-	dBm
	HT20 MCS6	-	-75.5	-	dBm
	HT20 MCS7	-	-74.0	-	dBm
Maximum Receive Level	1 Mbps DSSS	-	-	0	dBm
	6M bps OFDM	-	-	0	dBm

Note: Above Rx performance values base on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

8.2.2. Wi-Fi 2.4GHz Band RF Transmitter Specification

Table 17. WLAN 2.4 GHz Transmitter Performance Specifications.

Parameter	Description	Minimum	Typical	Maximum	Units
Frequency Range	-	2400	-	2500	MHz
TX power	1 Mbps DSSS	-	21	-	dBm
	11 Mbps DSSS	-	21	-	dBm
	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	17	-	dBm
	HT20 MCS0	-	19	-	dBm
	HT20 MCS7	-	16	-	dBm
TX EVM	1 Mbps DSSS	-	8	-	%
	11 Mbps DSSS	-	8	-	%
	6 Mbps OFDM	-	-5	-	dB
	54 Mbps OFDM	-	-25	-	dB
	HT20 MCS0	-	-5	-	dB
	HT20 MCS7	-	-28	-	dB
Carrier suppression	-	-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-	-45	dBm/MHz
	3rd Harmonic	-	-	-45	dBm/MHz

Note: Above Tx performance values base on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

Note: Target TX power is configurable based on different applications or each certification requirements. Recommend to back off 3dB for mass production pass rate and include corner case margin.

8.3. Bluetooth Radio Characteristic

Values in below table are typical value and reference point is antenna port include front-end loss. It might slightly change depend on different RF front-end design or PCB design. Both the transmitter specifications and the receiver specifications follow the Bluetooth SIG specifications.

8.3.1. BT RF Transmitter Specifications

Table 18. Bluetooth Transmitter Performance Table-BLE

Parameter	Description	Minimum	Typical	Maximum	Units
Frequency Range	-	2402	-	2480	MHz
Tx Output Power	-	2.5	4.5	6.5	dBm
Adjacent channel transmit power	F = F0 ± 1 MHz	-	-15	-	dB
	F = F0 ± 2 MHz		-53		dB
	F = F0 ± 3 MHz		-56		dB
	F = F0 ± > 3 MHz	-	-57	-	dB
Δ f1avg	-	-	246	-	kHz
Δ f2max	-	-	220	-	kHz
Δ f2avg/Δ f1avg	-	-	0.92	-	-
ICFT	-	-	-15	-	KHz
Drift rate	-	-	2	-	kHz/50μs
Initial drift rate	-	-	-2	-	kHz

Note: Above Tx performance values base on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

8.3.2. BT RF Receiver Specifications

Table 19. Bluetooth Receiver Performance Table-BLE

Parameter	Description	Minimum	Typical	Maximum	Units
Frequency Range	-	2402	-	2480	MHz
Rx Sensitivity @30.8% PER	Without spur channel	-	-100	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	8	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-4	-	dB
	F = F0 + 2 MHz	-	-40	-	dB
	F = F0 - 2 MHz	-	-25	-	dB
	F = F0 + 3 MHz	-	-45	-	dB
	F = F0 - 3 MHz	-	-20	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-30	-	-	dBm
	2000 MHz ~ 2400 MHz	-35	-	-	dBm
	2500 MHz ~ 3000 MHz	-35	-	-	dBm
	3000 MHz ~ 12.5 GHz	-30	-	-	dBm
Intermodulation	-	-30	-	-	dBm

Note: Above Rx performance values base on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

9. Electrical Characteristics

9.1. Temperature Limit Ratings

Table 20. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-20	+85	°C
Junction Temperature	0	+125	°C

9.2. Temperature Characteristics

Table 21. Thermal Properties

PCB (layer)	$T_{ambient}$(°C)	θ_{JA}(°C/W)	Ψ_{JT}(°C/W)	Ψ_{JB}(°C/W)
2	70	62.09	0.93	11.81

Note: The above values are based on the Realtek EVB.

9.3. Power Supply DC Characteristics

The power supply DC characteristic list in below table.

Table 22. Power Supply DC Characteristics.

Parameter	Symbol	Minimum	Typical	Maximum	Units
DC Supply Voltage for VDD_IN (3.3V)	VDD_IN	2.97	3.3	3.63	V
DC Supply Voltage for VDD_IN (5V)	VDD_IN	4.5	5	5.5	V
DC Supply Voltage for 3.3V Power Rail	VD33_SDIO VA33_XTAL VA33_SYN VA33_RF VA33_PA VA33_TR VD33_FLASH VD33_OUT	2.97	3.3	3.63	V
DC Supply Voltage for 1.1V Power Rail	VD11_CORE	1.09	1.146	1.20	V
DC Supply Voltage for GPIO/Embedded Flash	VD1833_LPC	2.97	3.3	3.63	V
DC Supply Voltage for Embedded PSRAM1	VD1833_LPC	1.7	1.8	1.95	V
3.3V Rating Current	IDD33*	-	-	500	mA

Note 1: Only the RTL8720CM-VA2-CG/RTL8720CM-VT2-CG have an embedded PSRAM, VD1833_LPC needed to provide 1.8V for PSRAM power supply.
Note 2: IDD33 is measured by Realtek EVB, 21dBm CCK 11M with DCDC MT3121

9.4. Digital IO Pin DC Characteristics

Table 23. Typical Digital IO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level	-	1.377	1.683	1.908	V
V_{T-}	Schmitt-trigger Low Level	-	0.729	0.957	1.116	V
I_{IL}	Input-Leakage Current	VIN=3.3V or 0	-10	±1	10	μA
	Driving for Normal Pins		4	-	16	mA
	Driving for SDIO Device Pins		4	-	16	mA
	Loading for Normal Pins			15		pF
	Loading for SDIO Device Pins			15		pF
	Pull Resistance for Normal Pins	3.3V	-	75	-	KΩ
	Pull Resistance for SDIO Device Pins	3.3V	-	50	-	KΩ

9.5. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltage are specified reference to GND unless otherwise specified.

Table 24. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
VD33_SDIO VD33_FLASH	GND-0.3	3.63	V
VD11_CORE	GND-0.3	1.20	V
VD1833_LPC	GND-0.3	1.95	V
Voltage on GPIO pins	GND-0.3	3.63	V

9.6. ESD Characteristics

Table 25. ESD Characteristics

Reliability test	Standards	Test condition	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	±2000V	Pass
Charge Device Model (CDM)	JEDEC EIA/JESD22-C101	±500V	Pass

9.7. Power State and Power Sequence

9.7.1. Power On or Resuming from Deep Sleep Sequence

The timing sequence of power on or resuming from deep sleep is given in Figure 21.

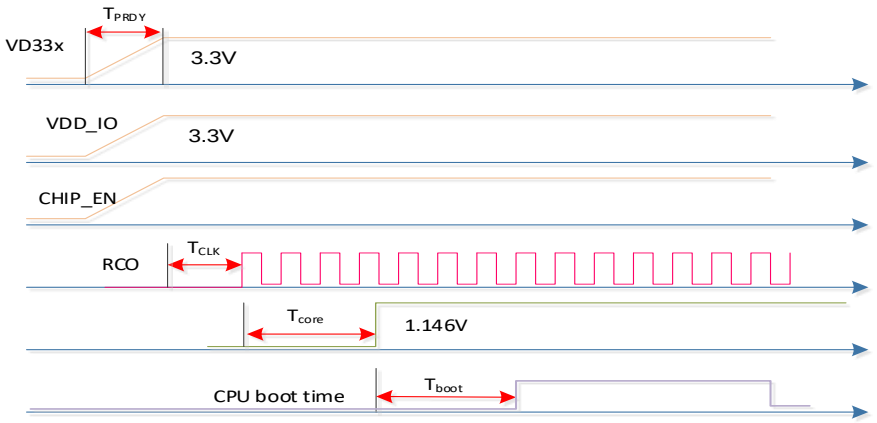


Figure 21. Power-On Sequence or Resume from Deep Sleep

Table 26. Timing spec for power on sequence

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_{PRDY}	3.3V ready time	0.6	-	5	ms
T_{CLK}	Internal ring clock stable time after 3.3V ready	1	-	-	ms
T_{core}	Core power ready time	1.5	-	-	ms

Note: Pin28 (VD1833_LPC) should be stable before the core power is ready for RTL8720CM series.

9.7.2. Resume from Standby Mode Sequence

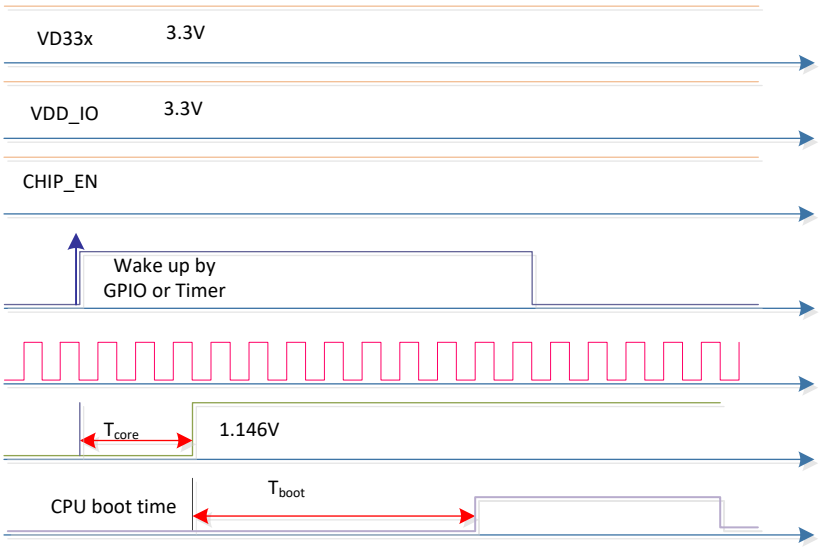


Figure 22. Timing Sequence resume from Standby

Table 27. Timing spec for resume from standby mode sequence.

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_{core}	Core power ready time	1.5	-	-	ms

Note: Pin28 (VD1833_LPC) would always be exist for RTL8720CM series.

9.7.3. Shutdown Sequence

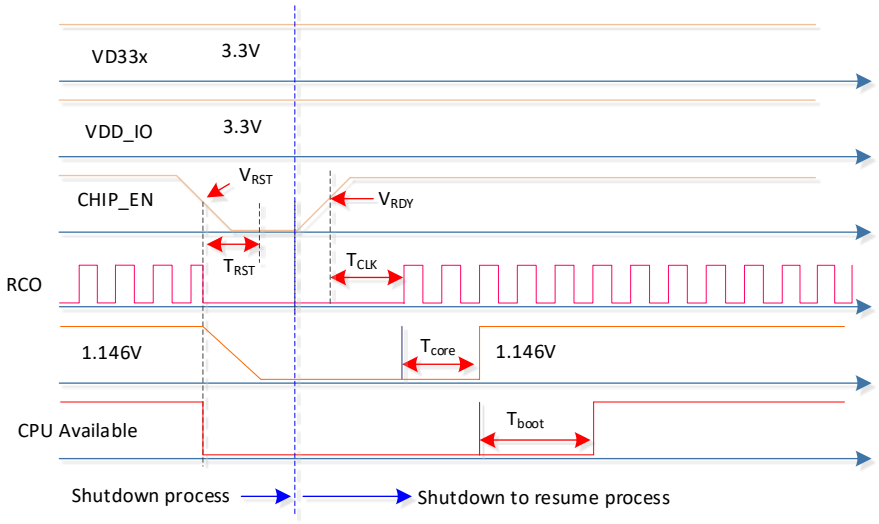


Figure 23. Timing Sequence of Shutdown

Table 28. Timing spec for shutdown sequence.

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{RST}	Shutdown occurs after CHIP_EN lower than this voltage	-	-	0.8	V
T_{RST}	The require time that CHIP_EN lower than V_{RST}	1	-	-	ms
V_{RDY}	Enable PMC after CHIP_EN higher than this voltage	2	-	-	V
T_{CLK}	Internal ring clock stable time after 3.3V ready	1	-	-	ms
T_{core}	Core power ready time	1.5	-	-	ms

Note: Pin28 (VD1833_LPC) would always be exist for RTL8720CM series.

9.7.4. BOR Sequence

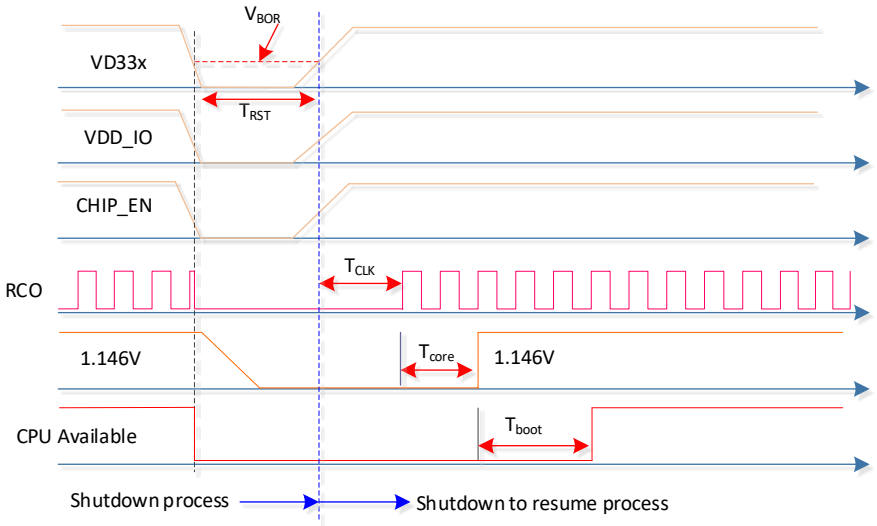


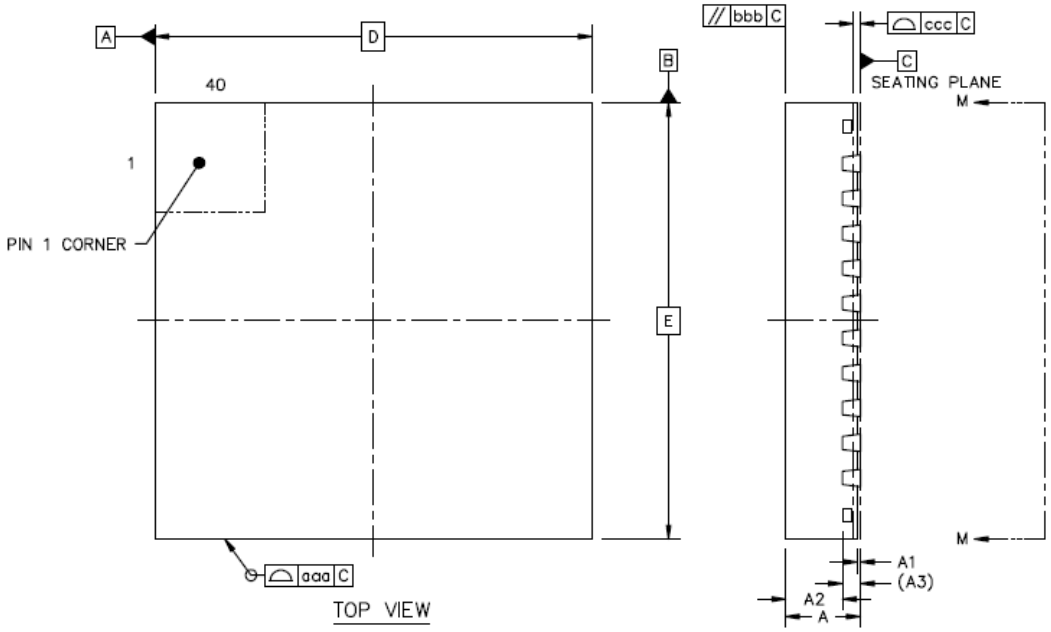
Figure 24. Timing Sequence of BOR

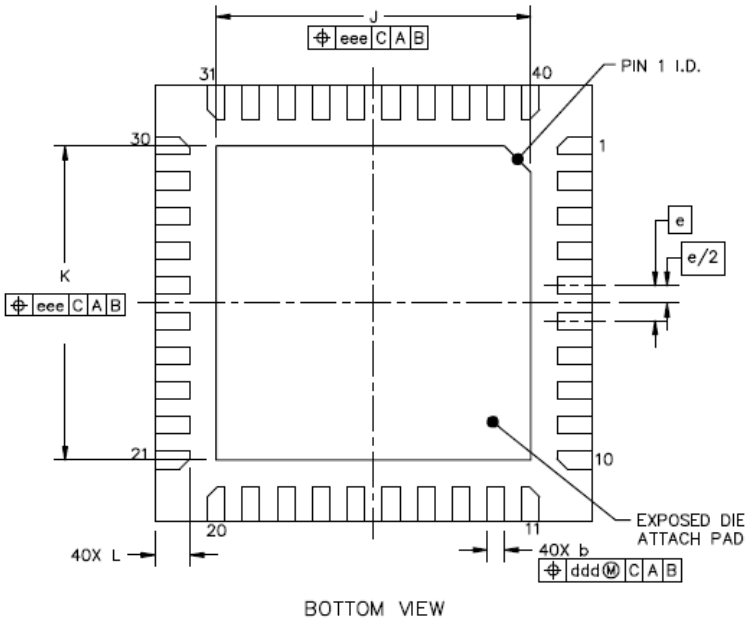
Table 299. Timing Specification for BOR Sequence

Symbol	Parameter	Min	Typ.	Max	Units
V_{BOR}	BOR occurs after 3.3V is lower than this voltage	2	2.24	2.42	V
T_{RST}	The require time that 3.3V lower than V_{BOR}	1	-	-	ms
T_{CLK}	Internal Ring Clock Stable Time after 3.3V ready	1	-	-	ms
T_{core}	Core Power Ready Time	1.5	-	-	ms

10. Mechanical Dimensions

10.1. Package Specification





10.2. Mechanical Dimensions Notes

Table 30. Table of Mechanical Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.80	0.85	0.90
A_1	0.00	0.02	0.05
A_3	0.20 REF		
b	0.15	0.20	0.25
D/E	5.00 BSC		
D2/E2	3.35	3.61	3.86
e	0.40 BSC		
L	0.30	0.40	0.50

Note：CONTROLLING DIMENSION：MILLIMETER(mm). REFERENCE DOCUMENTL：JEDEC MO-220.

11. Ordering Information

Table 31. Ordering Information

Part Number	Package
RTL8720CF-VH2-CG	QFN40, 'Green' Package. MCM 2MB Flash
RTL8720CM-VH2-CG	QFN40, 'Green' Package. MCM 4MB PSRAM

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