Realtek
AmebaZII+ Datasheet

This document provides features and information on AmebaZII+ series microcontroller.

Rev. 1.1

Sept., 2024

Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com

COPYRIGHT

DISCLAIMER

Please Read Carefully:
Realtek Semiconductor Corp., (Realtek) reserves the right to make corrections, enhancements, improvements and other changes to its products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

Reproduction of significant portions in Realtek data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Realtek is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions.

Buyers and others who are developing systems that incorporate Realtek products (collectively, "Customers") understand and agree that Customers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Customers have full and exclusive responsibility to assure the safety of Customers' applications and compliance of their applications (and of all Realtek products used in or for Customers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Customer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Customer agrees that prior to using or distributing any applications that include Realtek products, Customer will thoroughly test such applications and the functionality of such Realtek products as used in such applications.

Realtek's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation kits, (collectively, "Resources") are intended to assist designers who are developing applications that incorporate Realtek products; by downloading, accessing or using Realtek's Resources in any way, Customer (individually or, if Customer is acting on behalf of a company, Customer's company) agrees to use any particular Realtek Resources solely for this purpose and subject to the terms of this Notice.

Realtek's provision of Realtek Resources does not expand or otherwise alter Realtek's applicable published warranties or warranty disclaimers for Realtek's products, and no additional obligations or liabilities arise from Realtek providing such Realtek Resources. Realtek reserves the right to make corrections, enhancements, improvements and other changes to its Realtek Resources. Realtek has not conducted any testing other than that specifically described in the published documentation for a particular Realtek Resource.

Customer is authorized to use, copy and modify any individual Realtek Resource only in connection with the development of applications that include the Realtek product(s) identified in such Realtek Resource. No other license, express or implied, by estoppel or otherwise to any other Realtek intellectual property right, and no license to any technology or intellectual property right of Realtek or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Realtek products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of Realtek Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from Realtek under the patents or other Realtek's intellectual property.

Realtek's Resources are provided "as is" and with all faults. Realtek disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any epidemic failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights.

Realtek shall not be liable for and shall not defend or indemnify Customer against any claim, including but not limited to any infringement claim that related to or is based on any combination of products even if described in Realtek Resources or otherwise. In no event shall Realtek be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of Realtek's Resources or use thereof, and regardless of whether Realtek has been advised of the possibility of such damages. Realtek is not responsible for any failure to meet such industry standard requirements.

Where Realtek specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Customers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any Realtek products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death. Such equipment includes, without limitation, all medical devices identified by the U.S.FDA as Class III devices and equivalent classifications outside the U.S.

Customers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Customers' own risk. Customers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Customer will fully indemnify Realtek and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's

non-compliance with the terms and provisions of this Notice.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the engineer's reference and provides detailed development information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this document.

Contents

Contents **4**

Ordering Information **6**

1 Product Overview **7**

1.1 General Description 7
1.2 Features 7
1.3 Block Diagram 7
1.4 Power Architecture 8
1.4.1 Regulator Architecture 9
1.4.2 Shutdown Mode 9
1.4.3 Deep-Sleep Mode 10
1.4.4 Standby Mode 10
1.4.5 Sleep Mode 11
1.4.6 Snooze Mode 12

2 Chip Pinout Information **14**

2.1 Pin Assignments 14
2.2 Pin Definitions 14
2.2.1 Power-on Trap Pins 14
2.2.2 RF Pins 15
2.2.3 Power Pins 15
2.2.4 Clock Pins 15
2.2.5 Chip Enable Pin 15
2.2.6 Digital I/O Pins 15

3 Memory Organization **17**

3.1 Memory Architecture 17
3.1.1 Internal ROM 17
3.1.2 Internal SRAM 17
3.2 Memory Mapping 17
3.2.1 Programming Space 17
3.2.2 I/O Space 17
3.2.3 Extension Memory Space 18
3.3 SPI NOR Flash 18

4 Peripheral Interfaces **19**

4.1 General Purpose DMA Controller 19
4.1.1 Features 19
4.1.2 Block Diagram 19
4.2 General Purpose Timer (GTimer) 19
4.2.1 Features 19
4.2.2 Block Diagram 20
4.3 GPIO Functions 20
4.3.1 Features 20
4.4 UART Interface 20
4.4.1 Features 21
4.4.2 UART Specification 21
4.5 SDIO Device Mode Interface 22
4.5.1 Features 22
4.5.2 Bus Timing Specification 22
4.6 SPI Interface 23
4.6.1 Features 23
4.6.2 SPI Protocol 23
4.7 I2C Interface 24
4.7.1 Features 25
4.7.2 Block Diagram 25
4.8 PWM Interface 25

4.8.1 Features 25
4.8.2 Block Diagram 26
4.9 Security Engine 26

5 RF Characteristics 28

5.1 RF Block Diagram 28
5.2 Wi-Fi Radio Characteristics 28
5.2.1 Wi-Fi 2.4GHz Band RF Receiver Specifications 28
5.2.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications 29
5.3 Bluetooth Radio Characteristics 29
5.3.1 BT RF Transmitter Specifications 29
5.3.2 BT RF Receiver Specifications 30

6 Electrical Characteristics 31

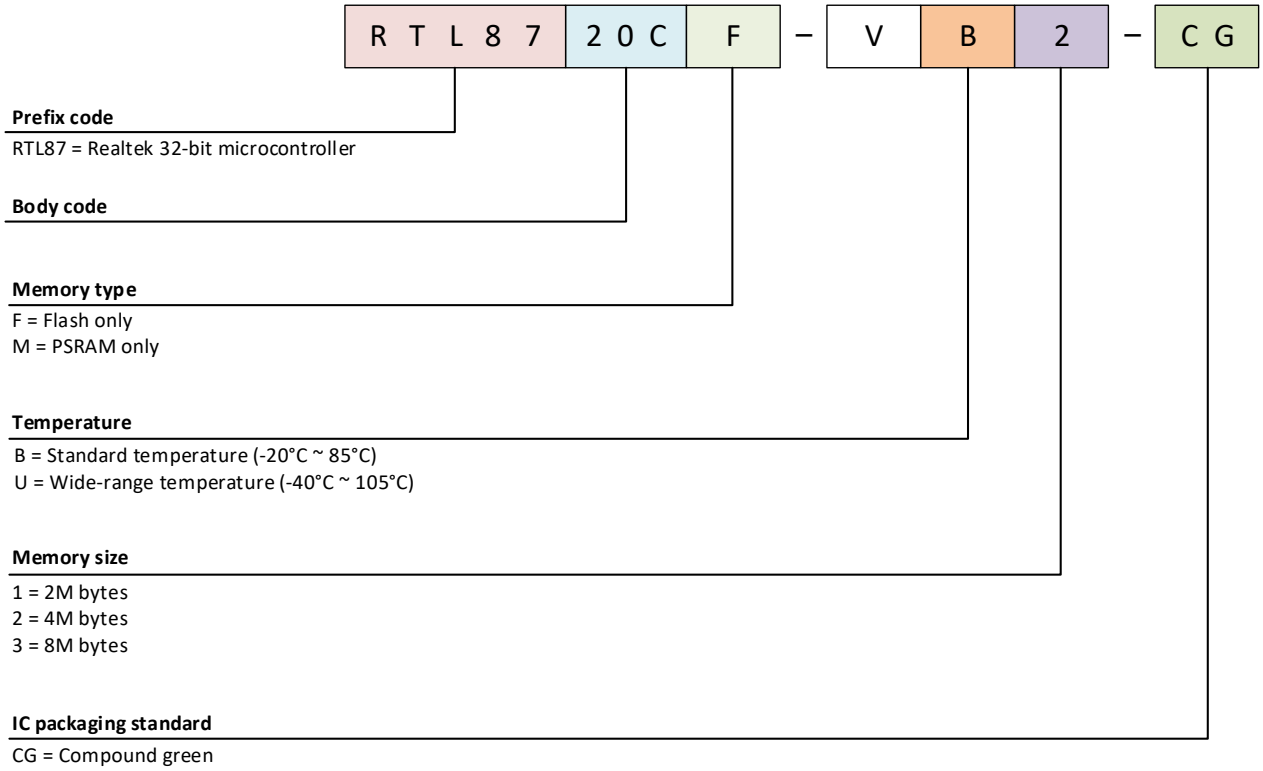
6.1 Temperature Limit Ratings 31
6.2 Power Supply DC Characteristics 31
6.3 Typical Digital I/O Pin DC Characteristics 31
6.4 ESD Characteristics 32
6.5 Power Sequence 32
6.5.1 Power-on or Resuming from Deep-Sleep Sequence 32
6.5.2 Resuming from Standby Sequence 33
6.5.3 Shutdown Sequence 33
6.5.4 Power Down Sequence 34

7 Package Information 35

7.1 Package Outline 35
7.2 Thermal Characteristics 35

Revision History 37

Ordering Information



Part number	Package	Flash	PSRAM	Operating Voltage	Status
RTL8720CF-VB1-CG	QFN40	2MB	-	3.3V or 5V	
RTL8720CF-VB2-CG	QFN40	4MB	-	3.3V or 5V	
RTL8720CF-VU2-CG	QFN40	4MB	-	3.3V or 5V	

1 Product Overview

1.1 General Description

The Realtek AmebaZII+ series is a highly integrated single chip with a low-power IEEE 802.11n Wireless LAN (WLAN) compatible network controller. It combines a Real-M300 (KM4) CPU that is based on ARMv8-M architecture, and integrates a WLAN MAC, a 1T1R capable WLAN baseband, an RF circuit, and Bluetooth Low Energy (BLE) in a single chip. It also provides configurable GPIOs that can be configured as digital peripherals for various applications and control usage.

The AmebaZII+ series integrates internal memory for full Wi-Fi protocol functions. The embedded memory configuration also enables simple application development.

1.2 Features

Item	Feature
MCU	● Real-M300 (KM4) clock frequency up to 100MHz ● Cache 32KB/D-Cache 16KB ● Supports DMA ● eXecute In Place (XIP) on Flash
Internal Memory	● Supports 384KB ROM ● Supports 384KB RAM ● Supports external flash interface ● Supports MCM embedded Flash
Secure	● Supports secure boot ● Crypto engine: MD5, SHA-1, SHA2-224, SHA2-256, HMAC, AES
Wi-Fi	● 802.11 b/g/n compatible 1x1, 2.4GHz ● 802.11e QoS Enhancement (WMM) ● Wi-Fi WEP, WPA, WPA2, WPA3, WPS. Open, shared key, and pair-wise key authentication services ● Supports low power Tx/Rx for short-range application ● Supports antenna diversity ● Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU) ● Low latency immediate High-Throughput Block Acknowledgement (HT-BA) ● Long NAV for media reservation with CF-End for NAV release ● Integrated balun, PA/LNA
Bluetooth Low Energy (BLE)	● BLE 4.2 ● Supports LE secure connections ● Supports LE scatternet ● Supports 1 Master/1 Slave
Peripheral Interfaces	● 3 x UART interface, baud rate up to 4MHz and all of them can be configured as LOGUART ● 1 x I2C, max. clock 400Kbps ● 1 x SDIO 2.0 Device, up to 50MHz ● 1 x SPI, Master clock up to 25Mbps/Slave clock up to 5Mbps ● 8 x PWM with configurable duration and duty cycle from 0 ~ 100% ● 16 x programmable GPIOs ● 1 GDMA with 2 channels
Clock Source	40MHz crystal oscillator
Package Type	QFN40, 5mm x 5mm x 0.85mm

1.3 Block Diagram

The AmebaZII+ diagram provides a general application scenario. External devices can be connected with various peripheral interfaces. The PMU and related blocks for low power application are also shown in Figure 1-1.

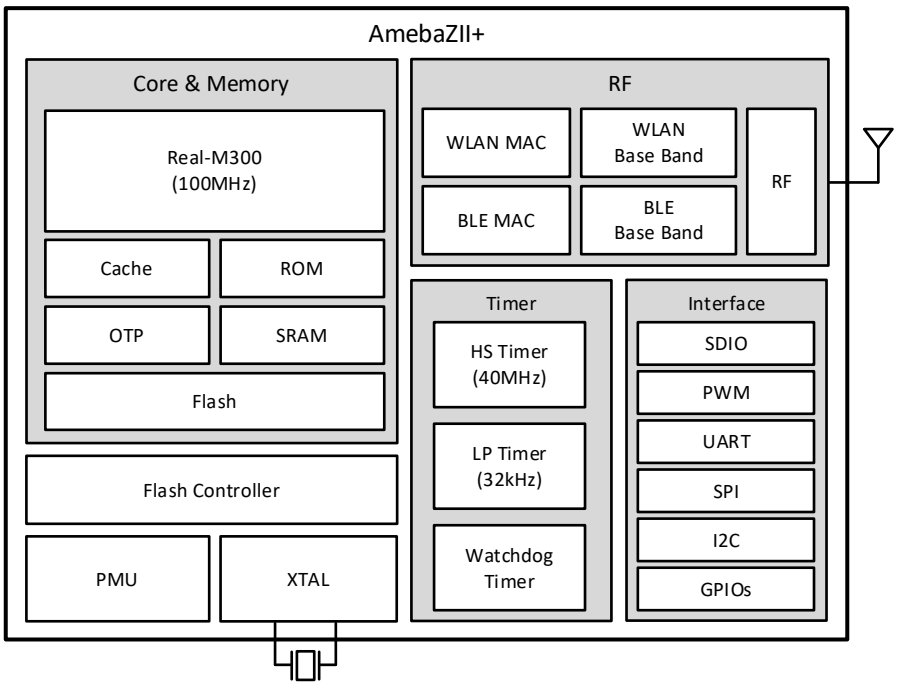


Figure 1-1 Block diagram

1.4 Power Architecture

Figure 1-2 illustrates the Power Management Control Unit (PMU) architecture of AmebaZII+. The PMU provides the following functions:

- SWR 1.1V output from 3.3V (optional for LDO mode)
- LDO 3.3V output from 5V
- LDO 2.5V output for writing E-fuse from 3.3V
- Wakeup system detector to resume from low power state

1.4.1 Regulator Architecture

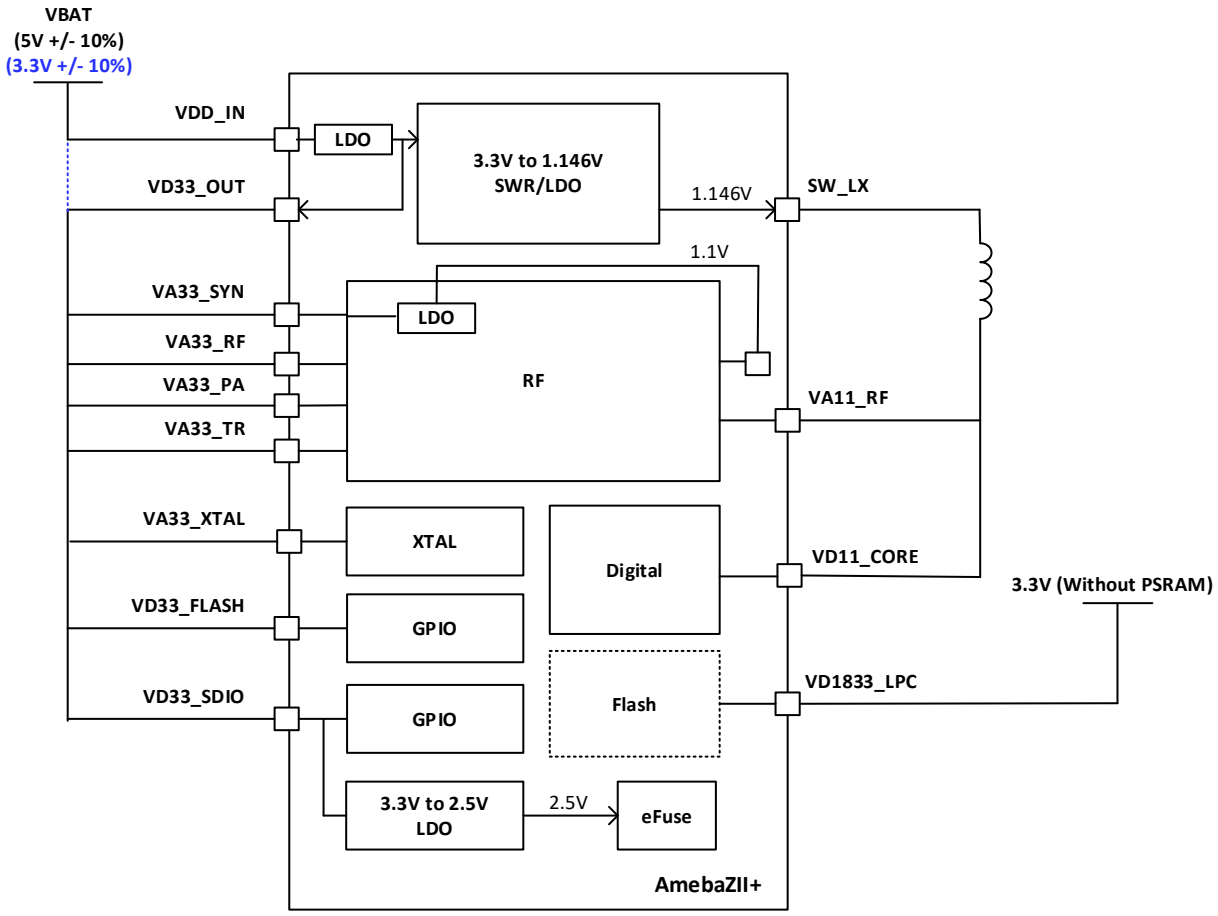


Figure 1-2 Regulator architecture

1.4.2 Shutdown Mode

CHIP_EN de-asserts to shut down the whole chip, without external power cut components required. CHIP_EN pulled high triggers the system into active mode.

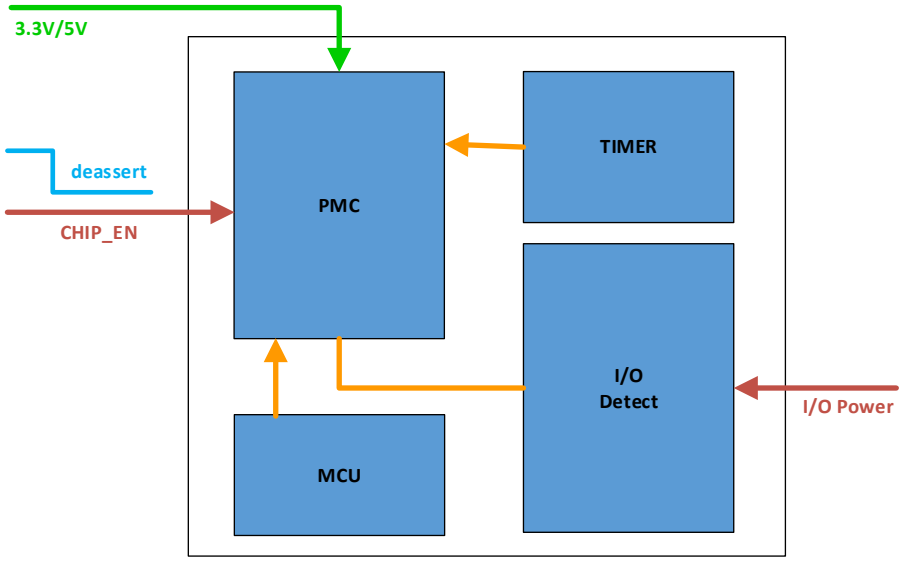


Figure 1-3 Power diagram of shutdown mode

1.4.3 Deep-Sleep Mode

CHIP_EN remains high. Users can invoke the deep-sleep API to enter deep-sleep mode. Specified interrupts can wake up the system.

The wake flow is:
(1) Wake up ISR is high
(2) PMC
(3) Enable CPU
(4) Reboot flow

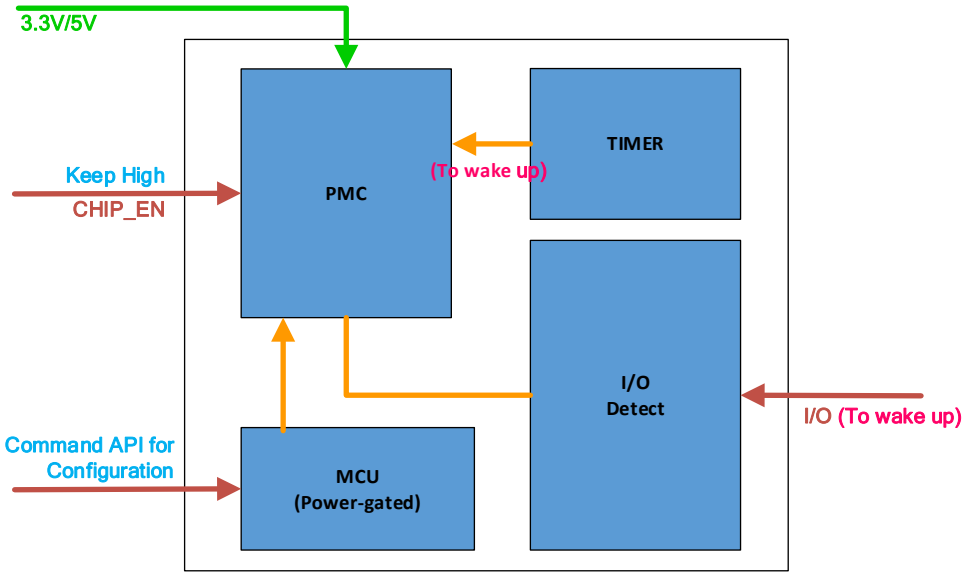


Figure 1-4 Power diagram of deep-sleep mode

Table 1-1 Wakeup source of deep-sleep mode

Wakeup source	Description
Low Precision Timer	-
Wake pins	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depending on package), GPIOA_8 (depending on package), GPIOA_9 (depending on package), GPIOA_10 (depending on package), GPIOA_11 (depending on package), GPIOA_12 (depending on package), GPIOA_13, GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18, GPIOA_19, GPIOA_20, GPIOA_23

1.4.4 Standby Mode

CHIP_EN remains high. Users can invoke the standby API to enter standby mode. Specified interrupts can wake up the system.

The wake flow is:
(1) Wake up ISR is high
(2) PMC
(3) Enable CPU
(4) Fast reboot flow

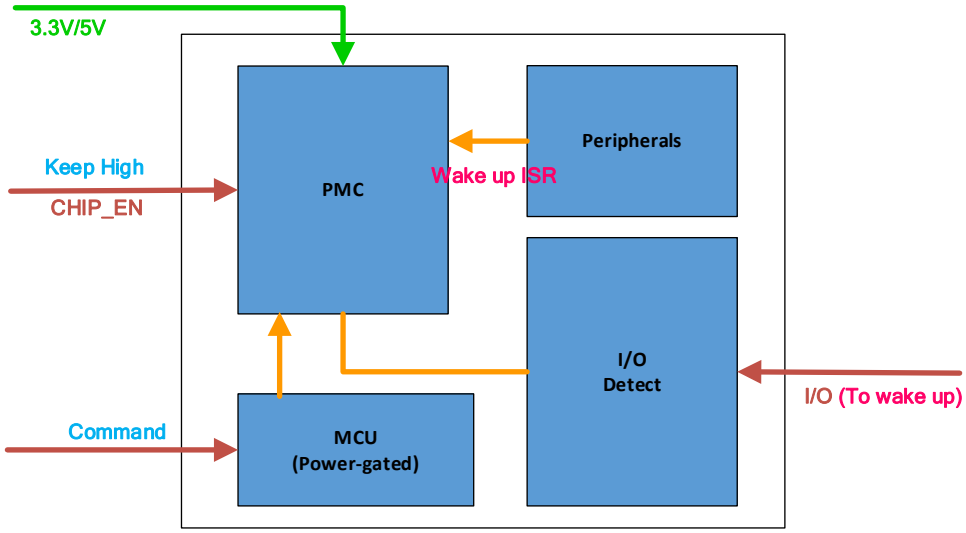


Figure 1-5 Power diagram of standby mode

Table 1-2 Wakeup source of standby mode

Wakeup source	Description
Low Precision Timer	-
Wake pins	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depending on package), GPIOA_8 (depending on package), GPIOA_9 (depending on package), GPIOA_10 (depending on package), GPIOA_11 (depending on package), GPIOA_12 (depending on package), GPIOA_13, GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18, GPIOA_19, GPIOA_20, GPIOA_23
UART0	-
WLAN	-
PWM	-
HS Timer	-

1.4.5 Sleep Mode

CHIP_EN remains high. Users can invoke sleep API to enter sleep mode. Specified interrupts can wake up the system.

The wake flow is:
(1) Wake up ISR is high
(2) PMC
(3) Enable CPU
(4) Execution of instructions continues

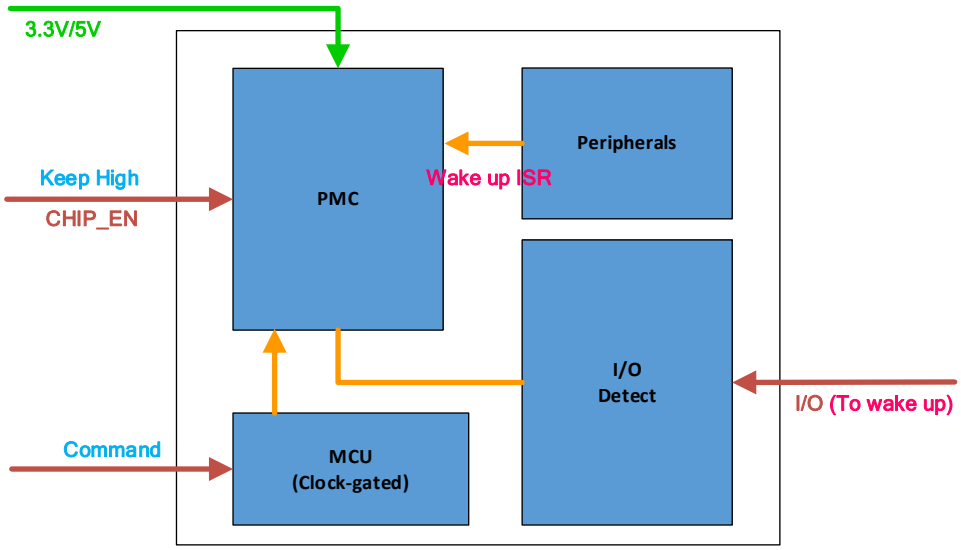


Figure 1-6 Power diagram of sleep mode

Table 1-3 Wakeup source of sleep mode

Wakeup source	Description
Low Precision Timer	-
Wake pins	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depending on package), GPIOA_8 (depending on package), GPIOA_9 (depending on package), GPIOA_10 (depending on package), GPIOA_11 (depending on package), GPIOA_12 (depending on package), GPIOA_13, GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18, GPIOA_19, GPIOA_20, GPIOA_23
UART0	-
WLAN	-
PWM	-
HS Timer	-
SDIO Device	-

1.4.6 Snooze Mode

CHIP_EN remains high. Specified interrupts can wake up the system.

The wake flow is:
(1) WLAN power on request
(2) Receive particular beacon
(3) Wake up ISR is high
(4) PMC
(5) Enable CPU
(6) Execution of instructions continues or fast reboot occurs

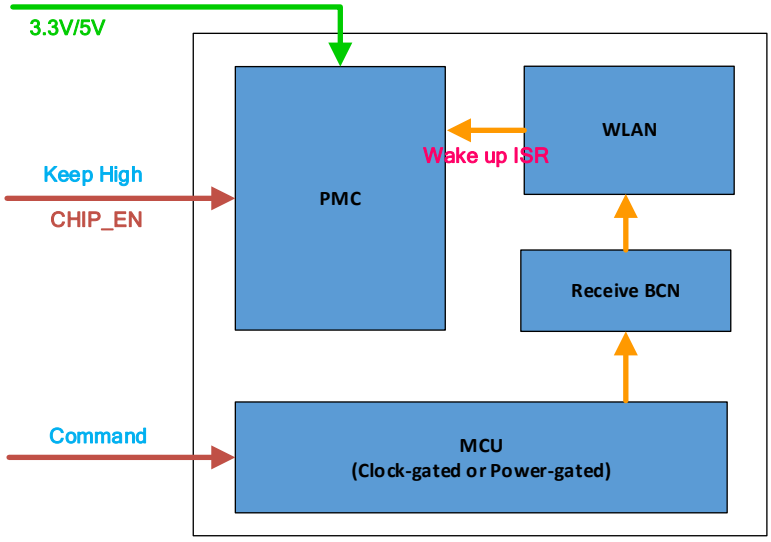


Figure 1-7 Power diagram of snooze mode

2 Chip Pinout Information

2.1 Pin Assignments

The RTL8720CF series is a 40-pin, 5mm x 5mm quad flat no-leads package with 0.4mm pitch.

Green package is indicated by the letter 'G' in Figure 2-1.

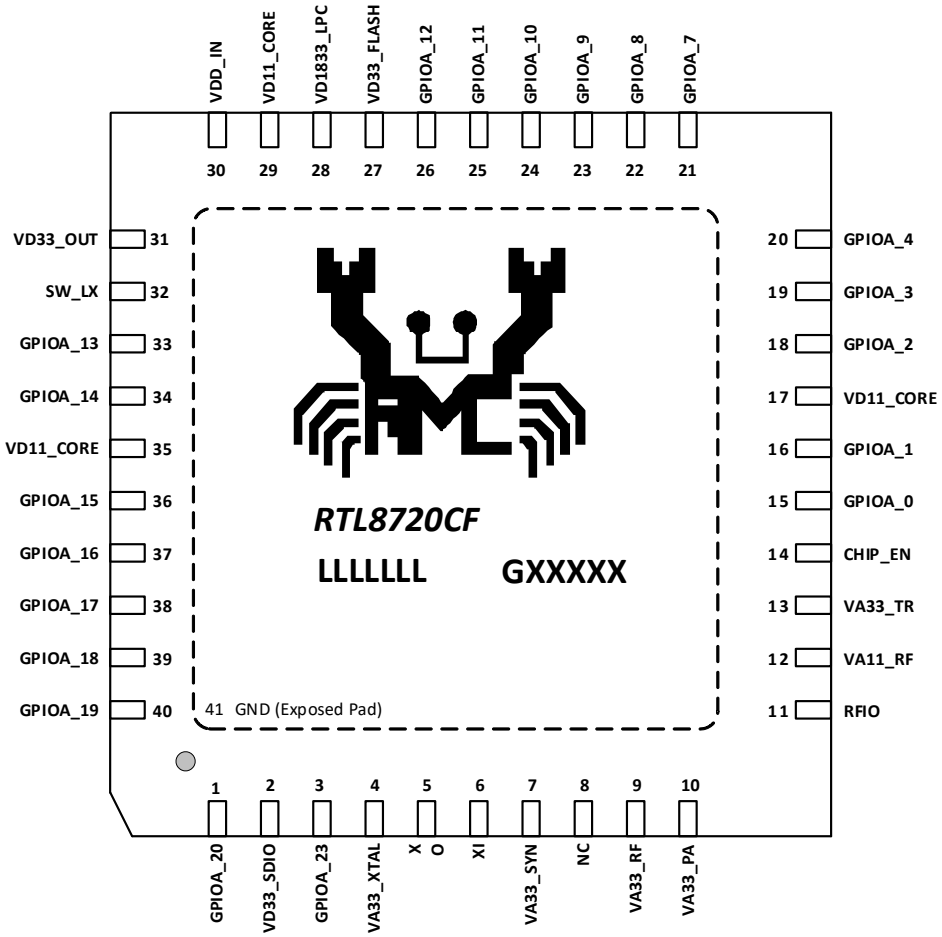


Figure 2-1 RTL8720CF series pinout

2.2 Pin Definitions

The abbreviations of pin types are listed below:

- I/O: Input/output pin
- I: Input only pin
- O: Output only pin
- PI: Power input pin
- PO: Power output pin
- RST: Reset pin

2.2.1 Power-on Trap Pins

Symbol	Type	Pin number	Description
GPIOA_0 (TEST_MODE_SEL)	I	15	1: Enter into test/debug mode 0: Normal operation mode

			(GPIOA_0, GPIOA_13) = (1, 1): Enter into download image mode
GPIOA_1 (Autoload_Fail)	I	16	1: eFuse settings are not loaded 0: eFuse settings are loaded
GPIOA_23 (SPS_LDO_SEL)	I	3	1: LDO 0: SWR

2.2.2 RF Pins

Symbol	Type	Pin number	Description
RF_IO	I/O	11	WLAN RF signal

2.2.3 Power Pins

Symbol	Type	Pin number	Description
VD33_SDIO	PI	2	3.3V power for SDIO.
VA33_XTAL	PI	4	3.3V power for XTAL.
VA33_SYN	PI	7	3.3V power for Synthesizer.
VA33_RF	PI	9	3.3V power for RF.
VA33_PA	PI	10	3.3V power for RF PA.
VA11_RF	PI	12	1.15V power for RF.
VA33_TR	PI	13	3.3V power for RF.
VD11_CORE	PI	17	1.15V power for digital core.
VD33_FLASH	PI	27	3.3V power for IO.
VD1833_LPC	PI	28	3.3V power for embedded MCM Flash.
VD11_CORE	PI	29	1.15V power for digital core.
VDD_IN	PI	30	5V/3.3V power input.
VD33_OUT	PO PI	31	● 3.3V output from LDO (when PIN30 VDD_IN is 5V input). ● 3.3V power (when PIN30 VDD_IN is 3.3V input).
SW_LX	PO	32	1.15V output power from SWR/LDO.
VD11_CORE	PI	35	1.15V power for digital core.

2.2.4 Clock Pins

Symbol	Type	Pin number	Description
XI	I	6	Input of 40MHz Crystal Clock Reference.
XO	O	5	Output of 40MHz Crystal Clock Reference.

2.2.5 Chip Enable Pin

Symbol	Type	Pin number	Description
CHIP_EN	I	14	1: Enable chip 0: Shutdown chip

2.2.6 Digital I/O Pins

The AmebaZII+ supports a maximum of 20 GPIO pins and all of them are configurable. Refer to the following table for detailed information and pinmux rules.

Symbol	Type	Pin number	Description
GPIOA_20	I/O	1	GPIO pins
GPIOA_23	I/O	3	
GPIOA_0	I/O	15	
GPIOA_1	I/O	16	
GPIOA_2	I/O	18	
GPIOA_3	I/O	19	

GPIOA_4	I/O	20	
GPIOA_7	I/O	21	
GPIOA_8	I/O	22	
GPIOA_9	I/O	23	
GPIOA_10	I/O	24	
GPIOA_11	I/O	25	
GPIOA_12	I/O	26	
GPIOA_13	I/O	33	
GPIOA_14	I/O	34	
GPIOA_15	I/O	36	
GPIOA_16	I/O	37	
GPIOA_17	I/O	38	
GPIOA_18	I/O	39	
GPIOA_19	I/O	40	

NOTE

Default states of all pins are High-impedance; unused pins should be kept floating.

The functions of each GPIO pin are listed in Table 2-1.

Table 2-1 GPIO pin function

Pin Name	Flash/SDIO	JTAG	UART	SPI/WL_LED	I2C	PWM
GPIOA_0	-	JTAG_CLK	UART1_IN	-	-	PWM[0]
GPIOA_1	-	JTAG_TMS	UART1_OUT	BT_LED	-	PWM[1]
GPIOA_2	-	JTAG_TDO	UART1_IN	SPI_CSn	I2C_SCL	PWM[2]
GPIOA_3	-	JTAG_TDI	UART1_OUT	SPI_SCL	I2C_SDA	PWM[3]
GPIOA_4	-	JTAG_TRST	UART1_CTS	SPI_MOSI	-	PWM[4]
GPIOA_7	SPI_M_CS	-	-	SPI_CSn	-	-
GPIOA_8	SPI_M_CLK	-	-	SPI_SCL	-	-
GPIOA_9	SPI_M_DATA[2]	-	UART0_RTS	SPI_MOSI	-	-
GPIOA_10	SPI_M_DATA[1]	-	UART0_CTS	SPI_MISO	-	-
GPIOA_11	SPI_M_DATA[0]	-	UART0_OUT	-	I2C_SCL	PWM[0]
GPIOA_12	SPI_M_DATA[3]	-	UART0_IN	-	I2C_SDA	PWM[1]
GPIOA_13	-	-	UART0_IN	-	-	PWM[7]
GPIOA_14	SDIO_INT	-	UART0_OUT	-	-	PWM[2]
GPIOA_15	SD_D[2]	-	UART2_IN	SPI_CSn	I2C_SCL	PWM[3]
GPIOA_16	SD_D[3]	-	UART2_OUT	SPI_SCL	I2C_SDA	PWM[4]
GPIOA_17	SD_CMD	-	-	-	-	PWM[5]
GPIOA_18	SD_CLK	-	-	-	-	PWM[6]
GPIOA_19	SD_D[0]	-	UART2_CTS	SPI_MOSI	I2C_SCL	PWM[7]
GPIOA_20	SD_D[1]	-	UART2_RTS	SPI_MISO	I2C_SDA	PWM[0]
GPIOA_23	-	-	-	LED_0	-	PWM[7]

NOTE

GPIOA_13/GPIOA_14 can operate at 3.3V or 5V in case selected as UART function when VDD_IN is 5V input; other UART pins operate at 3.3V only.

3 Memory Organization

3.1 Memory Architecture

The AmebaZII+ integrates ROM, internal SRAM, and extended NOR Flash to provide applications with a variety of memory requirements.

3.1.1 Internal ROM

The internal integration of 384KB ROM provides high access speed and low memory leak. The ROM memory clock speed is up to 100MHz.

The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Peripheral Drivers & API
- Non-flash booting functions and drivers
- Security function libs

3.1.2 Internal SRAM

The maximum internal integration of 384KB SRAM provides instruction, data, and buffer usage. The maximum clock speed is up to 100MHz.

3.2 Memory Mapping

The memory map includes all available memory and register offsets in AmebaZII+.

3.2.1 Programming Space

The programming space designed for software instruction storage is listed below.

Start address	Size	Secure	Cache support?	IP function
0x0000_0000	384KB	Configurable	-	ITCM ROM
0x1000_0000	384KB	Configurable	-	TCM SRAM
0x2000_0000	32KB	Non-Secure	Y	Additional SRAM for BT

3.2.2 I/O Space

The address map of each peripheral hardware is listed below.

Start address	Size	Secure	Cache support?	IP function
0x2000_0000	32KB	Non-secure	Y	Additional SRAM for BT
0x4000_0000	2KB	Non-secure	-	SYS Control (SYSON)
0x4000_1000	2KB	Non-secure	-	GPIO
0x4000_1C00	1KB	Non-secure	-	PWM
0x4000_2000	4KB	Non-secure	-	HS Timer
0x4000_3000	1KB	Non-secure	-	UART0
0x4000_3800	2KB	Non-secure	-	LP Timer
0x4002_0000	4KB	Non-secure	-	SPI Flash Controller
0x4004_0000	1KB	Non-secure	-	UART1
0x4004_0400	1KB	Non-secure	-	UART2
0x4004_2000	1KB	Non-secure	-	SPI
0x4004_4000	1KB	Non-secure	-	I2C
0x4005_0000	16KB	Non-secure	-	SDIO Device
0x4006_0000	2KB	Non-secure	-	GDMA
0x4007_0000	16KB	Non-secure	-	Crypto Engine
0x4008_0000	256KB	Non-secure	-	WLAN

0x4060_0000	4KB	Non-secure	-	PSRAM Controller
0x5000_0800	2KB	Secure	-	SYS Control (SYSON)
0x5000_2000	4KB	Secure	-	HS Timer
0x5006_0000	2KB	Secure	-	GDMA
0x5007_0000	16KB	Secure	-	Crypto Engine

3.2.3 Extension Memory Space

The external Flash memory address base is from 0x9800_0000 to 0x9BFF_FFFF. The address map of extension memory hardware is listed below.

Name	Physical address	Size	IP function
Flash	0x9800_0000 0x9BFF_FFFF	64MB	External Flash memory

3.3 SPI NOR Flash

The AmebaZII+ supports NOR Flash via SPI interface.

SPI NOR Flash Features:

- SPI baud rate supports 50/33/25/20MHz
- Supports eXecute In Place (XIP)
- Supports memory-mapped I/O interface for read operation
- Supports 32K/16K I/D read cache, 4-way associative
- Supports decryption on the fly
- Supports SPI mode (SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI)
- Supported flash size: Up to 64MB

4 Peripheral Interfaces

4.1 General Purpose DMA Controller

The Realtek Direct Memory Access Controller (DMAC) is a DMA controller with AXI interface. Usually, the CPU sends sequential read/write commands controlling data transfer. However, the CPU cannot execute instructions when it is handling the transfer. To release CPU resources, the DMAC can manage the data transfer completely. The CPU configures DMAC registers to setup a transfer and then enables the channel to start the transfer. The CPU does not have to handle the transfer until there is a DMAC trigger interrupt. The DMAC interrupt is generated when the transfer is done, or the transfer encounters errors.

4.1.1 Features

- Advanced eXtensible Interface 4 (AXI4) master interface and Advanced Peripheral Bus 3 (APB3) slave interface
- 32 bits data bus width
- Two channels. Each channel can be configured with an independent source address and destination address to initiate a transfer. The channel has a proprietary FIFO to push or pop data
- The maximum transfer length per transfer is up to 4095 data items. Each data item can be configured to 1 byte, 2 bytes, or 4 bytes width
- DMA hardware request interface
  - Handshake interface with peripherals to control data flow
- Transfer abort feature
  - The transfer can be stopped safely. The DMAC reports the correct data length already received or transmitted after the termination
- Secure mode access
  - Secure access control for master interface. Non-authorized access cannot access data

4.1.2 Block Diagram

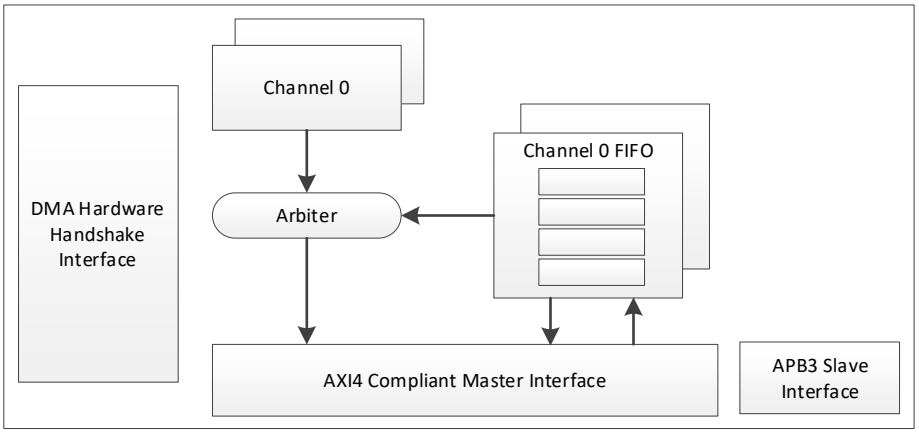


Figure 4-1 Block diagram of DMAC

4.2 General Purpose Timer (GTimer)

For various system timing or flow control usage, the general purpose timer provides a counter and timer mode that can be used for any type of time related event generation or timing measurement.

4.2.1 Features

- 8 GTimers supported at HS domain; the source clock is from 40MHz
- 1 GTimer supported at LP domain; the source clock is from 32kHz
- Supports counter mode and timer mode
- Each GTimer supports 4 match events

4.2.2 Block Diagram

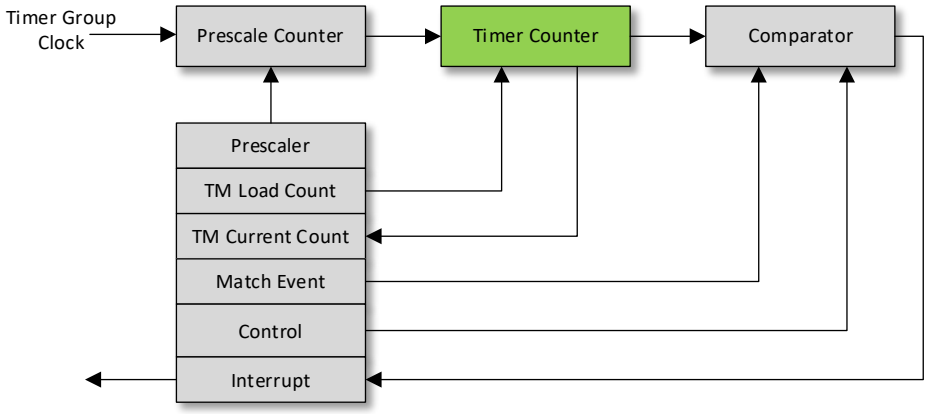


Figure 4-2 Functional diagram of GTimer

4.3 GPIO Functions

Each of the General Purpose Input/Output (GPIO) pins are software configurable as an output or as an input. In embedded system design, integration and control between different devices and the SoC are significant when planning a new architecture system. For the SoC, the most essential approach for interfacing external devices of the SOC is via the GPIO interfaces. This can provide simple digital input/output IO control. A simple IO pad architecture is shown in Figure 4-3.

4.3.1 Features

- GPO and GPI functions
- Supports interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

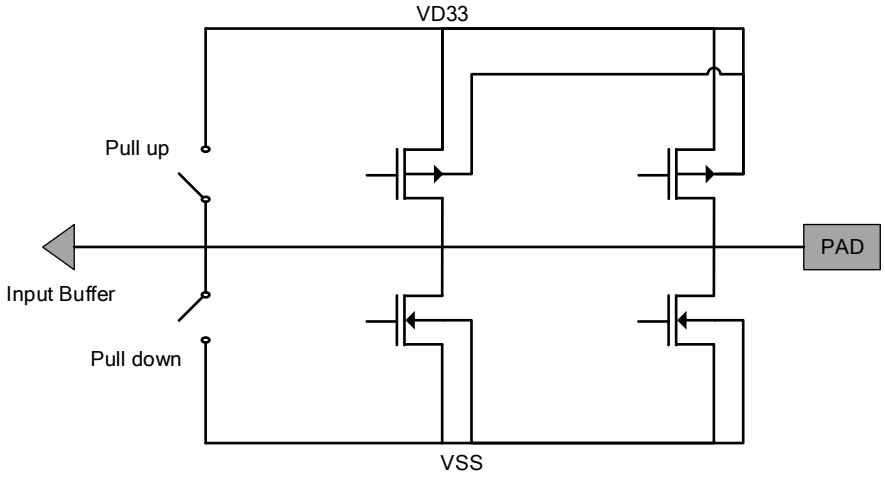


Figure 4-3 I/O pad architecture

4.4 UART Interface

UART is a popular serial interface for system information, debug logs and device information exchange. UART supports hardware acceleration such as transmit/receive data FIFO, DMA transfer etc., which makes UART easier to use.

The UART signal level is 3.3V or 5V. The host provides the power source with the targeted power level to the UART interface via the I/O power.

4.4.1 Features

- Supports 3 x UART (max. baud rate 4MHz and DMA mode)
- UART (RS232 Standard) Serial Data Format
- Programmable Asynchronous Clock Support
- 16 bytes Transmit Data FIFO and 32 bytes Receive Data FIFO
- Programmable Receive Data FIFO Trigger Level
- Auto Flow Control
- DMA data moving support to reduce CPU loading

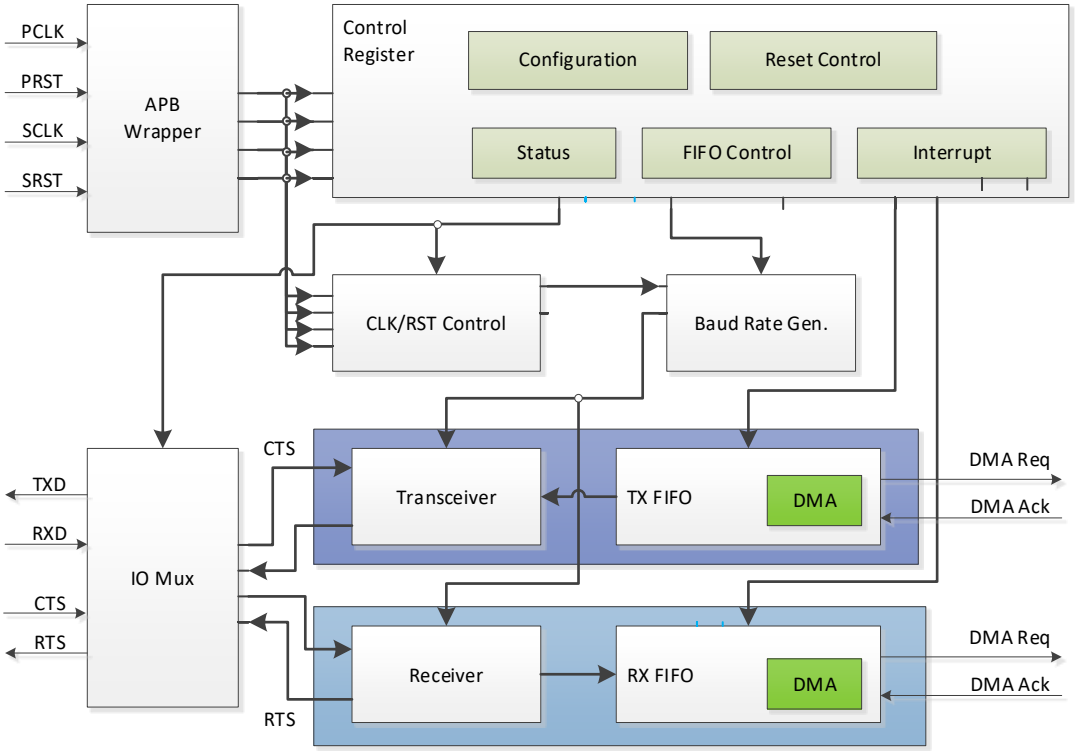


Figure 4-4 Functional diagram of UART

NOTE

Only the specified pins can operate in 5V. See section
The functions of each GPIO pin are listed in for details.

4.4.2 UART Specification

The UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k bit/s. Table 4-1 shows baud rate error calculations.

Table 4-1 UART baud rate specification

Desired baud rate	Actual baud rate	Error (%)
110	110.0533759	0.048523534
300	300.120048	0.040016006
600	600.240096	0.040016006
1200	1200.480192	0.040016006
2400	2400.960384	0.040016006
4800	4801.920768	0.040016006
9600	9603.841537	0.040016006
14400	14414.41441	0.1001001
19200	19230.76923	0.16025641
28800	28860.02886	0.208433542
38400	38461.53846	0.16025641

57600	57720.05772	0.208433542
76800	76923.07692	0.16025641
115200	115243.583	0.037832489
128000	128205.1282	0.16025641
153600	153846.1538	0.16025641
230400	231092.437	0.300536881
380400	380952.381	0.145210555
460800	460732.9843	0.014543339
500000	500000	0
921600	922431.8658	0.090263219
1000000	1000000	0
1382400	1383647.799	0.090263219
1444400	1452145.215	0.536223658
1500000	1506849.315	0.456621005
1843200	1856540.084	0.723745898
2000000	2000000	0
2100000	2105263.158	0.250626566
2764800	2784810.127	0.723745898
3000000	3013698.63	0.456621005
3250000	3283582.09	1.033295063
3692300	3728813.559	0.988910959
3750000	3793103.448	1.149425287
4000000	4000000	0

4.5 SDIO Device Mode Interface

The SDIO (Secure Digital Input Output) is an extension of the SD specification to cover I/O functions.

4.5.1 Features

- Supports SDIO 2.0 High Speed mode
- CIS can be configured with internal non-volatile memory for fast card detection
- Realtek SPI provides high efficiency SPI interface with interrupt and full duplex mode
- Supports high performance Ethernet to Wi-Fi transformation
- Supports non-flash booting when using an Ethernet to Wi-Fi transformation card

4.5.2 Bus Timing Specification

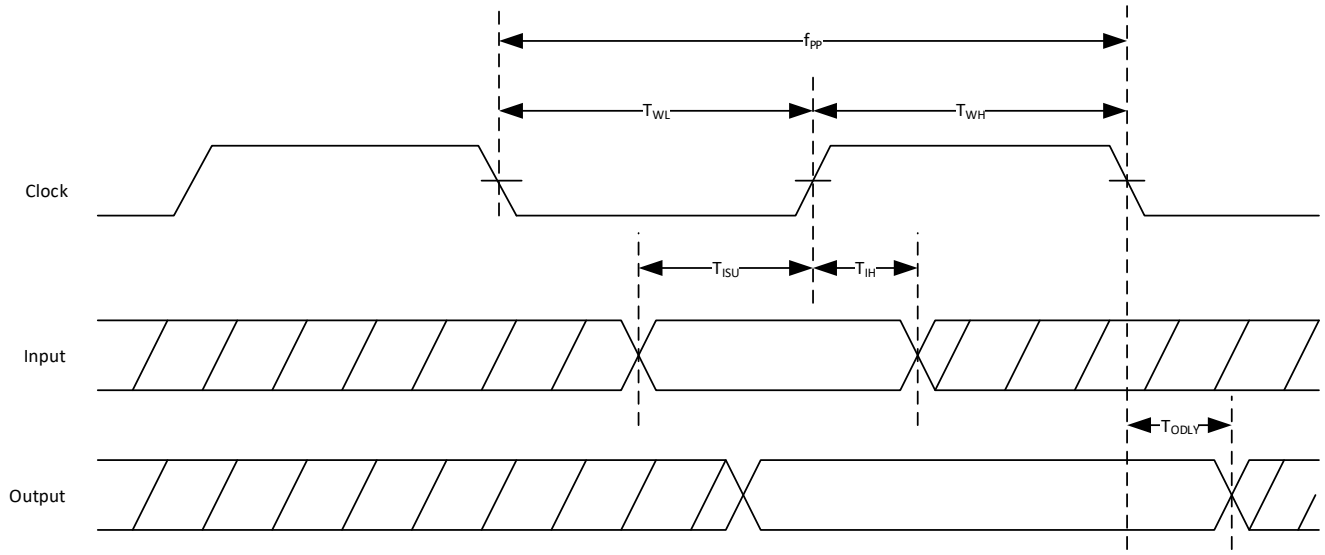


Figure 4-5 SDIO interface timing sequence

Table 4-2 SDIO interface timing parameters

Name	Parameter	Mode	Min.	Max.	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	Default	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	Default	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	Default	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	Default	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	Default	-	14	ns
		HS	-	14	ns

4.6 SPI Interface

The Serial Peripheral Interface (SPI) enables data communication between microcontrollers and other peripherals. High throughput and full-duplex capability with a simple hardware interface makes the SPI very efficient for various applications. The SPI is widely adopted to communicate with a variety of peripherals including sensors, control devices, memory, LCD, SD cards etc.

4.6.1 Features

- Supports 1 SPI port
- Supports Master/Slave mode
- Multiple Serial Interface Operations supported:
  - Motorola – SPI
  - Texas Instruments – SSI
  - National Semiconductor – Microwire
- Supports DMA to offload CPU bandwidth
- Maximum speed support for each SPI interface:
  - Supports baud rate up to 25MHz (Master mode)
  - Supports baud rate up to 6.25MHz (Slave mode Rx only)
  - Supports baud rate up to 5MHz (Slave mode TRx)
- Programmable clock bit-rate
- Programmable clock polarity (SCPOL) and phase (SCPH) for SPI protocol
- Supports 8 bit and 16 bit data frame size
- Supports bit swapping and byte swapping features
- The transmit FIFO and receive FIFO depth is 1024 bit (up to 64 data frames)

4.6.2 SPI Protocol

The SPI protocol mode can control via 2 parameters, SCPOL and SCPH. Both SCPOL and SCPH can be configured as 0 or 1 (SCPOL = 0/1, SCPH = 0/1) with a total of 4 modes as shown below.

- SCPOL defines inactive state of serial clock status:
  - 0: Low
  - 1: High
- SCPH defines serial clock toggle timing of the first data bit:
  - 0: Middle of the first data
  - 1: Start of the first data

4.6.2.1 SCPOL=0/SCPH=0

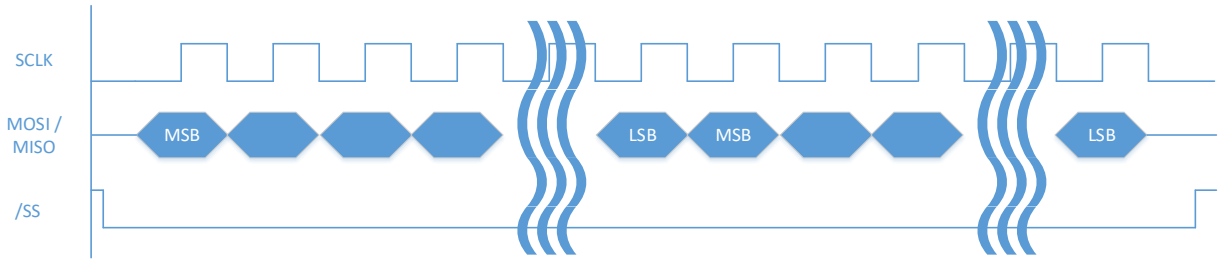


Figure 4-6 SPI protocol: mode 0 (SCPOL=0/SCPH=0)

4.6.2.2 SCPOL=0/SCPH=1

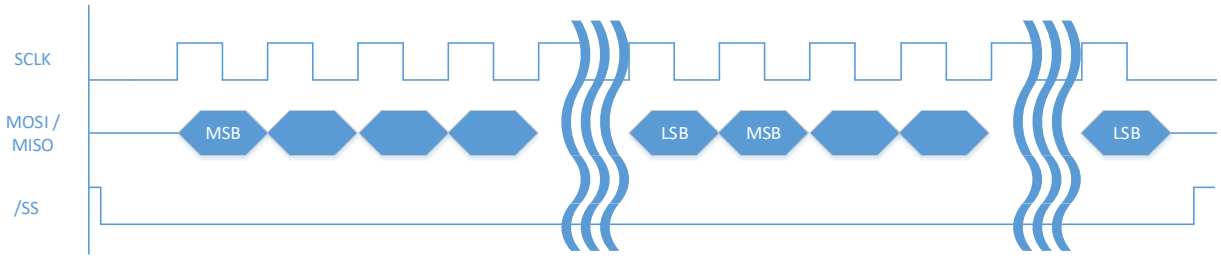


Figure 4-7 SPI protocol: mode 1 (SCPOL=0/SCPH=1)

4.6.2.3 SCPOL=1/SCPH=0

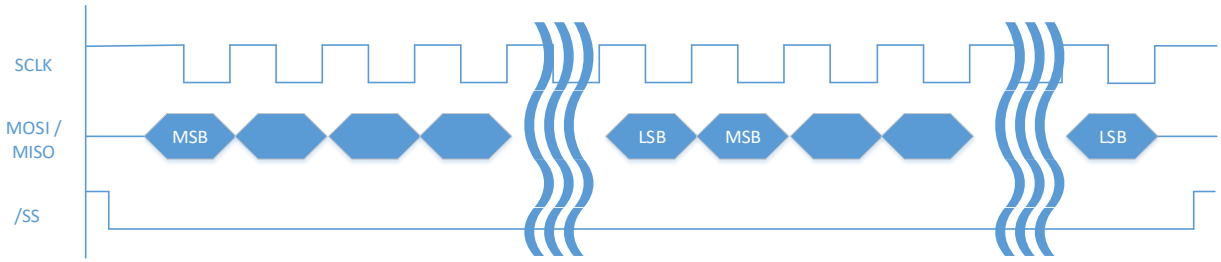


Figure 4-8 SPI protocol: mode 2 (SCPOL=1/SCPH=0)

4.6.2.4 SCPOL=1/SCPH=1

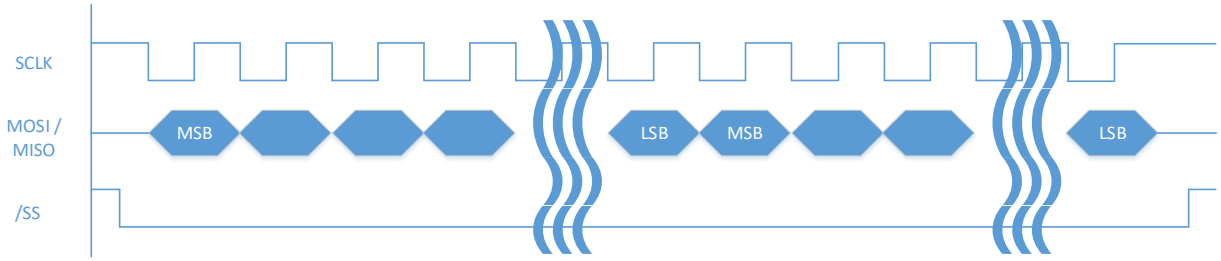


Figure 4-9 SPI protocol: mode 3 (SCPOL=1/SCPH=1)

4.7 I2C Interface

For external device connection, I2C is another popular serial interface since all I2C devices can be connected together, and only two wires (data and clock pin) are required for the I2C protocol. In a pin-limited system, I2C would be the ideal interface to integrate different external elements.

4.7.1 Features

- Supports maximum 1 x I2C ports
- Supports 3 different speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (<400 Kb/s)
  - High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
- Master or slave I2C operations
- 7-bit/10-bit addressing
- Supports Interrupt or polled mode operation
- Supports TX and RX DMA
- Transmit and receive buffers

4.7.2 Block Diagram

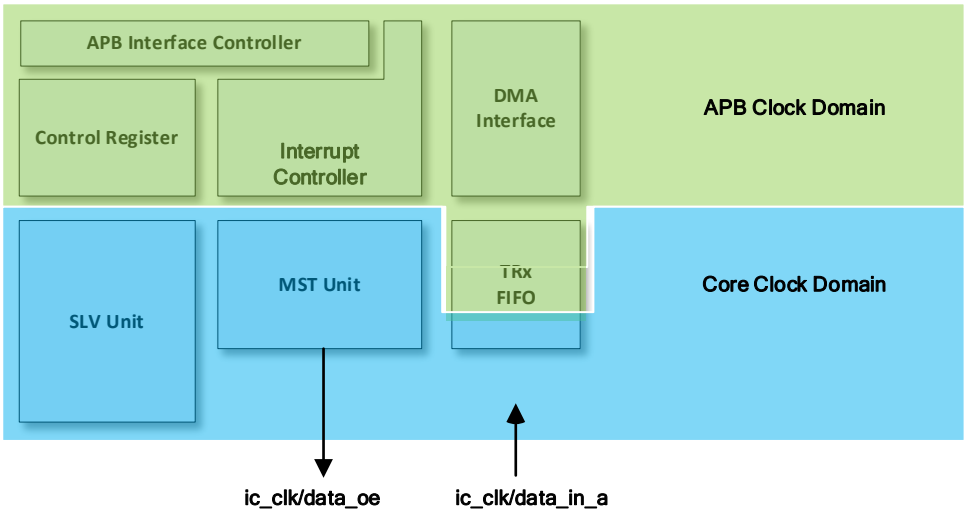


Figure 4-10 Functional diagram of I2C

4.8 PWM Interface

Pulse-Width Modulation (PWM) controllers generate pulse signals. The duty cycle, high time, and low time of pulse signals are programmable. In some particular applications, especially for LED and motor unit control, PWM is one of the most used interfaces. PWM interfaces can operate with GTimer, therefore PWM can work without involving the CPU.

4.8.1 Features

- Supports maximum 8 PWM functions
- 0 ~100% duty can be configured
- Use selected HS GTimer interrupt as counter source
- Minimum resolution is 50ns
- The period could be configured up to 8 seconds

4.8.2 Block Diagram

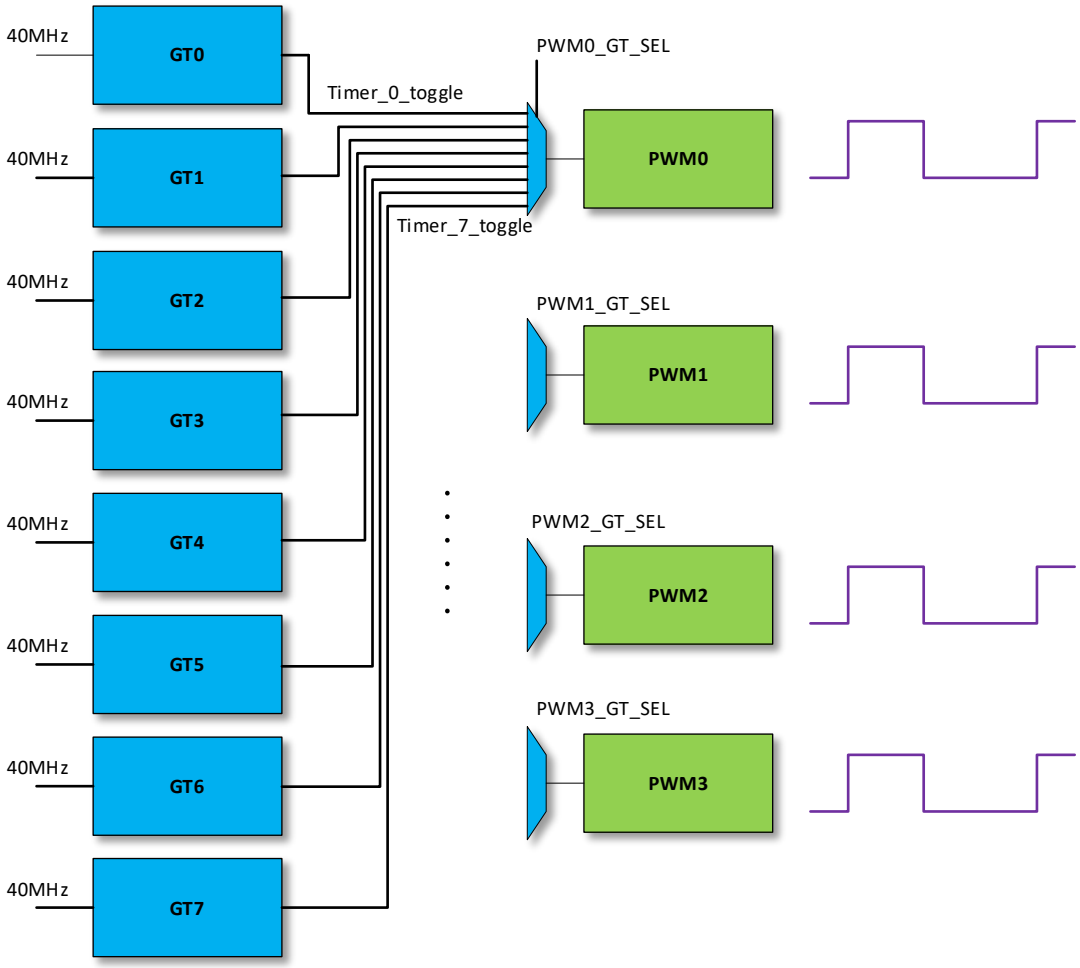


Figure 4-11 Functional diagram of PWM

4.9 Security Engine

In order to enhance security levels in embedded systems, the security engine offers various authentication and encryption/decryption functions to meet different states of security usage. A crypto engine provides low SW computing and high performance cryptographic operation (such as authentication, encryption, and decryption).

The security engine supports the following features:

- Provides low SW computing and high performance encryption
- Supported authentication algorithms:
  - General cryptographic hash function
    - MD5
    - SAH1
    - SHA2-224
    - SHA2-256
    - Sequential hash
  - HMAC (Hash-based message authentication code)
    - HMAC_MD5
    - HMAC_SHA1
    - HMAC_SHA2-224
    - HMAC_SHA2-256
  - Cipher (Encryption/Decryption) algorithms
    - AES-128/192/256
    - ECB (Electronic Codebook) mode

- CBC (Cipher Block Chaining) mode
- CTR (Counter) mode
- CFB (Cipher Feedback) mode
- OFB (Output Feedback) mode
- GCTR (Galois CTR) mode
- GMAC (Galois MAC) mode
- GHASH (Galois HASH) mode
- GCM (Galois/Counter Mode) mode

- CRC

5 RF Characteristics

The AmebaZII+ includes integrated WLAN RF transceiver architecture, and operates in 2.4GHz WLAN and Bluetooth systems.

5.1 RF Block Diagram

This section describes the AmebaZII+ RF block diagram. AmebaZII+ includes a Wi-Fi/BT subsystem that integrates a Wi-Fi/BT modem sharing a front-end RF (ADC, TRSW, LPF, PA, LNA, etc.), and this chip is compatible with IEEE 802.11 b/g/n protocol.

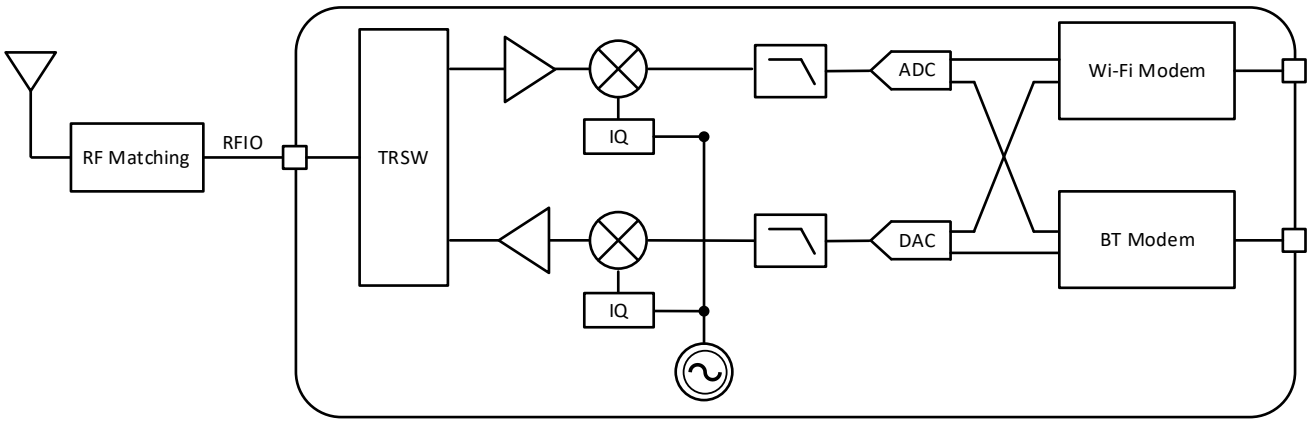


Figure 5-1 RF block diagram

5.2 Wi-Fi Radio Characteristics

Values in the following sections are typical values, and the reference point is the antenna port including front-end loss. These values may change slightly depending on different RF front-end designs or PCB designs.

5.2.1 Wi-Fi 2.4GHz Band RF Receiver Specifications

Table 5-1 Wi-Fi 2.4GHz band RF receiver specifications

Parameter	Description	Min.	Typ.	Max	Unit
Frequency Range	-	2400	-	2500	MHz
802.11b RX Sensitivity (8% PER)	1 Mbps DSSS	-	-99.0	-	dBm
	2 Mbps DSSS	-	-95.5	-	dBm
	5.5 Mbps DSSS	-	-93.5	-	dBm
	11 Mbps DSSS	-	-90.0	-	dBm
802.11g RX Sensitivity (10% PER)	6 Mbps OFDM	-	-94.0	-	dBm
	9 Mbps OFDM	-	-93.0	-	dBm
	12 Mbps OFDM	-	-91.5	-	dBm
	18 Mbps OFDM	-	-89.0	-	dBm
	24 Mbps OFDM	-	-86.0	-	dBm
	36 Mbps OFDM	-	-82.5	-	dBm
	48 Mbps OFDM	-	-78.0	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
802.11n RX Sensitivity (10% PER)	HT20 MCS0	-	-93.5	-	dBm
	HT20 MCS1	-	-91.0	-	dBm
	HT20 MCS2	-	-88.5	-	dBm
	HT20 MCS3	-	-85.5	-	dBm
	HT20 MCS4	-	-82.5	-	dBm
	HT20 MCS5	-	-77.0	-	dBm
	HT20 MCS6	-	-75.5	-	dBm

	HT20 MCS7	-	-74.0	-	dBm
Maximum Receive Level	1 Mbps DSSS	-	-	0	dBm
	6M bps OFDM	-	-	0	dBm

NOTE

The above Rx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

5.2.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications

Table 5-2 Wi-Fi 2.4GHz band RF transmitter specifications

Parameter	Description	Min	Typ.	Max	Unit
Frequency Range	-	2400	-	2500	MHz
TX power	1 Mbps DSSS	-	21	-	dBm
	11 Mbps DSSS	-	21	-	dBm
	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	17	-	dBm
	HT20 MCS0	-	19	-	dBm
	HT20 MCS7	-	16	-	dBm
TX EVM	1 Mbps DSSS	-	8	-	%
	11 Mbps DSSS	-	8	-	%
	6 Mbps OFDM	-	-5	-	dB
	54 Mbps OFDM	-	-25	-	dB
	HT20 MCS0	-	-5	-	dB
	HT20 MCS7	-	-28	-	dB
Carrier suppression	-	-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-	-45	dBm/MHz
	3rd Harmonic	-	-	-45	dBm/MHz

NOTE

- *The above Tx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.*
- *Target TX power is configurable based on different applications or certification requirements. We recommend to back off 3dB for mass production pass rate, and include a corner case margin.*

5.3 Bluetooth Radio Characteristics

Values in the following sections are typical values, and the reference point is the antenna port including front-end loss. These values may change slightly depending on different RF front-end designs or PCB designs. Both the transmitter specifications and the receiver specifications follow Bluetooth SIG specifications.

5.3.1 BT RF Transmitter Specifications

Table 5-3 Bluetooth transmitter performance (BLE)

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range	-	2402	-	2480	MHz
Tx Output Power	-	2.5	4.5	6.5	dBm
Adjacent channel transmit power	F = F0 ± 1 MHz	-	-15	-	dB
	F = F0 ± 2 MHz	-	-53	-	dB
	F = F0 ± 3 MHz	-	-56	-	dB
	F = F0 ± > 3 MHz	-	-57	-	dB
Δ f1avg	-	-	246	-	kHz
Δ f2max	-	-	220	-	kHz
Δ f2avg/Δ f1avg	-	-	0.92	-	-
ICFT	-	-	-15	-	KHz
Drift rate	-	-	2	-	kHz/50μs
Initial drift rate	-	-	-2	-	kHz

NOTE

The above Tx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

5.3.2 BT RF Receiver Specifications

Table 5-4 Bluetooth receiver performance (BLE)

Parameter	Description	Min	Typ.	Max	Unit
Parameter	Description	Minimum	Typical	Maximum	Units
Frequency Range	-	2402	-	2480	MHz
Rx Sensitivity @30.8% PER	Without spur channel	-	-100	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	Co-channel	-	6	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-4	-	dB
	F = F0 + 2 MHz	-	-50	-	dB
	F = F0 - 2 MHz	-	-25	-	dB
	F = F0 + 3 MHz	-	-55	-	dB
	F = F0 - 3 MHz	-	-25	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-30	-	-	dBm
	2000 MHz ~ 2400 MHz	-35	-	-	dBm
	2500 MHz ~ 3000 MHz	-35	-	-	dBm
	3000 MHz ~ 12.5 GHz	-30	-	-	dBm
Intermodulation	-	-	-32	-	dBm

NOTE

The above Rx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

6 Electrical Characteristics

6.1 Temperature Limit Ratings

Table 6-1 Temperature limit ratings

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_S	Storage Temperature		-55	-	+150	°C
T_A	Ambient Operating Temperature	Standard temperature IC	-20	-	+85	°C
		Wide-range temperature IC	-40	-	+105	°C
T_J max.	Maximum junction Temperature[1][2]		-	-	+125	°C

NOTE

[1] The junction temperature must not exceed T_J max. in all TA ranges. When TA is high and the power consumption of device is also high, a well-designed thermal management should be implemented to the board system to guarantee proper TJ. Refer to Section Thermal Characteristics to estimate TJ.

[2] The IC must not operate at junction temperature of 125°C for extended periods of time.

6.2 Power Supply DC Characteristics

Table 6-2 Power supply DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_IN	DC Supply Voltage for VDD_IN (3.3V)	2.97	3.3	3.63	V
VDD_IN	DC Supply Voltage for VDD_IN (5V)	4.5	5	5.5	V
VD33_SDIO VA33_XTAL VA33_SYN VA33_RF VA33_PA VA33_TR VD33_FLASH VD33_OUT	DC Supply Voltage for 3.3V Power Rail	2.97	3.3	3.63	V
VD11_CORE	DC Supply Voltage for 1.1V Power Rail	1.09	1.146	1.20	V
VD1833_LPC	DC Supply Voltage for GPIO/Embedded Flash	2.97	3.3	3.63	V

6.3 Typical Digital I/O Pin DC Characteristics

Table 6-3 Typical digital I/O DC parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-Trigger High Level	-	1.377	1.683	1.908	V
V_{T-}	Schmitt-Trigger Low Level	-	0.729	0.957	1.116	V
I_{IL}	Input-Leakage Current	VIN = 3.3V or 0	-10	±1	10	μA
-	Driving for Normal Pins	-	4	-	16	mA
I_{OH}	Driving for 5V UART Pins (GPIOA_13/GPIOA_14)	3.3V/5V	4/4	-	8/8	mA
I_{OL}	Driving for 5V UART Pins (GPIOA_13/GPIOA_14)	3.3V/5V	4/4	-	8/8	mA
-	Driving for SDIO Device Pins	-	4	-	16	mA
-	Loading for Normal Pins	-	-	15	-	pF
-	Loading for 5V UART Pins (GPIOA_13/GPIOA_14)		-	15	-	pF
-	Loading for SDIO Device Pins	-	-	15	-	pF
-	Pull Resistance for Normal Pins	3.3V	-	75	-	KΩ

-	Pull Resistance for 5V UART Pins (GPIOA_13/GPIOA_14)	3.3V/5V	-	80/120	-	KΩ
-	Pull Resistance for SDIO Device Pins	3.3V	-	50	-	KΩ

NOTE

The pull resistance values are typical values checked in the manufacturing process, and are not tested.

6.4 ESD Characteristics

Table 6-4 ESD characteristics

Reliability test	Standard	Test condition	Result
Human Body Model (HBM)	JESD22-A114F-2008	±2000V	Pass
Machine Model (MM)	JESD22-A115C-2010	±100V	Pass
Charge Device Model (CDM)	JESD22-C101F-2013	±500V	Pass

6.5 Power Sequence

6.5.1 Power-on or Resuming from Deep-Sleep Sequence

The timing sequence of power-on or resuming from deep-sleep is given in Figure 6-1.

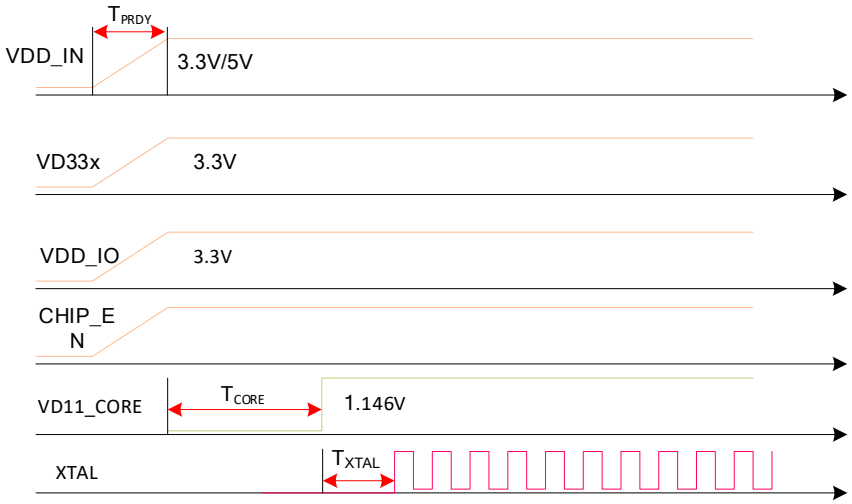


Figure 6-1 Power-on or resuming from deep-sleep sequence

Table 6-5 Timing specification for power-on sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{PRDY}	3.3V Ready Time	0.6	-	5	ms
	5V Ready Time	1	-	5	ms
T_{CORE}	Core Power Ready Time	-	14	-	ms
T_{XTAL}	XTAL Ready Time after Core Power	-	5	-	ms

6.5.2 Resuming from Standby Sequence

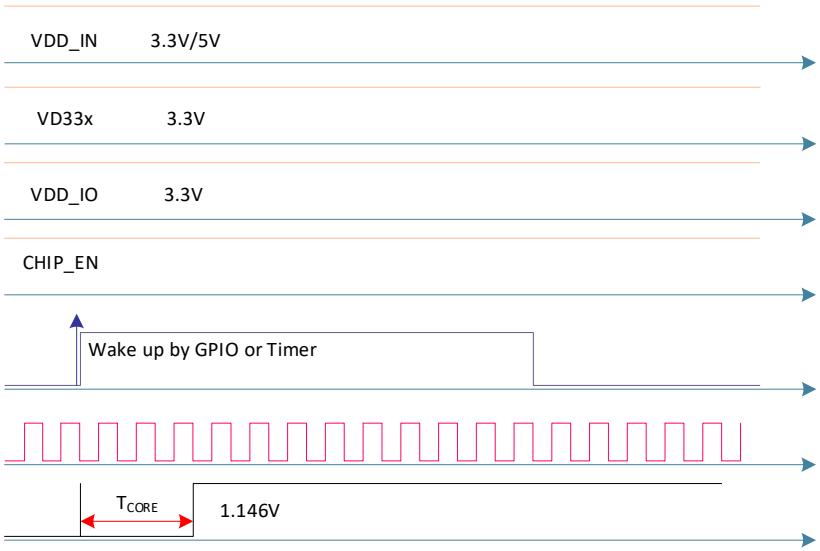


Figure 6-2 Resuming from standby sequence

Table 6-6 Timing specification for resuming from standby Sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{CORE}	Core Power Ready Time	1.5	-	-	ms

6.5.3 Shutdown Sequence

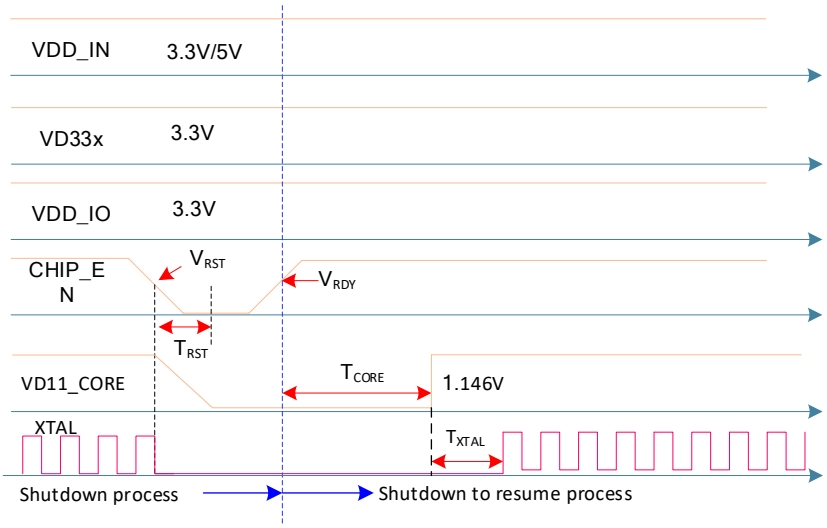


Figure 6-3 Shutdown sequence

Table 6-7 Timing specification for shutdown sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{RST}	Shutdown occurs after CHIP_EN is lower than this voltage	-	-	0.8	V
T_{RST}	Required time that CHIP_EN is lower than V_{RST}	1	-	-	ms
V_{RDY}	Enable PMC after CHIP_EN is higher than this voltage	2	-	-	V
T_{CORE}	Core Power Ready Time	-	14	-	ms
T_{XTAL}	XTAL Ready Time after Core Power	-	5	-	ms

6.5.4 Power Down Sequence

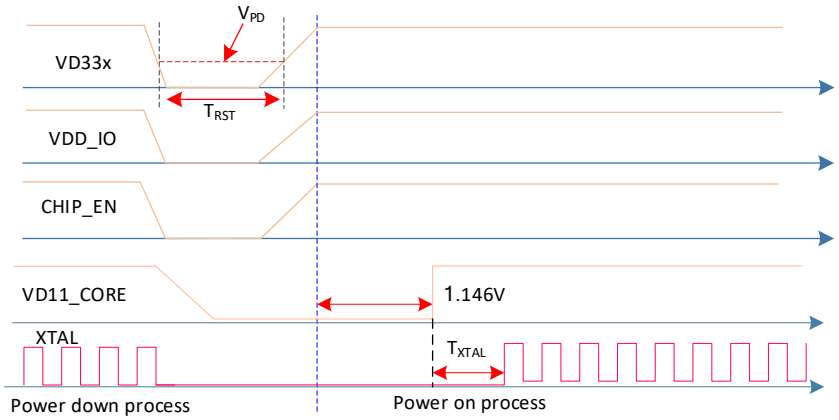


Figure 6-4 Power down sequence

Table 6-8 Timing specification for power down sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{PD}	Power Down Voltage	-	-	0.5	V
T_{RST}	Required time that VD33x and VDD_IO is lower than V_{PD}	1	-	-	ms
T_{CORE}	Core Power Ready Time	-	14	-	ms
TXTAL	XTAL Ready Time after Core Power	-	5	-	ms

7 Package Information

In order to meet environmental requirements, Realtek offers devices in different grades of ECOPACK® packages, depending on the level of environmental compliance.

7.1 Package Outline

The QFN40 is a 40-pin, 5mm x 5mm quad flat no-leads package with 0.4mm pitch.

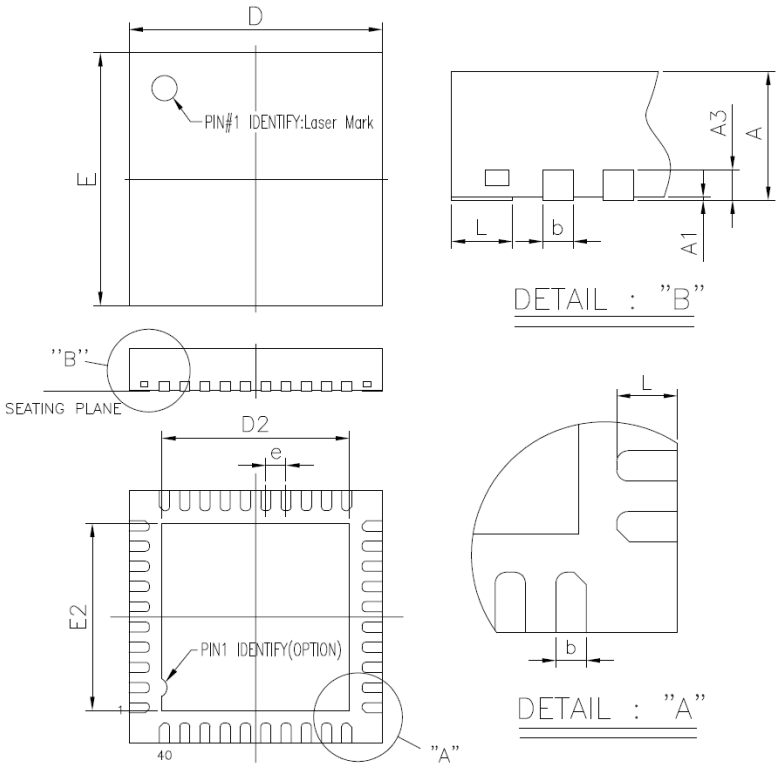


Figure 7-1 QFN40 package outline

Table 7-1 QFN40 package mechanical data

Symbol	Dimension (millimeter)		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D/E	5.00 BSC		
D2/E2	3.35	3.61	3.86
e	0.40 BSC		
L	0.30	0.40	0.50

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M.-1994.*
- *Values in inches are converted from mm and rounded to 2 decimal digits.*

7.2 Thermal Characteristics

Symbol	Parameter[1]	Package	Condition	Value[2][3]	Unit
θ_{JA}	Junction-to-ambient thermal resistance	QFN, 40-pin	Based on the Realtek EVB with still air	62.09	°C/W
Ψ_{JT}	Junction-to-top center thermal	QFN, 40-pin	Based on the Realtek EVB with still air	0.93	

	characterization parameter				
Ψ_{JB}	Junction-to-board thermal characterization parameter	QFN, 40-pin	Based on the Realtek EVB with still air	11.81	

NOTE

[1] Refer to EIA/JESD51-2, Integrated circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air) for more information.

[2] These values are based on customized PCB systems designed by Realtek, and will vary in function of board thermal characteristics and other components on the board.

[3] An ambient temperature of 85°C is assumed.

Revision History

Date	Revision	Release Notes
2024-09-03	1.1	Added the section: Ordering Information
2024-07-12	1.0	Initial release