Priyal Riddhish Chhatrapati

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EDUCATION

Georgia Institute of Technology (GPA - N.A.) Aug. 2021 – Present
Master of Science in ECE with specialization in Computer Systems and Software Atlanta, GA

- **Coursework**: Advanced Programming Techniques, Advanced Computer Architecture
- **Research**: Accelerating Convolutional Neural Network using Specialized Hardware

BITS Pilani (GPA - 9.1/10) Aug. 2016 – May 2020
Bachelor of Engineering in Electronics and Instrumentation Engineering Goa, India

- **Coursework**: Computer Architecture, Object Oriented Programming, Real Time Operating Systems(Audit), Algorithms(Audit)
- **Research**: Approximate Computing for Fault Tolerant Data Storages(National University of Singapore)

EXPERIENCE

SiFive Sept 2020 – June 2021
Engineer - VLSI Bangalore, India

- Developed **MIPI CSI-2 v3.0 bus**; Standard Interface between Cameras and Host Processor;
- Co-authored Specification Document for the CSI-2 bus; Co-authored Microarchitectural Document for the CSI-2 bus
- Implemented CSI-2 bus using Verilog; **Saving ~$100,000** in licensing costs and royalties.

National University of Singapore Aug 2019 – Dec 2019
Intern Singapore

- Developed a Python **Codec** to do error correction for fault tolerant data storage using **Reed Solomon Codes**
- Set up scripts to manually induce errors in encoded multimedia files to check the effectiveness the storage
- Parallelized the scripts and reduced the runtime of experimentation by ~**20x**

Indian Institute of Technology May 2019 – July. 2019
Intern Chennai, India

- Developed a **CNN Inference Accelerator** to accelerate Convolutions; Achieved a performance boost of **10x**
- Ported TF Convolutions to run on the accelerator instead of CPU for experimentation

PROJECTS

Trace Based L1 Cache Simulator (C/C++)

- Developed a Simulator supporting variable block size, associativity and cache size
- Reports number of hits, misses and latency

Chat Client using FLUSH RELOAD attack(C/C++)

- Receiver spying on Sender using Flush Reload attack on Shared LLC
- Sender and Receiver talk to each other without using IPC mechanisms(Message passing, shared memory)

Trace based Microprocessor Performance Simulator(C/C++)

- Developed a Simulator with Parametric support for Forwarding and SuperScalar Execution
- Reports Number of Cycles, Stalls, Data dependencies and CPI