1. Description

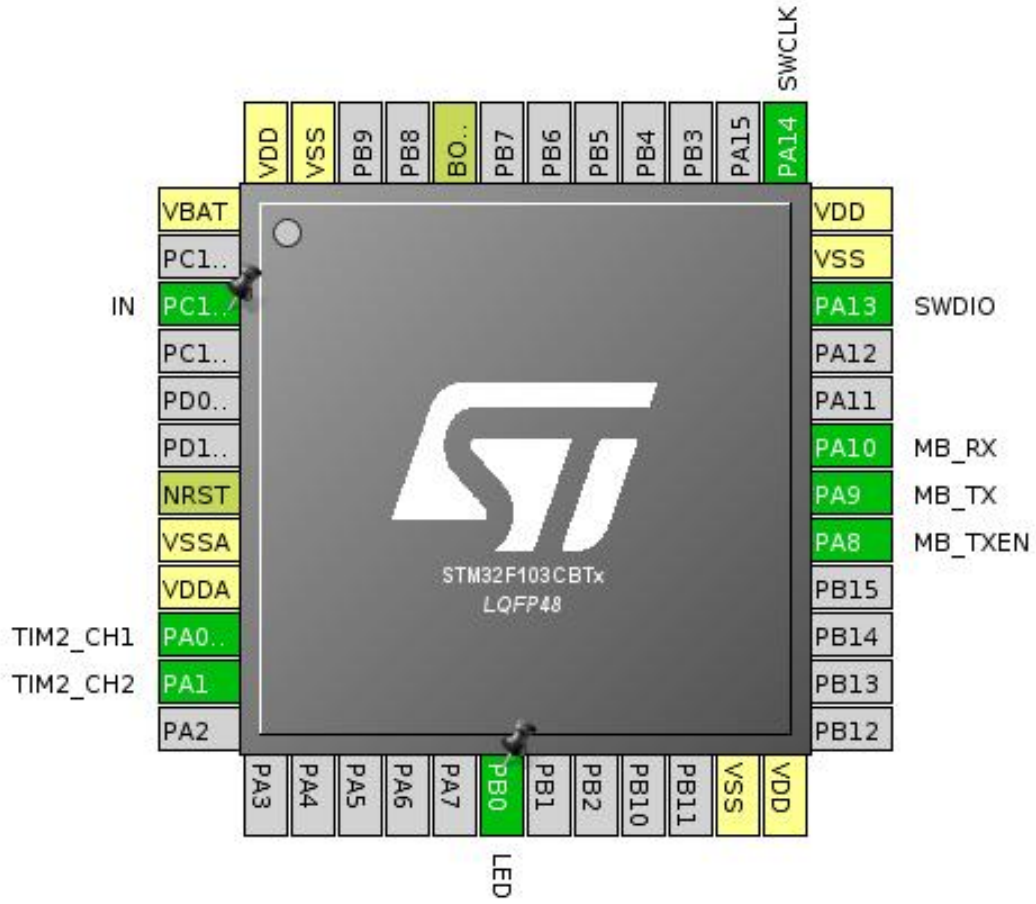
1.1. Project

Project Name	stm32F103-mbdimmer
Board Name	custom
Generated with:	STM32CubeMX 4.9.0
Date	01/19/2020

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103CBTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN *	I/O	GPIO_Input	IN
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	TIM2_CH1	
11	PA1	I/O	TIM2_CH2	
18	PB0 *	I/O	GPIO_Output	LED
23	VSS	Power		
24	VDD	Power		
29	PA8 *	I/O	GPIO_Output	MB_TXEN
30	PA9	I/O	USART1_TX	MB_TX
31	PA10	I/O	USART1_RX	MB_RX
34	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. IPs and Middleware Configuration

4.1. ADC1

mode: Temperature Sensor Channel

mode: Vrefint Channel

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Conversions	Enable
Rank	1
Channel	**Channel Temperature Sensor ***
Sampling Time	1.5 Cycles

ADCgroup:

Number Of Conversion	1
External Trigger Conversion Edge	None
Number Of Conversions	0
Number Of Conversion	1
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

4.2. IWDG

mode: Activated

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

4.3. SYS

Debug: Serial-Wire

4.4. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

4.5. TIM4

mode: Clock Source

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.6. USART1

Mode: Asynchronous

Basic Parameters:

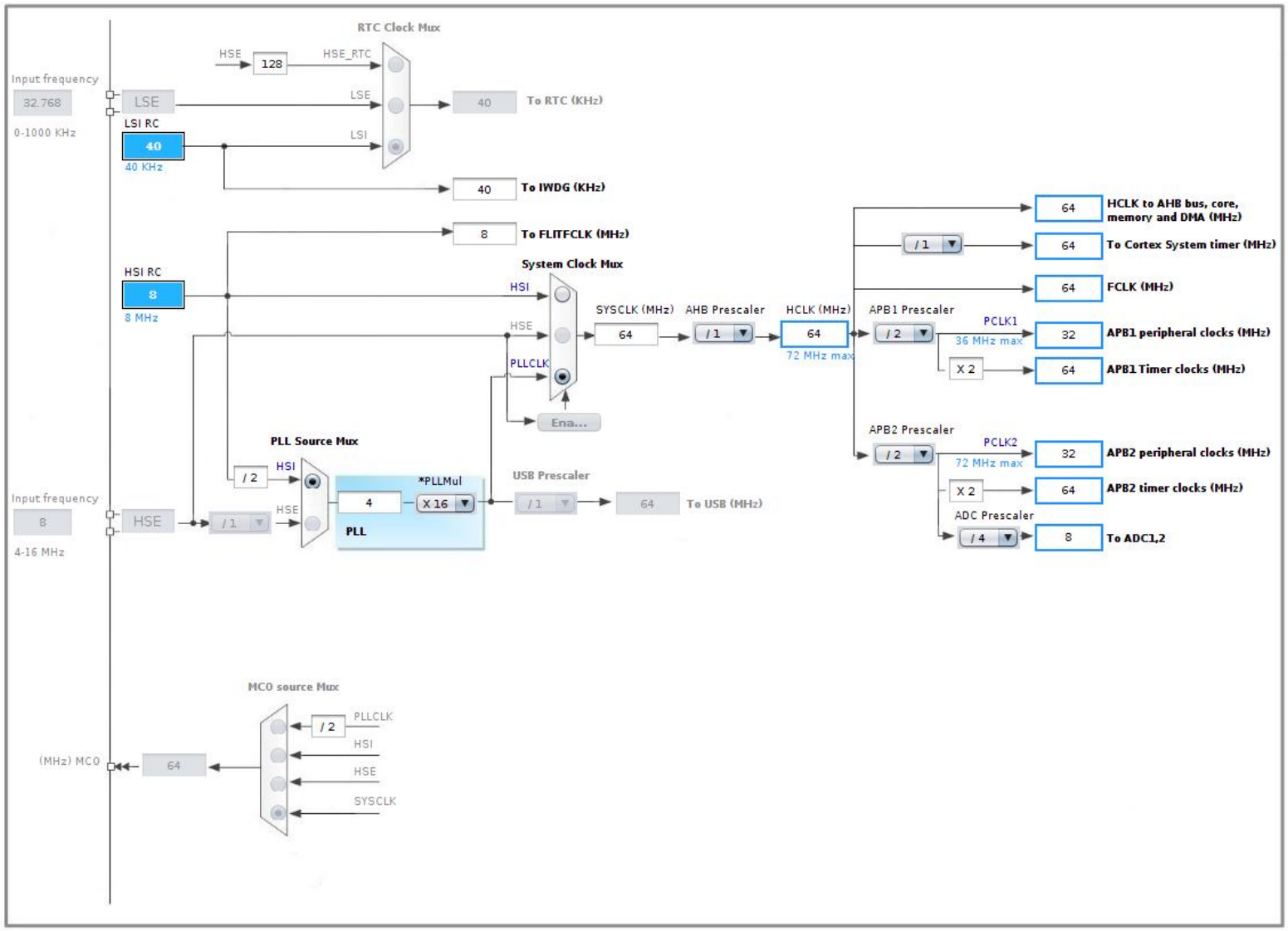
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

2. Clock Tree Configuration



3. Power Plugin report

3.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103CBTx
Datasheet	13587_Rev16

3.2. Parameter Selection

Temperature	25
Vdd	3.3

3.3. Sequence

Step	STEP1
Mode	RUN
Range	No Scale
Fetch type	FLASH
Clock Config.	HSI PLL
Clock Source Freq.	8.0 MHz
CPU Freq.	64.0 MHz
Periph.	GPIOA GPIOB GPIOC IWDG TIM2 TIM4 USART1
Additional Cons.	0 mA
Average Current	27.78 mA
Duration	1 ms
DMIPS	80.0

3.4. Results

Sequence time	1 ms	Average current	27.78 mA

Battery Life	0	Average DMIPS	80.0 DMIPS

3.5. Chart