

CS2310: Foundations of Computer System Design Lab

August-November 2021 Semester

Assignment 3

Date: 31st August, 2021

Deadline for Submission: 11.59PM on 6th September, 2021

Design of 16-bit adder/subtractor for integers using the following:

1. 16-bit ripple carry adder
2. 4-bit CLA based 16-bit adder without using higher-level propagate and generate terms
3. 4-bit CLA based 16-bit adder using higher-level propagate and generate terms

Overflow detection logic also needs to be included.

Test cases for unsigned integers should include the following:

1. A pair of unsigned integer operands for addition without resulting in overflow
2. A pair of unsigned integer operands for addition resulting in overflow
3. A pair of unsigned integer operands for subtraction with a valid output

Test cases for signed integers should include the following:

1. A pair of positive integers for addition without resulting in overflow
2. A pair of positive integers for addition resulting in overflow
3. A pair of negative integers for addition without resulting in overflow
4. A pair of negative integers for addition resulting in overflow.
5. A pair of operands of opposite sign for addition. There is no overflow for this condition.
6. A pair of operands of opposite sign for subtraction without resulting in overflow
7. A pair of operands of opposite sign for subtraction resulting in overflow