CS2310: Foundations of Computer System Design Lab

August-November 2021 Semester

Assignment 4

Date: 14th September, 2021

Deadline for Submission: 11.59PM on 21th September, 2021

Design an 8-bit Wallace tree multiplier circuit using carry save addition (CSA) based 3-to-2 reducers followed by CLA with higher-level propagate and generate terms.

(a) Unsigned integer multiplier

(b) Signed integer multiplier

Test cases for unsigned integer multiplier:

2 pairs of operands that do not result in overflow.

1 pair of operands that results in overflow.

Test cases for signed integer multiplier:

Following pairs of operands that do not result in overflow:

1 pair of positive operands

1 pair of positive multiplicand operand and negative multiplier operand

1 pair of negative multiplicand operand and positive multiplier operand

1 pair of negative operands

Following pairs of operands that result in overflow:

1 pair of operands of the same sign

1 pair of operands of opposite signs