R61503B

262,144-color, 176RGB x 220-dot graphics a-Si TFT liquid crystal panel controller driver

REJxxxxxxx-xxxxZ
Rev.0.12
January.11.2005

- **Index**

Description

The R61503B is a one-chip controller driver LSI for 262,144-color TFT panel, incorporating RAM for a maximum 176RGB x 220-dot graphics display and 528-channel source driver. The R61503B provides a one-chip solution to drive TFT panel by generating gate drive signal and liquid crystal drive power supply.

To transfer data efficiently, the R61503B supports high-speed interface via 8-/9-/16-/18-bit port as system interface to microcomputer and high-speed RAM write function. As moving picture interface, the R61503B supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 18-/16-/6-bit port and VSYNC interface (system interface + VSYNC). The moving picture interface enables moving picture display at the arbitrary position determined by window address setting. The window address setting enables displaying a moving picture and the data written in the internal RAM simultaneously and allows transferring moving picture data not constrained by the position of still picture display. By writing moving picture data via moving picture interface in the window address area, the number of data transfer can be minimized and the power consumption by the system can be reduced.

The R61503B can operate at low voltage up to 1.65V for the power supply to the I/O interface unit and it incorporates a voltage follower circuit to generate liquid crystal drive voltage. The R61503B's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products such as digital cellular phones and small PDAs, where long battery life is a major concern.

Features

- One-chip controller driver for 176RGB x 220-dot graphics display in 262,144 colors on TFT panel
- One-chip solution for a-Si TFT panel
- System interface
  - High-speed interface via 8-, 9-, 16-, 18-bit parallel ports
  - Clock synchronous serial interface
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 6-, 16-, 18-bit ports
  - VSYNC interface (System interface + VSYNC)
- High-speed RAM write function
- Window address function to specify a rectangular area in the internal RAM to write data
  - Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
- Color display control functions
  - γ-correction function to display in 262k colors
  - 1-line unit vertical scroll function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby function
  - 8-color display function
  - Partial display function
  - Input power supply voltages: Vcc = 2.5V ~ 3.6 V (logic regulator power supply)
    IOVcc = 1.65V ~ 3.6 V (interface I/O power supply)
    Vci = 2.5V ~ 3.6 V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply: DDVDH-AGND = 4.5V ~ 6.0V
  - Gate drive power supply: VGH-VGL ≤ 28.0V
  - Vcom drive (Vcom power supply): VcomH = (DDVDH+0.5)V ~ 2.5V
    VcomL = (Vci+0.5)V ~ GND
- 87,120-byte internal RAM
- Internal liquid crystal drive circuit: 528-channel source output and 220-channel gate output
- N-line-inversion liquid crystal drive to invert polarity of liquid crystal in a cycle of arbitrary line period
- Internal oscillator, Hardware Reset
- Reversible source output shift direction
- TFT storage capacitor: Cst only
- Internal EPROM: for user identification code (4 bits) and Vcom level adjustment (12 bits)

Table 1 R61503B's power supply main specifications

No.	Item		R61503B
1	TFT data lines		528 output
2	TFT gate lines		220 output
3	TFT display storage capacitor		Cst only (Common Vcom formula)
4	Liquid crystal drive output	S1~S528	V0 ~ V31 grayscales
		G1~G220	VGH-VGL
		Vcom	VcomH/VcomL
5	Input voltage	IOVcc (interface voltage)	1.65V ~ 3.60V Power supply to IM0/ID, IM1-3, RESET, DB17-0, RD, SDI, SDO, WR/SCL, RS, CS*, VSYNC, HSYNC, DOTCLK, ENABLE Connect to Vcc and Vci on the FPC when IOVcc, Vcc and Vci are at the same electrical potential.
		Vcc (logic regulator power supply) see Note 1	2.50V ~ 3.60V Connect to IOVcc and Vci on the FPC when IOVcc, Vcc and Vci are at the same electrical potential.
		VDD(Internal logic power supply) see Note 2	1.5V
		Vci (liquid crystal drive power supply) see Note 2	2.50V ~ 3.60V Connect to IOVcc and Vcc on the when IOVcc, Vcc and Vci are at the same electrical potential.
5	Internal step-up circuits	DDVDH	Vci1 x 2
		VGH	Vci1 x 6, x 5, x 4
		VGL	Vci1 x –2, x -3, x -4, x -5

Notes: 1. When the internal logic regulator is used.
2. Generated from the internal logic regulator power supply circuit.

Block Diagram

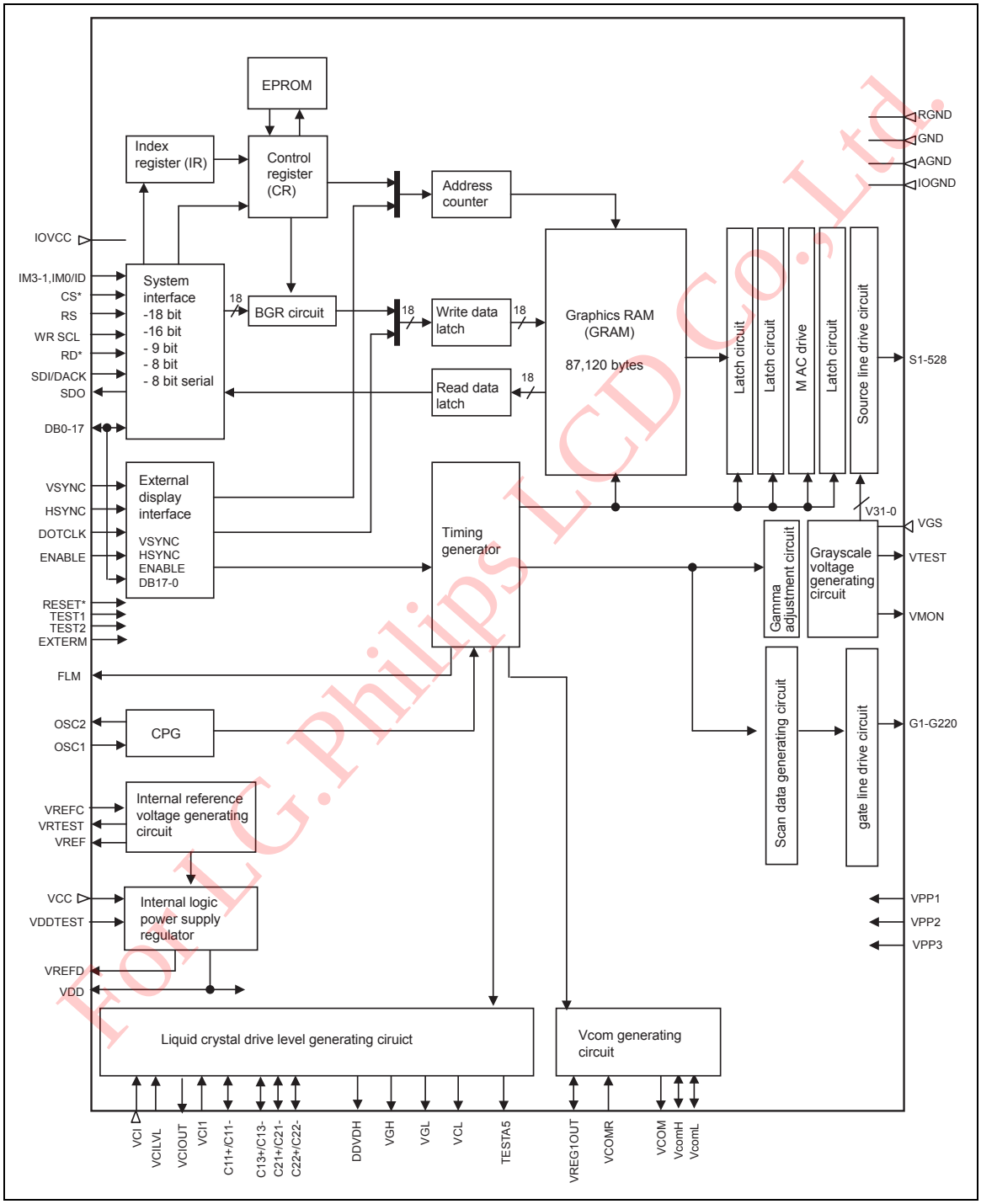


Figure 1

Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>Number</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM3-1
IM0/ID</td><td>4</td><td>I</td><td>IOGND1 or IOVcc1</td><td>Selects MPU interface format. Amplitude: IOVCC-IOGND.
When selecting clock synchronous serial interface, IM0 pin is used to set the device code ID.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface format</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Clock synchronous serial interface</td><td>SDI/SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting disabled</td><td>-</td></tr>
</table></td><td>-</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVcc-IOGND
Low: the R61503B is selected and accessible
High: the R61503B is not selected and not accessible.</td><td>-</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVcc-IOGND
Low: select Index or status register
High: select control register</td><td>IOVcc</td></tr>
<tr><td>WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WR* is low. Synchronous clock signal (SCL) in serial interface operation.
Amplitude: IOVcc-IOGND</td><td>IOVcc</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RD* is low.
Amplitude: IOVcc-IOGND</td><td>IOVcc</td></tr>
<tr><td>SDI/DACK</td><td>1</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. When DAKE = 1, chip select signal is outputted for DMA transfer single address mode. In this case, the R61503B becomes accessible when the signal is Low and it becomes inaccessible when the signal is High. Amplitude: IOVcc-IOGND</td><td>IOGND or IOVcc</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVcc-IOGND</td><td>Open</td></tr>
</table>

Table 3 Interface (continued)

Signal	Number	I/O	Connect to	Function	When not in use
DB0-DB17	18	I/O	MPU	Parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVcc-IOGND). Fix unused pins to either IOVcc or GND level. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. Parallel bi-directional data bus for RGB interface operation (Amplitude: IOVcc-IOGND). 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used.	IOGND or IOVCC
ENABLE	1	I	MPU	Data enable signal for RGB interface operation. (Amplitude: IOVcc-IOGND). Low: accessible (select) High: Note accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	IOGND or IOVcc
VSYNC	1	I	MPU	Frame synchronous signal for RGB interface operation. Low active. (Amplitude: IOVcc-IOGND).	IOGND or IOVcc
HSYNC	1	I	MPU	Line synchronous signal for RGB interface operation. Low active. (Amplitude: IOVcc-IOGND).	IOGND or IOVcc
DOTCLK	1	I	MPU	Dot clock signal for RGB interface operation. The data is inputted on the rising edge of DOTCLK. (Amplitude: IOVcc-IOGND).	IOGND or IOVcc
FLM	1	O	MPU	Frame head pulse to synchronize RAM data write operation with the frame head position. (Amplitude: IOVcc-IOGND).	Open

Table 4 Reset an d oscillator

Signal	Number	I/O	Connect to	Function	When not in use
RESET*	1	I	MPU or external RC circuit	Reset signal. Initializes the R61503B when RESET input is low. Make sure to execute a power-on reset when turning on the power supply. (Amplitude: IOVcc1-IOGND1).	-
OSC1 OSC2	2	I O	Oscillator	Connect an external resistor for RC oscillation.	-

Table 5 Power supply

Signal	Number	I/O	Connect to	Function	When not in use
Vcc	1	-	Power supply	Power supply to internal logic regulator circuit: Vcc = 2.5V~3.6V. Vcc ≥ IOVcc	-
GND	1	-	Power supply	Internal logic GND: GND = 0V.	-
RGND	1	-	Power supply	Internal RAM GND: RGND and GND must be at the same electrical potential. In case of COG, connect to GND on the FPC to prevent noise.	-
VDD VDDOUT	1	O	Stabilizing capacitor	Internal logic regulator output used for internal logic power supply. Connect a stabilizing capacitor.	-
IOVcc	1	-	Power supply	Power supply to interface pins: RESET; CS; WR; RD; RS; DB17-0; VSYNC; HSYNC; DOTCLK; ENABLE. IOVcc = 1.65V ~ 3.6V. Vcc ≥ IOVcc In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.	-
IOGND	1	-	Power supply	GND of interface pins: RESET; CS; WR; RD; RS; DB17-0; VSYNC; HSYNC; DOTCLK; ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.	-
AGND	1	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.	-
Vci	1	I	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.6V.	-
VciLVL	1	I	Reference power supply	VciLVL and Vci must be at the same electrical potential. Connect VciLVL to an external power supply of 2.5V ~ 3.6V. In case of COG, connect to Vci on the FPC to prevent noise.	-
VPP1	1	I	Power supply or open	Internal EPROM power supply. Apply the following voltages on VPP1 ~ VPP3 respectively according to the power supply ON sequence.	Open
VPP2	1	I	Power supply or open		Open
VPP3	1	I	Power supply or open		Open

Operation mode	VPP1	VP2	VPP3
EPROM write	9.0±0.3V	7.0±0.3V	GND
EPROM read	Open	Open	Open

Table 6 Step-up circuit

Signal	Number	I/O	Connect to	Function	When not in use
VciOUT	1	O	Stabilizing capacitor, Vci1	Internal reference voltage generated between Vci and GND. The output voltage level is set by instruction (VC).	-
Vci1	1	I/O	VciOUT	Reference voltage for step-up circuit 1. Vci1 must be set so that the output voltages DDVDH, VGH, VGL are generated within the respective setting ranges.	-
DDVDH	1	O	Stabilizing capacitor	DDVDH is generated from Vci1 in the step-up circuit 1. The step-up factor is set by instruction (BT). DDVDH = 4.5V ~ 6.0V	-
VGH	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2. The step-up factor is set by instruction (BT). VGH = max. 15.0V	-
VGL	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2. The step-up factor is set by instruction (BT). VGL = max. -10.0V	-
C11+, C11	2	I O	Step-up capacitor	Capacitor connection pins of the step-up circuit 1.	-
C13+, C13- C21+, C21- C22+, C22-	6	I O	Step-up capacitor	Capacitor connection pins of the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.	-
VCL	1	O	Stabilizing capacitor	Power supply for VcomL drive.	-

Table 7 Liquid crystal drive

Signal	Number	I/O	Connect to	Function	When not in use
VREG1 OUT	1	O	Stabilizing capacitor	VREG1OUT is generated from VciLVL and the output level is set by instruction (VRH) and used for (1) source driver grayscale reference voltage VDH, (2) VcomH level reference voltage, (3) Vcom amplitude reference voltage and (4) liquid crystal drive electrical potential in 8-color display mode. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 2.5V ~ (DDVDH – 0.5)V	Open
Vcom	1	O	TFT common electrode	Power supply to TFT common electrode. The Vcom amplitude is determined by VcomH and VcomL levels. The alternating cycle can be changed by setting register. Also halting/starting Vcom output can be controlled by instruction (COM).	Open
VcomH	1	O	Stabilizing capacitor	The High level of Vcom. The VcomH output level can be determined by either internal electronic volume or external variable resistor (VcomR).	Open
VcomL	1	O	Stabilizing capacitor	The Low level of Vcom.	Open
VcomR	1	I	Variable resistor or open	Connect a variable resistor between VREG1OUT and GND when adjusting the VcomH level externally.	Open
VGS	1	I	GND	Reference level of grayscale voltage generating circuit.	-
S1~S528	528	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S528.	Open
G1~G220	220	O	LCD	Gate output signal Gate select level: VGH Gate non-select level: VGL	Open

Table 8 Liquid crystal drive

Signal	Number	I/O	Connect to	Function	When not in use
VTEST	1	O	Open	Test pin. Leave it open.	Open
VREFC	1	I	AGND	Test pin. Fix it to AGND level.	-
VREF	1	O	Open	Test pin. Leave it open.	Open
VDDTEST	1	I	AGND	Test pin. Fix it to AGND level.	-
VREFD	1	O	Open	Test pin. Leave it open.	Open
VMON	1	O	Open	Test pin. Leave it open.	Open
TESTA5		O	Open	Test pin. Leave it open.	Open
IOVccDUM1, IOVccDUM2	2	O	-	Use when fixing the electrical potential of unused interface pins and fixed pins. When not in use, leave it open.	Open
IOGNDDUM 1, IOGNDDUM 2	2	O	-	Use when fixing the electrical potential of unused interface pins and fixed pins. When not in use, leave it open.	Open
OSC1DUM 1-4	4	O	-	Test pins. Leave them open.	Open
OSC2DUM 1-2	2	O	-	Test pins. Leave them open.	Open
AGNDDUM1	1	O	-	Use when fixing VREFC, VDDTEST	Open
DUMMYR 1-10	10	-	-	DUMMYR1 and DUMMYR10, DUMMYR2 and DUMMYR9, DUMMYR3 and DUMMYR4, DUMMYR5 and DUMMYR8, DUMMYR6 and DUMMYR7 are short-circuited within the LSI for measuring COG contact resistance.	Open
VGLDMY 1-4	4	O	-	Dummy pads. Leave them open.	Open
TESTO 1-32	32	O	-	Dummy pads. Leave them open.	Open
TEST1	1	I	IOGND	Test pin. Connect to IOGND.	IOGND
EXTERM	1	I	IOGND	Test pin. Connect to IOGND.	IOGND

Patents of dummy pin which is used to fix pin to Vcc or GND are pending and granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484
Korean Application No. 19997002322
Taiwanese Application No.086103756
(PCT/JP96/02728(W098/12597)

R61503B PAD arrangement

Rev0.0 2005.11.09

●Chip Size：17.2mm x 1.43mm
●Chip Thickness：400μm(typ.)
●Pad Coordinate：Pad Center
●Coordinate Origin：Chip Center

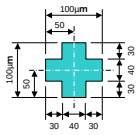
●Au BUMP Size
(1) 50μm x 80μm
No.1 ~ No.236

(2) 80μm x 50μm
No.237~No.241, No.1006~No.1010

(3) 19μm x 120μm
No.242 ~ No1005

●Au BUMP Pitch：Refer to Coordinate
●Au BUMP height：15μm(typ.)
●Number in the Diagram refers to the number in the Coordinates table

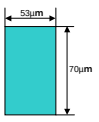
●Alignment Mark
(1-a), (1-b)



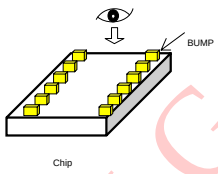
(2-a)

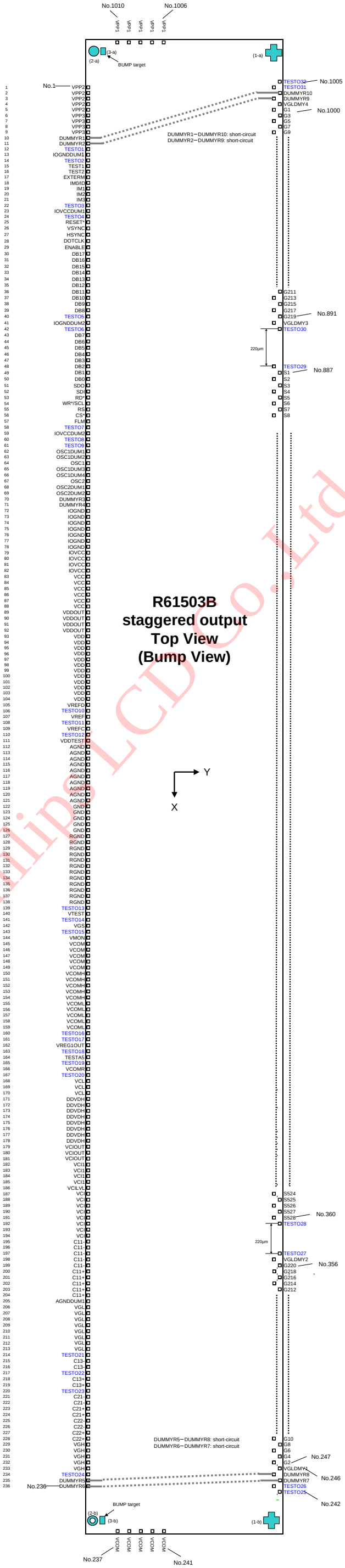
(2-b)

●BUMP Target Cell (3-a)(3-b)



Top View





R61503B staggered output Top View (Bump View)

R61503 PAD coordinates (Unit: μm)

2005.04.08 rev1.0

pad No	pad name	X	Y
1	VPP2	-8225.0	-581.5
2	VPP2	-8155.0	-581.5
3	VPP2	-8085.0	-581.5
4	VPP2	-8015.0	-581.5
5	VPP2	-7945.0	-581.5
6	VPP3	-7875.0	-581.5
7	VPP3	-7805.0	-581.5
8	VPP3	-7735.0	-581.5
9	VPP3	-7665.0	-581.5
10	DUMMYR1	-7595.0	-581.5
11	DUMMYR2	-7525.0	-581.5
12	TESTO1	-7455.0	-581.5
13	IOGNDDUM1	-7385.0	-581.5
14	TESTO2	-7315.0	-581.5
15	TEST1	-7245.0	-581.5
16	TEST2	-7175.0	-581.5
17	EXTERM	-7105.0	-581.5
18	IM0/ID	-7035.0	-581.5
19	IM1	-6965.0	-581.5
20	IM2	-6895.0	-581.5
21	IM3	-6825.0	-581.5
22	TESTO3	-6755.0	-581.5
23	IOVCCDUM1	-6685.0	-581.5
24	TESTO4	-6615.0	-581.5
25	RESET*	-6545.0	-581.5
26	VSYNC	-6475.0	-581.5
27	HSYNC	-6405.0	-581.5
28	DOTCLK	-6335.0	-581.5
29	ENABLE	-6265.0	-581.5
30	DB17	-6195.0	-581.5
31	DB16	-6125.0	-581.5
32	DB15	-6055.0	-581.5
33	DB14	-5985.0	-581.5
34	DB13	-5915.0	-581.5
35	DB12	-5845.0	-581.5
36	DB11	-5775.0	-581.5
37	DB10	-5705.0	-581.5
38	DB9	-5635.0	-581.5
39	DB8	-5565.0	-581.5
40	TESTO5	-5495.0	-581.5
41	IOGNDDUM2	-5425.0	-581.5
42	TESTO6	-5355.0	-581.5
43	DB7	-5285.0	-581.5
44	DB6	-5215.0	-581.5
45	DB5	-5145.0	-581.5
46	DB4	-5075.0	-581.5
47	DB3	-5005.0	-581.5
48	DB2	-4935.0	-581.5
49	DB1	-4865.0	-581.5
50	DB0	-4795.0	-581.5

pad No	pad name	X	Y
51	SDO	-4725.0	-581.5
52	SDI	-4655.0	-581.5
53	RD*	-4585.0	-581.5
54	WR*/SCL	-4515.0	-581.5
55	RS	-4445.0	-581.5
56	CS*	-4375.0	-581.5
57	FLM	-4305.0	-581.5
58	TESTO7	-4235.0	-581.5
59	IOVCCDUM2	-4165.0	-581.5
60	TESTO8	-4095.0	-581.5
61	TESTO9	-4025.0	-581.5
62	OSC1DUM1	-3955.0	-581.5
63	OSC1DUM2	-3885.0	-581.5
64	OSC1	-3815.0	-581.5
65	OSC1DUM3	-3745.0	-581.5
66	OSC1DUM4	-3675.0	-581.5
67	OSC2	-3605.0	-581.5
68	OSC2DUM1	-3535.0	-581.5
69	OSC2DUM2	-3465.0	-581.5
70	DUMMYR3	-3395.0	-581.5
71	DUMMYR4	-3325.0	-581.5
72	IOGND	-3255.0	-581.5
73	IOGND	-3185.0	-581.5
74	IOGND	-3115.0	-581.5
75	IOGND	-3045.0	-581.5
76	IOGND	-2975.0	-581.5
77	IOGND	-2905.0	-581.5
78	IOGND	-2835.0	-581.5
79	IOVCC	-2765.0	-581.5
80	IOVCC	-2695.0	-581.5
81	IOVCC	-2625.0	-581.5
82	IOVCC	-2555.0	-581.5
83	VCC	-2485.0	-581.5
84	VCC	-2415.0	-581.5
85	VCC	-2345.0	-581.5
86	VCC	-2275.0	-581.5
87	VCC	-2205.0	-581.5
88	VCC	-2135.0	-581.5
89	VDDOUT	-2065.0	-581.5
90	VDDOUT	-1995.0	-581.5
91	VDDOUT	-1925.0	-581.5
92	VDDOUT	-1855.0	-581.5
93	VDD	-1785.0	-581.5
94	VDD	-1715.0	-581.5
95	VDD	-1645.0	-581.5
96	VDD	-1575.0	-581.5
97	VDD	-1505.0	-581.5
98	VDD	-1435.0	-581.5
99	VDD	-1365.0	-581.5
100	VDD	-1295.0	-581.5

R61503 PAD coordinates (Unit: μm)

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pad No	pad name	X	Y
101	VDD	-1225.0	-581.5
102	VDD	-1155.0	-581.5
103	VDD	-1085.0	-581.5
104	VDD	-1015.0	-581.5
105	VREFD	-945.0	-581.5
106	TESTO10	-875.0	-581.5
107	VREF	-805.0	-581.5
108	TESTO11	-735.0	-581.5
109	VREFC	-665.0	-581.5
110	TESTO12	-595.0	-581.5
111	VDDTEST	-525.0	-581.5
112	AGND	-455.0	-581.5
113	AGND	-385.0	-581.5
114	AGND	-315.0	-581.5
115	AGND	-245.0	-581.5
116	AGND	-175.0	-581.5
117	AGND	-105.0	-581.5
118	AGND	-35.0	-581.5
119	AGND	35.0	-581.5
120	AGND	105.0	-581.5
121	AGND	175.0	-581.5
122	GND	245.0	-581.5
123	GND	315.0	-581.5
124	GND	385.0	-581.5
125	GND	455.0	-581.5
126	GND	525.0	-581.5
127	RGND	595.0	-581.5
128	RGND	665.0	-581.5
129	RGND	735.0	-581.5
130	RGND	805.0	-581.5
131	RGND	875.0	-581.5
132	RGND	945.0	-581.5
133	RGND	1015.0	-581.5
134	RGND	1085.0	-581.5
135	RGND	1155.0	-581.5
136	RGND	1225.0	-581.5
137	RGND	1295.0	-581.5
138	RGND	1365.0	-581.5
139	TESTO13	1435.0	-581.5
140	VTEST	1505.0	-581.5
141	TESTO14	1575.0	-581.5
142	VGS	1645.0	-581.5
143	TESTO15	1715.0	-581.5
144	VMON	1785.0	-581.5
145	VCOM	1855.0	-581.5
146	VCOM	1925.0	-581.5
147	VCOM	1995.0	-581.5
148	VCOM	2065.0	-581.5
149	VCOM	2135.0	-581.5
150	VCOMH	2205.0	-581.5

pad No	pad name	X	Y
151	VCOMH	2275.0	-581.5
152	VCOMH	2345.0	-581.5
153	VCOMH	2415.0	-581.5
154	VCOMH	2485.0	-581.5
155	VCOML	2555.0	-581.5
156	VCOML	2625.0	-581.5
157	VCOML	2695.0	-581.5
158	VCOML	2765.0	-581.5
159	VCOML	2835.0	-581.5
160	TESTO16	2905.0	-581.5
161	TESTO17	2975.0	-581.5
162	VREG1OUT	3045.0	-581.5
163	TESTO18	3115.0	-581.5
164	TESTA5	3185.0	-581.5
165	TESTO19	3255.0	-581.5
166	VCOMR	3325.0	-581.5
167	TESTO20	3395.0	-581.5
168	VCL	3465.0	-581.5
169	VCL	3535.0	-581.5
170	VCL	3605.0	-581.5
171	DDVDH	3675.0	-581.5
172	DDVDH	3745.0	-581.5
173	DDVDH	3815.0	-581.5
174	DDVDH	3885.0	-581.5
175	DDVDH	3955.0	-581.5
176	DDVDH	4025.0	-581.5
177	DDVDH	4095.0	-581.5
178	DDVDH	4165.0	-581.5
179	VCIOUT	4235.0	-581.5
180	VCIOUT	4305.0	-581.5
181	VCIOUT	4375.0	-581.5
182	VCI1	4445.0	-581.5
183	VCI1	4515.0	-581.5
184	VCI1	4585.0	-581.5
185	VCI1	4655.0	-581.5
186	VCILVL	4725.0	-581.5
187	VCI	4795.0	-581.5
188	VCI	4865.0	-581.5
189	VCI	4935.0	-581.5
190	VCI	5005.0	-581.5
191	VCI	5075.0	-581.5
192	VCI	5145.0	-581.5
193	VCI	5215.0	-581.5
194	VCI	5285.0	-581.5
195	C11-	5355.0	-581.5
196	C11-	5425.0	-581.5
197	C11-	5495.0	-581.5
198	C11-	5565.0	-581.5
199	C11-	5635.0	-581.5
200	C11+	5705.0	-581.5

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pad No	pad name	X	Y
201	C11+	5775.0	-581.5
202	C11+	5845.0	-581.5
203	C11+	5915.0	-581.5
204	C11+	5985.0	-581.5
205	AGNDDUM1	6055.0	-581.5
206	VGL	6125.0	-581.5
207	VGL	6195.0	-581.5
208	VGL	6265.0	-581.5
209	VGL	6335.0	-581.5
210	VGL	6405.0	-581.5
211	VGL	6475.0	-581.5
212	VGL	6545.0	-581.5
213	VGL	6615.0	-581.5
214	TESTO21	6685.0	-581.5
215	C13-	6755.0	-581.5
216	C13-	6825.0	-581.5
217	TESTO22	6895.0	-581.5
218	C13+	6965.0	-581.5
219	C13+	7035.0	-581.5
220	TESTO23	7105.0	-581.5
221	C21-	7175.0	-581.5
222	C21-	7245.0	-581.5
223	C21+	7315.0	-581.5
224	C21+	7385.0	-581.5
225	C22-	7455.0	-581.5
226	C22-	7525.0	-581.5
227	C22+	7595.0	-581.5
228	C22+	7665.0	-581.5
229	VGH	7735.0	-581.5
230	VGH	7805.0	-581.5
231	VGH	7875.0	-581.5
232	VGH	7945.0	-581.5
233	VGH	8015.0	-581.5
234	TESTO24	8085.0	-581.5
235	DUMMYR5	8155.0	-581.5
236	DUMMYR6	8225.0	-581.5
237	VCOM	8466.5	-410.7
238	VCOM	8466.5	-340.7
239	VCOM	8466.5	-270.7
240	VCOM	8466.5	-200.7
241	VCOM	8466.5	-130.7
242	TESTO25	8210.5	566.5
243	TESTO26	8189.5	411.5
244	DUMMYR7	8168.5	566.5
245	DUMMYR8	8147.5	411.5
246	VGLDMY1	8126.5	566.5
247	G2	8105.5	411.5
248	G4	8084.5	566.5
249	G6	8063.5	411.5
250	G8	8042.5	566.5

pad No	pad name	X	Y
251	G10	8021.5	411.5
252	G12	8000.5	566.5
253	G14	7979.5	411.5
254	G16	7958.5	566.5
255	G18	7937.5	411.5
256	G20	7916.5	566.5
257	G22	7895.5	411.5
258	G24	7874.5	566.5
259	G26	7853.5	411.5
260	G28	7832.5	566.5
261	G30	7811.5	411.5
262	G32	7790.5	566.5
263	G34	7769.5	411.5
264	G36	7748.5	566.5
265	G38	7727.5	411.5
266	G40	7706.5	566.5
267	G42	7685.5	411.5
268	G44	7664.5	566.5
269	G46	7643.5	411.5
270	G48	7622.5	566.5
271	G50	7601.5	411.5
272	G52	7580.5	566.5
273	G54	7559.5	411.5
274	G56	7538.5	566.5
275	G58	7517.5	411.5
276	G60	7496.5	566.5
277	G62	7475.5	411.5
278	G64	7454.5	566.5
279	G66	7433.5	411.5
280	G68	7412.5	566.5
281	G70	7391.5	411.5
282	G72	7370.5	566.5
283	G74	7349.5	411.5
284	G76	7328.5	566.5
285	G78	7307.5	411.5
286	G80	7286.5	566.5
287	G82	7265.5	411.5
288	G84	7244.5	566.5
289	G86	7223.5	411.5
290	G88	7202.5	566.5
291	G90	7181.5	411.5
292	G92	7160.5	566.5
293	G94	7139.5	411.5
294	G96	7118.5	566.5
295	G98	7097.5	411.5
296	G100	7076.5	566.5
297	G102	7055.5	411.5
298	G104	7034.5	566.5
299	G106	7013.5	411.5
300	G108	6992.5	566.5

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pad No	pad name	X	Y
301	G110	6971.5	411.5
302	G112	6950.5	566.5
303	G114	6929.5	411.5
304	G116	6908.5	566.5
305	G118	6887.5	411.5
306	G120	6866.5	566.5
307	G122	6845.5	411.5
308	G124	6824.5	566.5
309	G126	6803.5	411.5
310	G128	6782.5	566.5
311	G130	6761.5	411.5
312	G132	6740.5	566.5
313	G134	6719.5	411.5
314	G136	6698.5	566.5
315	G138	6677.5	411.5
316	G140	6656.5	566.5
317	G142	6635.5	411.5
318	G144	6614.5	566.5
319	G146	6593.5	411.5
320	G148	6572.5	566.5
321	G150	6551.5	411.5
322	G152	6530.5	566.5
323	G154	6509.5	411.5
324	G156	6488.5	566.5
325	G158	6467.5	411.5
326	G160	6446.5	566.5
327	G162	6425.5	411.5
328	G164	6404.5	566.5
329	G166	6383.5	411.5
330	G168	6362.5	566.5
331	G170	6341.5	411.5
332	G172	6320.5	566.5
333	G174	6299.5	411.5
334	G176	6278.5	566.5
335	G178	6257.5	411.5
336	G180	6236.5	566.5
337	G182	6215.5	411.5
338	G184	6194.5	566.5
339	G186	6173.5	411.5
340	G188	6152.5	566.5
341	G190	6131.5	411.5
342	G192	6110.5	566.5
343	G194	6089.5	411.5
344	G196	6068.5	566.5
345	G198	6047.5	411.5
346	G200	6026.5	566.5
347	G202	6005.5	411.5
348	G204	5984.5	566.5
349	G206	5963.5	411.5
350	G208	5942.5	566.5

pad No	pad name	X	Y
351	G210	5921.5	411.5
352	G212	5900.5	566.5
353	G214	5879.5	411.5
354	G216	5858.5	566.5
355	G218	5837.5	411.5
356	G220	5816.5	566.5
357	VGLDMY2	5795.5	411.5
358	TESTO27	5774.5	566.5
359	TESTO28	5554.5	566.5
360	S528	5533.5	411.5
361	S527	5512.5	566.5
362	S526	5491.5	411.5
363	S525	5470.5	566.5
364	S524	5449.5	411.5
365	S523	5428.5	566.5
366	S522	5407.5	411.5
367	S521	5386.5	566.5
368	S520	5365.5	411.5
369	S519	5344.5	566.5
370	S518	5323.5	411.5
371	S517	5302.5	566.5
372	S516	5281.5	411.5
373	S515	5260.5	566.5
374	S514	5239.5	411.5
375	S513	5218.5	566.5
376	S512	5197.5	411.5
377	S511	5176.5	566.5
378	S510	5155.5	411.5
379	S509	5134.5	566.5
380	S508	5113.5	411.5
381	S507	5092.5	566.5
382	S506	5071.5	411.5
383	S505	5050.5	566.5
384	S504	5029.5	411.5
385	S503	5008.5	566.5
386	S502	4987.5	411.5
387	S501	4966.5	566.5
388	S500	4945.5	411.5
389	S499	4924.5	566.5
390	S498	4903.5	411.5
391	S497	4882.5	566.5
392	S496	4861.5	411.5
393	S495	4840.5	566.5
394	S494	4819.5	411.5
395	S493	4798.5	566.5
396	S492	4777.5	411.5
397	S491	4756.5	566.5
398	S490	4735.5	411.5
399	S489	4714.5	566.5
400	S488	4693.5	411.5

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pad No	pad name	X	Y
401	S487	4672.5	566.5
402	S486	4651.5	411.5
403	S485	4630.5	566.5
404	S484	4609.5	411.5
405	S483	4588.5	566.5
406	S482	4567.5	411.5
407	S481	4546.5	566.5
408	S480	4525.5	411.5
409	S479	4504.5	566.5
410	S478	4483.5	411.5
411	S477	4462.5	566.5
412	S476	4441.5	411.5
413	S475	4420.5	566.5
414	S474	4399.5	411.5
415	S473	4378.5	566.5
416	S472	4357.5	411.5
417	S471	4336.5	566.5
418	S470	4315.5	411.5
419	S469	4294.5	566.5
420	S468	4273.5	411.5
421	S467	4252.5	566.5
422	S466	4231.5	411.5
423	S465	4210.5	566.5
424	S464	4189.5	411.5
425	S463	4168.5	566.5
426	S462	4147.5	411.5
427	S461	4126.5	566.5
428	S460	4105.5	411.5
429	S459	4084.5	566.5
430	S458	4063.5	411.5
431	S457	4042.5	566.5
432	S456	4021.5	411.5
433	S455	4000.5	566.5
434	S454	3979.5	411.5
435	S453	3958.5	566.5
436	S452	3937.5	411.5
437	S451	3916.5	566.5
438	S450	3895.5	411.5
439	S449	3874.5	566.5
440	S448	3853.5	411.5
441	S447	3832.5	566.5
442	S446	3811.5	411.5
443	S445	3790.5	566.5
444	S444	3769.5	411.5
445	S443	3748.5	566.5
446	S442	3727.5	411.5
447	S441	3706.5	566.5
448	S440	3685.5	411.5
449	S439	3664.5	566.5
450	S438	3643.5	411.5

pad No	pad name	X	Y
451	S437	3622.5	566.5
452	S436	3601.5	411.5
453	S435	3580.5	566.5
454	S434	3559.5	411.5
455	S433	3538.5	566.5
456	S432	3517.5	411.5
457	S431	3496.5	566.5
458	S430	3475.5	411.5
459	S429	3454.5	566.5
460	S428	3433.5	411.5
461	S427	3412.5	566.5
462	S426	3391.5	411.5
463	S425	3370.5	566.5
464	S424	3349.5	411.5
465	S423	3328.5	566.5
466	S422	3307.5	411.5
467	S421	3286.5	566.5
468	S420	3265.5	411.5
469	S419	3244.5	566.5
470	S418	3223.5	411.5
471	S417	3202.5	566.5
472	S416	3181.5	411.5
473	S415	3160.5	566.5
474	S414	3139.5	411.5
475	S413	3118.5	566.5
476	S412	3097.5	411.5
477	S411	3076.5	566.5
478	S410	3055.5	411.5
479	S409	3034.5	566.5
480	S408	3013.5	411.5
481	S407	2992.5	566.5
482	S406	2971.5	411.5
483	S405	2950.5	566.5
484	S404	2929.5	411.5
485	S403	2908.5	566.5
486	S402	2887.5	411.5
487	S401	2866.5	566.5
488	S400	2845.5	411.5
489	S399	2824.5	566.5
490	S398	2803.5	411.5
491	S397	2782.5	566.5
492	S396	2761.5	411.5
493	S395	2740.5	566.5
494	S394	2719.5	411.5
495	S393	2698.5	566.5
496	S392	2677.5	411.5
497	S391	2656.5	566.5
498	S390	2635.5	411.5
499	S389	2614.5	566.5
500	S388	2593.5	411.5

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pad No	pad name	X	Y
501	S387	2572.5	566.5
502	S386	2551.5	411.5
503	S385	2530.5	566.5
504	S384	2509.5	411.5
505	S383	2488.5	566.5
506	S382	2467.5	411.5
507	S381	2446.5	566.5
508	S380	2425.5	411.5
509	S379	2404.5	566.5
510	S378	2383.5	411.5
511	S377	2362.5	566.5
512	S376	2341.5	411.5
513	S375	2320.5	566.5
514	S374	2299.5	411.5
515	S373	2278.5	566.5
516	S372	2257.5	411.5
517	S371	2236.5	566.5
518	S370	2215.5	411.5
519	S369	2194.5	566.5
520	S368	2173.5	411.5
521	S367	2152.5	566.5
522	S366	2131.5	411.5
523	S365	2110.5	566.5
524	S364	2089.5	411.5
525	S363	2068.5	566.5
526	S362	2047.5	411.5
527	S361	2026.5	566.5
528	S360	2005.5	411.5
529	S359	1984.5	566.5
530	S358	1963.5	411.5
531	S357	1942.5	566.5
532	S356	1921.5	411.5
533	S355	1900.5	566.5
534	S354	1879.5	411.5
535	S353	1858.5	566.5
536	S352	1837.5	411.5
537	S351	1816.5	566.5
538	S350	1795.5	411.5
539	S349	1774.5	566.5
540	S348	1753.5	411.5
541	S347	1732.5	566.5
542	S346	1711.5	411.5
543	S345	1690.5	566.5
544	S344	1669.5	411.5
545	S343	1648.5	566.5
546	S342	1627.5	411.5
547	S341	1606.5	566.5
548	S340	1585.5	411.5
549	S339	1564.5	566.5
550	S338	1543.5	411.5

pad No	pad name	X	Y
551	S337	1522.5	566.5
552	S336	1501.5	411.5
553	S335	1480.5	566.5
554	S334	1459.5	411.5
555	S333	1438.5	566.5
556	S332	1417.5	411.5
557	S331	1396.5	566.5
558	S330	1375.5	411.5
559	S329	1354.5	566.5
560	S328	1333.5	411.5
561	S327	1312.5	566.5
562	S326	1291.5	411.5
563	S325	1270.5	566.5
564	S324	1249.5	411.5
565	S323	1228.5	566.5
566	S322	1207.5	411.5
567	S321	1186.5	566.5
568	S320	1165.5	411.5
569	S319	1144.5	566.5
570	S318	1123.5	411.5
571	S317	1102.5	566.5
572	S316	1081.5	411.5
573	S315	1060.5	566.5
574	S314	1039.5	411.5
575	S313	1018.5	566.5
576	S312	997.5	411.5
577	S311	976.5	566.5
578	S310	955.5	411.5
579	S309	934.5	566.5
580	S308	913.5	411.5
581	S307	892.5	566.5
582	S306	871.5	411.5
583	S305	850.5	566.5
584	S304	829.5	411.5
585	S303	808.5	566.5
586	S302	787.5	411.5
587	S301	766.5	566.5
588	S300	745.5	411.5
589	S299	724.5	566.5
590	S298	703.5	411.5
591	S297	682.5	566.5
592	S296	661.5	411.5
593	S295	640.5	566.5
594	S294	619.5	411.5
595	S293	598.5	566.5
596	S292	577.5	411.5
597	S291	556.5	566.5
598	S290	535.5	411.5
599	S289	514.5	566.5
600	S288	493.5	411.5

R61503 PAD coordinates (Unit: μm)

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pad No	pad name	X	Y
601	S287	472.5	566.5
602	S286	451.5	411.5
603	S285	430.5	566.5
604	S284	409.5	411.5
605	S283	388.5	566.5
606	S282	367.5	411.5
607	S281	346.5	566.5
608	S280	325.5	411.5
609	S279	304.5	566.5
610	S278	283.5	411.5
611	S277	262.5	566.5
612	S276	241.5	411.5
613	S275	220.5	566.5
614	S274	199.5	411.5
615	S273	178.5	566.5
616	S272	157.5	411.5
617	S271	136.5	566.5
618	S270	115.5	411.5
619	S269	94.5	566.5
620	S268	73.5	411.5
621	S267	52.5	566.5
622	S266	31.5	411.5
623	S265	10.5	566.5
624	S264	-10.5	411.5
625	S263	-31.5	566.5
626	S262	-52.5	411.5
627	S261	-73.5	566.5
628	S260	-94.5	411.5
629	S259	-115.5	566.5
630	S258	-136.5	411.5
631	S257	-157.5	566.5
632	S256	-178.5	411.5
633	S255	-199.5	566.5
634	S254	-220.5	411.5
635	S253	-241.5	566.5
636	S252	-262.5	411.5
637	S251	-283.5	566.5
638	S250	-304.5	411.5
639	S249	-325.5	566.5
640	S248	-346.5	411.5
641	S247	-367.5	566.5
642	S246	-388.5	411.5
643	S245	-409.5	566.5
644	S244	-430.5	411.5
645	S243	-451.5	566.5
646	S242	-472.5	411.5
647	S241	-493.5	566.5
648	S240	-514.5	411.5
649	S239	-535.5	566.5
650	S238	-556.5	411.5

pad No	pad name	X	Y
651	S237	-577.5	566.5
652	S236	-598.5	411.5
653	S235	-619.5	566.5
654	S234	-640.5	411.5
655	S233	-661.5	566.5
656	S232	-682.5	411.5
657	S231	-703.5	566.5
658	S230	-724.5	411.5
659	S229	-745.5	566.5
660	S228	-766.5	411.5
661	S227	-787.5	566.5
662	S226	-808.5	411.5
663	S225	-829.5	566.5
664	S224	-850.5	411.5
665	S223	-871.5	566.5
666	S222	-892.5	411.5
667	S221	-913.5	566.5
668	S220	-934.5	411.5
669	S219	-955.5	566.5
670	S218	-976.5	411.5
671	S217	-997.5	566.5
672	S216	-1018.5	411.5
673	S215	-1039.5	566.5
674	S214	-1060.5	411.5
675	S213	-1081.5	566.5
676	S212	-1102.5	411.5
677	S211	-1123.5	566.5
678	S210	-1144.5	411.5
679	S209	-1165.5	566.5
680	S208	-1186.5	411.5
681	S207	-1207.5	566.5
682	S206	-1228.5	411.5
683	S205	-1249.5	566.5
684	S204	-1270.5	411.5
685	S203	-1291.5	566.5
686	S202	-1312.5	411.5
687	S201	-1333.5	566.5
688	S200	-1354.5	411.5
689	S199	-1375.5	566.5
690	S198	-1396.5	411.5
691	S197	-1417.5	566.5
692	S196	-1438.5	411.5
693	S195	-1459.5	566.5
694	S194	-1480.5	411.5
695	S193	-1501.5	566.5
696	S192	-1522.5	411.5
697	S191	-1543.5	566.5
698	S190	-1564.5	411.5
699	S189	-1585.5	566.5
700	S188	-1606.5	411.5

R61503 PAD coordinates (Unit: μm)

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pad No	pad name	X	Y
701	S187	-1627.5	566.5
702	S186	-1648.5	411.5
703	S185	-1669.5	566.5
704	S184	-1690.5	411.5
705	S183	-1711.5	566.5
706	S182	-1732.5	411.5
707	S181	-1753.5	566.5
708	S180	-1774.5	411.5
709	S179	-1795.5	566.5
710	S178	-1816.5	411.5
711	S177	-1837.5	566.5
712	S176	-1858.5	411.5
713	S175	-1879.5	566.5
714	S174	-1900.5	411.5
715	S173	-1921.5	566.5
716	S172	-1942.5	411.5
717	S171	-1963.5	566.5
718	S170	-1984.5	411.5
719	S169	-2005.5	566.5
720	S168	-2026.5	411.5
721	S167	-2047.5	566.5
722	S166	-2068.5	411.5
723	S165	-2089.5	566.5
724	S164	-2110.5	411.5
725	S163	-2131.5	566.5
726	S162	-2152.5	411.5
727	S161	-2173.5	566.5
728	S160	-2194.5	411.5
729	S159	-2215.5	566.5
730	S158	-2236.5	411.5
731	S157	-2257.5	566.5
732	S156	-2278.5	411.5
733	S155	-2299.5	566.5
734	S154	-2320.5	411.5
735	S153	-2341.5	566.5
736	S152	-2362.5	411.5
737	S151	-2383.5	566.5
738	S150	-2404.5	411.5
739	S149	-2425.5	566.5
740	S148	-2446.5	411.5
741	S147	-2467.5	566.5
742	S146	-2488.5	411.5
743	S145	-2509.5	566.5
744	S144	-2530.5	411.5
745	S143	-2551.5	566.5
746	S142	-2572.5	411.5
747	S141	-2593.5	566.5
748	S140	-2614.5	411.5
749	S139	-2635.5	566.5
750	S138	-2656.5	411.5

pad No	pad name	X	Y
751	S137	-2677.5	566.5
752	S136	-2698.5	411.5
753	S135	-2719.5	566.5
754	S134	-2740.5	411.5
755	S133	-2761.5	566.5
756	S132	-2782.5	411.5
757	S131	-2803.5	566.5
758	S130	-2824.5	411.5
759	S129	-2845.5	566.5
760	S128	-2866.5	411.5
761	S127	-2887.5	566.5
762	S126	-2908.5	411.5
763	S125	-2929.5	566.5
764	S124	-2950.5	411.5
765	S123	-2971.5	566.5
766	S122	-2992.5	411.5
767	S121	-3013.5	566.5
768	S120	-3034.5	411.5
769	S119	-3055.5	566.5
770	S118	-3076.5	411.5
771	S117	-3097.5	566.5
772	S116	-3118.5	411.5
773	S115	-3139.5	566.5
774	S114	-3160.5	411.5
775	S113	-3181.5	566.5
776	S112	-3202.5	411.5
777	S111	-3223.5	566.5
778	S110	-3244.5	411.5
779	S109	-3265.5	566.5
780	S108	-3286.5	411.5
781	S107	-3307.5	566.5
782	S106	-3328.5	411.5
783	S105	-3349.5	566.5
784	S104	-3370.5	411.5
785	S103	-3391.5	566.5
786	S102	-3412.5	411.5
787	S101	-3433.5	566.5
788	S100	-3454.5	411.5
789	S99	-3475.5	566.5
790	S98	-3496.5	411.5
791	S97	-3517.5	566.5
792	S96	-3538.5	411.5
793	S95	-3559.5	566.5
794	S94	-3580.5	411.5
795	S93	-3601.5	566.5
796	S92	-3622.5	411.5
797	S91	-3643.5	566.5
798	S90	-3664.5	411.5
799	S89	-3685.5	566.5
800	S88	-3706.5	411.5

R61503 PAD coordinates (Unit: μm)

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pad No	pad name	X	Y
801	S87	-3727.5	566.5
802	S86	-3748.5	411.5
803	S85	-3769.5	566.5
804	S84	-3790.5	411.5
805	S83	-3811.5	566.5
806	S82	-3832.5	411.5
807	S81	-3853.5	566.5
808	S80	-3874.5	411.5
809	S79	-3895.5	566.5
810	S78	-3916.5	411.5
811	S77	-3937.5	566.5
812	S76	-3958.5	411.5
813	S75	-3979.5	566.5
814	S74	-4000.5	411.5
815	S73	-4021.5	566.5
816	S72	-4042.5	411.5
817	S71	-4063.5	566.5
818	S70	-4084.5	411.5
819	S69	-4105.5	566.5
820	S68	-4126.5	411.5
821	S67	-4147.5	566.5
822	S66	-4168.5	411.5
823	S65	-4189.5	566.5
824	S64	-4210.5	411.5
825	S63	-4231.5	566.5
826	S62	-4252.5	411.5
827	S61	-4273.5	566.5
828	S60	-4294.5	411.5
829	S59	-4315.5	566.5
830	S58	-4336.5	411.5
831	S57	-4357.5	566.5
832	S56	-4378.5	411.5
833	S55	-4399.5	566.5
834	S54	-4420.5	411.5
835	S53	-4441.5	566.5
836	S52	-4462.5	411.5
837	S51	-4483.5	566.5
838	S50	-4504.5	411.5
839	S49	-4525.5	566.5
840	S48	-4546.5	411.5
841	S47	-4567.5	566.5
842	S46	-4588.5	411.5
843	S45	-4609.5	566.5
844	S44	-4630.5	411.5
845	S43	-4651.5	566.5
846	S42	-4672.5	411.5
847	S41	-4693.5	566.5
848	S40	-4714.5	411.5
849	S39	-4735.5	566.5
850	S38	-4756.5	411.5

pad No	pad name	X	Y
851	S37	-4777.5	566.5
852	S36	-4798.5	411.5
853	S35	-4819.5	566.5
854	S34	-4840.5	411.5
855	S33	-4861.5	566.5
856	S32	-4882.5	411.5
857	S31	-4903.5	566.5
858	S30	-4924.5	411.5
859	S29	-4945.5	566.5
860	S28	-4966.5	411.5
861	S27	-4987.5	566.5
862	S26	-5008.5	411.5
863	S25	-5029.5	566.5
864	S24	-5050.5	411.5
865	S23	-5071.5	566.5
866	S22	-5092.5	411.5
867	S21	-5113.5	566.5
868	S20	-5134.5	411.5
869	S19	-5155.5	566.5
870	S18	-5176.5	411.5
871	S17	-5197.5	566.5
872	S16	-5218.5	411.5
873	S15	-5239.5	566.5
874	S14	-5260.5	411.5
875	S13	-5281.5	566.5
876	S12	-5302.5	411.5
877	S11	-5323.5	566.5
878	S10	-5344.5	411.5
879	S9	-5365.5	566.5
880	S8	-5386.5	411.5
881	S7	-5407.5	566.5
882	S6	-5428.5	411.5
883	S5	-5449.5	566.5
884	S4	-5470.5	411.5
885	S3	-5491.5	566.5
886	S2	-5512.5	411.5
887	S1	-5533.5	566.5
888	TESTO29	-5554.5	411.5
889	TESTO30	-5774.5	566.5
890	VGLDMY3	-5795.5	411.5
891	G219	-5816.5	566.5
892	G217	-5837.5	411.5
893	G215	-5858.5	566.5
894	G213	-5879.5	411.5
895	G211	-5900.5	566.5
896	G209	-5921.5	411.5
897	G207	-5942.5	566.5
898	G205	-5963.5	411.5
899	G203	-5984.5	566.5
900	G201	-6005.5	411.5

R61503 PAD coordinates (Unit: μm)

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pad No	pad name	X	Y
901	G199	-6026.5	566.5
902	G197	-6047.5	411.5
903	G195	-6068.5	566.5
904	G193	-6089.5	411.5
905	G191	-6110.5	566.5
906	G189	-6131.5	411.5
907	G187	-6152.5	566.5
908	G185	-6173.5	411.5
909	G183	-6194.5	566.5
910	G181	-6215.5	411.5
911	G179	-6236.5	566.5
912	G177	-6257.5	411.5
913	G175	-6278.5	566.5
914	G173	-6299.5	411.5
915	G171	-6320.5	566.5
916	G169	-6341.5	411.5
917	G167	-6362.5	566.5
918	G165	-6383.5	411.5
919	G163	-6404.5	566.5
920	G161	-6425.5	411.5
921	G159	-6446.5	566.5
922	G157	-6467.5	411.5
923	G155	-6488.5	566.5
924	G153	-6509.5	411.5
925	G151	-6530.5	566.5
926	G149	-6551.5	411.5
927	G147	-6572.5	566.5
928	G145	-6593.5	411.5
929	G143	-6614.5	566.5
930	G141	-6635.5	411.5
931	G139	-6656.5	566.5
932	G137	-6677.5	411.5
933	G135	-6698.5	566.5
934	G133	-6719.5	411.5
935	G131	-6740.5	566.5
936	G129	-6761.5	411.5
937	G127	-6782.5	566.5
938	G125	-6803.5	411.5
939	G123	-6824.5	566.5
940	G121	-6845.5	411.5
941	G119	-6866.5	566.5
942	G117	-6887.5	411.5
943	G115	-6908.5	566.5
944	G113	-6929.5	411.5
945	G111	-6950.5	566.5
946	G109	-6971.5	411.5
947	G107	-6992.5	566.5
948	G105	-7013.5	411.5
949	G103	-7034.5	566.5
950	G101	-7055.5	411.5

pad No	pad name	X	Y
951	G99	-7076.5	566.5
952	G97	-7097.5	411.5
953	G95	-7118.5	566.5
954	G93	-7139.5	411.5
955	G91	-7160.5	566.5
956	G89	-7181.5	411.5
957	G87	-7202.5	566.5
958	G85	-7223.5	411.5
959	G83	-7244.5	566.5
960	G81	-7265.5	411.5
961	G79	-7286.5	566.5
962	G77	-7307.5	411.5
963	G75	-7328.5	566.5
964	G73	-7349.5	411.5
965	G71	-7370.5	566.5
966	G69	-7391.5	411.5
967	G67	-7412.5	566.5
968	G65	-7433.5	411.5
969	G63	-7454.5	566.5
970	G61	-7475.5	411.5
971	G59	-7496.5	566.5
972	G57	-7517.5	411.5
973	G55	-7538.5	566.5
974	G53	-7559.5	411.5
975	G51	-7580.5	566.5
976	G49	-7601.5	411.5
977	G47	-7622.5	566.5
978	G45	-7643.5	411.5
979	G43	-7664.5	566.5
980	G41	-7685.5	411.5
981	G39	-7706.5	566.5
982	G37	-7727.5	411.5
983	G35	-7748.5	566.5
984	G33	-7769.5	411.5
985	G31	-7790.5	566.5
986	G29	-7811.5	411.5
987	G27	-7832.5	566.5
988	G25	-7853.5	411.5
989	G23	-7874.5	566.5
990	G21	-7895.5	411.5
991	G19	-7916.5	566.5
992	G17	-7937.5	411.5
993	G15	-7958.5	566.5
994	G13	-7979.5	411.5
995	G11	-8000.5	566.5
996	G9	-8021.5	411.5
997	G7	-8042.5	566.5
998	G5	-8063.5	411.5
999	G3	-8084.5	566.5
1000	G1	-8105.5	411.5

R61503 PAD coordinates (Unit: µm)

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pad No	pad name	X	Y
1001	VGLDMY4	-8126.5	566.5
1002	DUMMYR9	-8147.5	411.5
1003	DUMMYR10	-8168.5	566.5
1004	TESTO31	-8189.5	411.5
1005	TESTO32	-8210.5	566.5
1006	VPP1	-8466.5	-130.7
1007	VPP1	-8466.5	-200.7
1008	VPP1	-8466.5	-270.7
1009	VPP1	-8466.5	-340.7
1010	VPP1	-8466.5	-410.7

Alignment mark	X	Y
1-a	-8422.0	536.9
1-b	8422.0	536.9
2-a	-8421.5	-581.5
2-b	8421.5	-581.5
3-a	-8421.5	-505.0
3-b	8421.5	-505.0

Bump Arrangement

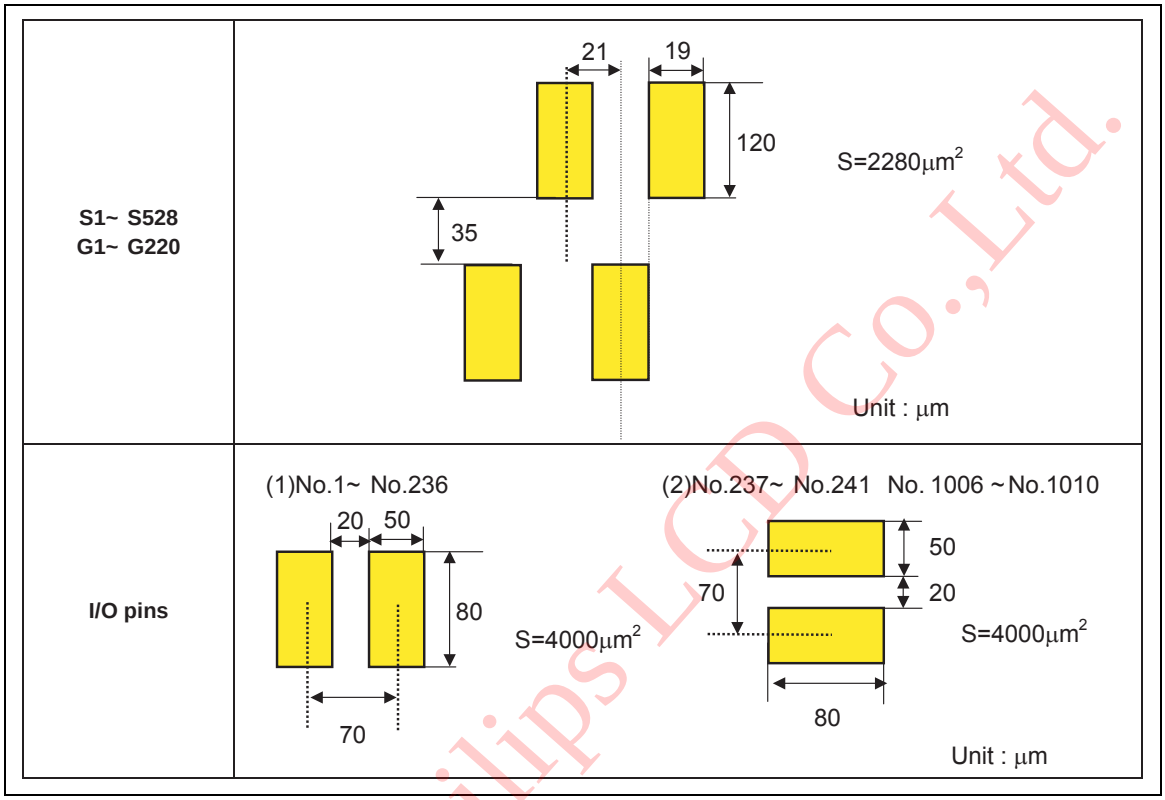


Figure 2

Block Function

1. System Interface

The R61503B supports the following system interfaces: 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The R61503B has 16-bit index register (IR), 18-bit write-data register (WDR), and 18-bit read-data register (RDR). The IR is the register to store index information from control register and the internal GRAM. The WDR is the register to temporarily store the data to be written to the internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via the RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the first read operation from the internal GRAM is performed. Valid data is read out when the second and subsequent read operations are performed.

The instruction execution time except starting oscillation takes 0 clock cycle and instructions can be written consecutively.

Table 9 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

WR*	RD*	RS	Function
0	1	0	Write index to IR
1	0	0	Read internal status
0	1	1	Write to control register/internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 10 Register Selection (clock synchronous serial interface)

Start byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Read internal status
0	1	Write to control register/internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

2. External Display Interface (RGB, VSYNC interfaces)

The R61503B supports RGB interface and VSYNC interface as the moving picture display interface (external display interface). When RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals according to the polarity of the enable signal (ENABLE) to prevent flicker on display while rewriting display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock and VSYNC signal, which is used for frame synchronization. The display data is written to the internal GRAM via system interface but there are restrictions in setting the speed and the method to write data to the internal RAM. For details, see the "External Display Interface" section.

The R61503B allows switching between the external display interface and the system interface by instruction so that the optimal interface is selected for the kind of picture on the panel (still and/or moving picture). The R61503B writes the display data to the internal GRAM to enable transferring data only when the frame data is updated, which contributes to the reduction of data to be transferred from the system and saving power required for the moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the address setting instruction is written in the IR, the address information is sent from the IR to the AC. When the data is written to the internal GRAM, the AC is automatically incremented (plus one) or decremented (minus one). The window address function enables writing data only within the rectangular area specified in GRAM by setting.

4. Graphics RAM (GRAM)

GRAM is graphics RAM, which can store a maximum 87,120-byte (176RGB x 220 (dots) x 18(bits)/8) bit pattern data using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale data in the γ-correction registers to enable a maximum 262k-color display.

6. Timing Generator

The timing generator generates timing signals to operate internal circuits such as GRAM. The R61503B generates timing signals for display operation such as the RAM read operation and for internal operation such as RAM access from MPU and outputs them separately to avoid mutual interference. Also FLM is generated internally and output from the timing generator.

7. Oscillator (OSC)

The R61503B generates the RC oscillation clock signal by connecting an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency can be changed by changing the resistance of the external resistor. Adjust the oscillation frequency according to operating voltage and frame frequency. In deep standby mode, RC oscillation is halted to reduce power consumption. For details, see "Oscillator".

8. Liquid crystal driver Circuit

The liquid crystal driver circuit of the R61503B consists of 528-channel source driver (S1 ~ S528) and 220-channel gate driver (G1 ~ G220). The display pattern data is latched when 528 bits of data are input. The latched data control the source driver and generates liquid crystal drive waveform. The shift direction of 528-bit source output from the source driver is determined by instruction (SS bit). The shift direction of gate output from the gate driver can be changed by setting the GS bit. The gate pin assignment can be changed by setting the SM bit. Sets SM and GS bits to select the optimal scan mode for the module.

9. Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

10. Liquid crystal drive power supply circuit

The liquid crystal drive power supply circuit generates the voltage levels to drive liquid crystal, VREG1OUT, DDVDH, VGL, VGH, Vcom.

GRAM Address MAP

Relation between GRAM addresses and positions on the screen (SS= "0", BGR= "0")

Table 11

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			.....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G220	"0000"H			"0001"H			"0002"H			"0003"H			.....	"00AC"H			"00AD"H			"00AE"H			"00AF"H		
G2	G219	"0100"H			"0101"H			"0102"H			"0103"H			.....	"01AC"H			"01AD"H			"01AE"H			"01AF"H		
G3	G218	"0200"H			"0201"H			"0202"H			"0203"H			.....	"02AC"H			"02AD"H			"02AE"H			"02AF"H		
G4	G217	"0300"H			"0301"H			"0302"H			"0303"H			.....	"03AC"H			"03AD"H			"03AE"H			"03AF"H		
G5	G216	"0400"H			"0401"H			"0402"H			"0403"H			.....	"04AC"H			"04AD"H			"04AE"H			"04AF"H		
G6	G215	"0500"H			"0501"H			"0502"H			"0503"H			.....	"05AC"H			"05AD"H			"05AE"H			"05AF"H		
G7	G214	"0600"H			"0601"H			"0602"H			"0603"H			.....	"06AC"H			"06AD"H			"06AE"H			"06AF"H		
G8	G213	"0700"H			"0701"H			"0702"H			"0703"H			.....	"07AC"H			"07AD"H			"07AE"H			"07AF"H		
G9	G212	"0800"H			"0801"H			"0802"H			"0803"H			.....	"08AC"H			"08AD"H			"08AE"H			"08AF"H		
G10	G211	"0900"H			"0901"H			"0902"H			"0903"H			.....	"09AC"H			"09AD"H			"09AE"H			"09AF"H		
G11	G210	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0AAC"H			"0AAD"H			"0AAE"H			"0AAF"H		
G12	G209	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0BAC"H			"0BAD"H			"0BAE"H			"0BAF"H		
G13	G208	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0CAC"H			"0CAD"H			"0CAE"H			"0CAF"H		
G14	G207	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0DAC"H			"0DAD"H			"0DAE"H			"0DAF"H		
G15	G206	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0EAC"H			"0EAD"H			"0EAE"H			"0EAF"H		
G16	G205	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0FAC"H			"0FAD"H			"0FAE"H			"0FAF"H		
G17	G204	"1000"H			"1001"H			"1002"H			"1003"H			.....	"10AC"H			"10AD"H			"10AE"H			"10AF"H		
G18	G203	"1100"H			"1101"H			"1102"H			"1103"H			.....	"11AC"H			"11AD"H			"11AE"H			"11AF"H		
G19	G202	"1200"H			"1201"H			"1202"H			"1203"H			.....	"12AC"H			"12AD"H			"12AE"H			"12AF"H		
G20	G201	"1300"H			"1301"H			"1302"H			"1303"H			.....	"13AC"H			"13AD"H			"13AE"H			"13AF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G213	G8	"D400"H			"D401"H			"D402"H			"D403"H			.....	"D4AC"H			"D4AD"H			"D4AE"H			"D4AF"H		
G214	G7	"D500"H			"D501"H			"D502"H			"D503"H			.....	"D5AC"H			"D5AD"H			"D5AE"H			"D5AF"H		
G215	G6	"D600"H			"D601"H			"D602"H			"D603"H			.....	"D6AC"H			"D6AD"H			"D6AE"H			"D6AF"H		
G216	G5	"D700"H			"D701"H			"D702"H			"D703"H			.....	"D7AC"H			"D7AD"H			"D7AE"H			"D7AF"H		
G217	G4	"D800"H			"D801"H			"D802"H			"D803"H			.....	"D8AC"H			"D8AD"H			"D8AE"H			"D8AF"H		
G218	G3	"D900"H			"D901"H			"D902"H			"D903"H			.....	"D9AC"H			"D9AD"H			"D9AE"H			"D9AF"H		
G219	G2	"DA00"H			"DA01"H			"DA02"H			"DA03"H			.....	"DAAC"H			"DAAD"H			"DAAE"H			"DAAF"H		
G220	G1	"DB00"H			"DB01"H			"DB02"H			"DB03"H			.....	"DBAC"H			"DBAD"H			"DBAE"H			"DBAF"H		

Relation between GRAM data and Display data (SS= “0”, BGR= “0”)

The following are the interface formats of the R61503B, showing the relationship between the data written in the GRAM and the display data (one pixel) in respective interface operations.

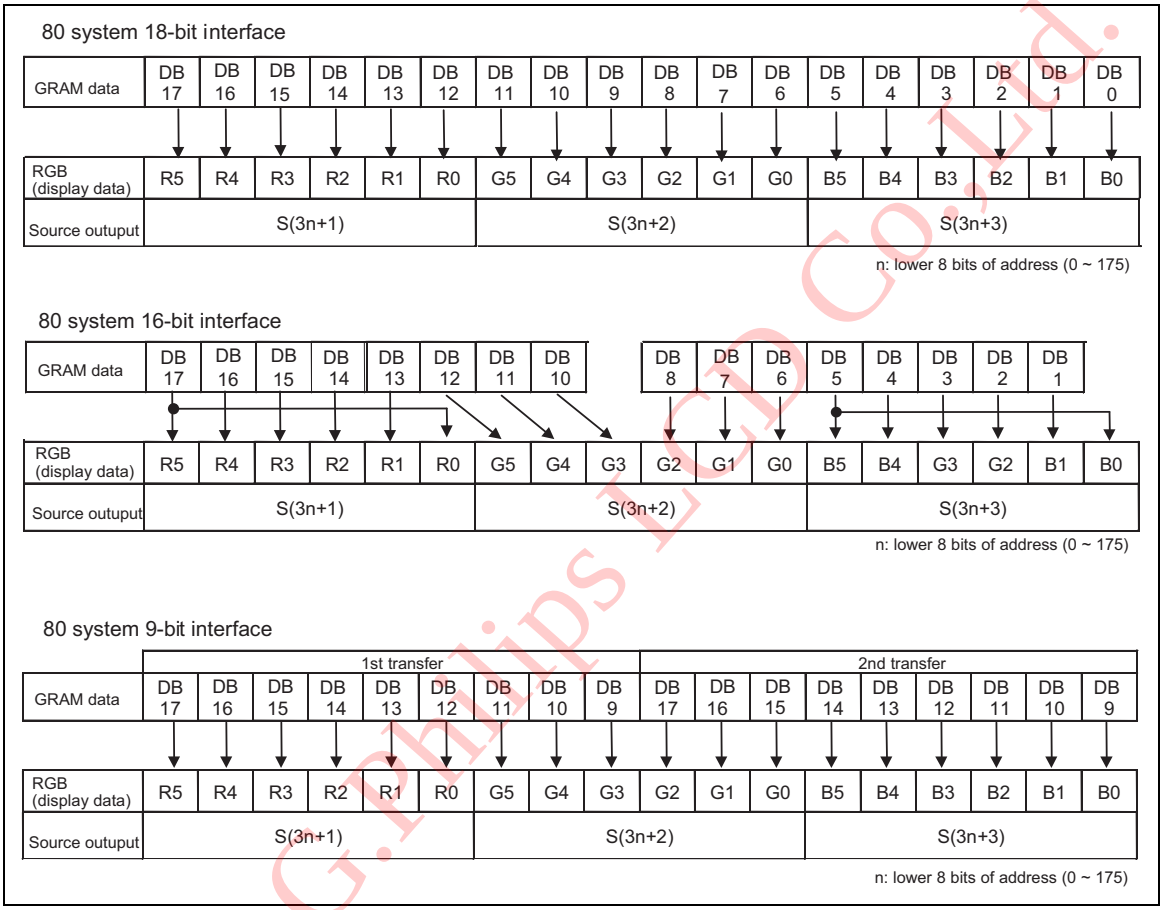


Figure 3 80-system interface (SS = “0”, BGR = “0”)

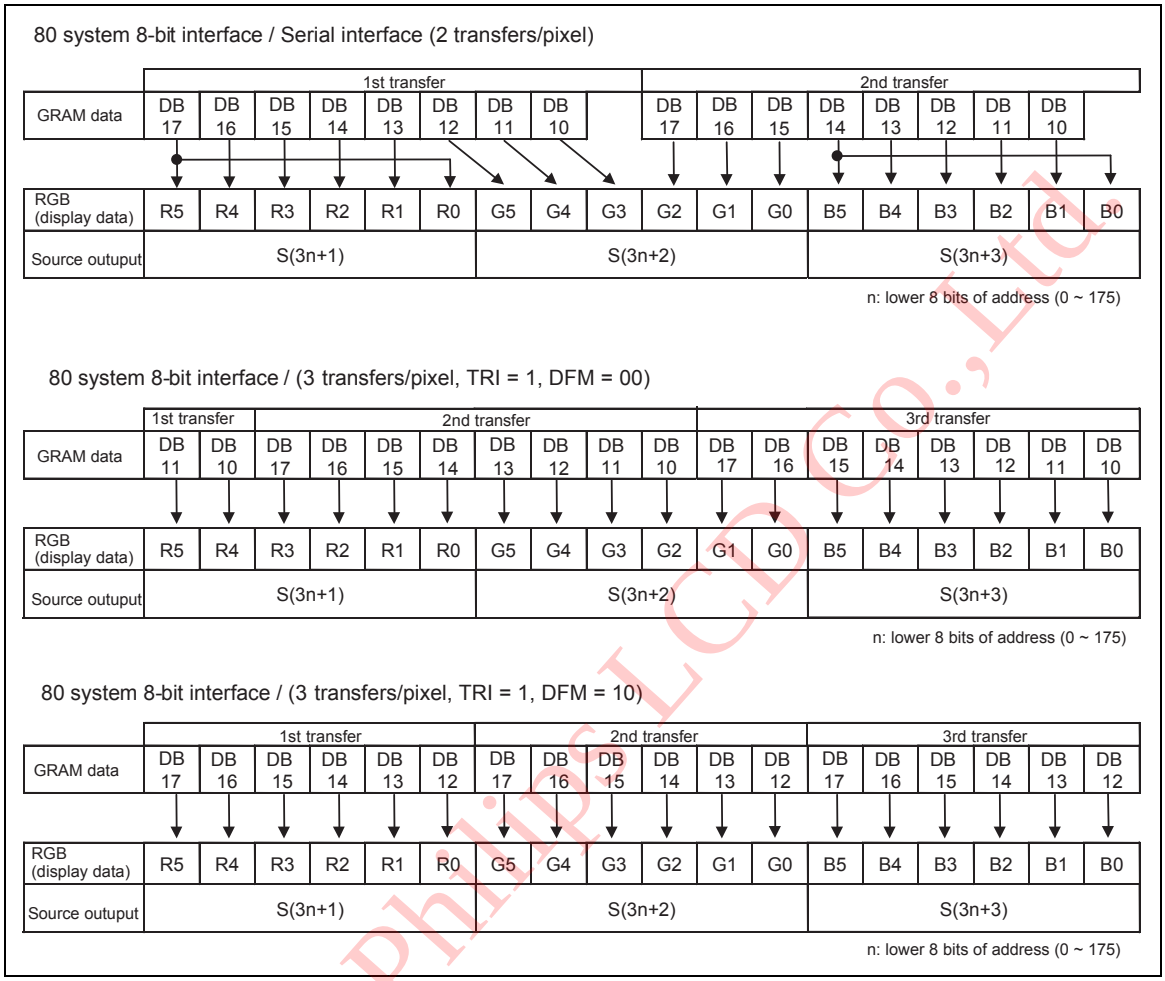


Figure 4 80-system interface (SS = "0", BGR = "0")

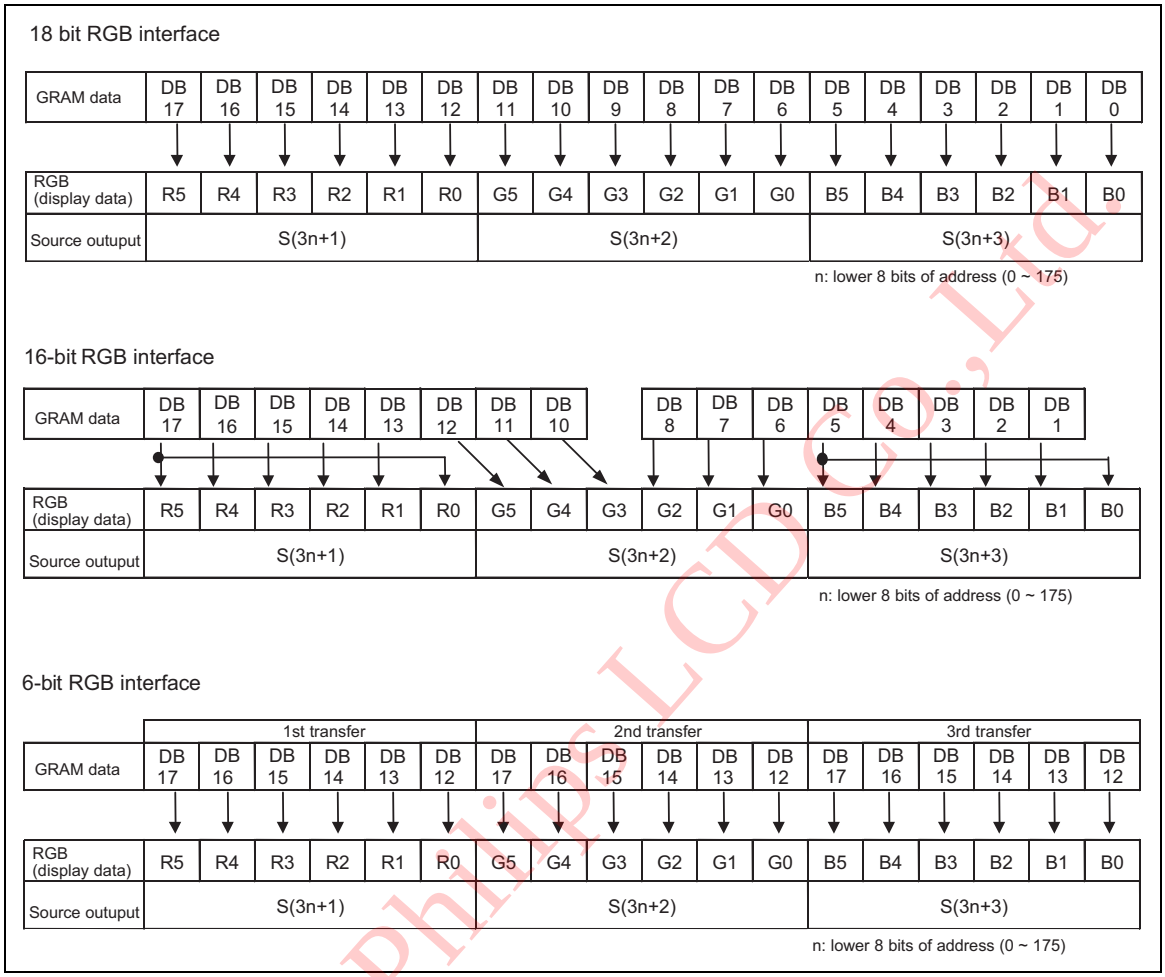


Figure 5 RGB interface (SS = “0”, BGR = “0”)

Relation between GRAM address and position on the screen (SS= “1”, BGR= “1”)

Table 12

S/G pin		S1 S2 S3	S4 S5 S6	S7 S8 S9	S10 S11 S12	.....	S517 S518 S519	S520 S521 S522	S523 S524 S525	S526 S527 S528
GS=0	GS=1	DB17-0	DB17-0	DB17-0	DB17-0	.....	DB17-0	DB17-0	DB17-0	DB17-0
G1	G220	“00AF”H	“00AE”H	“00AD”H	“00AC”H	.....	“0003“H	“0002“H	“0001“H	“0000“H
G2	G219	“01AF”H	“01AE”H	“01AD”H	“01AC”H	.....	“0103“H	“0102“H	“0101“H	“0100“H
G3	G218	“02AF”H	“02AE”H	“02AD”H	“02AC”H	.....	“0203“H	“0202“H	“0201“H	“0200“H
G4	G217	“03AF”H	“03AE”H	“03AD”H	“03AC”H	.....	“0303“H	“0302“H	“0301“H	“0300“H
G5	G216	“04AF”H	“04AE”H	“04AD”H	“04AC”H	.....	“0403“H	“0402“H	“0401“H	“0400“H
G6	G215	“05AF”H	“05AE”H	“05AD”H	“05AC”H	.....	“0503“H	“0502“H	“0501“H	“0500“H
G7	G214	“06AF”H	“06AE”H	“06AD”H	“06AC”H	.....	“0603“H	“0602“H	“0601“H	“0600“H
G8	G213	“07AF”H	“07AE”H	“07AD”H	“07AC”H	.....	“0703“H	“0702“H	“0701“H	“0700“H
G9	G212	“08AF”H	“08AE”H	“08AD”H	“08AC”H	.....	“0803“H	“0802“H	“0801“H	“0800“H
G10	G211	“09AF”H	“09AE”H	“09AD”H	“09AC”H	.....	“0903“H	“0902“H	“0901“H	“0900“H
G11	G210	“0AAF”H	“0AAE”H	“0AAD”H	“0AAC”H	.....	“0A03“H	“0A02“H	“0A01“H	“0A00“H
G12	G209	“0BAF”H	“0BAE”H	“0BAD”H	“0BAC”H	.....	“0B03“H	“0B02“H	“0B01“H	“0B00“H
G13	G208	“0CAF”H	“0CAE”H	“0CAD”H	“0CAC”H	.....	“0C03“H	“0C02“H	“0C01“H	“0C00“H
G14	G207	“0DAF”H	“0DAE”H	“0DAD”H	“0DAC”H	.....	“0D03“H	“0D02“H	“0D01“H	“0D00“H
G15	G206	“0EAF”H	“0EAE”H	“0EAD”H	“0EAC”H	.....	“0E03“H	“0E02“H	“0E01“H	“0E00“H
G16	G205	“0FAF”H	“0FAE”H	“0FAD”H	“0FAC”H	.....	“0F03“H	“0F02“H	“0F01“H	“0F00“H
G17	G204	“10AF”H	“10AE”H	“10AD”H	“10AC”H	.....	“1003“H	“1002“H	“1001“H	“1000“H
G18	G203	“11AF”H	“11AE”H	“11AD”H	“11AC”H	.....	“1103“H	“1102“H	“1101“H	“1100“H
G19	G202	“12AF”H	“12AE”H	“12AD”H	“12AC”H	.....	“1203“H	“1202“H	“1201“H	“1200“H
G20	G201	“13AF”H	“13AE”H	“13AD”H	“13AC”H	.....	“1303“H	“1302“H	“1301“H	“1300“H
:	:	:	:	:	:		:	:	:	:
:	:	:	:	:	:		:	:	:	:
G213	G8	“D4AF”H	“D4AE”H	“D4AD”H	“D4AC”H	.....	“D403“H	“D402“H	“D401“H	“D400“H
G214	G7	“D5AF”H	“D5AE”H	“D5AD”H	“D5AC”H	.....	“D503“H	“D502“H	“D501“H	“D500“H
G215	G6	“D6AF”H	“D6AE”H	“D6AD”H	“D6AC”H	.....	“D603“H	“D602“H	“D601“H	“D600“H
G216	G5	“D7AF”H	“D7AE”H	“D7AD”H	“D7AC”H	.....	“D703“H	“D702“H	“D701“H	“D700“H
G217	G4	“D8AF”H	“D8AE”H	“D8AD”H	“D8AC”H	.....	“D803“H	“D802“H	“D801“H	“D800“H
G218	G3	“D9AF”H	“D9AE”H	“D9AD”H	“D9AC”H	.....	“D903“H	“D902“H	“D901“H	“D900“H
G219	G2	“DAAF”H	“DAAE”H	“DAAD”H	“DAAC”H	.....	“DA03“H	“DA02“H	“DA01“H	“DA00“H
G220	G1	“DBAF”H	“DBAE”H	“DBAD”H	“DBAC”H	.....	“DB03“H	“DB02“H	“DB01“H	“DB00“H

Relation between GRAM data and Display data (SS= “1”, BGR= “1”)

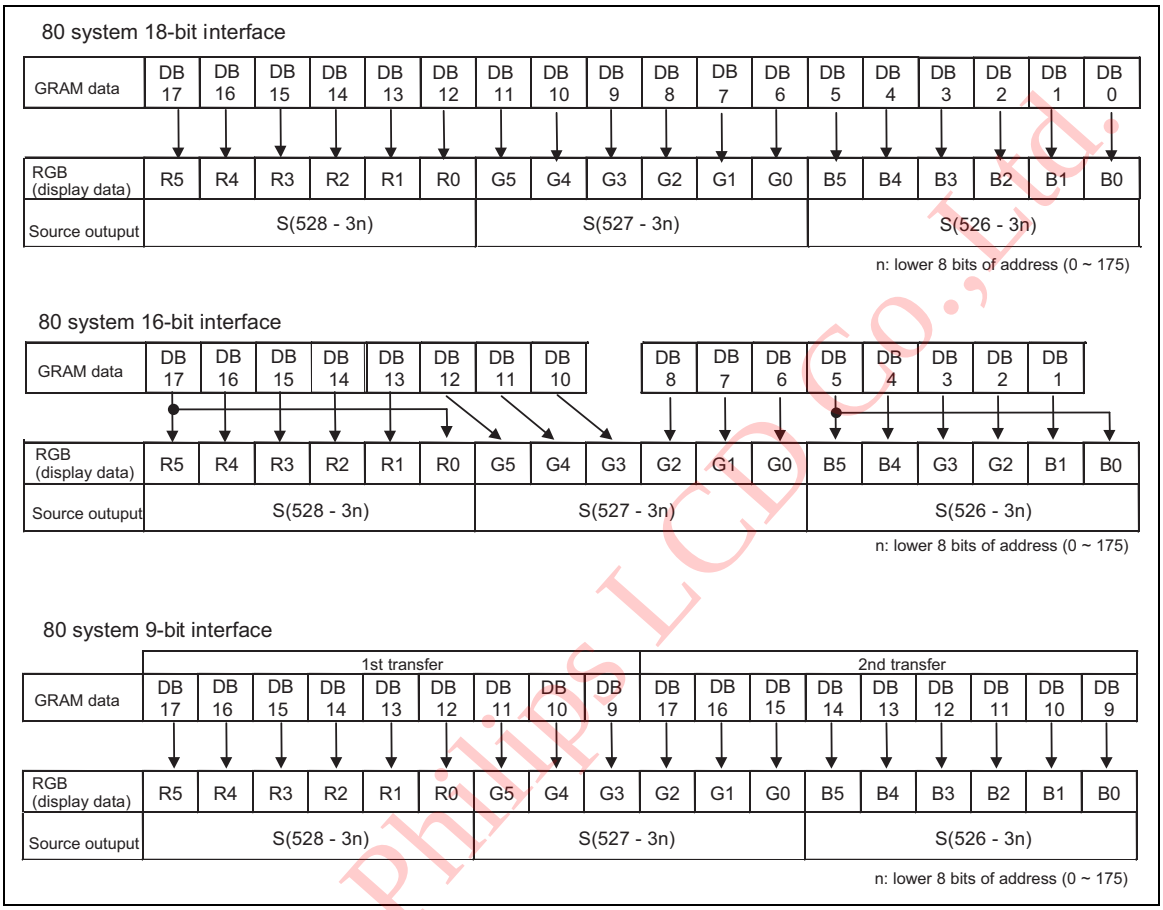


Figure 6 80-system interface (SS = “1”, BGR = “1”)

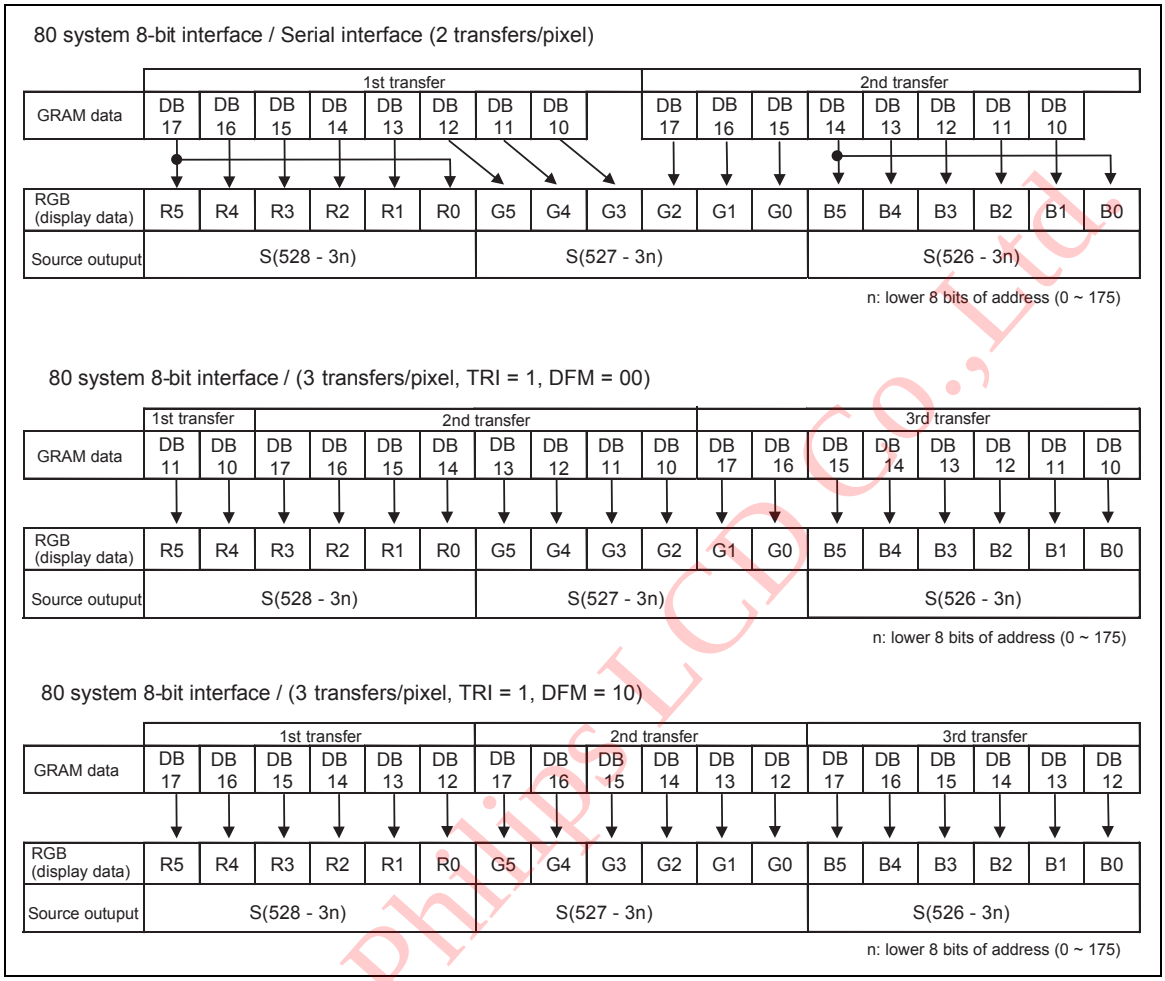


Figure 7 80-system interface (SS = "1", BGR = "1")

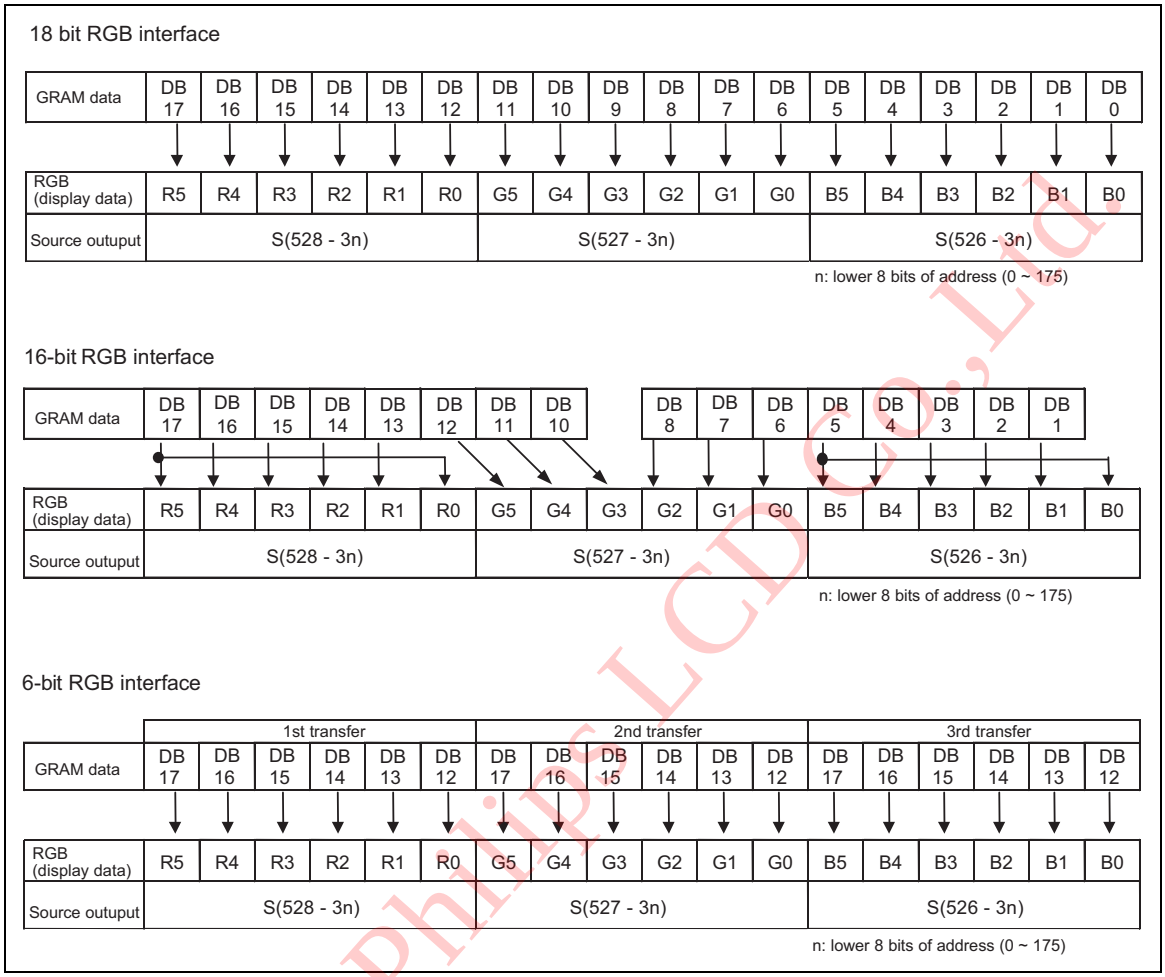


Figure 8 RGB interface (SS = “1”, BGR = “1”)

Instruction

The R61503B adopts 18-bit bus architecture to interface to high-performance microcomputer. The R61503B starts internal processing when the control information sent via 18-, 16-, 9-, 8-bit ports is stored in the instruction register (IR) and the data register (DR). Since the internal operation of the R61503B is controlled by the signals sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (IB15 to IB0) are called instruction. The R61503B accesses the internal GRAM in units of 18 bits. The instructions of the R61503B are categorized into the following 8 groups.

1. Index specification
2. Status Read
3. Display control
4. Power management control
5. GRAM address setting
6. Transfer data to/from the internal GRAM
7. γ-correction
8. EPROM control

Normally, the instruction to write data in the GRAM is used the most often. In order to minimize the data transfer and lessen the programming load on the microcomputer, the R61503B rewrites data only within the window address area and updates internal GRAM address in the address counter automatically as it writes data in the internal GRAM. The R61503B writes instruction consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

Instruction data format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface as shown below.

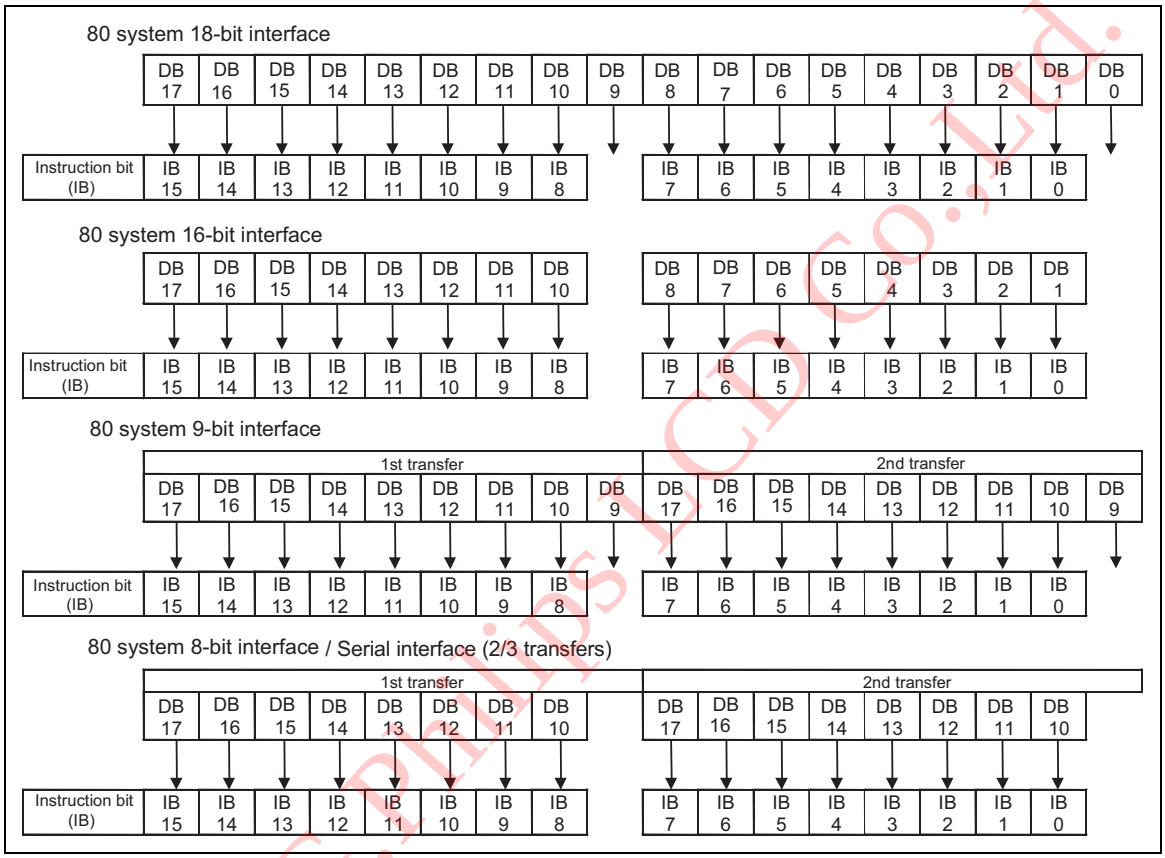


Figure 9 Instruction format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface (see Figure 9 Instruction format).

Index specification/Status read/Display control instructions

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register represents the index of the control register to be accessed (R00h ~ RFFh) and for RAM control using binary numbers from "0000_0000" to "1111_1111". The access to a register and instruction bits in it is prohibited unless the index is specified in the index register.

Status read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The internal status of the R61503B can be read out from the SR register.

L[7:0]: represents the line where the R61503B drives liquid crystal.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	1

The start oscillation instruction starts the oscillator from a halt in standby mode. After executing this instruction, wait at least 10 ms to stabilize the oscillator before issuing next instruction.

The device code "1503"H is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = "0", the source driver output shift from S1 to S528.
When SS = "1", the source driver output shift from S528 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S528.

When SS = "0" and BGR = "0", RGB dots are assigned one to one from S1 to S528.
When SS = "1" and BGR = "1", RGB dots are assigned one to one from S528 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R70h) to select the optimal scan mode for the module. See " Scan mode setting".

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

EOR: By setting EOR = "1", the polarity of C pattern waveform (one-line inversion waveform) is inverted according to the result of EOR (exclusive OR) between the odd/even-number frame select signal and the one-line inversion signal. Set EOR = 1 when the number of lines to drive liquid crystal is not compatible with one-line inversion waveform. For details, see "one-line inversion AC drive".

B/C: When B/C = "0", the liquid crystal drive signal becomes frame-inversion waveform and inverts the polarity of liquid crystal in every frame cycle. When B/C = "1", liquid crystal drive signal becomes one-line inversion waveform and inverts the polarity of liquid crystal in every line cycle. For details, see "line inversion AC drive".

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM [1]	DFM [0]	BGR	0	0	HWM	0	0	0	I/D [1]	I/D [0]	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61503B writes data in the internal GRAM.

AM = "0", sets the horizontal direction.
AM = "1", sets the vertical direction.

When a window address area is specified in GRAM, the R61503B writes data within the window address area in the direction determined by the I/D1-0, AM settings.

I/D[1:0]: The RAM address is automatically incremented (+1) when I/D = "1" and decremented (-1) when I/D = "0" as the R61503B writes data in the GRAM. The I/D[0] bit sets either increment or decrement of RAM address (AD[7:0]) in horizontal direction. The I/D[1] bit sets either increment or decrement decrement of RAM address (AD[15:8]) in vertical direction. The AM bit sets either horizontal or vertical direction in updating RAM address automatically when writing data in the internal RAM.

HWM: When HWM = "1", the R61503B writes data in the internal GRAM in high speed with low power consumption. In this write operation, the R61503B latches the data in units of horizontal lines of window address area in the line buffer and writes the data line by line at a time in the window address area to minimize the number of RAM access and thereby reduce power consumption.

When HWM = "1", make sure the data is written to the end of the horizontal line within the window address area in each RAM write operation. If not, the RAM write operation in that line becomes a failure.

Note 1: Dummy write operation is not required in the R61503B's high speed write operation.
Note 2: The data in the line buffer is cleared when terminating the RAM write operation in the middle of horizontal line and writing other instruction.
Note 3: When switching from high-speed RAM write operation to index write operation, wait at least 2 normal-mode write cycle periods (t_{cycw}) after writing data in the internal RAM.

BGR: Reverses the order of assigning 18-bit RGB data to the data bus (DB17-0) from RGB to BGR.

When BGR = 0, the order of RGB dots is not reversed when writing data to the GRAM.
When BGR = 1, the order of RGB dots is reversed when writing data to the GRAM.

DFM[1:0]: Sets the interface format when transferring 18-bit data via 80-system 16-/8-bit interface in combination with TRI bit. Make sure to set DFM[1:0] = "00", when not using 16-/8-bit interface. See the figures in the "System interface" section for details on the interface format in RAM write operation.

TRI: Sets the interface format when transferring 18-bit data via 80-system 16-/8-bit interface in combination with DFM[1:0] bits.

In 8-bit interface operation,

TRI =0: 16-bit RAM data is transferred in two transfers via 8-bit interface.
TRI =1: 18-bit RAM data is transferred in three transfers via 8-bit interface.

In 16-bit interface operation,

TRI =0: 16-bit RAM data is transferred in one-transfer via 16-bit interface.
TRI =1: 18-bit RAM data is transferred in two transfers via 16-bit interface.

Make sure to set TRI = “0”, when not using 16-/8-bit interface. Also, set TRI = “0” in read operation.

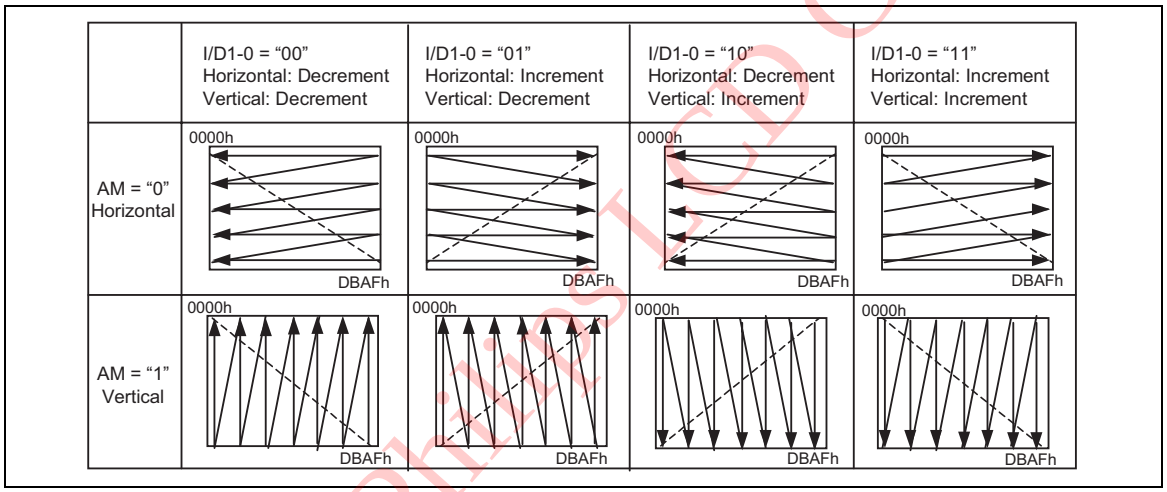


Figure 10 Automatic address transition direction setting (AM, I/D[1:0])

Note: When a window address area is specified in the GRAM, the data is written within the window address area.

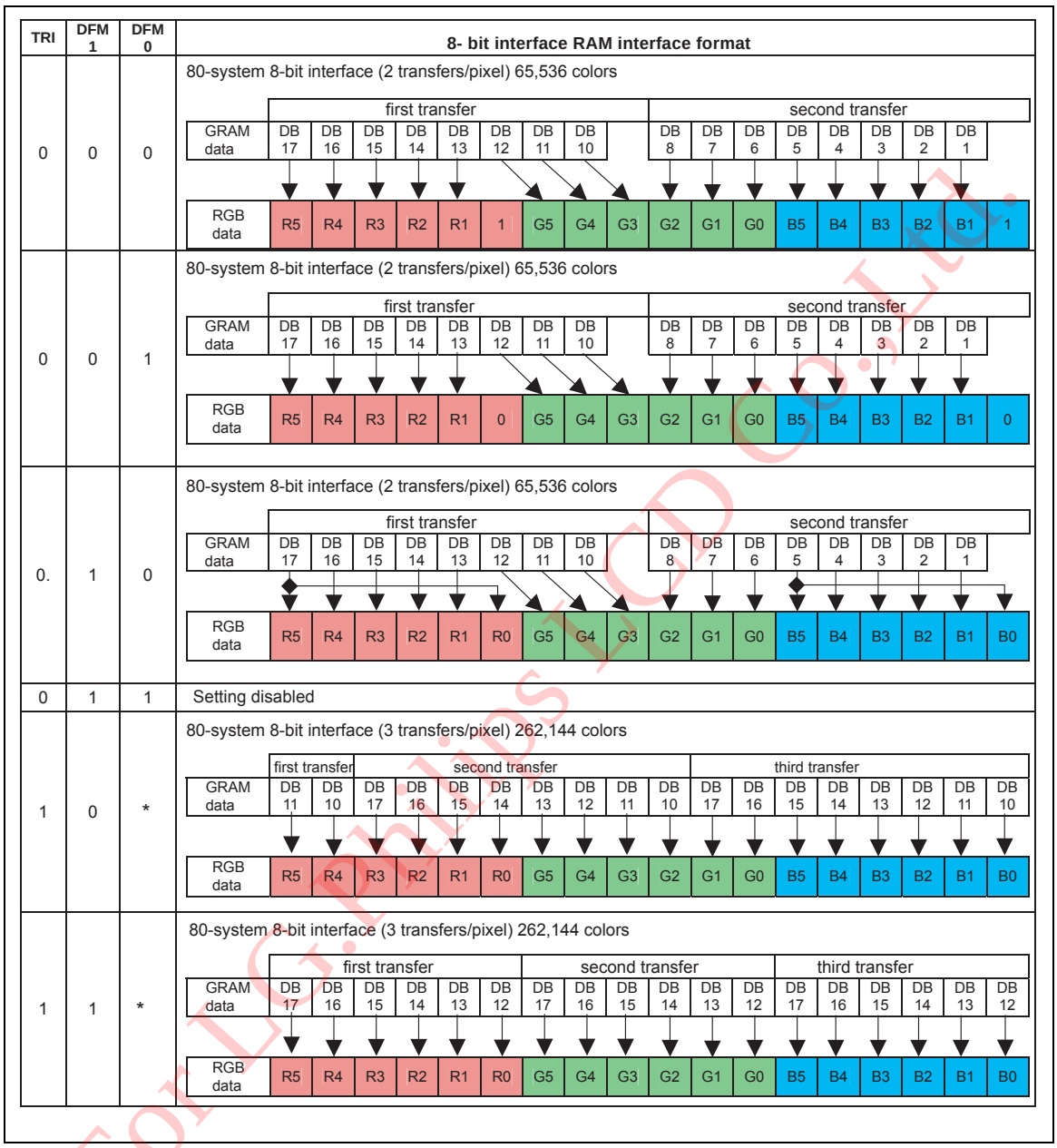


Figure 11 8-bit interface RAM write interface format

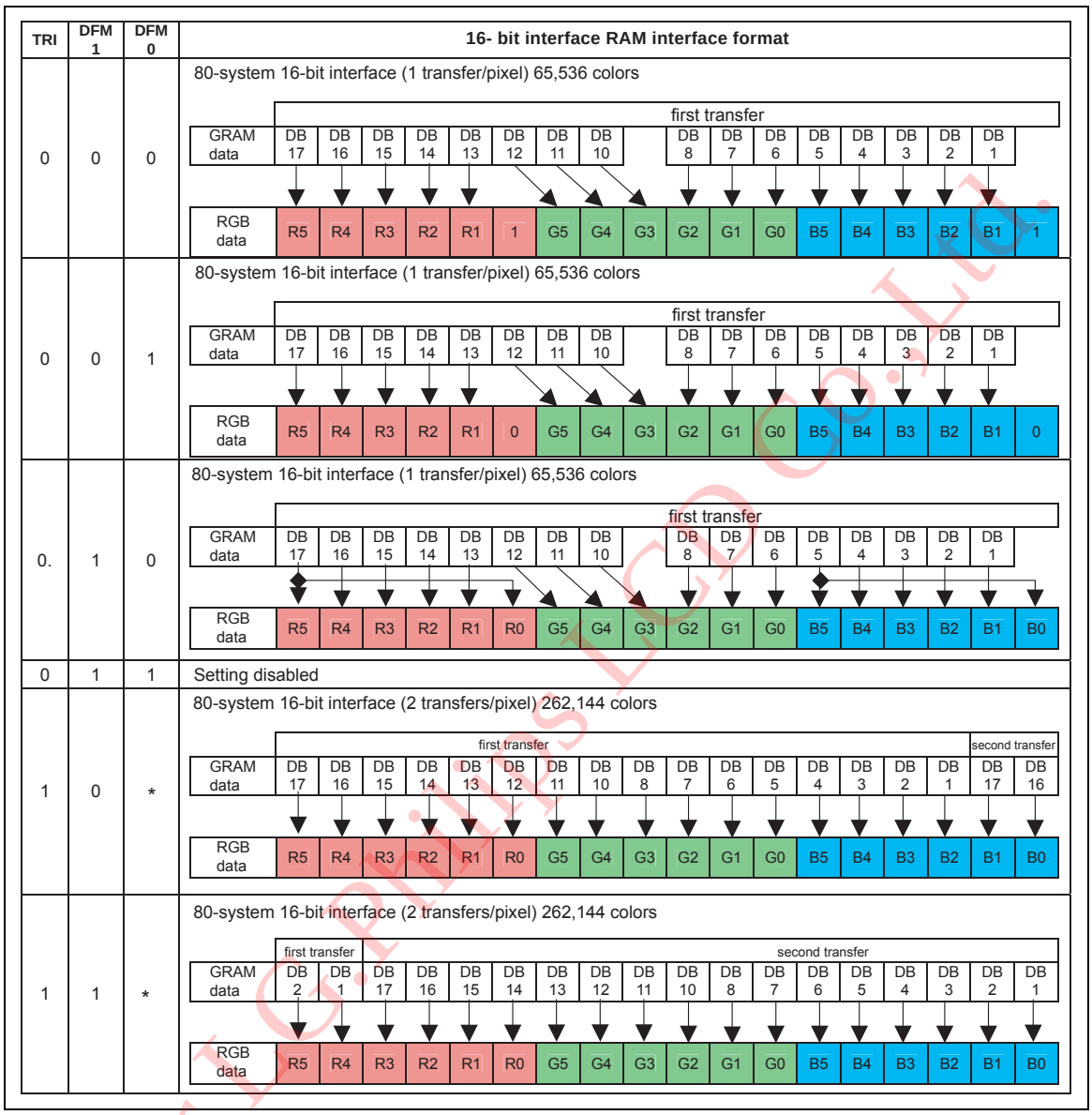


Figure 12 16-bit interface RAM write interface format

Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV [1]	RCV [0]	0	0	RCH [1]	RCH [0]	0	0	RSZ [1]	RSZ [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSZ[1:0]: Sets the resizing factor. When the RSZ bits are set for resizing, the R61503B writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions, which are contracted according to the factor respectively. See "Resizing function".

RCH[1:0]: Sets the number of remainder pixels in horizontal direction when resizing a picture. By specifying the number of remainder pixels by RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

RCV[1:0]: Sets the number of remainder pixels in vertical direction when resizing a picture. By specifying the number of remainder pixels by RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 13 Resizing factor (RSR)

RSR [1:0]	Resizing Scale
2'h0	No resizing (x1)
2'h1	x 1/2
2'h2	Setting inhibited
2'h3	x 1/4

Table 14 Remainder Pixels in Horizontal Direction (RCH)

RCH [1:0]	Number of remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Note: 1 pixel = 1RGB

Table 15 Remainder Pixels in Vertical Direction (RCV)

RCV [1:0]	Number of remainder Pixels in Vertical Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Note: 1 pixel = 1RGB

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE [1]	PTDE [0]	0	0	BASEE	0	0	0	GON	DTE	CL	0	D[1]	D[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0". When writing D1 = "0", the graphics display data is retained in the internal GRAM and the R61503B displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2'b01, the R61503B continues internal display operation. When the display is turned off by setting D1-0 = 2'b00, the R61503B's internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF. For details, see "Instruction Setting".

Table 16

D[1:0]	BASEE	Source output (S1 ~S528)	R61503B's internal operation
2'h0	*	GND	Halt
2'h1	*	GND	Operate
2'h2	*	Non-lit display level	Operate
2'h3	0	Non-lit display level	Operate
	1	Base image display	Operate

Notes: 1. The data write operation from the microcomputer to the internal RAM is performed irrespective of the setting of the D[1:0] bits.
2. The internal state of the R61503B in standby mode become the same as when D[1:0] = 2'b00. This does not mean the D[1:0] setting is changed when setting the standby mode.
3. The D[1:0] setting is valid on both 1st and 2nd displays.
4. The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = "1", the R61503B enters the 8-color mode. Follow the 8-color mode setting sequence when setting the 8-color mode. In 8-color mode, the grayscale amplifiers other than those for the V0 and V31 level are halted. If used in combination with frame-inversion liquid crystal drive, the power consumption will be further reduced.

DTE, GON: Controls the output of liquid crystal panel output signal.

Table 17

GON	DTE	Panel output signal
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE: Base image display enable bit. When BASEE = "0", no base image is displayed. The R61503B drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has precedence over the BASEE setting.

PTDE0: Partial image 1 enable bit
PTDE1: Partial image 2 enable bit

PTDE0/1 = 0: turns off partial image. Only base image is displayed.
PTDE0/1 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP [3]	FP [2]	FP [1]	FP [0]	0	0	0	0	BP [3]	BP [2]	BP [1]	BP [0]
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [3:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [3:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Note on Setting BP and FP

Set the BP and FP bits as follows in respective operation modes.

Table 18 BP and FP Settings

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 19 Front and Back Porch period (Line periods)

FP[3:0] BP[3:0]	Front and Back Porch period (Line periods)
4'h0	Setting inhibited
4'h1	Setting inhibited
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting inhibited

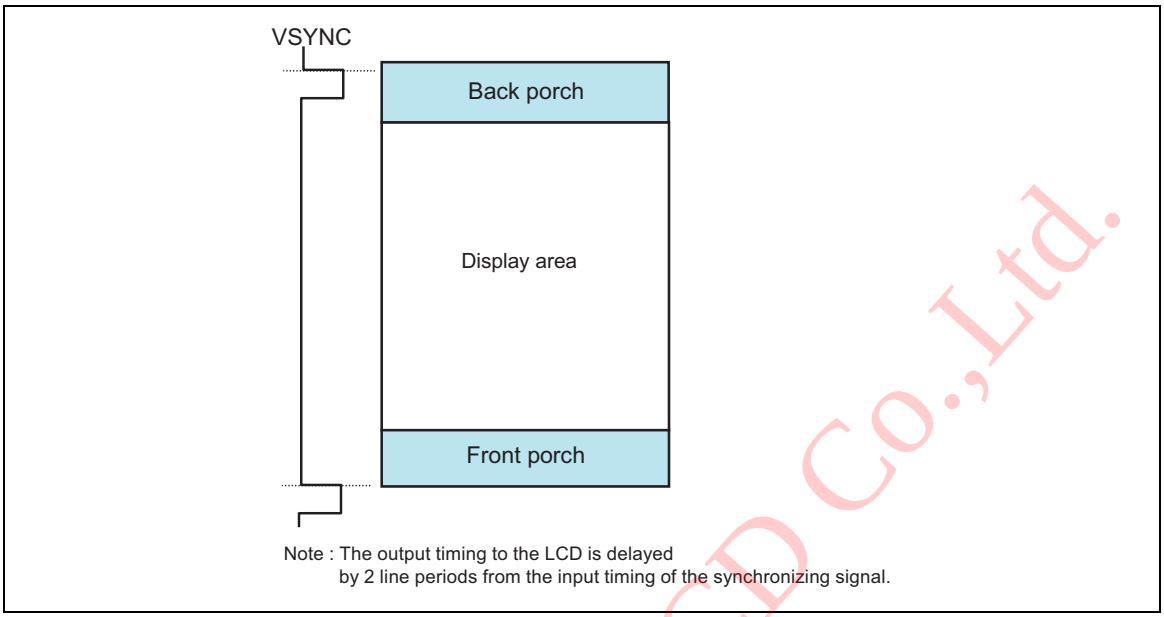


Figure 13 Front, Back Porch periods

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS [2]	PTS [1]	PTS [0]	0	0	PTG [1]	PTG [0]	ISC [3]	ISC [2]	ISC [1]	ISC [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ICS[3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 20

ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz	ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz
4'h0	0 frame	-	4'h8	17 frames	284ms
4'h1	3 frames	50ms	4'h9	19 frames	317ms
4'h2	5 frames	84ms	4'hA	21 frames	351ms
4'h3	7 frames	117ms	4'hB	23 frames	384ms
4'h4	9 frames	150ms	4'hC	25 frames	418ms
4'h5	11 frames	184ms	4'hD	27 frames	451ms
4'h6	13 frames	217ms	4'hE	29 frames	484ms
4'h7	15 frames	251ms	4'hF	31 frames	518ms

PTG[1:0]: Sets the scan mode in non-display area.

Table 21

PTG[1]	PTG[0]	Scan mode in non-display area	Source output level in non-display area	Vcom output
0	**0**	Normal scan	PTS[2:0] setting	AC output
0	**1**	VGL (fixed)	PTS[2:0] setting	AC output
1	**0**	Interval scan	PTS[2:0] setting	AC output
1	**1**	Setting disabled	-	-

PTS[2:0]: Sets the source output level in non-display area drive period (front/back porch period and blank area between partial displays). When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V31 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 22 Source output level and voltage generating operation in non-display drive period

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3'h0	V31	V0	V0 to V31	Register setting (DC0, DC1)
3'h1	Setting inhibited	Setting inhibited	-	-
3'h2	GND	GND	V0 to V31	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V31	Register setting (DC0, DC1)
3'h4	V31	V0	V0 and V31	1/2 the frequency set by DC0, DC1
3'h5	Setting inhibited	Setting inhibited	-	-
3'h6	GND	GND	V0 and V31	1/2 the frequency set by DC0, DC1
3'h7	Hi-Z	Hi-Z	V0 and V31	1/2 the frequency set by DC0, DC1

Notes: 1. The power efficiency can be improved by halting grayscale amplifiers and slowing down the step-up clock frequency only in non-display drive period.

2. The gate output level in non-lit display area drive period is determined by PTG[1:0].

External Display interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61503B performs display operation.

Table 23 RGB interface operation

RIM[1:0]	RGB Interface operation
2'h0	18-bit RGB interface (1 transfer/pixel)
2'h1	16-bit RGB interface (1 transfer/pixel)
2'h2	6-bit RGB interface (3 transfers/pixel)
2'h3	Setting inhibited

Notes: 1: Instruction bits are set via system interface.
2: Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 24 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 25 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

The R61503B selects the optimum interface according to the displayed image by setting instruction as follows.

In moving picture display operation via RGB or VSYNC interface, write data in high-speed write mode (HWM = 1) in order to access RAM in high-speed with low power consumption.

Table 26

The state of display	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 2'h0)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 2'h1)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 2'h1)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 2'h2)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61503B transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function can minimize the total number of data transfer for moving picture display by transferring only the data to be written in the moving picture RAM area when it is written and enables the R61503B to display a moving picture and the data in other than the moving picture RAM area simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61503B by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the settings of these periods.

RGB interface operation (2)

This mode enables the R61503B to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61503B to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61503B according to the instruction settings for these periods.

External display interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK
DPL = "1" The data is input on the falling edge of DOTCLK

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".
EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of the SYNC pin.

HSPL = "0" Low active
HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active
VSPL = "1" High active

Power control

Power control 1/2 (R10h/R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SAP	BT [3]	BT [2]	BT [1]	BT [0]	APE	0	AP [1]	AP [0]	0	DSTB	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	VC [2]	VC [1]	VC [0]
Default		0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0

Top: R10h, bottom: R11h

STB: When STB = 1, the R61503B enters the standby mode. In standby mode, the R61503B halts RC oscillation and receiving external clock signal to halt the display operation completely. In setting the standby mode, follow the standby mode setting sequence. The R61503B accepts only the following instructions in standby mode. The instruction register setting is retained in standby mode.

1. Exit standby mode (STB = 0)
2. Start oscillation

SLP: When SLP = 1, the R61503B enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and the GRAM data and the instruction setting are maintained in sleep mode.

DSTB: When DSTB = 1, the R61503B enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the R61503B enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP1-0 = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

APE: Liquid crystal power supply enable bit. Set APE = "1" when starting the generation of liquid crystal power supply according to the liquid crystal power supply startup sequence. After starting up the power supply circuit, set APE = "1".

Table 27

APE	Liquid crystal power supply circuit	Grayscale voltage generating circuit
1'h0	Halt	Halt
1'h1	Operate	Operate

BT[3:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

SAP: When SAP = "0", the internal source output circuit is halted (S1-S528 = GND). When SAP = "1", grayscale voltages are output from the source output circuit. Set SAP = "0" when turning on the power supply such as liquid crystal power supply circuit. After starting up the power supply circuit, set SAP = "1".

VC[2:0]: Sets the factor of VciLVL to generate the reference voltages VciOUT, Vci1.

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

Table 28 Step-up factor for step-up circuits 1/2

BT[3:0]	DDVDH	VCL	VGH	VGL	Capacitor connection pins
3'h0	VCI1×2 [x 2]	-VCI1	DDVDH×3 [x 6]	-(VCI1+DDVDH×2) [x -5]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h1				-(DDVDH×2) [x -4]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h2				-(VCI1+DDVDH) [x -3]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±,
3'h3			VCI1+DDVDH×2 [x 5]	-(VCI1+DDVDH×2) [x -5]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h4				-(DDVDH×2) [x -4]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h5				-(VCI1+DDVDH) [x -3]	DDVDH, VGH, VGL, VCL C11±, C13±C21±, C22±
3'h6			DDVDH×2 [x 4]	-(DDVDH×2) [x -4]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h7				-(VCI1+DDVDH) [x -3]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h8	Setting disabled				
3'h9	VCI1×2 [x 2]	-VCI1	DDVDH×3 [x 6]	-(VDDVDH) [x -2]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'hA	Setting disabled				
3'hB	Setting disabled				
3'hC	VCI1×2 [x 2]	-VCI1	VCI1+DDVDH×2 [x 5]	-(VDDVDH) [x -2]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'hD	Setting disabled				
3'hE	VCI1×2 [x 2]	-VCI1	DDVDH×2 [x 4]	-(VDDVDH) [x -2]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'hF	Setting disabled				

Notes: 1. The factors in the brackets show the step-up factors from Vci1.
2. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL levels.
3. Make sure DDVDH = max. 6.0V, VGH = max. 15.0V, VGL = min. – 10.0V.

Table 29 constant current in operational amplifiers

AP[1:0]	In LCD drive power supply amplifiers	In grayscale voltage amplifiers
2'h0	Halt operational amplifiers and step-up circuits	Halt
2'h1	0.5	0.62
2'h2	0.75	0.71
2'h3	1	1

Note: The values in the table represent the ratios of currents in respective settings to the current when AP[1:0] = 2'h3.

Table 30 operating frequencies of step-up circuits 1/2

DC0[2:0]	Step-up circuit 1 Operating frequency (f_{DCDC1})
3'h0	Fosc / 8
3'h1	fosc / 16
3'h2	fosc / 32
3'h3	fosc / 64
3'h4	fosc / 128
3'h5	Setting disabled
3'h6	Halt the step-up circuit 1
3'h7	Setting disabled

DC1[2:0]	Step-up circuit 2 Operating frequency (f_{DCDC2})
3'h0	fosc / 16
3'h1	fosc / 32
3'h2	fosc / 64
3'h3	fosc / 128
3'h4	fosc / 256
3'h5	Setting disabled
3'h6	Halt the step-up circuit 2
3'h7	Setting disabled

Note: Make sure $f_{DCDC1} \geq f_{DCDC2}$ when setting the operating frequencies of the step-up circuits 1/2.

Table 31 Reference voltage setting

VC[2:0]	VciOUT (reference voltage) Vci1 voltage
3'h0	0.94 x VciLVL
3'h1	0.89 x VciLVL
3'h2	Setting disabled
3'h3	Setting disabled
3'h4	0.76 x VciLVL
3'h5	Setting disabled
3'h6	Setting disabled
3'h7	1.00 x VciLVL

Power control 3/4 (R12h/R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VON	0	0	0	VCMR	0	0	PSON	PON	VRH [3]	VRH [2]	VRH [1]	VRH [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	VCOMG	0	0	0	VDV [3]	VDV [2]	VDV [1]	VDV [0]	VCM SEL	0	0	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Top: R12h, bottom: R13h

VRH[3:0]: Sets the factor (1.40 ~ 2.10) of VciLVL, the level of which is determined by instruction (VC), to generate the VREG1OUT voltage.

PON: Controls ON/OFF of the VLOUT3 output. When setting the PON bit, follow the power supply startup sequence.

PON = "0": Stop the step-up operation to generate VLOUT3.
PON = "1": Start the step-up operation to generate VLOUT3.

PSON: Starts up the internal power supply sequencer. First set PSE = "1" to enable the internal power supply sequencer and then set PSON = 1 to start up the internal power supply sequencer.

VCMR: Selects either external resistor (VcomR) or internal electric volume (VCM) to set the electrical potential of VcomH (Vcom center voltage level).

Table 32

VCMR	VCOMH electrical potential
0	VCOMR (variable resistor)
1	Internal electronic volume

Note: The internal electronic volume is set by instruction (VCM[4:0]).

VON: Controls Vcom output and its output level in combination with the following bit setting.

Table 33

GON	VON	VCOMG	Vcom output level
0	*	*	GND
1	0	*	GND
1	1	0	VcomH/GND
1	1	1	VcomH/VcomL

VCM[4:0]: Selects the internal electronic volume applied to VREG1OUT to set the VcomH electrical potential. Set VCMR = 1 when setting the VcomH electrical potential with internal electronic volume.

VCMSEL: Selects either the setting in the internal register (VCM[4:0]) or the setting written in the internal EPROM (R29h or R2Ah) to set the VcomH level.

VDV[3:0]: Sets the factor applied to VREG1OUT to define the amplitude of Vcom.

Table 34 VREG1OUT

VRH[3:0]	VREG1OUT	VRH[3:0]	VREG1OUT
4'h0	Halt (Hi-Z)	4'h8	VciLVL x 1.75
4'h1	VciLVL x 1.40	4'h9	VciLVL x 1.80
4'h2	VciLVL x 1.45	4'hA	VciLVL x 1.85
4'h3	VciLVL x 1.50	4'hB	VciLVL x 1.90
4'h4	VciLVL x 1.55	4'hC	VciLVL x 1.95
4'h5	VciLVL x 1.60	4'hD	VciLVL x 2.00
4'h6	VciLVL x 1.65	4'hE	VciLVL x 2.05
4'h7	VciLVL x 1.70	4'hF	VciLVL x 2.10

Note: Set VC and VRH so that VREG1OUT becomes equal or less than (DDVDH -5.0)V.

Table 35

VCMSEL	VcomH level setting
0	Enable the setting in R13H (VCM[4:0])
1	Enable the setting in the internal EPROM (R29h or R2Ah)

Table 36 VCM: internal electronic volume adjustment

VCM[4:0]	VCOMH	VCM[4:0]	VCOMH
5'h00	VREG1OUT x 0.69	5'h10	VREG1OUT x 0.85
5'h01	VREG1OUT x 0.70	5'h11	VREG1OUT x 0.86
5'h02	VREG1OUT x 0.71	5'h12	VREG1OUT x 0.87
5'h03	VREG1OUT x 0.72	5'h13	VREG1OUT x 0.88
5'h04	VREG1OUT x 0.73	5'h14	VREG1OUT x 0.89
5'h05	VREG1OUT x 0.74	5'h15	VREG1OUT x 0.90
5'h06	VREG1OUT x 0.75	5'h16	VREG1OUT x 0.91
5'h07	VREG1OUT x 0.76	5'h17	VREG1OUT x 0.92
5'h08	VREG1OUT x 0.77	5'h18	VREG1OUT x 0.93
5'h09	VREG1OUT x 0.78	5'h19	VREG1OUT x 0.94
5'h0A	VREG1OUT x 0.79	5'h1A	VREG1OUT x 0.95
5'h0B	VREG1OUT x 0.80	5'h1B	VREG1OUT x 0.96
5'h0C	VREG1OUT x 0.81	5'h1C	VREG1OUT x 0.97
5'h0D	VREG1OUT x 0.82	5'h1D	VREG1OUT x 0.98
5'h0E	VREG1OUT x 0.83	5'h1E	VREG1OUT x 0.99
5'h0F	VREG1OUT x 0.84	5'h1F	VREG1OUT x 1.00

Notes 1. Set VcomH from (DDVDH-0.5)V to 2.5V.
2. The VCM[4:0] setting is enabled when VCMR = 1.

Table 37 VDV: VCS (= Vcom) amplitude

VDV[3:0]	VCS (= Vcom) amplitude
4'h00	VREG1OUT x 0.70
4'h01	VREG1OUT x 0.72
4'h02	VREG1OUT x 0.74
4'h03	VREG1OUT x 0.76
4'h04	VREG1OUT x 0.78
4'h05	VREG1OUT x 0.80
4'h06	VREG1OUT x 0.82
4'h07	VREG1OUT x 0.84
4'h08	VREG1OUT x 0.86
4'h09	VREG1OUT x 0.88
4'h0A	VREG1OUT x 0.90
4'h0B	VREG1OUT x 0.92
4'h0C	VREG1OUT x 0.94
4'h0D	VREG1OUT x 0.96
4'h0E	VREG1OUT x 0.98
4'h0F	VREG1OUT x 1.00

Note: Set the Vcom amplitude from 2.5V to (DDVDH-0.5)V.

VCOMG: When VCOMG = 1, the VcomL voltage can be set in the negative range (1.0 ~ Vci+0.5V (max.)). When VCOMG = 0, the amplifiers for the negative voltage are halted to reduce power consumption. When VCOMG = 0, the VDV[3:0] setting is disabled. In this case the Vcom alternating amplitude is determined by the VCM[5:0] setting, which determines the VcomH level. PON must be set to 1 the setting VCOMG = 1 is enabled.

Power Sequence Control 5 (R18h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PSE: Power supply startup enable bit. The power supply startup operation is started by setting PSON = 1 when PSE = 1. When the power supply startup operation is completed, the PSE bit is set to "0".

Power Sequence Control 6 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DC5: Changes the cycle of base clock for the step-up operation. When setting DC5 = 1, the step-up clock is synchronized with the 1H period, i.e. the step-up clock is reset every 1H period. By changing the setting of DC5 bit, the step-up clock cycles DC0 and DC1 are also changed.

Table 38

DC5	Base clock f_{bc}
0	f_{OSC}
1	f_{OSC}/2, synchronized with the 1H period

Table 39 operating frequencies of step-up circuits 1/2

DC0[2:0]	Step-up circuit 1 Operating frequency (f_{DCDC1})
3'h0	f_{bc} / 8
3'h1	f_{bc} / 16
3'h2	f_{bc} / 32
3'h3	f_{bc} / 64
3'h4	f_{bc} / 128
3'h5	Setting disabled
3'h6	Halt the step-up circuit 1
3'h7	Setting disabled

DC1[2:0]	Step-up circuit 2 Operating frequency (f_{DCDC2})
3'h0	f_{bc} / 16
3'h1	f_{bc} / 32
3'h2	f_{bc} / 64
3'h3	f_{bc} / 128
3'h4	f_{bc} / 256
3'h5	Setting disabled
3'h6	Halt the step-up circuit 2
3'h7	Setting disabled

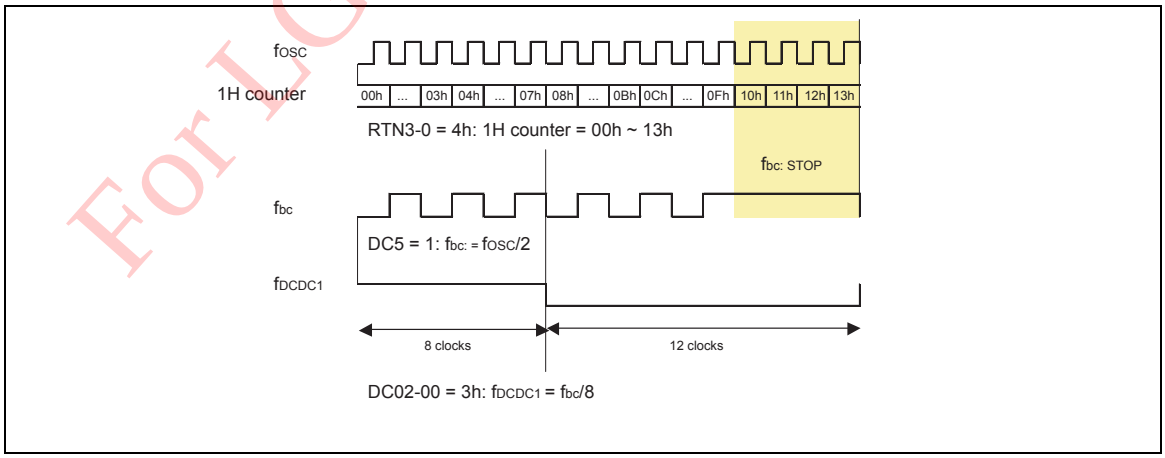


Figure 14

RAM access instruction

RAM Address set horizontal address(R20h),
RAM Address set vertical address(R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Top: R20h, Bottom: R21h

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the AM, I/D[1:0] settings as the R61503B writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 40 GRAM address range

AD[16:0]	GRAM Setting
17'h00000 ~ 17'h 000AF	Bitmap data for G1
"00100" ~ "001AF"	Bitmap data for G2
"00200" ~ "002AF"	Bitmap data for G3
"00300" ~ "003AF"	Bitmap data for G4
:	:
"0D800" ~ "0D8AF"	Bitmap data for G217
"0D900" ~ "0D9AF"	Bitmap data for G218
"0DA00" ~ "0DAAF"	Bitmap data for G219
"0DB00" ~ "0DBAF"	Bitmap data for G220

Write/Read RAM data

Write Data to GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation.															

WD[17:0]: The R61503B develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The R61503B automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. In deep standby mode, GRAM access is disenabled. In 8-/16-bit interface operation, the MSBs of R and B dot are written as the LSBs of respective dot to expand data into 18 bits. In this case, 65,536 colors are available.

Note: When writing data in GRAM via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict with each other.

Table 41 GRAM data and LCD output level (REV = "0")

GRAM data (RGB)	Selected grayscale	
	Negative	Positive
000000	V0	V31
000001	(V0+V1)/2	(V30+V31)/2
000010	V1	V30
000011	(V1+V2)/2	(V29+V30)/2
000100	V2	V29
000101	(V2+V3)/2	(V28+V29)/2
000110	V3	V28
000111	(V3+V4)/2	(V27+V28)/2
001000	V4	V27
001001	(V4+V5)/2	(V26+V27)/2
001010	V5	V26
001011	(V5+V6)/2	(V25+V26)/2
001100	V6	V25
001101	(V6+V7)/2	(V24+V25)/2
001110	V7	V24
001111	(V7+V8)/2	(V23+V24)/2
010000	V8	V23
010001	(V8+V9)/2	(V22+V23)/2
010010	V9	V22
010011	(V9+V10)/2	(V21+V22)/2
010100	V10	V21
010101	(V10+V11)/2	(V20+V21)/2
010110	V11	V20
010111	(V11+V12)/2	(V19+V20)/2
011000	V12	V19
011001	(V12+V13)/2	(V18+V19)/2
011010	V13	V18
011011	(V13+V14)/2	(V17+V18)/2
011100	V14	V17
011101	(V14+V15)/2	(V16+V17)/2
011110	V15	V16
011111	(V15+V16)/2	(V15+V16)/2

GRAM data (RGB)	Selected grayscale	
	Negative	Positive
100000	V16	V15
100001	(V16+V17)/2	(V14+V15)/2
100010	V17	V14
100011	(V17+V18)/2	(V13+V14)/2
100100	V18	V13
100101	(V18+V19)/2	(V12+V13)/2
100110	V19	V12
100111	(V19+V20)/2	(V11+V12)/2
101000	V20	V11
101001	(V20+V21)/2	(V10+V11)/2
101010	V21	V10
101011	(V21+V22)/2	(V9+V10)/2
101100	V22	V9
101101	(V22+V23)/2	(V8+V9)/2
101110	V23	V8
101111	(V23+V24)/2	(V7+V8)/2
110000	V24	V7
110001	(V24+V25)/2	(V6+V7)/2
110010	V25	V6
110011	(V25+V26)/2	(V5+V6)/2
110100	V26	V5
110101	(V26+V27)/2	(V4+V5)/2
110110	V27	V4
110111	(V27+V28)/2	(V3+V4)/2
111000	V28	V3
111001	(V28+V29)/2	(V2+V3)/2
111010	V29	V2
111011	(V29+V30)/2	(V1+V2)/2
111100	V30	V1
111101	(V30+V31)/2	(V0+V1)/2
111110	(V30+2xV31)/3	(2xV0+V1)/3
111111	V31	V0

RAM Access via RGB interface and System interface

The R61503B writes all data in GRAM in RGB interface operation in order to rewrite the data only within the moving picture area and transfer only the data to be written over the moving picture area. The power consumption required for moving picture display can be reduced and RAM data update can be done in short period by specifying window address area and enabling high-speed write function. The R61503B also allows writing the display data in other than the moving picture area in GRAM via system interface while not updating the moving picture frame.

The R61503B allows RAM access via system interface in RGB interface operation. In RGB interface operation, the data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. When switching to RAM access via RGB interface from RAM access via system interface, make sure to wait for read/write bus cycle time. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

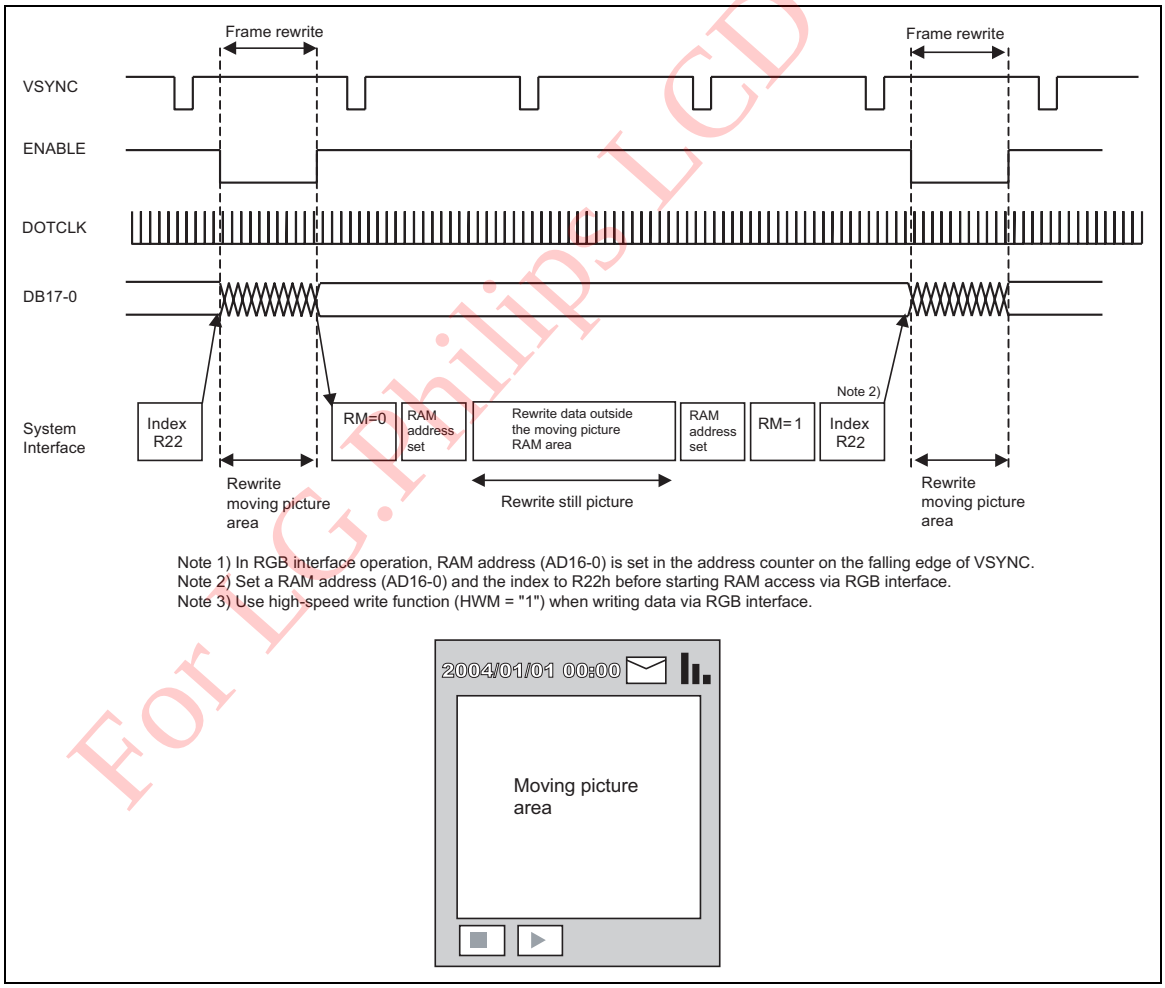


Figure 15

Read Data from GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

RD[17:0]: 18-bit data read from the GRAM. RAM read data RD[17:0] is transferred via different data bus in different interface operation.

When the R61503B reads data from the GRAM to the microcomputer, the first word, which is read immediately after the RAM address set instruction is executed, is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the R61503B reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

Note: This register is not available in RGB interface operation.

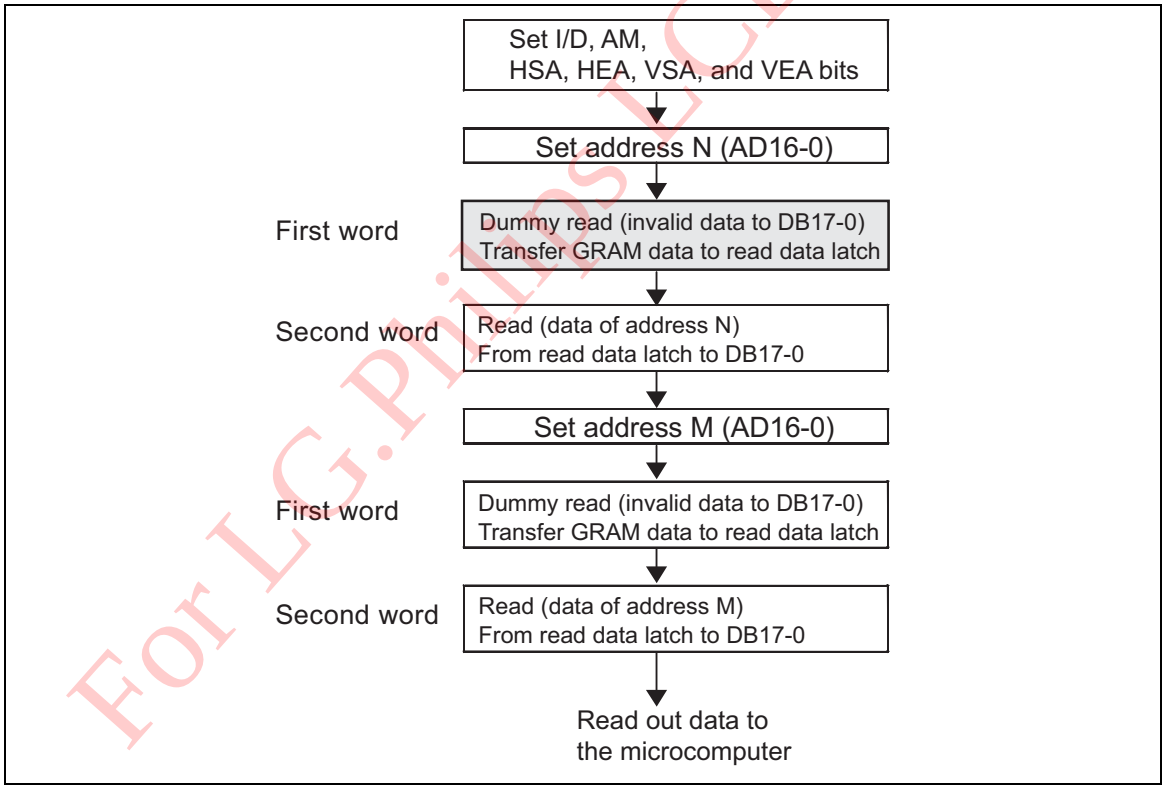


Figure 16 GRAM read sequence

EPROM read data 1 (R28h), EPROM read data 2(R29h), EPROM read data 3(R2Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28	W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID [3]	UID [2]	UID [1]	UID [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R29	W	1	0	0	0	0	0	0	0	0	EVCME0	0	0	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R2A	W	1	0	0	0	0	0	0	0	0	EVCME1	0	0	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UID[3:0]: Data in Address 1, which is read from the internal EPROM and used as the user identification code. See "EPROM control" for details.

EVCME0, EVCM1: Select either EVCM0[4:0] or EVCM1[4:0] in the internal EPROM to set the VcomH level when setting VcomH by internal electronic volume. When VCMSEL = 1, the setting written in the internal EPROM, i.e. either EVCM0[4:0] or EVCM1[4:0], is used instead of VCM[4:0], i.e. internal register setting.

Table 42

EVCME1	EVCME0	VcomH setting
0	0	6'h0
0	1	EVCM0[4:0] (data written in Address 2)
1	0	Setting disabled
1	1	EVCM1[4:0] (data written in Address 3)

EVCM0[4:0]: Data in Address 2 in the EPROM to adjust the VcomH voltage using internal electronic volume.

EVCM1[4:0]: Data in Address 3 in the EPROM to adjust the VcomH voltage using internal electronic volume.

γ Control Instruction

γ Control (1) ~ (9) (R30h ~ R3Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP 1[2]	PKP 1[1]	PKP 1[0]	0	0	0	0	0	PKP 0[2]	PKP 0[1]	PKP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31	W	1	0	0	0	0	0	PKP 3[2]	PKP 3[1]	PKP 3[0]	0	0	0	0	0	PKP 2[2]	PKP 2[1]	PKP 2[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32	W	1	0	0	0	0	0	PKP 5[2]	PKP 5[1]	PKP 5[0]	0	0	0	0	0	PKP 4[2]	PKP 4[1]	PKP 4[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R33	W	1	0	0	0	0	0	PRP 1[2]	PRP 1[1]	PRP 1[0]	0	0	0	0	0	PRP 0[2]	PRP 0[1]	PRP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R34	W	1	0	0	0	0	0	PKN 1[2]	PKN 1[1]	PKN 1[0]	0	0	0	0	0	PKN 0[2]	PKN 0[1]	PKN 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35	W	1	0	0	0	0	0	PKN 3[2]	PKN 3[1]	PKN 3[0]	0	0	0	0	0	PKN 2[2]	PKN 2[1]	PKN 2[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36	W	1	0	0	0	0	0	PKN 5[2]	PKN 5[1]	PKN 5[0]	0	0	0	0	0	PKN 4[2]	PKN 4[1]	PKN 4[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37	W	1	0	0	0	0	0	PRN 1[2]	PRN 1[1]	PRN 1[0]	0	0	0	0	0	PRN 0[2]	PRN 0[1]	PRN 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38	W	1	0	0	0	VRP 1[4]	VRP 1[3]	VRP 1[2]	VRP 1[1]	VRP 1[0]	0	0	0	VRP 0[4]	VRP 0[3]	VRP 0[2]	VRP 0[1]	VRP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39	W	1	0	0	0	VRN 1[4]	VRN 1[3]	VRN 1[2]	VRN 1[1]	VRN 1[0]	0	0	0	VRN 0[4]	VRN 0[3]	VRN 0[2]	VRN 0[1]	VRN 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3A	W	1	0	0	0	VAJN 1[4]	VAJN 1[3]	VAJN 1[2]	VAJN 1[1]	VAJN 1[0]	0	0	0	VAJP 0[4]	VAJP 0[3]	VAJP 0[2]	VAJP 0[1]	VAJP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PKP5-0[2:0] γ fine adjustment register for positive polarity
PRP1-0[2:0] gradient adjustment register for positive polarity
PKN5-0[2:0] γ fine adjustment register for negative polarity
PRN1-0[2:0] gradient adjustment register for negative polarity
VRP1-0[4:0] amplitude adjustment register for positive polarity
VAJP0[4:0] amplitude adjustment register for positive polarity
VRN1-0[4:0] amplitude adjustment register for negative polarity
VAJN1[4:0] amplitude adjustment register for negative polarity

See "γ Correction function" for details.

Window address control instruction

Window horizontal RAM start address (R50h), Window horizontal RAM end address (R51h)

Window vertical RAM start address (R52h), Window vertical RAM end address (R52h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50	W/R	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	W/R	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
	Default		0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1
R52	W/R	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53	W/R	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]
	Default		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

HSA[7:0]/HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that "00"h ≤ HSA[7:0] < HEA[7:0] ≤ "AF"h.

VSA[8:0]/VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that "00"h ≤ VSA[8:0] < VEA[8:0] ≤ "DB"h.

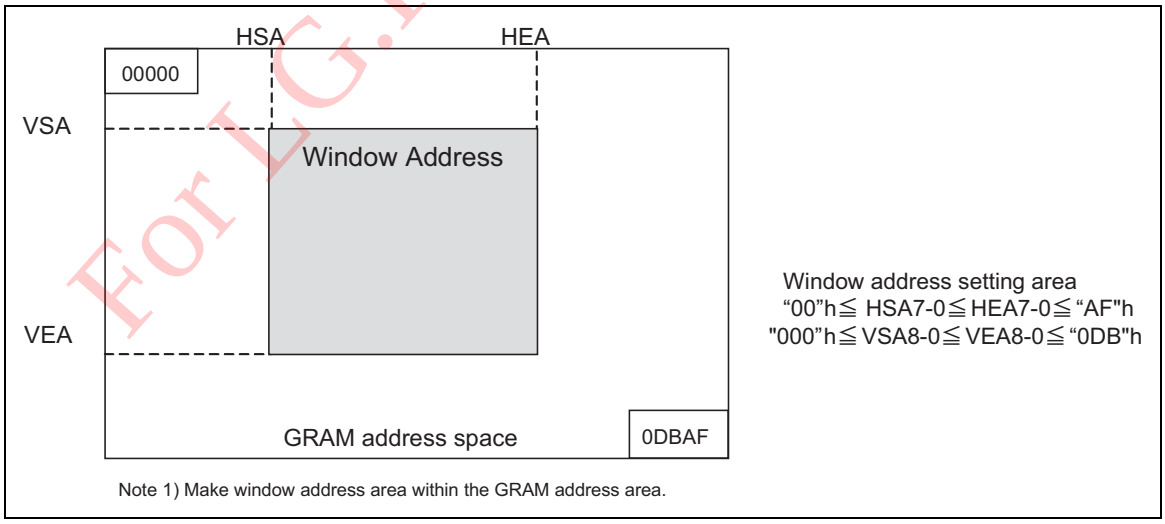


Figure 17 GRAM address map and window address area

Base image display control instruction

Driver output control (R70h), Base image display control (R71h), Vertical scroll control (R7Ah),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R70	W/R	1	GS	0	0	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	0	0	0	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R71	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R7A	W/R	1	0	0	0	0	0	0	0	0	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[4:0]: Specifies the gate line where the gate driver starts scan.

Table 43

SCN [4:0]	Scan start position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
4'h00	G1	G220	G1	G220
4'h01	G9	G212	G17	G204
4'h02	G17	G204	G33	G188
4'h03	G25	G196	G49	G172
4'h04	G33	G188	G65	G156
4'h05	G41	G180	G81	G140
4'h06	G49	G172	G97	G124
4'h07	G57	G164	G113	G108
4'h08	G65	G156	G129	G92
4'h09	G73	G148	G145	G76
4'h0A	G81	G140	G161	G60
4'h0B	G89	G132	G177	G44
4'h0C	G97	G124	G193	G28
4'h0D	G105	G116	G209	G12
4'h0E	G113	G108	G2	G6
4'h0F	G121	G100	G18	G219
4'h10	G129	G92	G34	G203
4'h11	G137	G84	G50	G187
4'h12	G145	G76	G66	G171
4'h13	G153	G68	G82	G155
4'h14	G161	G60	G98	G139
4'h15	G169	G52	G114	G123
4'h16	G177	G44	G130	G107
4'h17	G185	G36	G146	G91
4'h18	G193	G28	G162	G75
4'h19	G201	G20	G178	G59
4'h1A	G209	G12	G194	G43
4'h1B	G217	G4	G210	G27
4'h1C-4'h1F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NL[4:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[4:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 44

NL [4:0]	LCD drive line
6'h00	0 line
6'h01	16 lines
6'h02	24 lines
6'h03	32 lines
6'h04	40 lines
6'h05	48 lines
6'h06	56 lines
6'h07	64 lines
6'h08	72 lines
6'h09	80 lines
6'h0A	88 lines
6'h0B	96 lines
6'h0C	104 lines
6'h0D	112 lines
6'h0E	120 lines
6'h0F	128 lines

NL [4:0]	LCD drive line
6'h10	136 lines
6'h11	144 lines
6'h12	152 lines
6'h13	160 lines
6'h14	168 lines
6'h15	176 lines
6'h16	184 lines
6'h17	192 lines
6'h18	200 lines
6'h19	208 lines
6'h1A	216 lines
6'h1B	220 lines

GS: Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G220.
When GS = 1, the scan direction is from G220 to G1

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the R61503B to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during the front, back porch periods and blank periods is determined by register setting (PTS).

Table 45 GRAM Data-grayscale level inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V31	V0
	:	:	:
	18'hFFFFF	V0	V31
1	18'h00000	V0	V31
	:	:	:
	18'hFFFFF	V31	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the R61503B starts displaying the base image from the line (of the physical display) determined by VL[7:0] bits. VL[7:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 46

VLE	Base image
0	Fixed
1	Enable scrolling

VL[7:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[7:0]. Make sure BSA(0) +VL[7:0] ≤ BEA(220).

Partial control instruction

Partial image 1 display position (R80h)

Partial image 1 RAM start address (R81h), Partial image 1 RAM end address (R82h)

Partial image 2 display position (R83h)

Partial image 2 RAM Address (R84h), Partial image 2 RAM end address (R85h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R80	W	1	0	0	0	0	0	0	0	0	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	W		0	0	0	0	0	0	0	0	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	W		0	0	0	0	0	0	0	0	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R83	W	1	0	0	0	0	0	0	0	0	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R84	W	1	0	0	0	0	0	0	0	0	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85	W	1	0	0	0	0	0	0	0	0	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[7:0]: Sets the display position of partial image 1.
PTDP1[7:0]: Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display area: (PTDP0, PTDP0+(PTEA0 – PTSA0))
Coordinates of partial image 2 display area: (PTDP1, PTDP1+(PTEA1 – PTSA1))

If PTDP0 is set to “8’h00”, the partial image 1 is displayed from the 1st line of the panel on the base image.

PTSA0[7:0] PTEA0[7:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[7:0] ≤ PTEA0[7:0].

PTSA1[7:0] PTEA1[7:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[7:0] ≤ PTEA1[7:0].

Panel interface control instruction

Panel interface control 1 (R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTNI[3:0]: Sets 1H (line) period. This setting is enabled while the R61503B's display operation is synchronized with internal clock signal.

DIVI[1:0]: Sets the division ratio of internal clock frequency. The R61503B's internal operation is synchronized with the frequency-divided internal clock, the frequency of which is divided by the division ratio set by DIVI[1:0]. When changing the DIVI[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, the frame frequency must be adjusted. See "Frame-Frequency Adjustment Function" for details.

DIVI[1:0] is disenabled in RGB interface operation.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line + BP + FP)}} \quad [Hz]$$

fosc : RC oscillation frequency

Line: Number of lines to drive the LCD (NL bits)

Division ratio: DIVI

Clocks per line: RTNI

Table 47 clocks in 1H period (internal clock operation: 1 clock = 1 OSC)

RTNI[3:0]	Clocks per Line	RTNI[3:0]	Clocks per Line
4'h0	16 clocks	4'h8	24 clocks
4'h1	17 clocks	4'h9	25 clocks
4'h2	18 clocks	4'hA	26 clocks
4'h3	19 clocks	4'hB	27 clocks
4'h4	20 clocks	4'hC	28 clocks
4'h5	21 clocks	4'hD	29 clocks
4'h6	22 clocks	4'hE	30 clocks
4'h7	23 clocks	4'hF	31 clocks

Table 48 Division ratio of the internal operation clock

DIVI[1:0]	Division Ratio	Internal Operation Clock Frequency
2'h0	1/1	fosc / 1
2'h1	1/2	fosc / 2
2'h2	1/4	fosc / 4
2'h3	1/8	fosc / 8

Note: fosc: RC oscillation frequency

Panel interface control 2 (R91h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOI [2]	NOI [1]	NOI [0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOI[2:0]: Sets the gate output non-overlap period when the R61503B's display operation is synchronized with internal clock signal.

Table 49

NOI[2:0]	Gate non-overlap period
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

Panel interface control 3 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI [2]	SDTI [1]	SDTI [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDTI[2:0]: Sets the source output position when the R61503B's display operation is synchronized with internal clock signal.

Table 50

SDTI[2:0]	Source output position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The source output position is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

Panel interface control 4 (R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	0	RTNE [5]	RTNE [4]	RTNE [3]	RTNE [2]	RTNE [1]	RTNE [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTNE[5:0]: Sets RTNE in combination with DIVE so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK included in 1H (line) period, when the R61503B's display operation is synchronized with RGB interface signals.

DIVE (division ratio) x RTNE (DOTCLKs) ≤ DOTCLKs in 1H period.

DIVE[1:0]: Sets the division ratio of DOTCLK. The R61503B's internal operation is synchronized with the frequency-divided DOTCLK, the frequency of which is divided by the division ratio set by DIVE[1:0]. This setting is enabled while the R61503B's display operation is synchronized with RGB interface signals.

Table 51 DOTCLKs in 1H period (RGB interface operation)

RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)
6'h00	Setting inhibited	6'h10	16 clocks	6'h20	32 clocks	6'h30	48 clocks
6'h01	Setting inhibited	6'h11	17 clocks	6'h21	33 clocks	6'h31	49 clocks
6'h02	Setting inhibited	6'h12	18 clocks	6'h22	34 clocks	6'h32	50 clocks
6'h03	Setting inhibited	6'h13	19 clocks	6'h23	35 clocks	6'h33	51 clocks
6'h04	Setting inhibited	6'h14	20 clocks	6'h24	36 clocks	6'h34	52 clocks
6'h05	Setting inhibited	6'h15	21 clocks	6'h25	37 clocks	6'h35	53 clocks
6'h06	Setting inhibited	6'h16	22 clocks	6'h26	38 clocks	6'h36	54 clocks
6'h07	Setting inhibited	6'h17	23 clocks	6'h27	39 clocks	6'h37	55 clocks
6'h08	Setting inhibited	6'h18	24 clocks	6'h28	40 clocks	6'h38	56 clocks
6'h09	Setting inhibited	6'h19	25 clocks	6'h29	41 clocks	6'h39	57 clocks
6'h0A	Setting inhibited	6'h1A	26 clocks	6'h2A	42 clocks	6'h3A	58 clocks
6'h0B	Setting inhibited	6'h1B	27 clocks	6'h2B	43 clocks	6'h3B	59 clocks
6'h0C	Setting inhibited	6'h1C	28 clocks	6'h2C	44 clocks	6'h3C	60 clocks
6'h0D	Setting inhibited	6'h1D	29 clocks	6'h2D	45 clocks	6'h3D	61 clocks
6'h0E	Setting inhibited	6'h1E	30 clocks	6'h2E	46 clocks	6'h3E	62 clocks
6'h0F	Setting inhibited	6'h1F	31 clocks	6'h2F	47 clocks	6'h3F	63 clocks

Table 52 Division Ratio of DOTCLK (RGB interface operation)

DIVE[1:0]	Division Ratio	Internal operation clock unit in RGB interface operation			
		18-bit RGB Interface	DOTCLK = 5MHz	6-bit x3 transfers RGB Interface	DOTCLK = 15MHz
2'h0	Setting inhibited	Setting inhibited	-	Setting inhibited	-
2'h1	1/4	4 DOTCLKs	0.8 μS	12 DOTCLKs	0.8 μS
2'h2	1/8	8 DOTCLKs	1.6 μS	24 DOTCLKs	1.6 μS
2'h3	1/16	16 DOTCLKs	3.2 μS	48 DOTCLKs	3.2 μS

Panel interface control 5 (R94h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	NOE [3	NOE [2]	NOE [1]	NOE [0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOE[3:0]: Sets the gate output non-overlap period when the R61503B's display operation is synchronized with RGB interface signals.

Table 53

NOE[3:0]	Gate non-overlap period	NOE[3:0]	Gate non-overlap period
4'h0	0 clocks	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clock
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

Panel interface control 6 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE [2]	SDTE [1]	SDTE [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDTE[2:0]: Sets the source output position and Vcom alternating position. This setting is enabled while the R61503B's display operation is synchronized with RGB interface signals.

Table 54

SDTE[2:0]	Source output position Vcom alternating position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

Source driver output control 1/2/3/4/5 (R98h, R99h, R9Ah, R9Bh, R9Ch)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R98	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VSEL [1]	VSEL [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R99	W		0	0	0	CPB WI[4]	CPB WI[3]	CPB WI[2]	CPB WI[1]	CPB WI[0]	0	0	0	CPA WI[4]	CPA WI[3]	CPA WI[2]	CPA WI[1]	CPA WI[0]
	Default		0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1
R9A	W	1	0	0	0	CNB WI[4]	CNB WI[3]	CNB WI[2]	CNB WI[1]	CNB WI[0]	0	0	0	CNA WI[4]	CNA WI[3]	CNA WI[2]	CNA WI[1]	CNA WI[0]
	Default		0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1
R9B	W	1	0	0	CPB WE[5]	CPB WE[4]	CPB WE[3]	CPB WE[2]	CPB WE[1]	CPB WE[0]	0	0	CPA WE[5]	CPA WE[4]	CPA WE[3]	CPA WE[2]	CPA WE[1]	CPA WI[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R9C	W	1	0	0	CNB WE[5]	CNB WE[4]	CNB WE[3]	CNB WE[2]	CNB WE[1]	CNB WE[0]	0	0	CNA WE[5]	CNA WE[4]	CNA WE[3]	CNA WE[2]	CNA WE[1]	CNA WI[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VSEL[1:0]: Changes the grayscale output order.

Table 55

VSEL[1:0]	Grayscales outputted in CPAW, CNAW periods	Grayscales outputted in CPBW, CNBW periods
00	V0,V2,V4,V6,V8,V10,V12,V14, V17,V19,V21,V23,V25,V27,V29,V31	V1,V3,V5,V7,V9,V11,V13,V15, V16,V18,V20,V22,V24,V26,V28,V30
01	V0,V2,V4,V6,V8,V10,V12,V14, V16,V18,V20,V22,V24,V26,V28,V30	V1,V3,V5,V7,V9,V11,V13,V15, V17,V19,V21,V23,V25,V27,V29,V31
10	V1,V3,V5,V7,V9,V11,V13,V15, V17,V19,V21,V23,V25,V27,V29,V31	V0,V2,V4,V6,V8,V10,V12,V14, V16,V18,V20,V22,V24,V26,V28,V30
11	V1,V3,V5,V7,V9,V11,V13,V15, V16,V18,V20,V22,V24,V26,V28,V30	V0,V2,V4,V6,V8,V10,V12,V14, V17,V19,V21,V23,V25,V27,V29,V31

CPAWI[4:0], CPBWI[4:0]: Sets the positive-polarity source output period. This setting is enabled while the R61503B's display operation is synchronized with internal clock signal.

CNAWI[4:0], CNBWI[4:0]: Sets the negative-polarity source output period. This setting is enabled while the R61503B's display operation is synchronized with internal clock signal.

In setting these bits, make sure

CPAWI[4:0] + CPBWI[4:0] ≤ 1H – 1 clock period
CNAWI[4:0] + CNBWI[4:0] ≤ 1H – 1 clock period

CPAWE[5:0], CPBWE[5:0]: Sets the positive-polarity source output period. This setting is enabled while the R61503B's display operation is synchronized with RGB interface signals.

CNAWE[5:0], CNBWE[5:0]: Sets the negative-polarity source output period. This setting is enabled while the R61503B's display operation is synchronized with RGB interface signals.

In setting these bits, make sure

CPAWE[5:0] + CPBWE[5:0] ≤ 1H – 1 clock period
CNAWE[5:0] + CNBWE[5:0] ≤ 1H – 1 clock period

Table 56

CPAWI[4:0] CPBWI[4:0] CNAWI[4:0] CNBWI[4:0]	Source output period	CPAWE[5:0] CPBWE[5:0] CNAWE[5:0] CNBWE[5:0]	Source output period	CPAWE[5:0] CPBWE[5:0] CNAWE[5:0] CNBWE[5:0]	Source output period
5'h00	Setting disabled	6'h00	Setting disabled	6'h20	32 clocks
5'h01	1 clocks	6'h01	1 clocks	6'h21	33 clocks
5'h02	2 clocks	6'h02	2 clocks	6'h22	34 clocks
5'h03	3 clocks	6'h03	3 clocks	6'h23	35 clocks
5'h04	4 clocks	6'h04	4 clocks	6'h24	36 clocks
5'h05	5 clocks	6'h05	5 clocks	6'h25	37 clocks
5'h06	6 clocks	6'h06	6 clocks	6'h26	38 clocks
5'h07	7 clocks	6'h07	7 clocks	6'h27	39 clocks
5'h08	8 clocks	6'h08	8 clocks	6'h28	40 clocks
5'h09	9 clocks	6'h09	9 clocks	6'h29	41 clocks
5'h0A	10 clocks	6'h0A	10 clocks	6'h2A	42 clocks
5'h0B	11 clocks	6'h0B	11 clocks	6'h2B	43 clocks
5'h0C	12 clocks	6'h0C	12 clocks	6'h2C	44 clocks
5'h0D	13 clocks	6'h0D	13 clocks	6'h2D	45 clocks
5'h0E	14 clocks	6'h0E	14 clocks	6'h2E	46 clocks
5'h0F	15 clocks	6'h0F	15 clocks	6'h2F	47 clocks
5'h10	16 clocks	6'h10	16 clocks	6'h30	48 clocks
5'h11	17 clocks	6'h11	17 clocks	6'h31	49 clocks
5'h12	18 clocks	6'h12	18 clocks	6'h32	50 clocks
5'h13	19 clocks	6'h13	19 clocks	6'h33	51 clocks
5'h14	20 clocks	6'h14	20 clocks	6'h34	52 clocks
5'h15	21 clocks	6'h15	21 clocks	6'h35	53 clocks
5'h16	22 clocks	6'h16	22 clocks	6'h36	54 clocks
5'h17	23 clocks	6'h17	23 clocks	6'h37	55 clocks
5'h18	24 clocks	6'h18	24 clocks	6'h38	56 clocks
5'h19	25 clocks	6'h19	25 clocks	6'h39	57 clocks
5'h1A	26 clocks	6'h1A	26 clocks	6'h3A	58 clocks
5'h1B	27 clocks	6'h1B	27 clocks	6'h3B	59 clocks
5'h1C	28 clocks	6'h1C	28 clocks	6'h3C	60 clocks
5'h1D	29 clocks	6'h1D	29 clocks	6'h3D	61 clocks
5'h1E	30 clocks	6'h1E	30 clocks	6'h3E	62 clocks
5'h1F	31 clocks	6'h1F	31 clocks	6'h3F	63 clocks

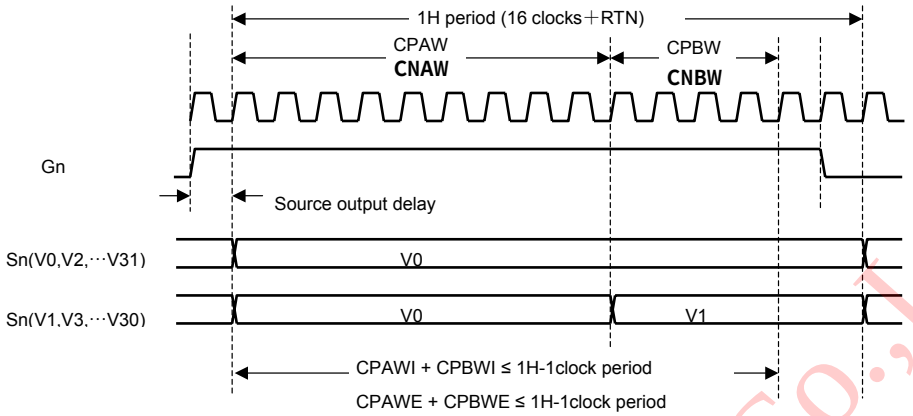


Figure 18

EPROM control

EPROM access control 1 (RA0h), EPROM access control 2 (RA1h)

Calibration control (RA4h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA0	W/R	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	EAD [1]	EAD [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA1	W/R		0	0	0	0	0	0	0	0	ED [7]	ED [6]	ED [5]	ED [4]	ED [3]	ED [2]	ED [1]	ED [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA4	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: Enable internal EPROM control bit (EOP). Follow the EPROM control sequence when setting TE. When resetting register (loading EOP = 2'h2) and executing a calibration, TE is set automatically according to the internal automatic sequence and it does not have to be set.

EOP[1:0]: Internal EPROM control bit. Follow the EPROM control sequence when setting EOP[1:0].

Table 57

EOP[1:0]	EPROM control
2'h0	Halt
2'h1	Write
2'h2	Reset register (load)

EAD[1:0]: Internal EPROM address. Set EAD[1:0] = 00 ~ 10 when writing to the internal EPROM. The EAD[1:0] setting determines to which register (R28h, R29h, R2Ah) the data ED[7:0] is written.

ED[7:0]: The data written in the Internal EPROM.

Table 58

EAD[1:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
2'h0	0	0	0	0	UID[3]	UID[2]	UID[1]	UID[0]
2'h1	EVCME0*	0	0	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
2'h2	EVCME1*	0	0	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

Note*: Make sure to write "1" to EVCME0, EVCME1.

CALB: When CALB = 1, the R61503B executes a calibration to the internal operation. Set CALB = 1 after power-on reset. The CALB setting is automatically returned to "0".

Instruction list

Main category		Sub category		Upper code								Lower code							
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
—	Index			*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read			L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
0*	Display control 1	00h	Start oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
			Device code read	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	1
		01h	Driver output control 1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
		02h	Liquid crystal drive waveform	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0
		03h	Entry mode	TRI	DFM1	DFM0	BGR	0	DACKE	HWM		0	0	ID1	ID0	AM	0	0	0
		04h	Resize control	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
		05h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		06h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		07h	Display control 1	0	0	PTDE1	PTDE0	0	0	BASEE	0	0	0	GON	DTE	CL	0	D1	D0
		08h	Display control 2	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
		09h	Display control 3	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
		0A-0Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Ch	External display interface 1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
		0Dh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Eh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Fh	External display interface 2	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
1*	Power control	10h	Power control 1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	0	AP1	AP0	0	DSTB	SLP	STB
		11h	Power control 2	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC01	0	VC2	VC1	VC0
		12h	Power control 3	0	0	0	VON	0	0	0	VCMR	0	0	PSON	PON	VRH3	VRH2	VRH1	VRH0
		13h	Power control 4	VCOMG	0	0	0	VDV3	VDV2	VDV1	VDV0	VCMSEL	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
		14h	Power control 6	DC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		15h- 17h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		18h	Power control 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
2*	RAM Access	20h	RAM Address set (horizontal direction)	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		21h	RAM Address set (vertical direction)	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		22h	RAM data write/ read	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interface's format.															
		23h- 27h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		28h	EPROM read data 1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0
		29h	EPROM read data 2	0	0	0	0	0	0	0	0	EVCME0	0	0	EVCM04	EVCM03	EVCM02	EVCM01	EVCM00
		2Ah	EPROM read data 3	0	0	0	0	0	0	0	0	EVCME1	0	0	EVCM14	EVCM13	EVCM12	EVCM11	EVCM10
		2Bh- 2Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3*	Gamma control	30h	Gamma control 1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
		31h	Gamma control 2	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
		32h	Gamma control 3	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
		33h	Gamma control 4	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
		34h	Gamma control 5	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
		35h	Gamma control 6	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
		36h	Gamma control 7	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
		37h	Gamma control 8	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
		38h	Gamma control 9	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	VRP04	VRP03	VRP02	VPR01	VRP00
		39h	Gamma control 10	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00
		3Ah	Gamma control 11	0	0	0	VAJN14	VAJN13	VAJN12	VAJN11	VAJN10	0	0	0	VAJP04	VAJP03	VAJP02	VAJP01	VAJP00
		3Bh-3Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Main category		Sub category		Upper code								Lower code							
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4*		40h- 4Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5*	Window address control	50h	Horizontal RAM address start position	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
		51h	Horizontal RAM address end position	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
		52h	Vertical RAM address start position	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
		53h	Vertical RAM address end position	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
		54h- 5Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6*		60h- 6Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7*	Base image display control	70h	Driver output control 2	GS	0	0	NL4	NL3	NL2	NL1	NL0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
		71h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV
		72h- 79h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		7Ah	Vertical scroll control	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL5	VL3	VL2	VL1	VL0
		7Bh- 7Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8*	Partial image control	80h	Partial image 1 display position	0	0	0	0	0	0	0	0	PTDP 07	PTDP 06	PTDP 05	PTDP 04	PTDP 03	PTDP 02	PTDP 01	PTDP 00
		81h	Partial image 1 RAM area (start line)	0	0	0	0	0	0	0	0	PTSA 07	PTSA 06	PTSA 05	PTSA 04	PTSA 03	PTSA 02	PTSA 01	PTSA 00
		82h	Partial image 1 RAM area (end line)	0	0	0	0	0	0	0	0	PTEA 07	PTEA 06	PTEA 05	PTEA 04	PTEA 03	PTEA 02	PTEA 01	PTEA 00
		83h	Partial image 2 display position	0	0	0	0	0	0	0	0	PTDP 17	PTDP 16	PTDP 15	PTDP 14	PTDP 13	PTDP 12	PTDP 11	PTDP 10
		84h	Partial image 2 RAM area (start line)	0	0	0	0	0	0	0	0	PTSA 17	PTSA 16	PTSA 15	PTSA 14	PTSA 13	PTSA 12	PTSA 11	PTSA 10
		85h	Partial image 2 RAM area (end line)	0	0	0	0	0	0	0	0	PTEA 17	PTEA 16	PTEA 15	PTEA 14	PTEA 13	PTEA 12	PTEA 11	PTEA 10
		86h- 8Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9*	Panel interface control	90h	Panel interface control 1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
		91h	Panel interface control 2	0	0	0	0	0	NOI2	NOI1	NOI0	0	0	0	0	0	0	0	0
		92h	Panel interface control 3	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI2	SDTI1	SDTI0
		93h	Panel interface control 4	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
		94h	Panel interface control 5	0	0	0	0	NOE3	NOE2	NOE1	NOE0	0	0	0	0	0	0	0	0
		95h	Panel interface control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE2	SDTE1	SDTE0
		96h- 97h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		98h	Source driver output control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VSEL1	VSEL0
		99h	Source driver output control 2	0	0	0	CPBWI 4	CPBWI 3	CPBWI 2	CPBWI 1	CPBWI 0	0	0	0	CPAWI 4	CPAWI 3	CPAWI 2	CPAWI 1	CPAWI 0
		9Ah	Source driver output control 3	0	0	0	CNBWI 4	CNBWI 3	CNBWI 2	CNBWI 1	CNBWI 0	0	0	0	CNAWI 4	CNAWI 3	CNAWI 2	CNAWI 1	CNAWI 0
		9Bh	Source driver output control 4	0	0	CPBW E5	CPBW E4	CPBW E3	CPBW E2	CPBW E1	CPBW E0	0	0	CPAW E5	CPAW E4	CPAW E3	CPAW E2	CPAW E1	CPAW E0
		9Ch	Source driver output control 5	0	0	CNBW E5	CNBW E4	CNBW E3	CNBW E2	CNBW E1	CNBW E0	0	0	CNAW E5	CNAW E4	CNAW E3	CNAW E2	CNAW E1	CNAW E0
		9Dh- 9Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A*	EPROM control	A0h	EPROM control 1	0	0	0	0	0	0	0	0	TE	0	EOP1	EOP0	0	0	EAD1	EAD0
		A1h	EPROM control 2	0	0	0	0	0	0	0	0	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		A2h-A3h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
		A5h-AFh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reset Function

The R61503B is initialized by the RESET input. During reset period, the R61503B is in a busy state and instruction from the MPU and GRAM access are not accepted. The R61503B's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 10 ms). During this period, GRAM access and initial instruction setting are prohibited.

1. Initial state of instruction bits (default)

See the instruction list of p.89. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (D1-0 = "00").

3. Output pin initial state * see Note

1.	LCD driver S1~S528	: GND
	G1~G220	: VGL (= GND)
2.	Vcom	: GND
3.	VcomH	: GND
4.	VcomL	: GND
5.	VREG1OUT	: VGS
6.	VciOUT	: Hi-z
7.	DDVDH	: Vci
8.	VGH	: DDVDH (= Vci)
9.	VGL	: GND
10.	Oscillator	: Oscillate

4. Initial state of input/output pins* see Note

1.	C11+	: Hi-z
2.	C11-	: Hi-z
3.	C13+	: Vci1 (= Hi-z)
4.	C13-	: GND
5.	C21+	: DDVDH (= Vci)
6.	C21-	: GND
7.	C22+	: DDVDH (= Vci)
8.	C22-	: GND
9.	VDD	: VDD

Note: The initial states of output and input pins become the states mentioned in the above when the R61503B's power supply circuit is connected as exemplified in "Connection example".

5. Note on Reset function

- When a RESET input is entered into the R61503B while it is in deep standby mode, the R61503B starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in deep standby mode.
- When transferring instruction and data in either two or three transfers via 8-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

Interface and data format

The R61503B supports system interface for setting instructions etc, and external display interface for displaying a moving picture. The R61503B can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61503B supports RGB interface and VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the R61503B writes display data while the data enable signal (ENABLE) allows write operation via RGB data signal bus (DB17-0). The display data is stored in the R61503B's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously. To access the R61503B's internal RAM in high speed with low power consumption, use high-speed write function (HWM = 1) in RGB or VSYNC interface operation.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The R61503B operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register. When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 59

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still picture)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving picture)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still picture while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

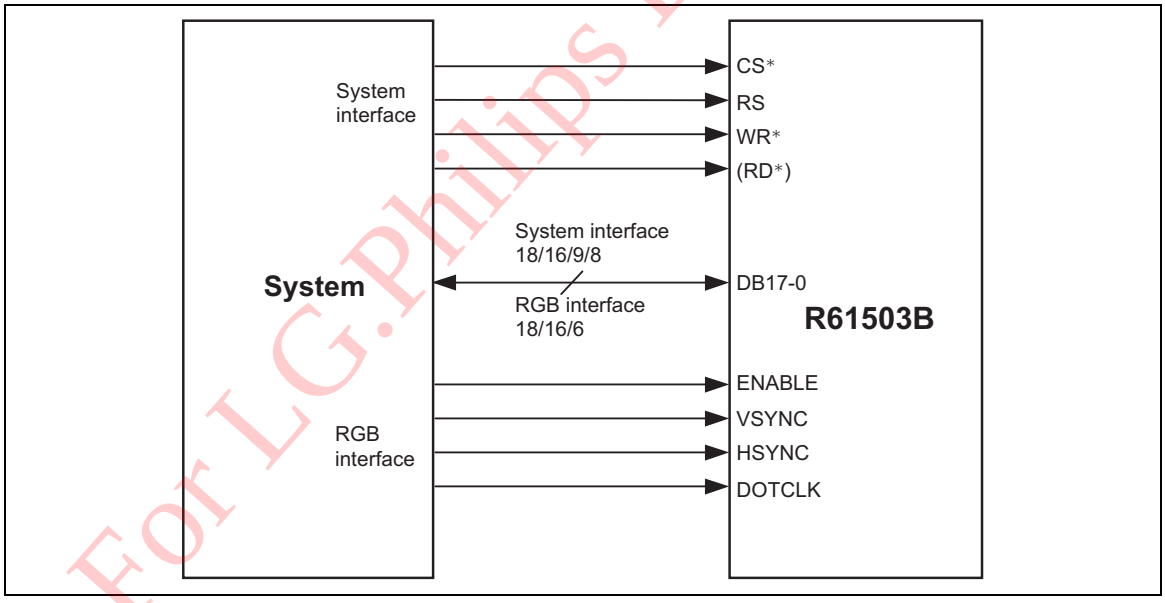


Figure 19

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61503B transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function can minimize the total number of data transfer for moving picture display by transferring only the data to be written in the moving picture RAM area when it is written and enables the R61503B to display a moving picture and the data in other than the moving picture RAM area simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61503B by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the setting of these periods.

RGB interface operation (2)

This mode enables the R61503B to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61503B to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61503B according to the instruction settings for these periods.

System Interface

The following kinds of system interface are available with the R61503B and the interface is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 60 IM bits settings and system interface

IM3	IM2	IM1	IM0	Interface operation	DB Pins	Colors
0	0	0	0	Setting disabled	-	-
0	0	0	1	Setting disabled	-	-
0	0	1	0	80-system 16-bit interface	DB17-10 and DB8-1	65,536, 262,144 See Note 1
0	0	1	1	80-system 8-bit interface	DB17-10	65,536, 262,144 See Note 2
0	1	0	*	Clock synchronous serial interface	DB1-0	65,536
0	1	1	*	Setting disabled	-	-
1	0	0	0	Setting disabled	-	-
1	0	0	1	Setting disabled	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	*	*	Setting disabled	-	-

Notes : 1. 262,144 colors in 2 transfers, 65,536 colors in 1 transfer.
2. 262,144 colors in 3 transfers, 65,536 colors in 2 transfers.

80-system 18-bit interface

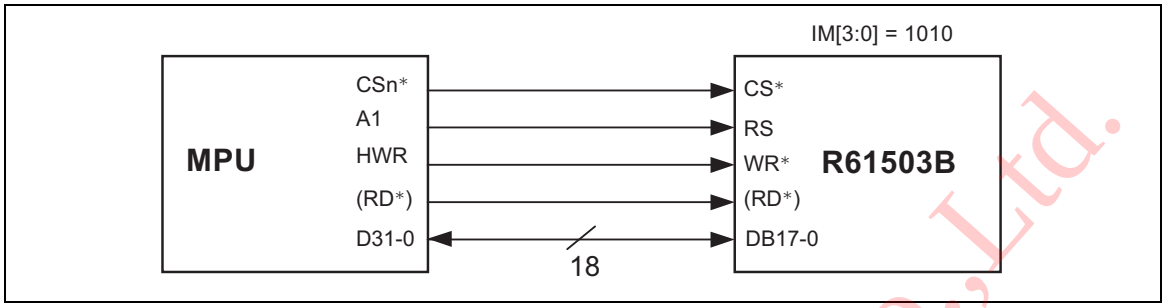


Figure 20

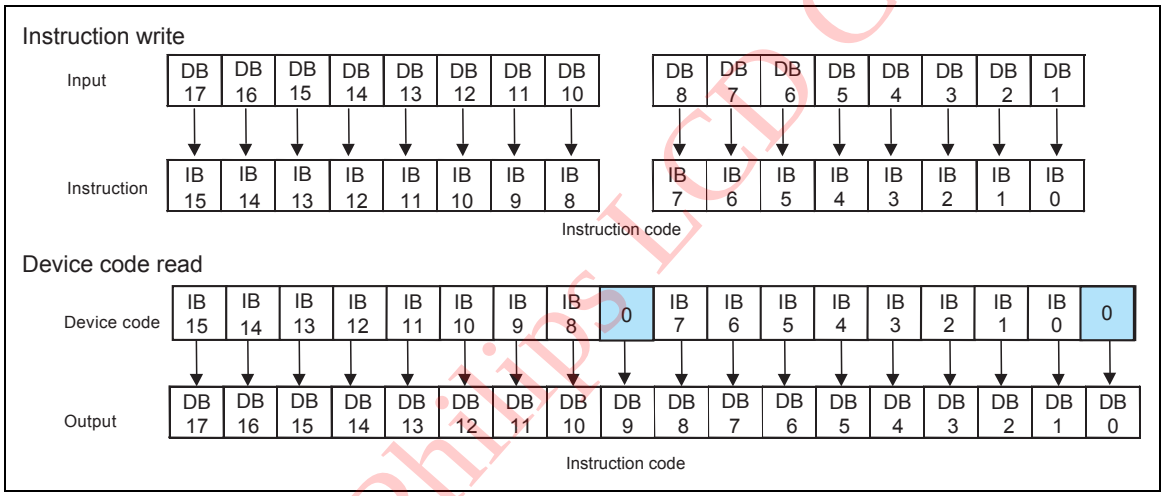


Figure 21 Instruction/Device code read (18-bit interface)

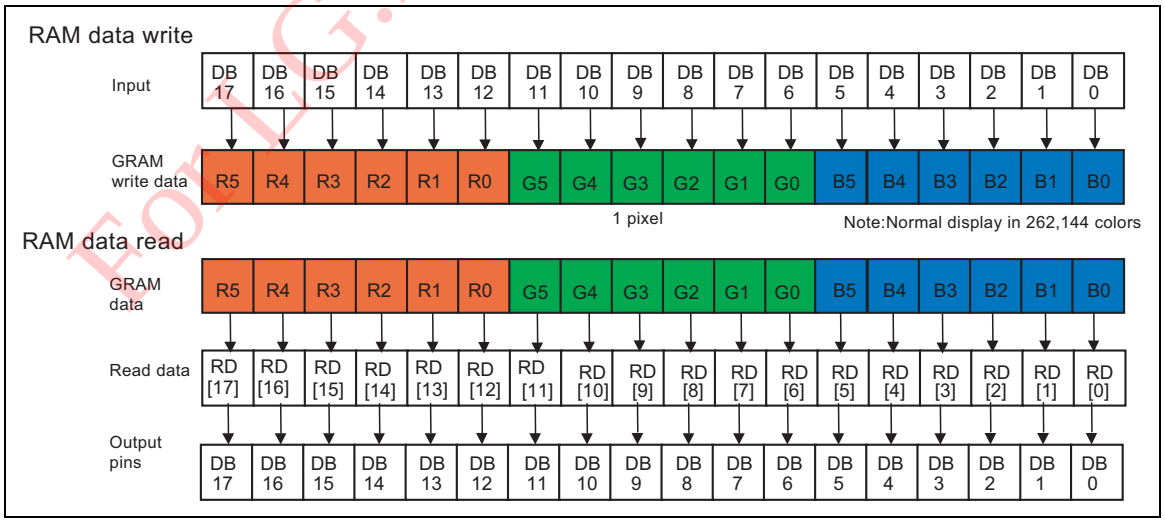


Figure 22 RAM data write/read (18-bit interface)

80-system 16-bit interface

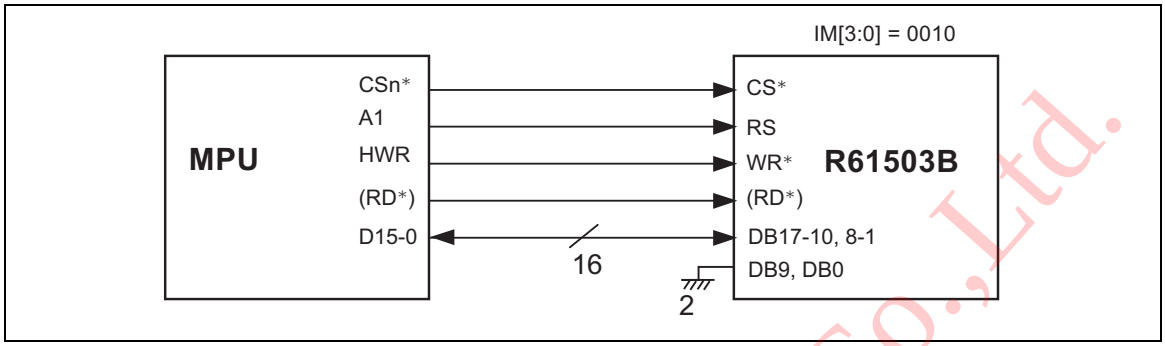


Figure 23

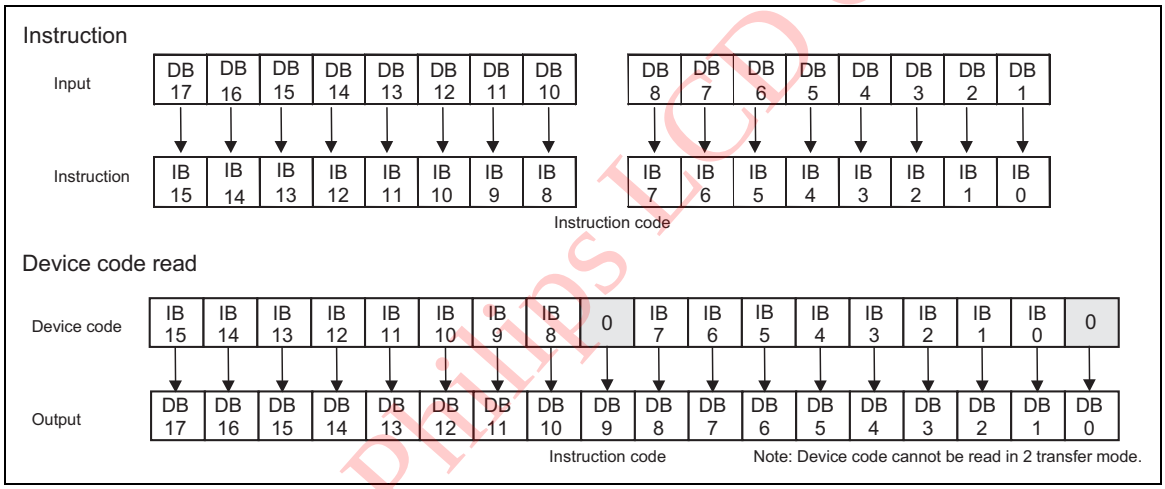


Figure 24 Instruction/Device code read (16-bit interface)

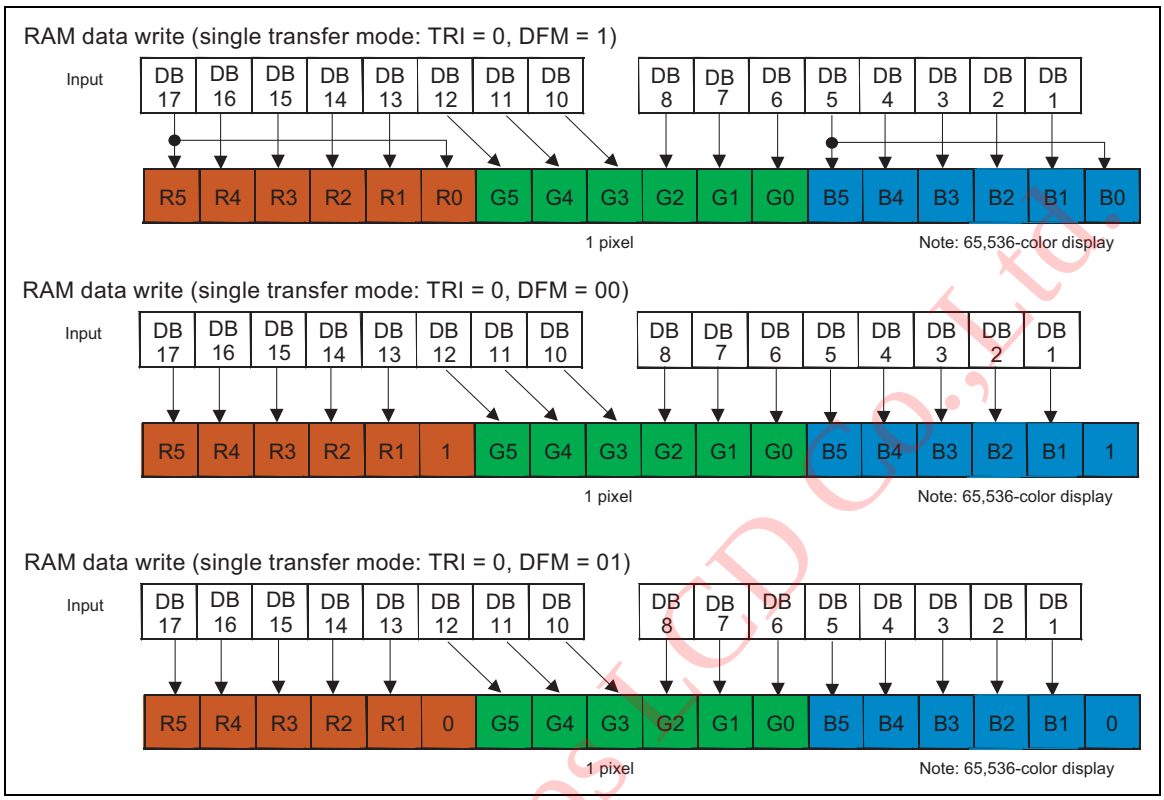


Figure 25 RAM data write (16-bit interface)

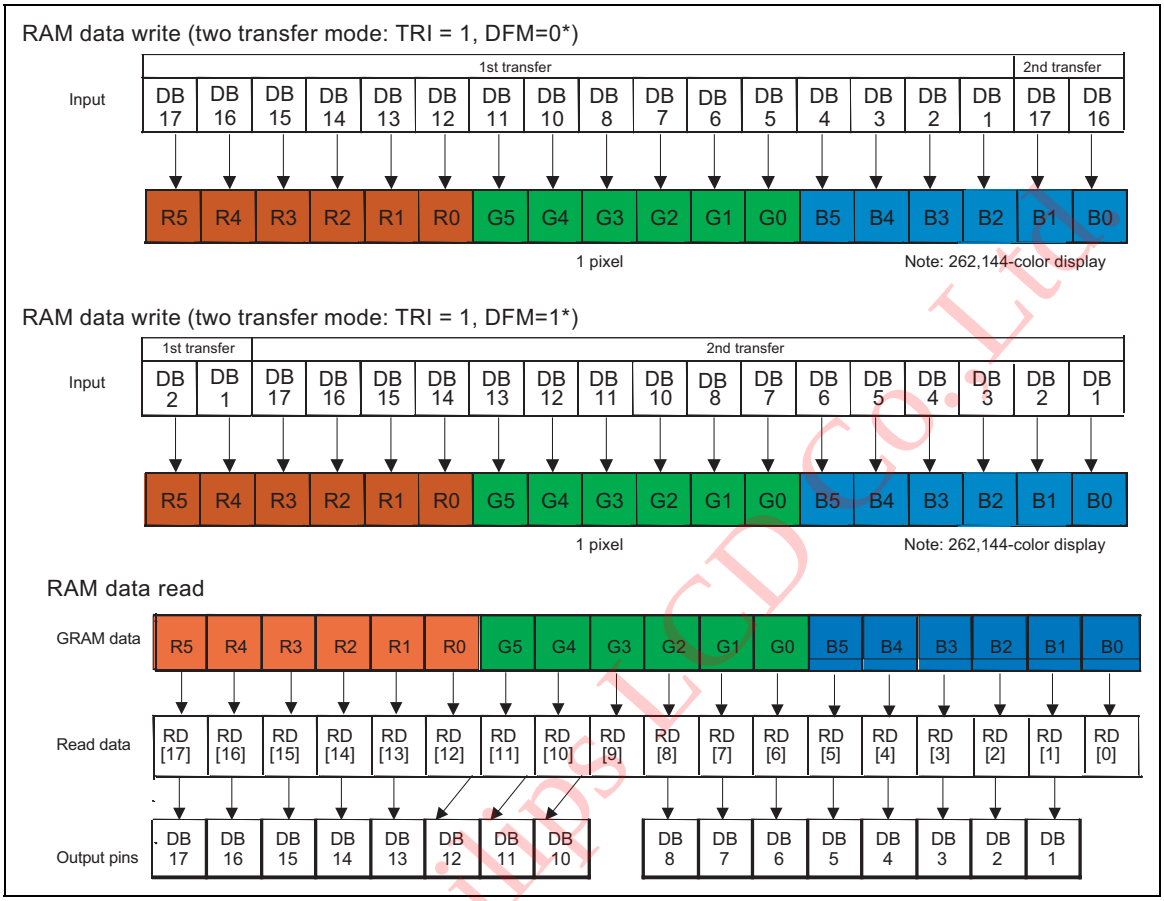


Figure 26 RAM data write/read (16-bit interface)

80-system 9-bit interface

When transferring 16-bit instruction via 9-bit interface (DB17~DB9), it is divided into upper and lower 8 bits (DB9 is not used) and the upper 8 bits are transferred first. The RAM write data is divided into upper and lower 9 bits and the upper 9 bits are transferred first. The unused DB8-0 pins must be fixed at either IOVcc or IOGND level. When writing in the index register, make sure to write the upper byte (8 bits).

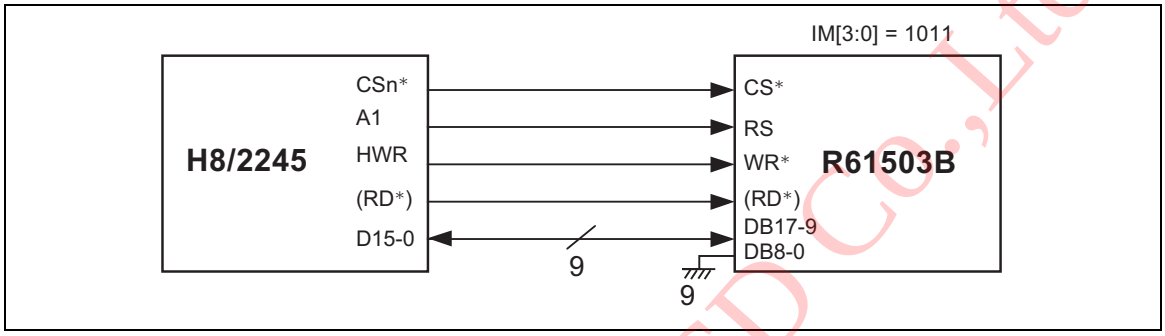


Figure 27

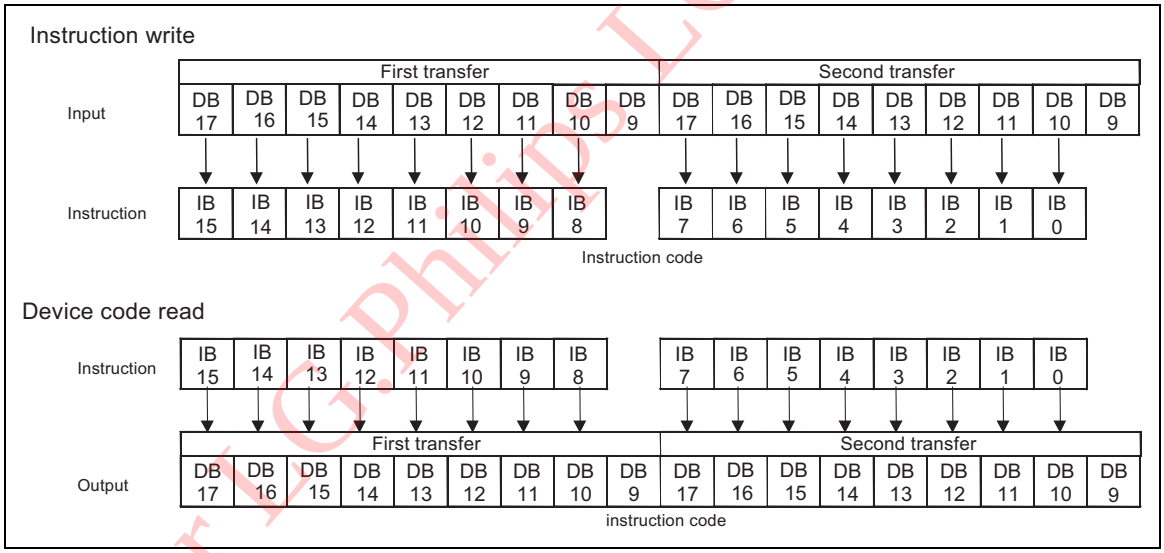


Figure 28 Instruction/Device code read (9-bit interface)

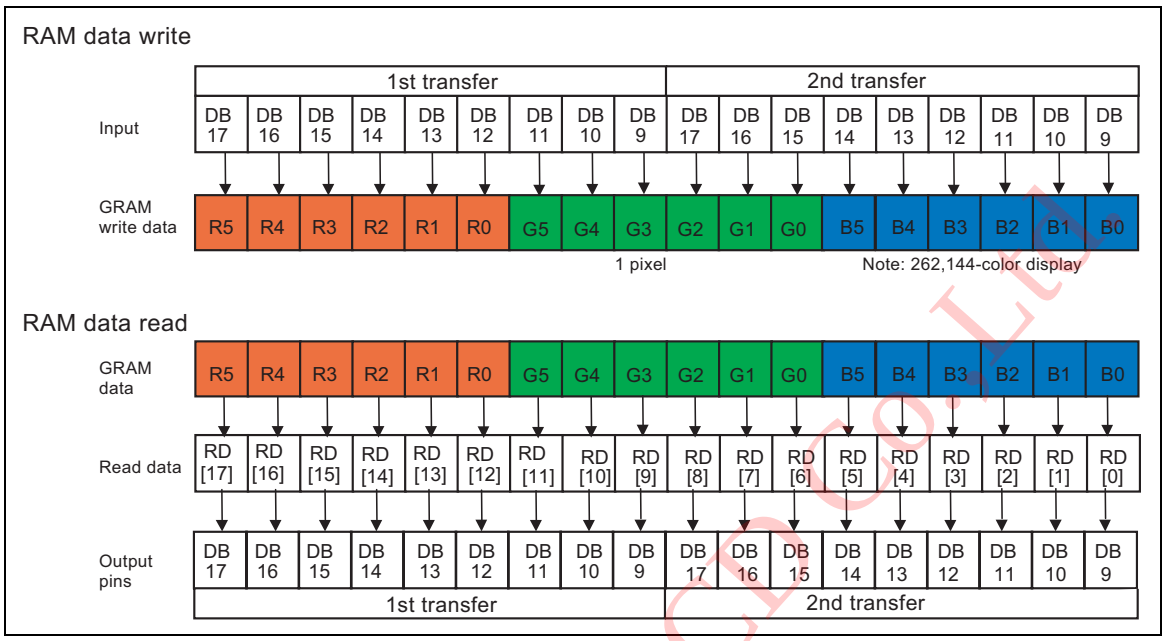


Figure 29 RAM data write/read (9-bit interface)

The R61503B supports data transfer synchronization function to reset the counters, which count the number of upper and lower 9 bits when transferring data via 9-bit bus interface. If a mismatch occurs in transferring upper and lower 9 bits due to noise and so on, "00"H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 9 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

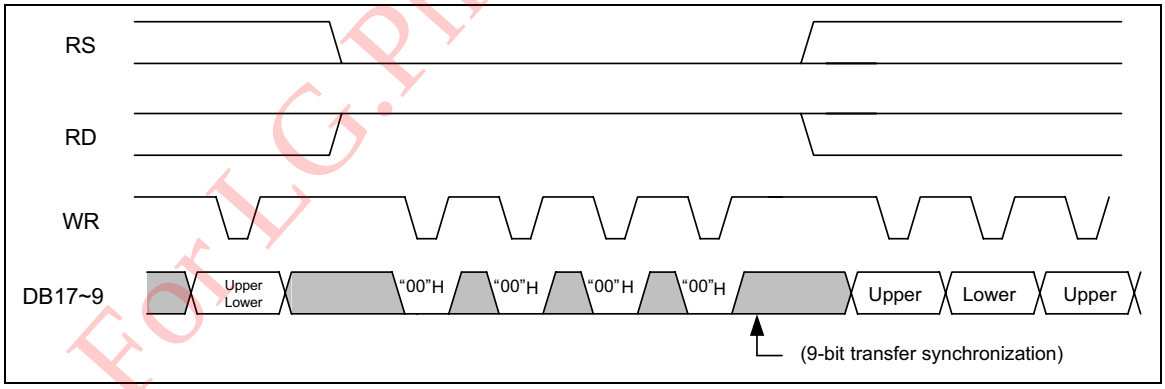


Figure 30 Data transfer synchronization (9-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

80-system 8-bit interface

When transferring 16-bit instruction via 8-bit interface (DB17~DB10), it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM write data is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The unused DB9-0 pins must be fixed at either IOVcc or IOGND level. When writing in the index register, make sure to write the upper byte (8 bits).

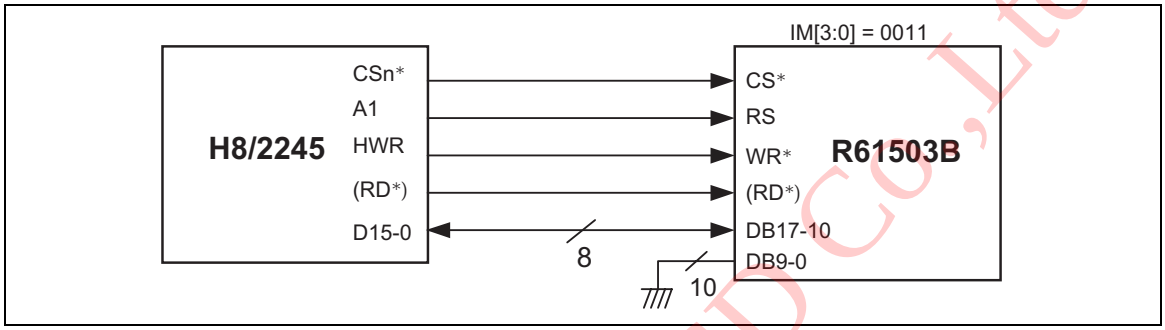


Figure 31

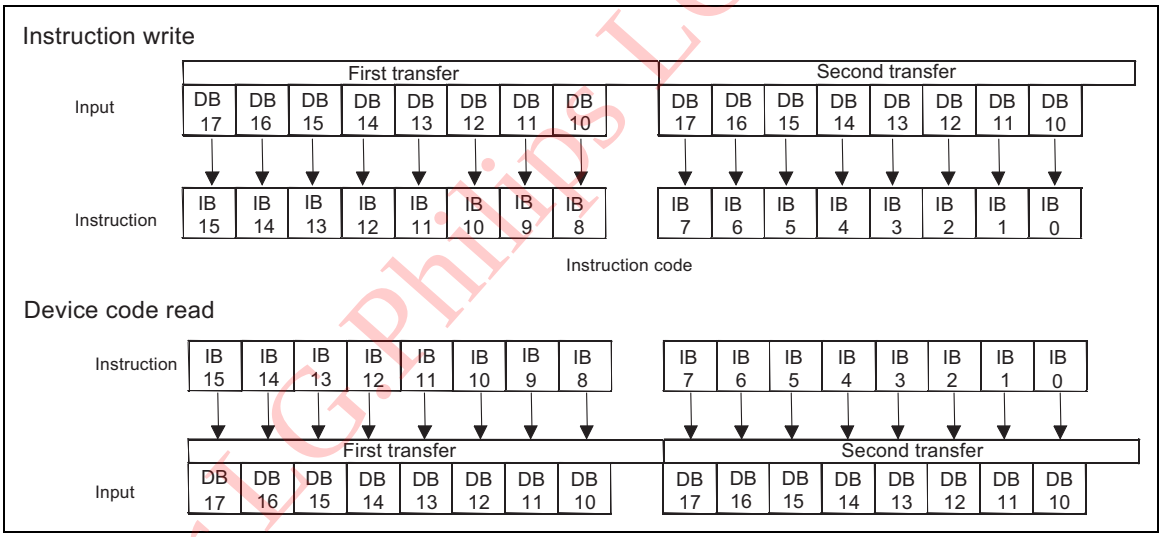


Figure 32 Instruction/Device code read (8-bit interface)

Note: Data cannot be read in 3-transfer mode.

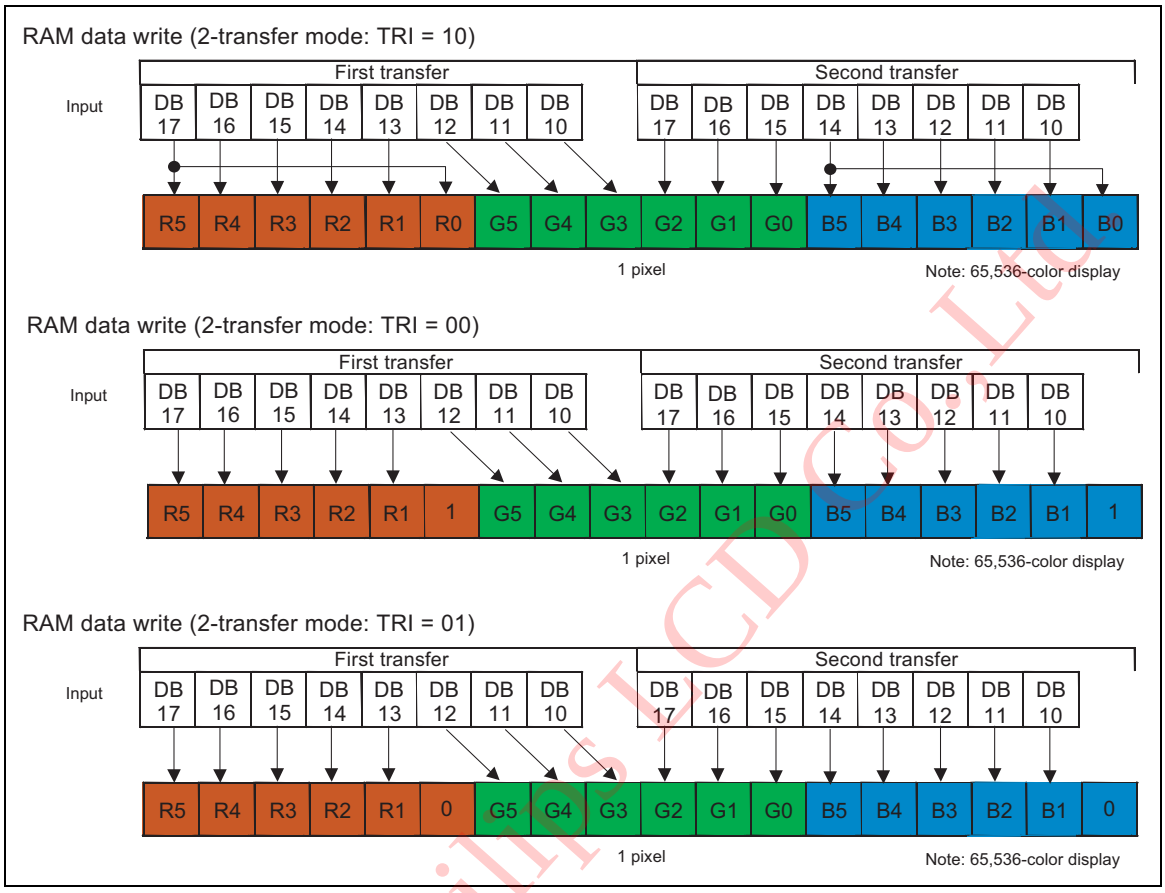


Figure 33 RAM data write (8-bit interface)

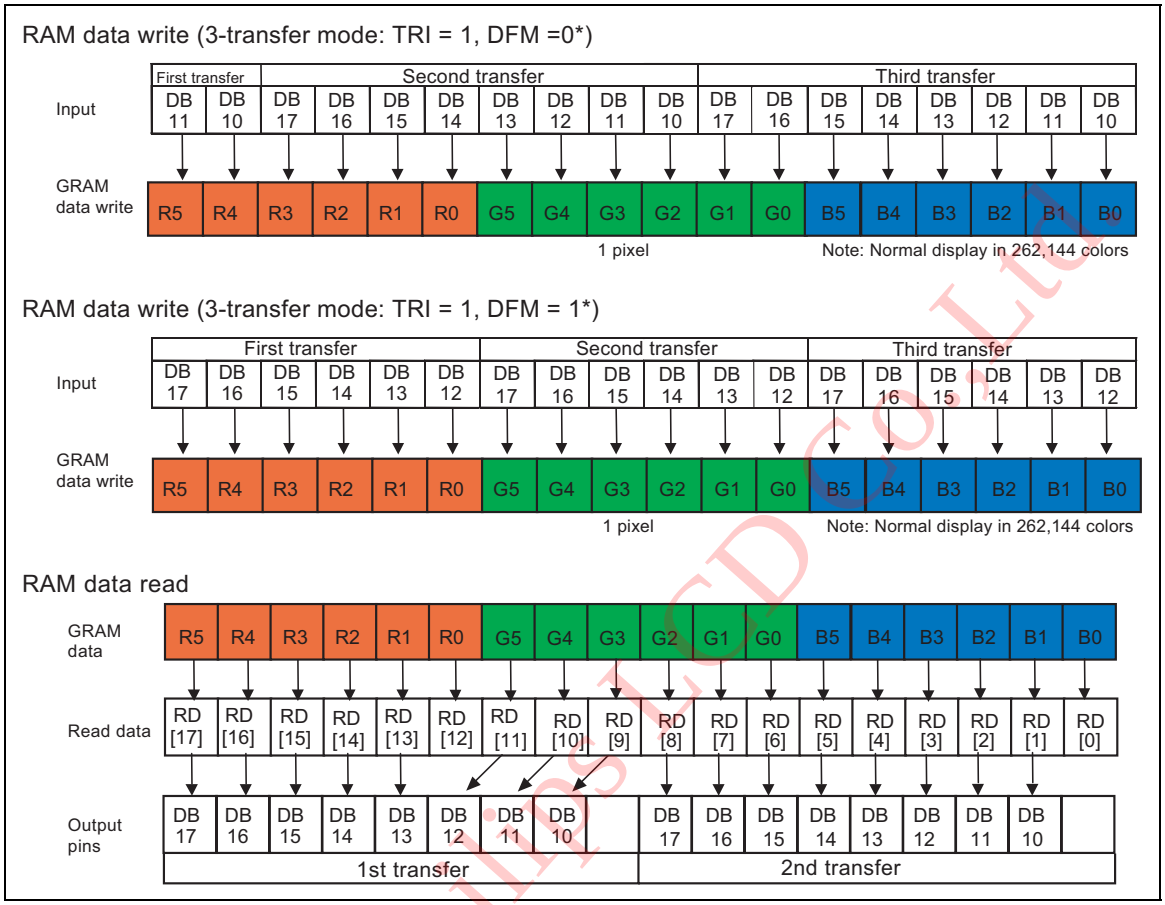


Figure 34 RAM data write/read (8-bit interface)

Note: Data cannot be read in 3-transfer mode.

The R61503B supports data transfer synchronization function to reset the counters, which count the number of upper and lower 8 bits when transferring data via 8-bit bus interface. If a mismatch occurs in transferring upper and lower 8 bits due to noise and so on, “00”H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 8 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

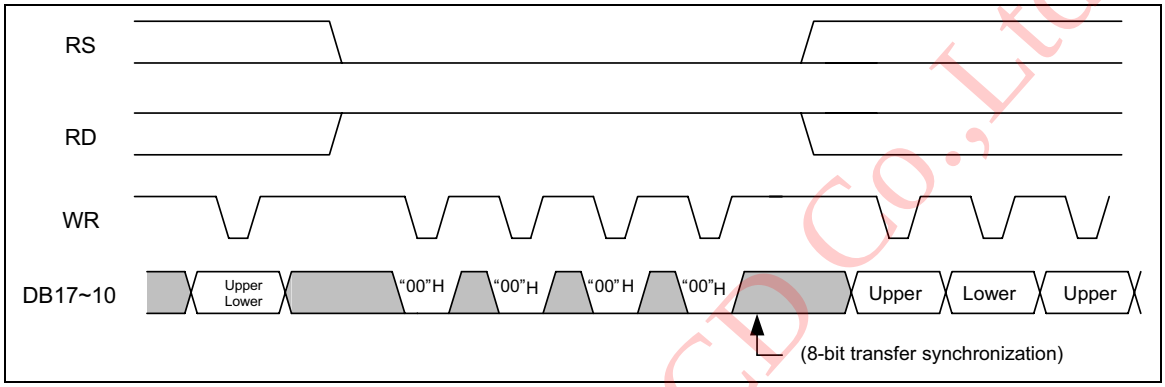


Figure 35 Data transfer synchronization (8-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

Serial interface

The serial interface is selected by setting the IM3/2/1 pins to IOGND/IOVcc/IOGND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The R61503B recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The R61503B is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the R61503B are compared and both 6-bit data match. Then, the R61503B starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the R61503B because the seventh bit of the start byte is register select bit (RS). When RS = 0, either index register write or status read operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61503B receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The R61503B writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the R61503B starts transferring or receiving data in units of bytes. The R61503B transfers data from the MSB. The R61503B's instruction consists of 16 bits and it is executed inside the R61503B after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The R61503B expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the R61503B following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The R61503B sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 61 Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is selected by setting the IM0/ID pin.

Table 62

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

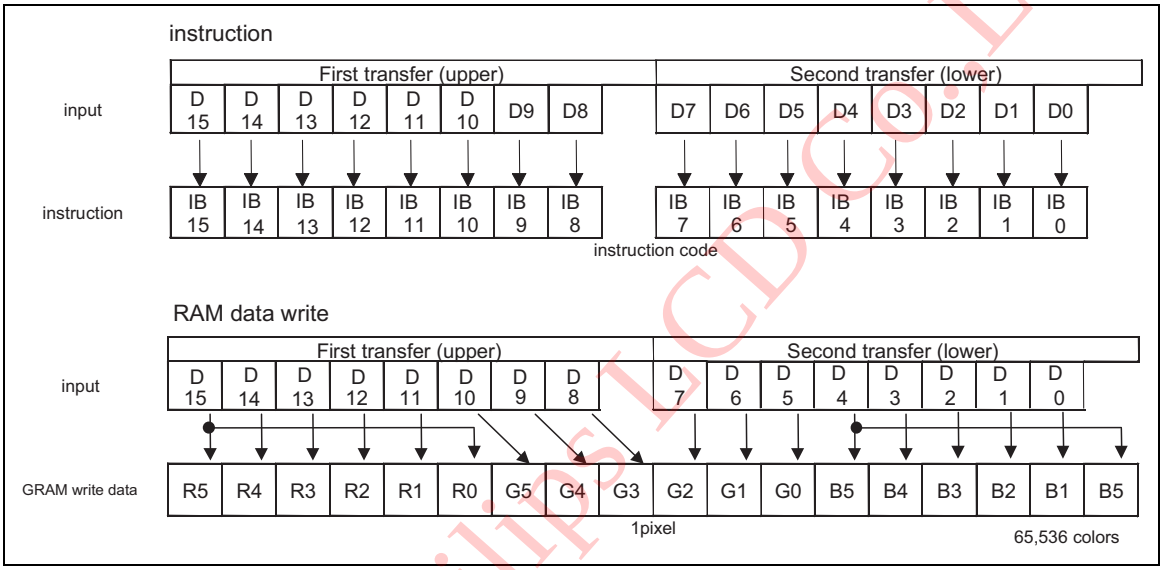


Figure 36 Instruction /RAM data write (Serial interface)

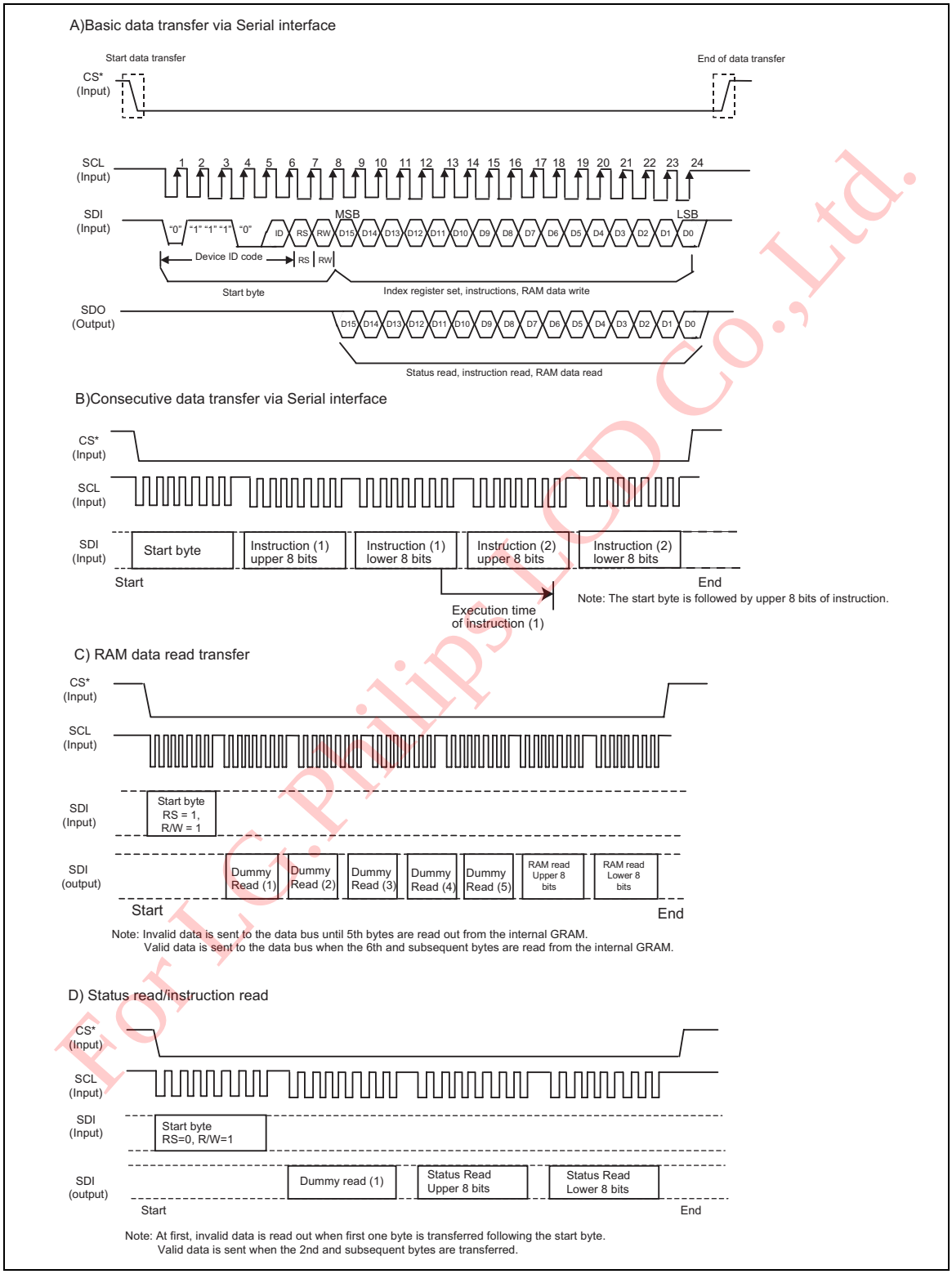


Figure 37 Serial interface data transfer timing

DMA transfer Single Address mode

The R61503B supports DMA transfer single address mode in order to perform data read operation from memory and data write operation to the R61503B in the same bus cycle, when the R61503B is connected with a microcomputer or an application processor compliant to the DMA transfer single address mode and SRAM or pseudo SRAM. By transferring data in this mode when transferring a large volume of data from external memory to the LCD driver, it becomes possible to reduce the time required for the data transfer and avoid occupying the data bus for a long period of time.

1. Pin function in DMA single address operation

DACK: In DMA single address mode, it serves as the same function as the CS pin of normal data transfer mode.

RD: the output is recognized as write strobe signal (WR) internally when the DACK pin is set to the low level (active).

WR: Fix WR to the "high" level.

CS: Fix CS to the "high" level.

RS: It is recognized "High" inside the R61503B to allow data transfer whenever the DACK pin is set to the low level (active).

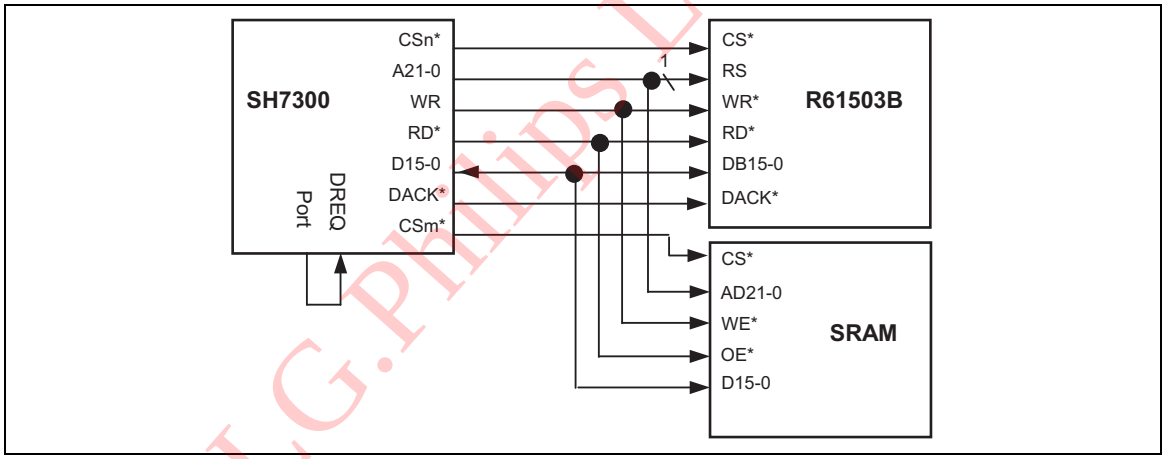


Figure 38

2. Sequence of transfer in DMA single address mode

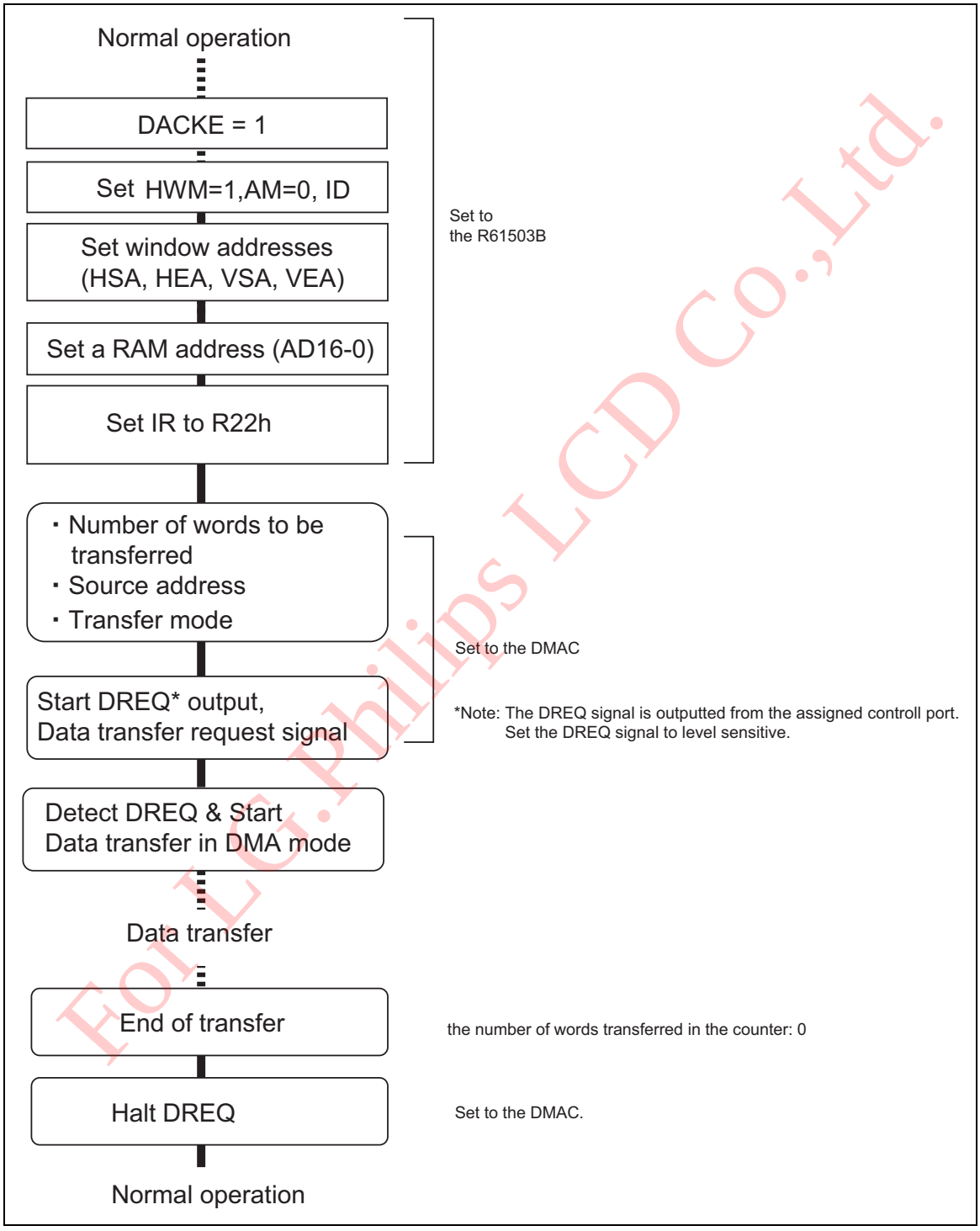


Figure 39

3. Notes to DMA single address mode

1. Do not set the DACK* pin and the CS* pin to the low level (active) simultaneously.
2. Once the system enters this mode and start transferring data, command access to the R61503B is prohibited.
3. Use high-speed write mode (HWM = 1) and write in horizontal direction when writing data in DMA single address mode.
4. Use the window address function and make sure the number of data transfer in DMA single address mode coincides with the number of data written in the window address area.
5. Wait at least for a time to complete two RAM write operations (time for 2 bus cycle periods of normal write operation, t_{cycw} x 2) after completing data transfer before issuing next instruction.
6. The R61503B does not support the data transfer from the R61503B to the external memory.
7. The DMA single address transfer mode of the R61503B is compliant to the normal cycle steal mode and the burst mode.

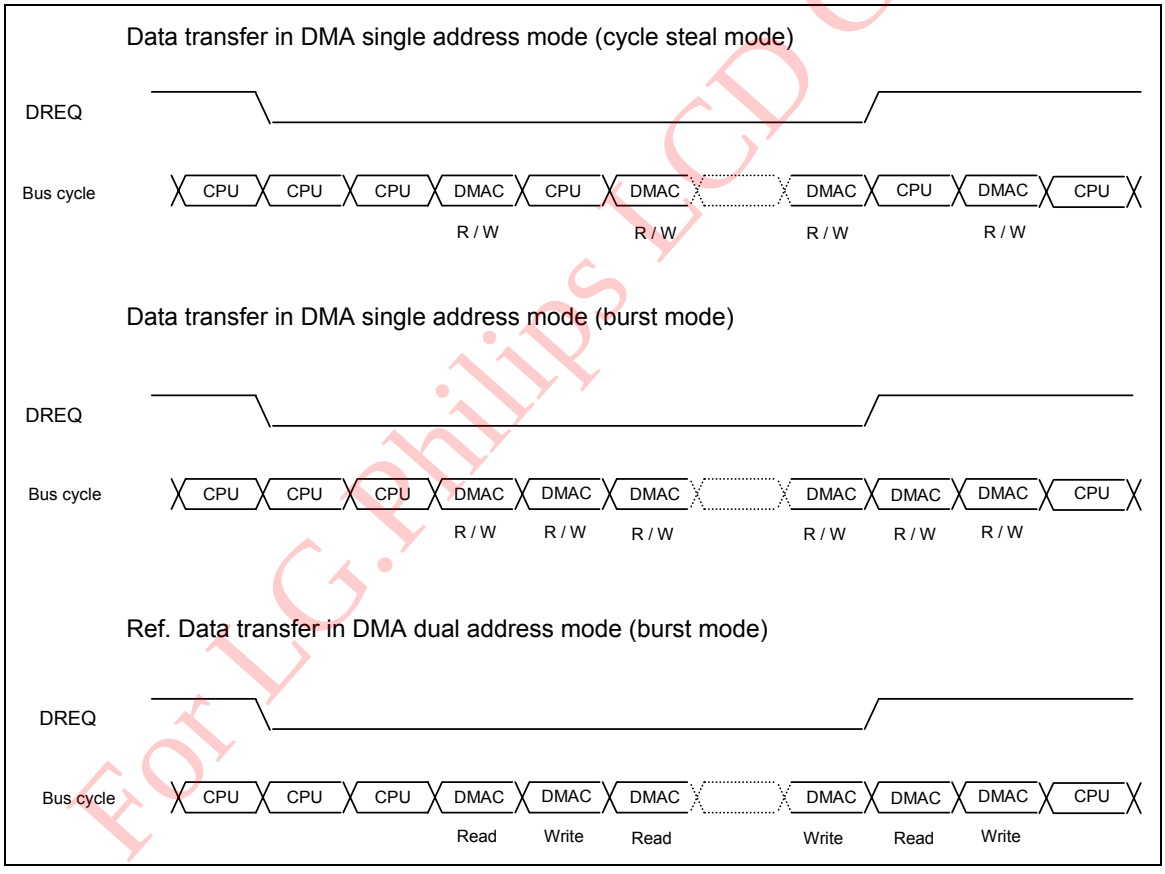


Figure 40

VSYNC Interface

The R61503B supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

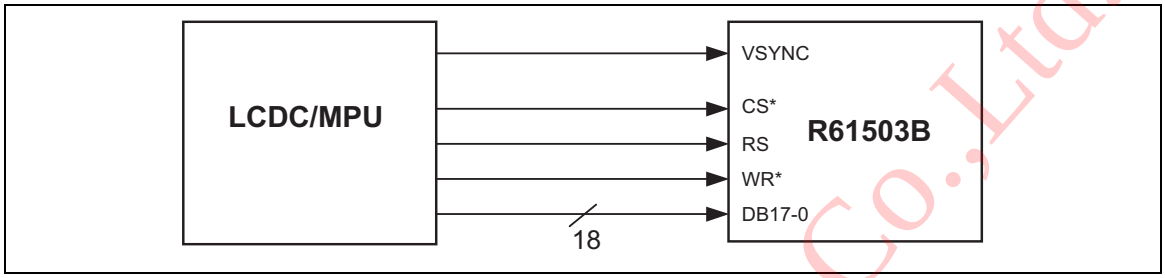


Figure 41 VSYNC interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61503B rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. By writing data using high-speed write function (HWM =1), the R61503B can write data via VSYNC interface in high speed with low power consumption.

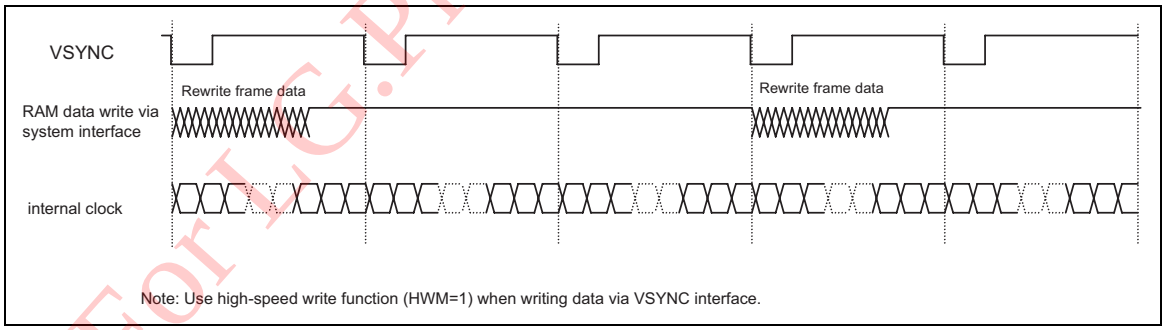


Figure 42 Moving picture data write via VSYNC

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$\textit{Internal clock frequency (fosc) [Hz]}$$
$$= \textit{FrameFrequency} \times (\textit{DisplayLines}(NL) + \textit{FrontPorch}(FP) + \textit{BackPorch}(BP)) \times 16(\textit{clocks}) \times \text{var}\,\textit{iance}$$

$$\textit{RAMWriteSpeed}(\text{min.})[Hz] > \frac{176 \times \textit{DisplayLines}(NL)}{(\textit{BackPorch}(BP) + \textit{DisplayLines}(NL) - m\,\text{arg}\,\textit{ins}) \times 16(\textit{clocks}) \times \frac{1}{\textit{fosc}}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Display size	176 RGB × 220 lines
Display lines	220 lines
Back/front porch	14/2 lines (BP = 1110/ FP = 0010)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]
= 60 Hz × (220 + 2 + 14) lines × 16 clocks × 1.1 / 0.9 = 277 kHz

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 176 × 220 / {((14 + 220 - 2) lines × 16 clock) / 277 kHz} = 2.89 MHz

Notes: 1. In this example, it is assumed that the R61503B starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the R61503B has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 2.89MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61503B starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

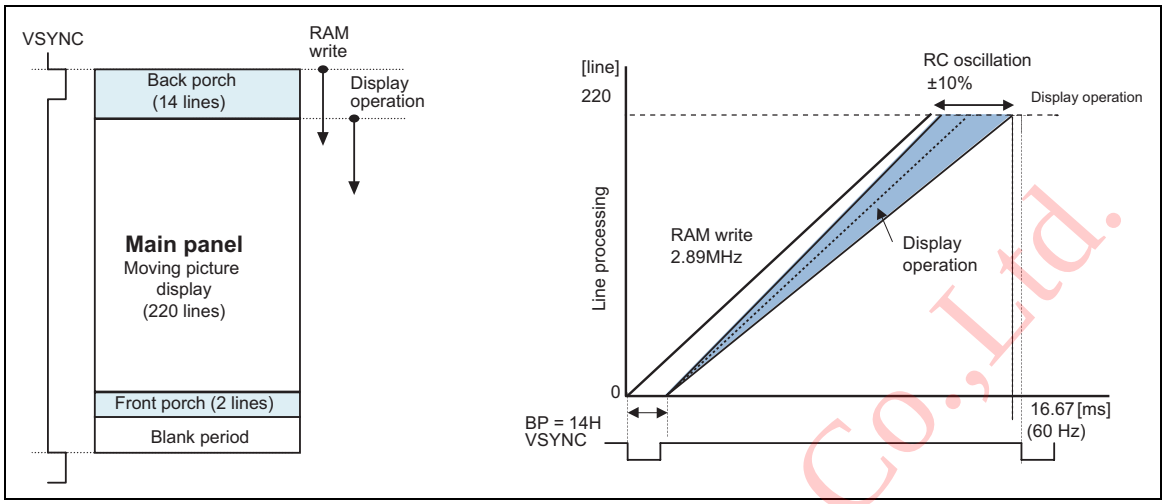


Figure 43 Write/display operation timing via VSYNC interface

Notes to VSYNC Interface operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margins in setting RAM write speed for VSYNC interface operation.

2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

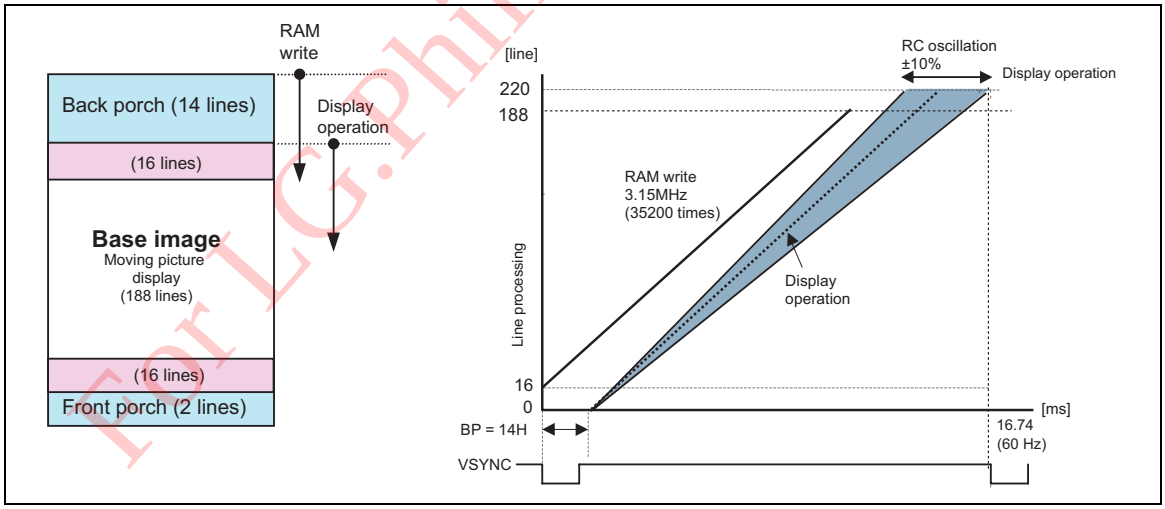


Figure 44 RAM write speed margin

3. The front porch period continues from the end of one frame period to the next VSYNC input.

4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.

5. The partial display and vertical scroll functions and interlaced scan are not available in VSYNC interface operation.

6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.

7. In VSYNC interface operation, use high-speed write function (HWM = 1) when writing display data to the internal RAM.

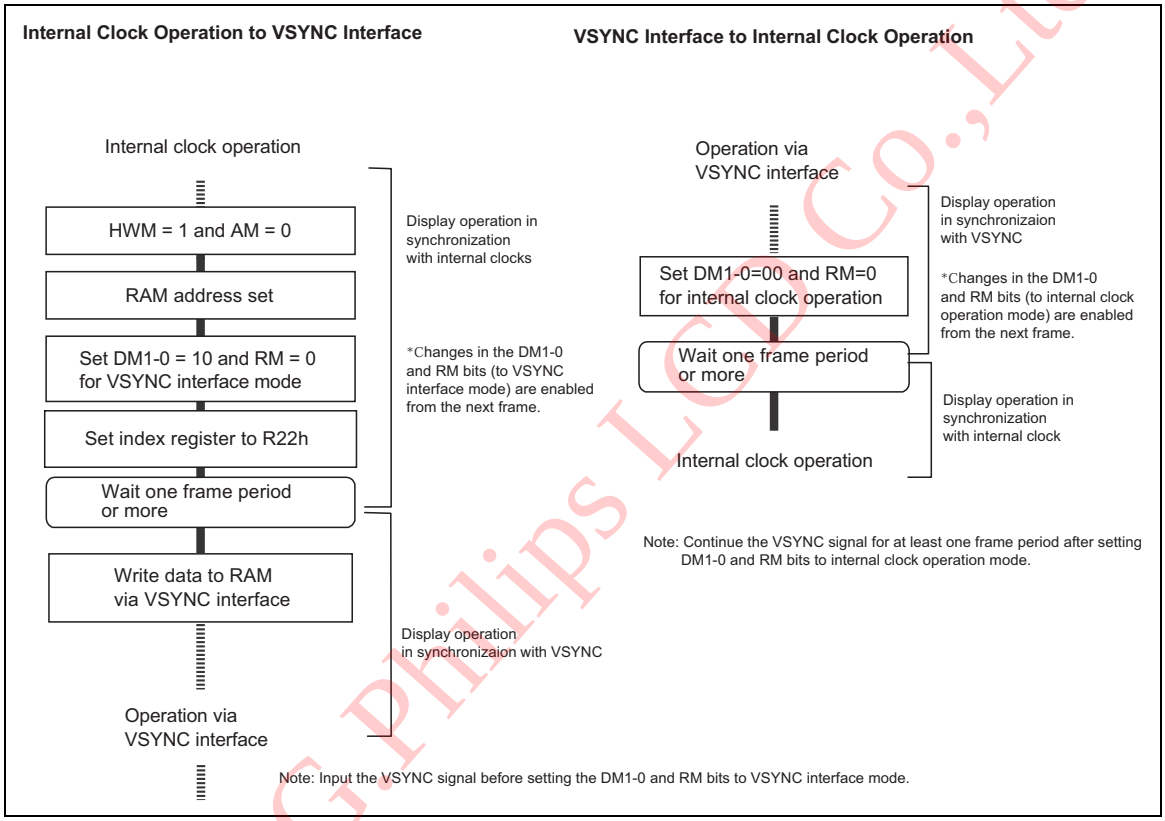


Figure 45 Sequence to switch between VSYNC and Internal clock operation modes

External Display Interface

The R61503B supports the RGB interface. The interface format is set by RM[1:0] bits. The internal RAM is accessible via RGB interface.

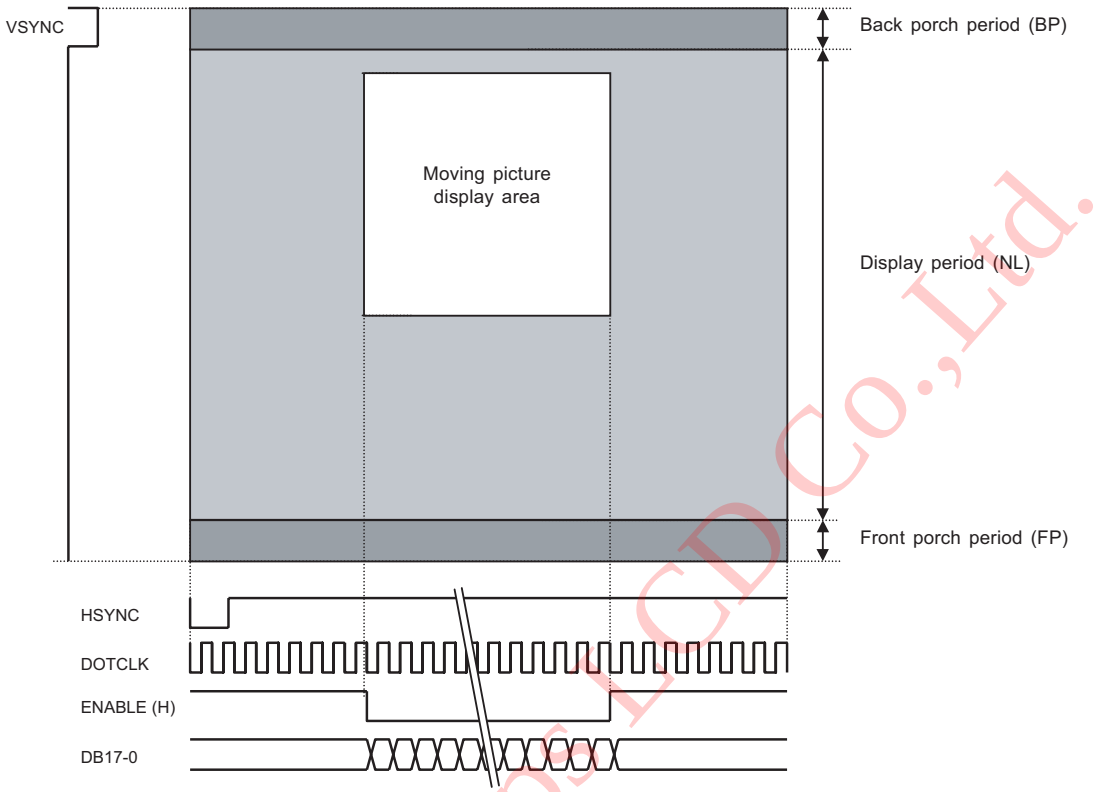
Table 63

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-10, DB8-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	-

Note: Using more than one RGB interface at a time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function and high-speed write mode (HWM = 1). In RGB interface operation, front and back porch periods must be made before and after the display period.



VSYNC: Frame synchronization signal	Back porch period (BPP):	14H ≧ BP ≧ 2H
HSYNC: Line synchronization signal	Front porch period (FPP):	14H ≧ FP ≧ 2H
DOTCLK: Dot clock		FPP + BPP = 16H
ENABLE: Data enable signal	Display period:	NL ≦ 220H
DB 17-0: RGB (6:6:6) display data	The number of lines for one frame:	FPP + NL + BPP

Notes: 1. The front porch period continues until next VSYNC input is detected.
2. Make sure the frequencies of VSYNC, HSYNC, and DOTCLK can guarantee the resolution required for the panel.
3. Keep DOTCLK input throughout the RGB interface operation.

Figure 46

ENABLE signal function

The following table shows the relationship between the ENABLE, EPL setting and RAM access operation. Whenever the R61503B performs write operation, ENABLE must be “Low” to allow write operation but this is not the determinant of enabling automatic address update in RAM write operation. EPL controls the active polarity of ENABLE signal.

Table 64

EPL	ENABLE	RAM write	RAM address
0	0	Enable	Update
0	1	Disenable	Retain
1	0	Disenable	Retain
1	1	Enable	Update

RGB interface timing

Signal timing chart of 16/18-bit RGB interface

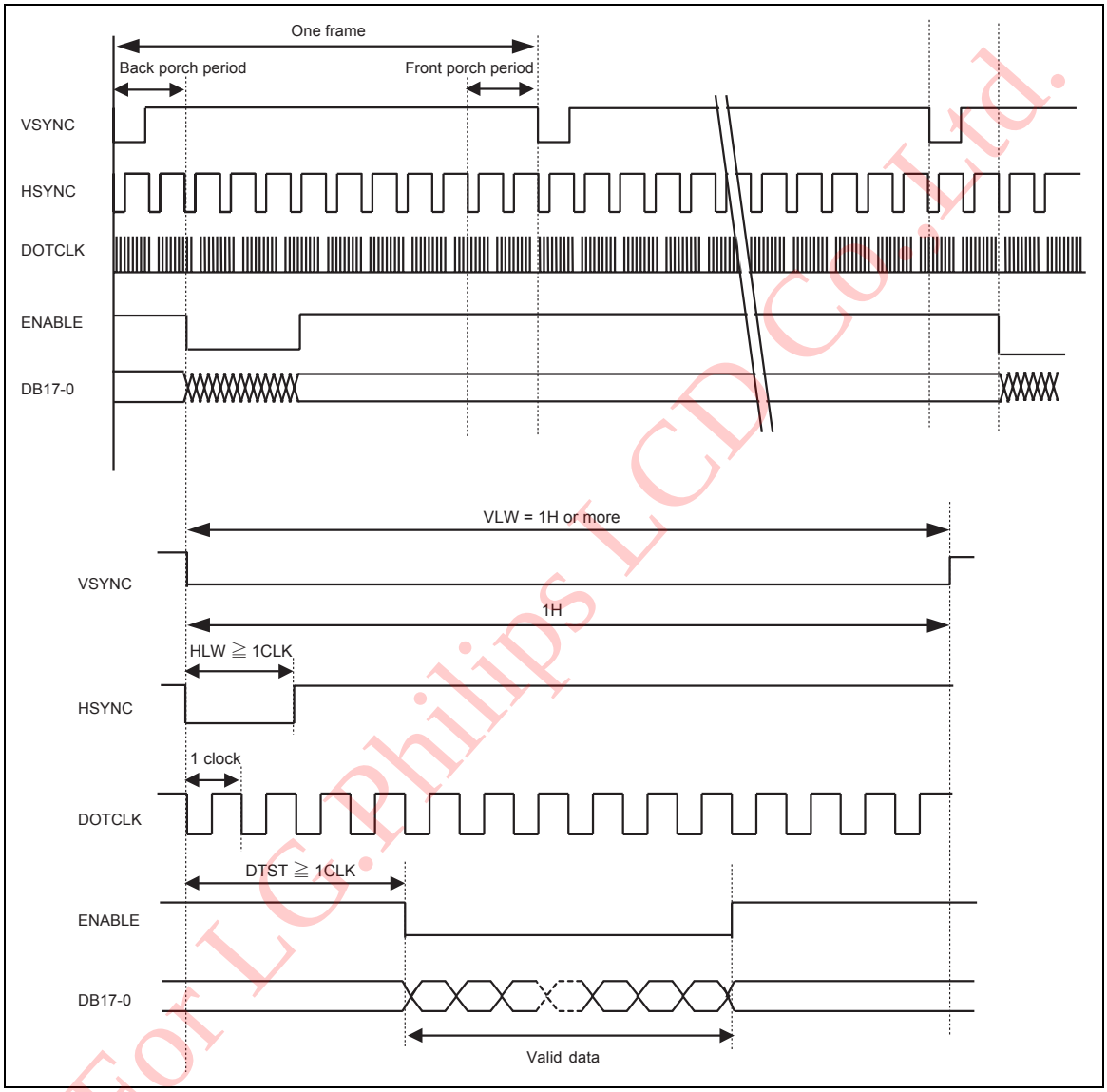


Figure 47

Notes: 1. VLW: VSYNC “Low” period
HLW: HSYNC “Low” period
DTST:data transfer setup time
2. Use high-speed write function (HWM = “1”) when writing data via RGB interface.

Timing chart of signals in 6-bit RGB interface operation

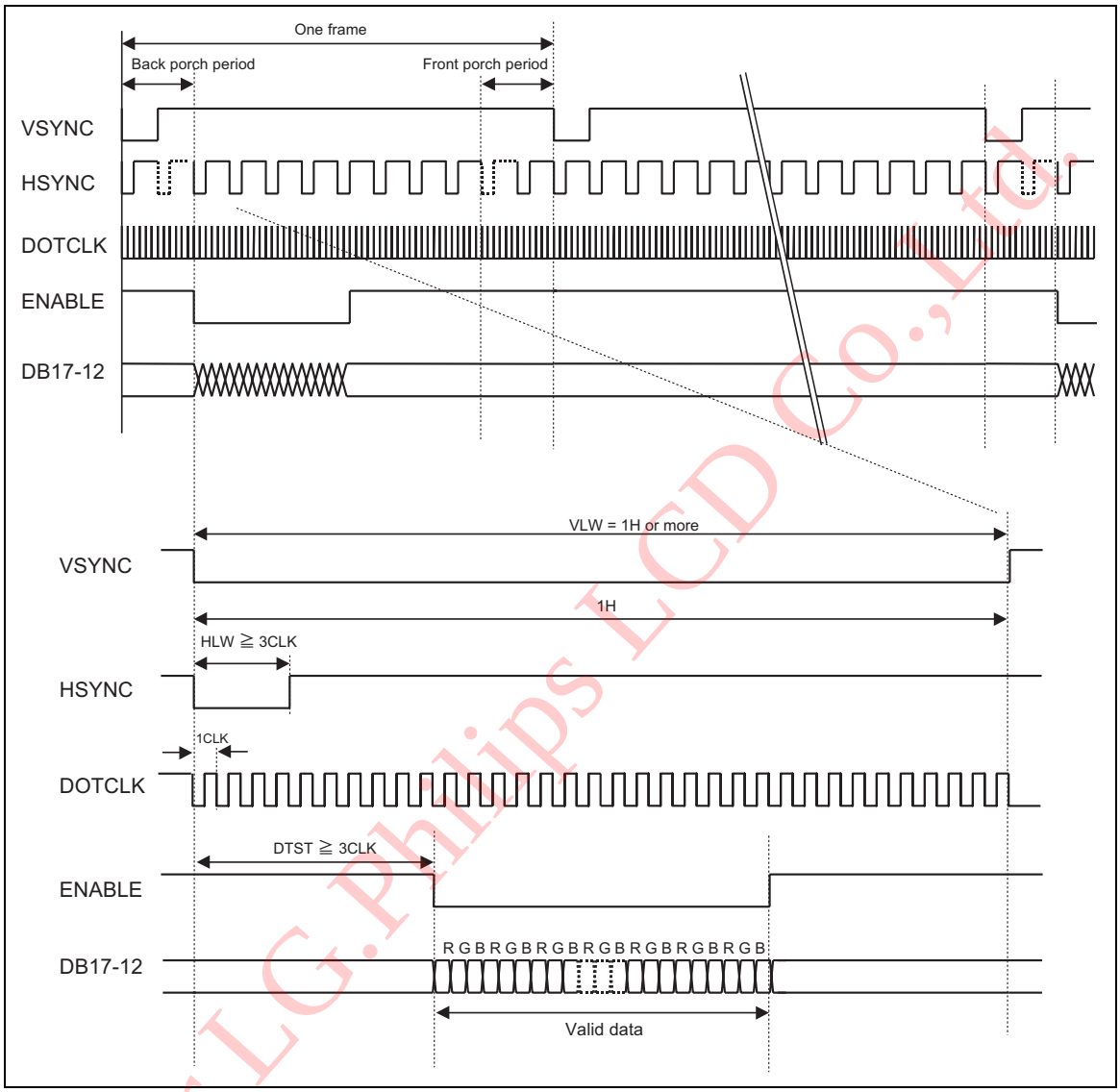


Figure 48

Notes: 1. VLW: VSYNC "Low" period
HLW: HSYNC "Low" period
DTST:data transfer setup time

2. Use high-speed write function (HWM = "1") when writing data via RGB interface.
3. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel data is transferred in units of three clocks via DB17-12.

Moving Picture Display via RGB Interface

The R61503B supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. It becomes possible to transfer only the data written over the moving picture area
4. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
5. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The R61503B allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the RAM via system interface, set ENABLE “High” to stop writing data via RGB interface. Then set RM = “0” to enable RAM access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = “1” and the index register to R22h to start accessing RAM via RGB interface. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

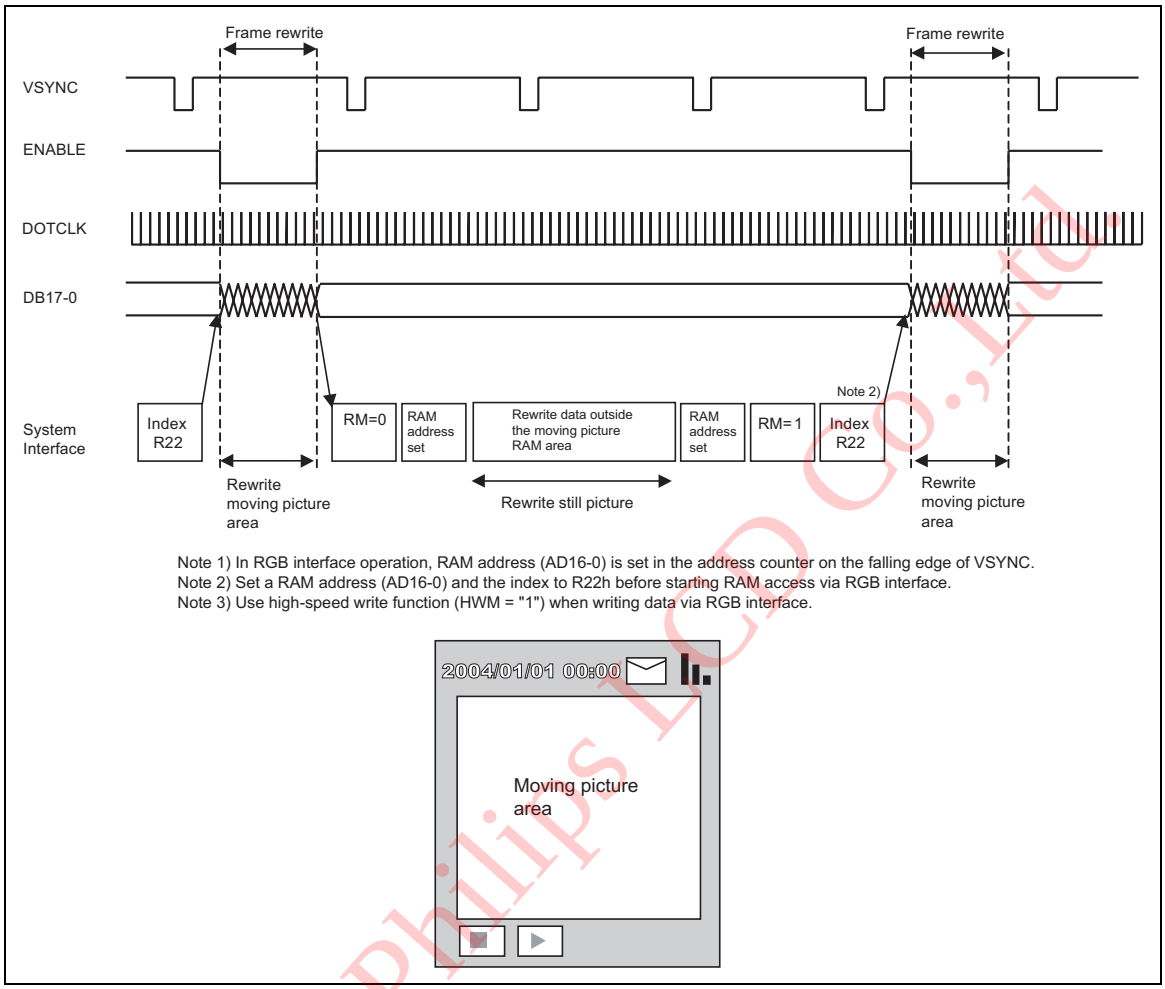


Figure 49 Updating a still picture area while displaying a moving picture

6-bit RGB interface

The 6-bit RGB interface is selected by setting the RIM1-0 bits to 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus (DB17-12) while the data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins (DB11 to 0) must be fixed at either IOVcc or GND level.

Instruction bits can be transferred only via system interface.

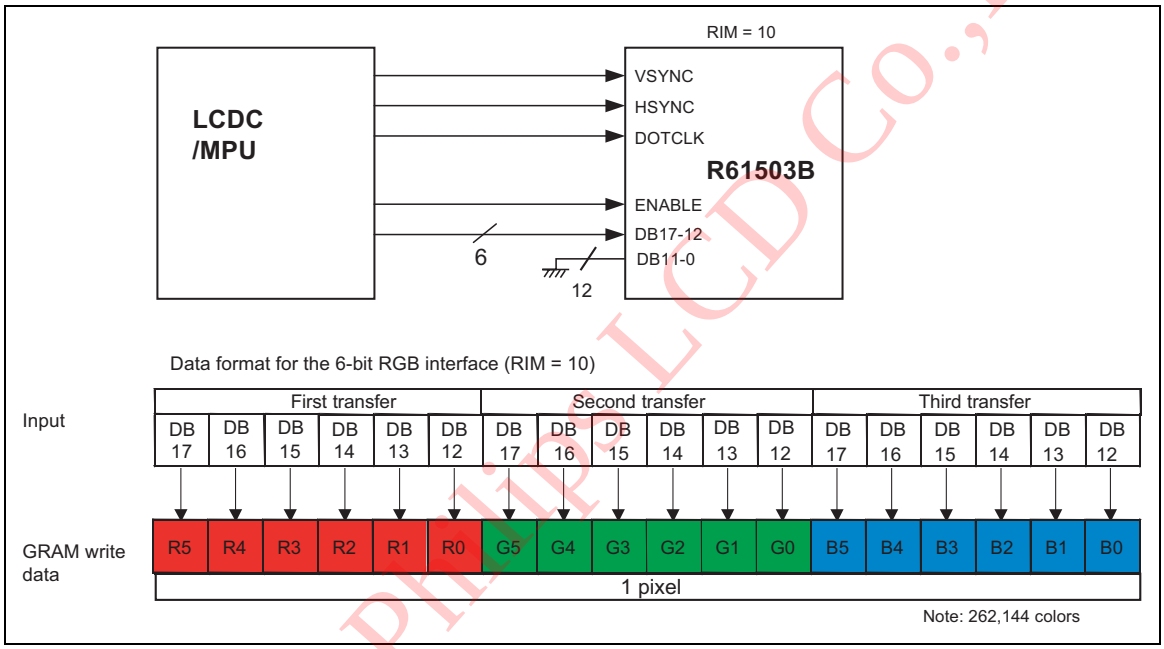


Figure 50 6-Bit RGB Interface and data format

Data transfer synchronization in 6-bit RGB interface operation

The R61503B has the counters, which count the first, second, third 6 bit transfers via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

Make sure the internal display operation within the R61503B is performed in units of pixels and input 3 DOTCLK to transfer one pixel data (RGB) via 6-bit interface. If the number of DOTCLK inputted in one frame period does not satisfy this condition, data transfer mismatch will occur and its effect will be carried over to the next frame.

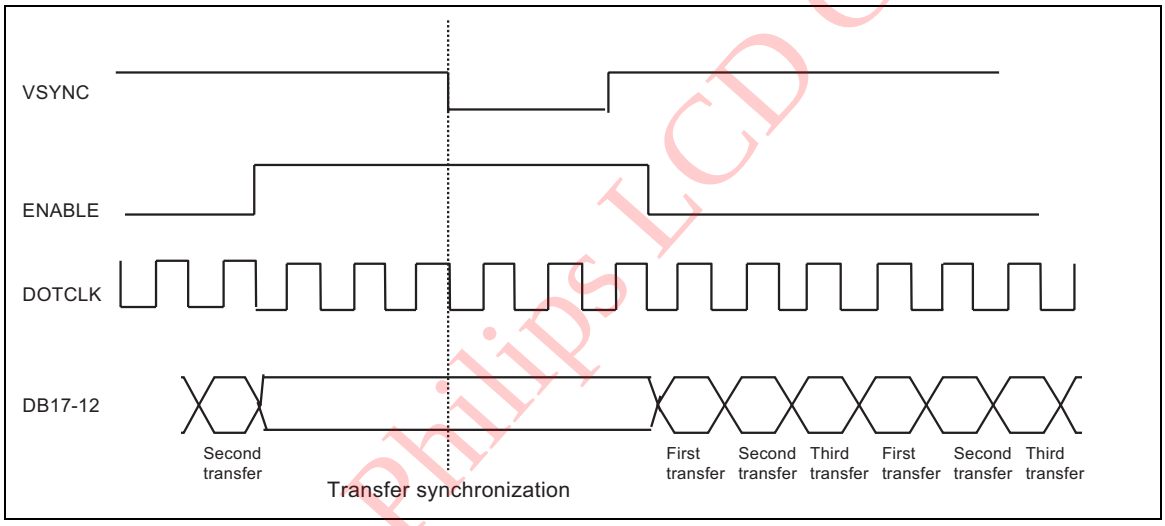


Figure 51 6-bit Transfer Synchronization

16-bit RGB interface

The 16-bit RGB interface is selected by setting the RIM1-0 bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-10, DB8-1) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

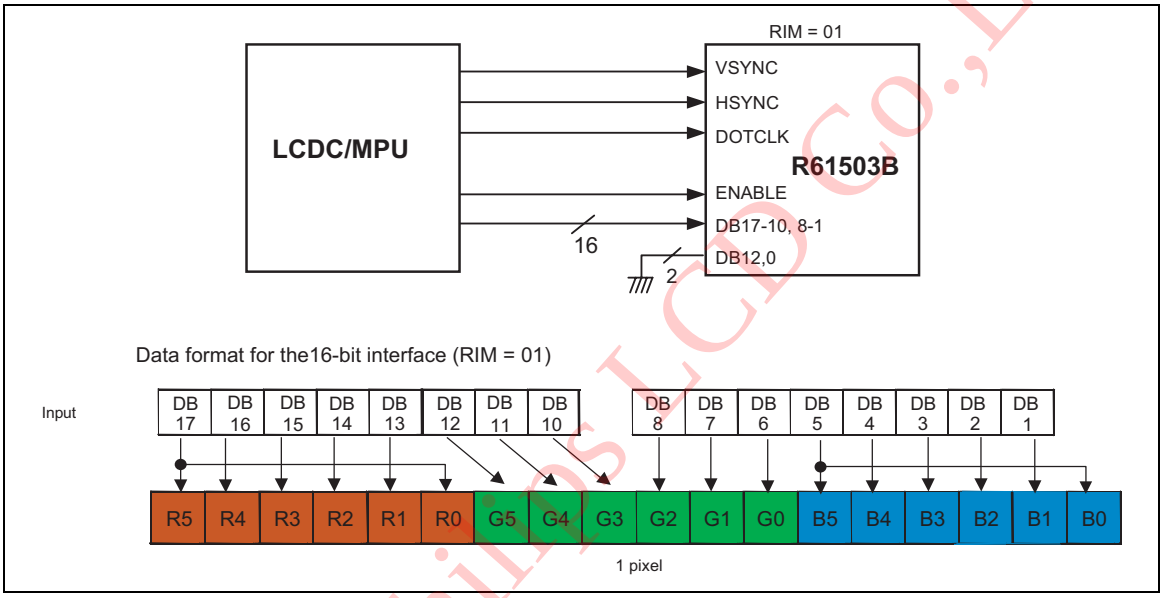


Figure 52 16-Bit RGB Interface and data format

18-bit RGB interface

The 18-bit RGB interface is selected by setting the RIM1-0 bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

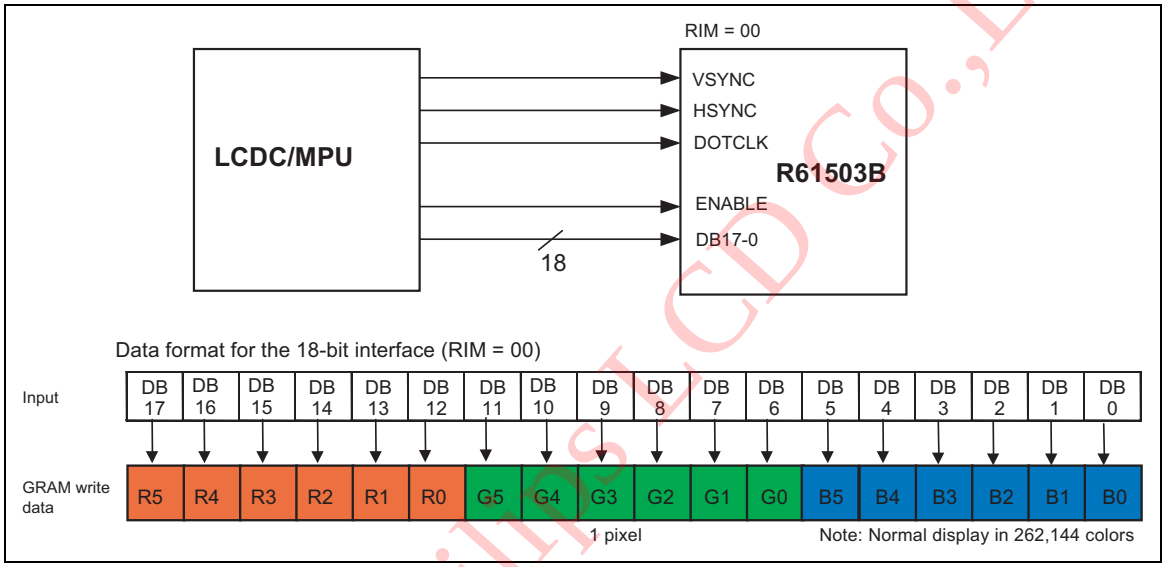


Figure 53 18-Bit RGB Interface and data format

Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Table 65 Functions Not Available in External Display Interface operation

Function	External Display Interface	Internal Clock Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The reference clock, which is used for determining the periods set by NOE[1:0], STDE[1:0] bits in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.
4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel data.
5. In 6-bit RGB interface operation, make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE signals so that the data transfer via DB17-12 is completed in units of pixels.
6. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.
7. In RGB interface operation, a front porch period continues after the end of frame period until next VSYNC input is detected.
8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to GRAM.
9. In RGB interface operation, RAM address AD15-0 is set in the address counter every frame on the falling edge of VSYNC.

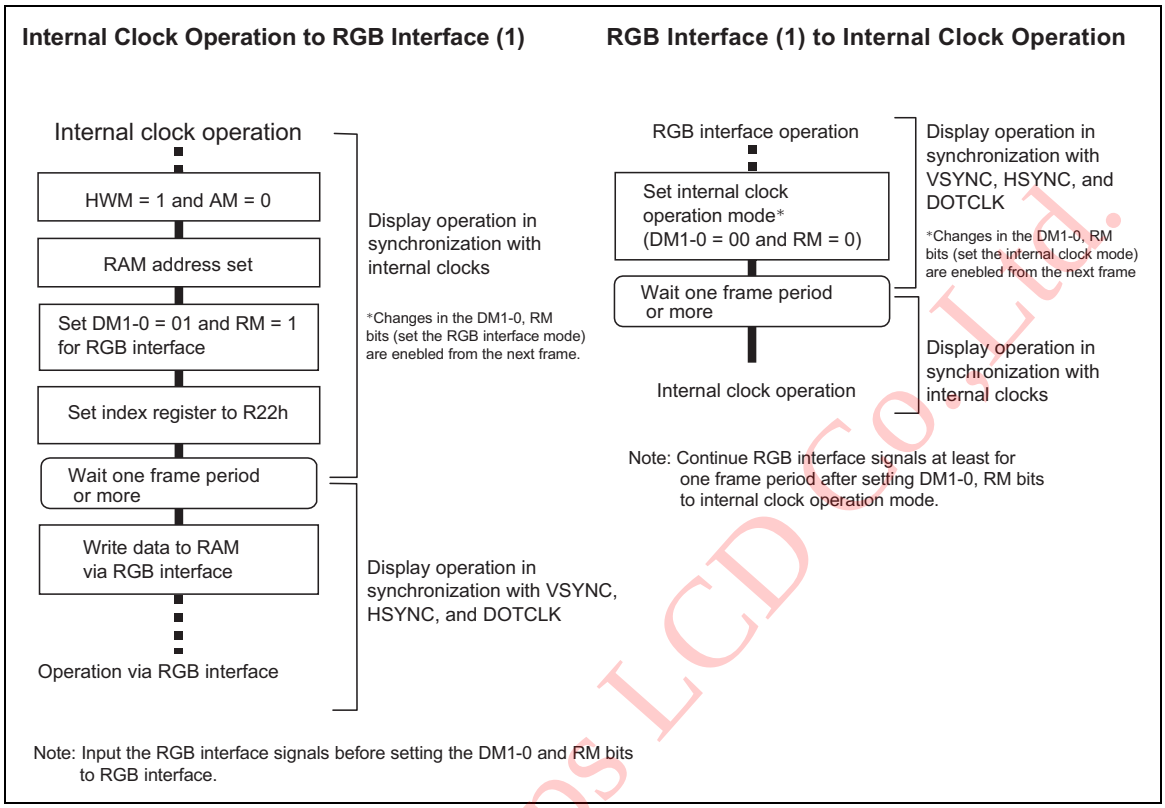


Figure 54 RGB interface operation and internal clock operation transition

RAM Address and Display Position on the Panel

The R61503B has memory to store the display data of 176RGB x 220 lines. The R61503B incorporates a circuit to control partial display, which allows switching the display driving mode between full-screen display mode and partial display mode.

The R61503B makes the display design setting and the panel driving position control setting separately and specifies the RAM area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image by setting PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

Normal display	BASEE = 1
Partial display	BASEE = 0, PTDE0/1 = 1

5. Change BASEE, PTDE0/1 setting to switch display modes (full-screen and partial display modes).

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 66

	Display ENABLE	Numbers of lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h0DB)

Notes 1: The base image is displayed from the first line of the panel.

2: Make sure NL ≤ 220 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h0DB, respectively.

Table 67

	Display ENABLE	Display position	RAM area
Partial image 1	PTDE0	PTDP0	(PTSA0, PTEA0)
Partial image 2	PTDE1	PTDP1	(PTSA1, PTEA1)

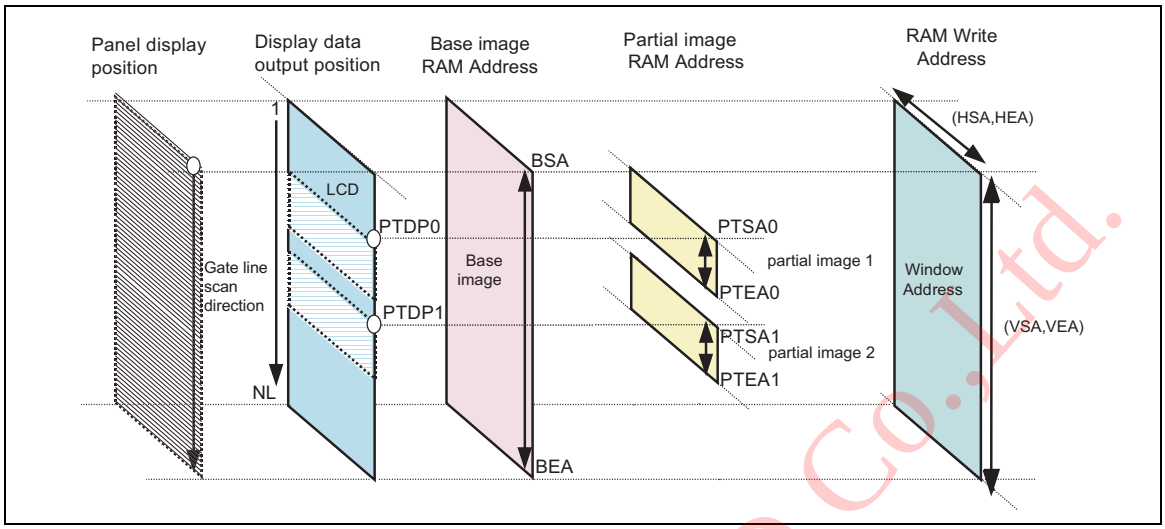


Figure 55 RAM Address, display position and drive position

Restrictions in setting display control instruction

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partial images do not overlap one another.

$$0 \leq \text{PTDP0} \leq \text{PTDP0} + (\text{PTEA0} - \text{PTSA0}) < \text{PTDP1} \leq \text{PTDP1} + (\text{PTEA1} - \text{PTSA1}) \leq \text{NL}$$

The following figure shows the relationship among the RAM address, display position, and the lines driven for the display.

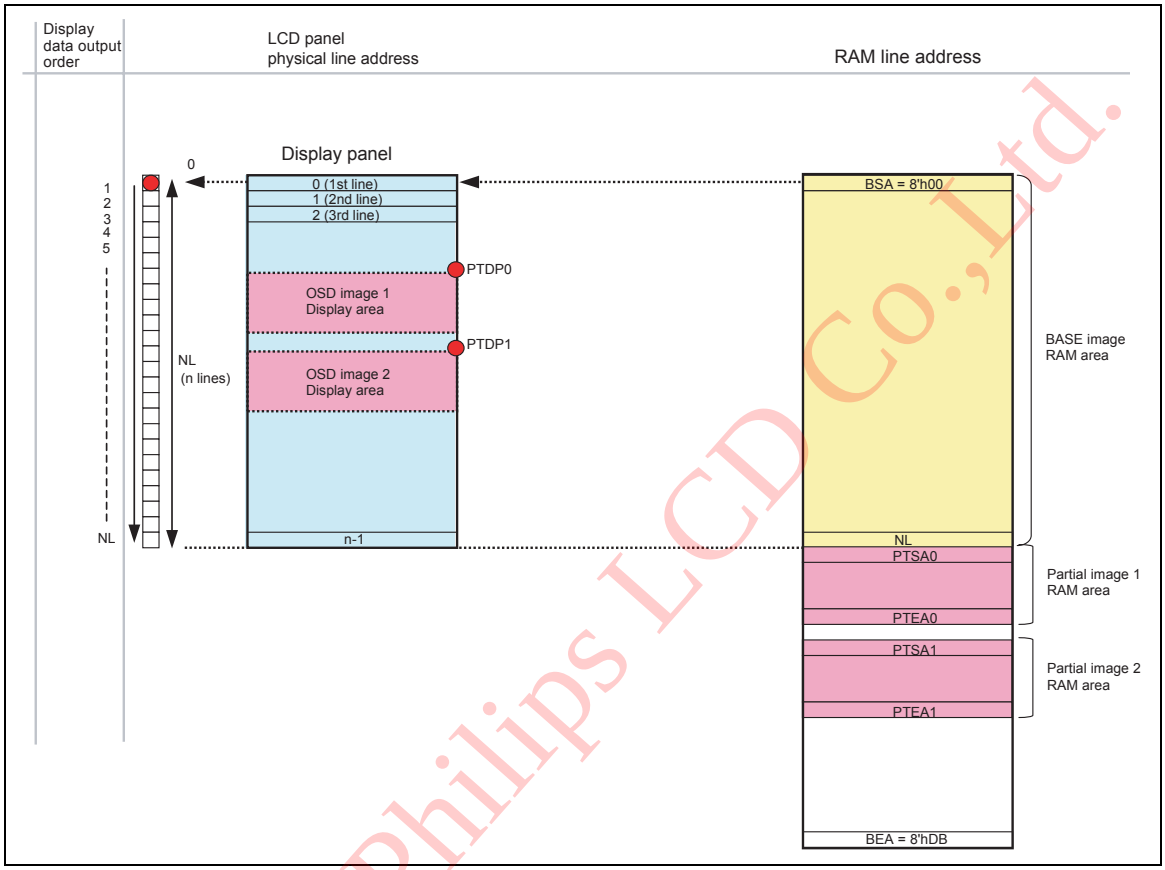


Figure 56 Display RAM address and panel display position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the R61503B's internal operation, the data is written in the RAM area specified by the window address setting (HEA/HSA[7:0], VEA/VES[8:0]).

Instruction setting example

The followings are examples of display design setting for 176(RGB) x 220(lines) panels.

1. Full screen display (no partial)

The following is an example of full screen display setting.

Table 68

Base image display instruction	
BASEE	1
NL[4:0]	5'h14

PTDE0	0
PTDE1	0

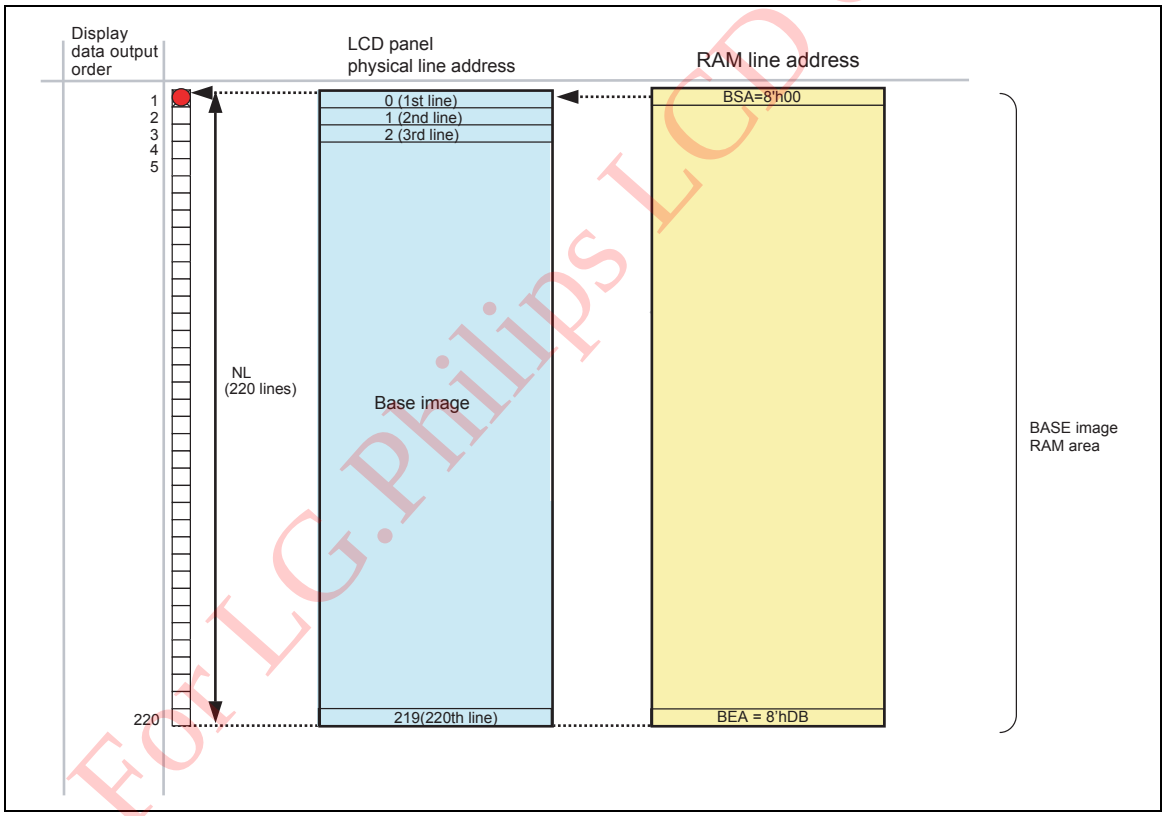


Figure 57 Full screen display (no partial)

2. Partial only

The following is an example of setting for partial image 1 only and turning off the base image. The partial image 1 is displayed at the position specified by PTDP0 bit.

Table 69

Base image display instruction	
BASEE	0
NL[4:0]	6'h14

partial image 1 display instruction	
PTDE0	1
PTSA0[7:0]	8'h00
PTEA0[7:0]	8'h0F
PTDP0[7:0]	8'h80

partial image 2 display instruction	
PTDE1	0
PTSA1[7:0]	8'h00
PTEA1[7:0]	8'h00
PTDP1[7:0]	8'h00

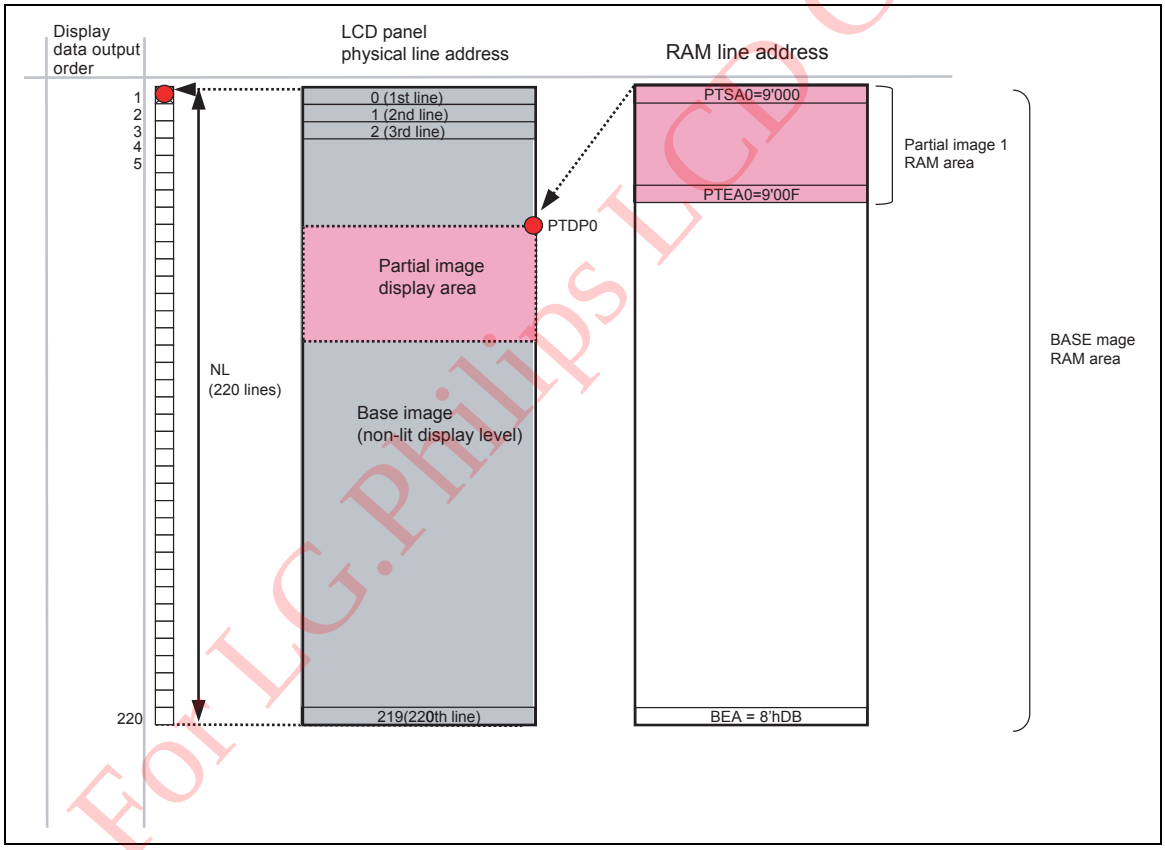


Figure 58 Partial display

Resizing function

The R61503B supports resizing function (x 1/2, x 1/4), executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit, which sets the contraction factor (x1/2 or x1/4) of the image. This function enables the R61503B to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The R61503B processes the contraction of an image simply by selecting pixels from original image data. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.

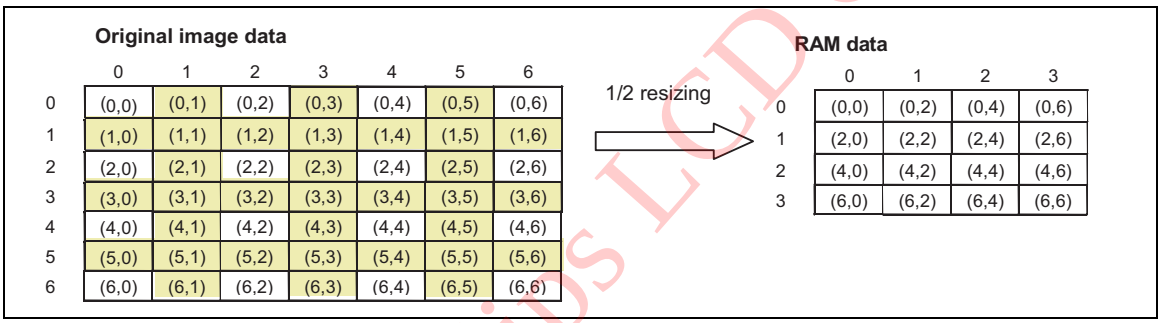


Figure 59 Resizing

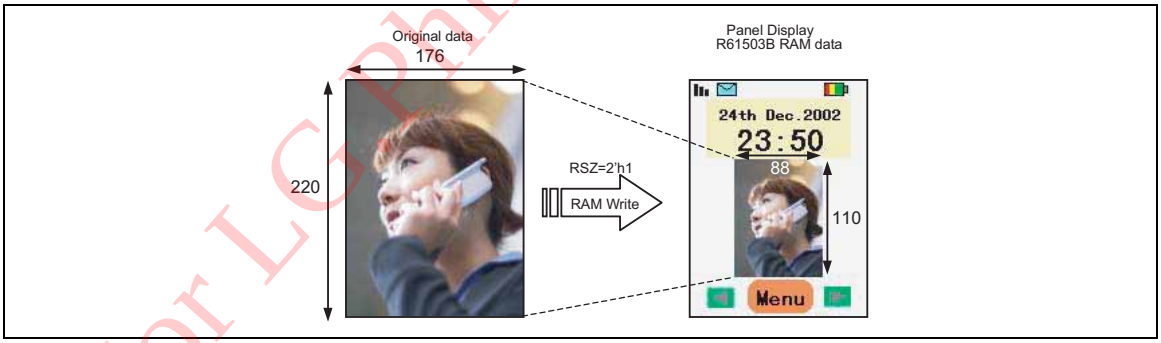


Figure 60 Resizing transfer, display example

Table 70

Original image size (X x Y)	Resized image size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
352x288 (CIF)	176x144	88x72
320x176 (QVGA)	160x120	80x60
176x144 (QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

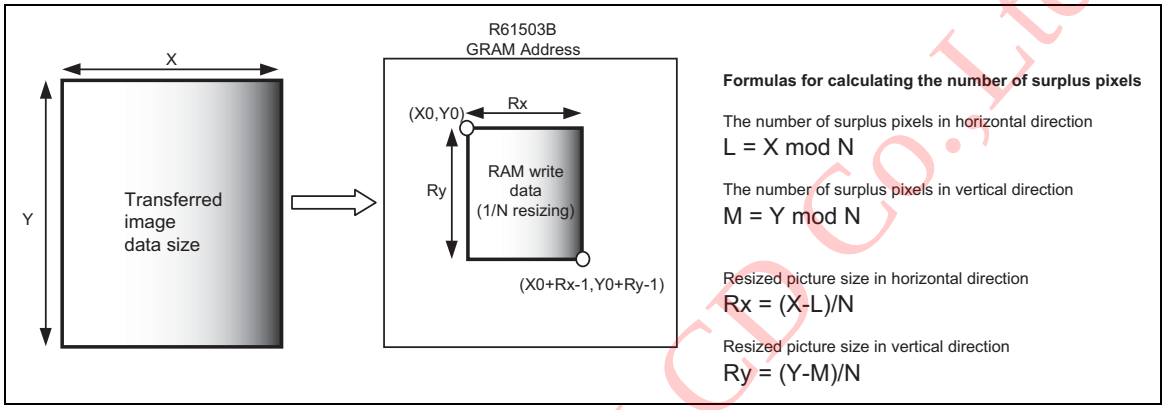


Figure 61 Resizing Setting, surplus pixel calculation

Table 71

Image (before resizing)	
Number of data in horizontal direction	X
Number of data in vertical direction	Y
Resizing ratio	1/N

Register setting in the R61503B		
Resizing setting	RSZ	N-1
Number of data in horizontal direction	RCV	L
Number of data in vertical direction	RCH	M
RAM writing start address	AD	(X0, Y0)
RAM window address	HSA	X0
	HEA	X0+Rx - 1
	VSA	Y0
	VEA	Y0+Ry - 1

Example of 1/2 resizing

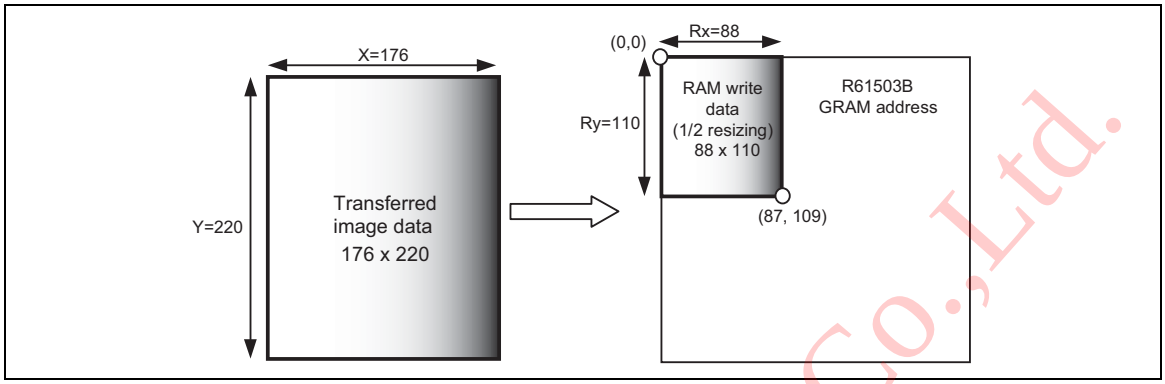


Figure 62 Resizing setting example (x 1/2)

Table 72

Image to transmit

Number of data in horizontal direction	X	176
Number of data in vertical direction	Y	220
Resizing ratio	1/N	1/2

Register setting in the R61503B

Resizing setting	RSZ	2'h1
Number of data in horizontal direction	RCV	2'h0
Number of data in vertical direction	RCH	2'h0
RAM writing start address	AD	17'h00000
RAM window address	HSA	8'h00
	HEA	8'h57
	VSA	9'h000
	VEA	9'h06D

Resizing instruction bits

Table 73 Resizing factor

RSZ[1:0]	Contraction factor
2h'0	No resizing (x 1)
2h'1	1/2 resizing (x 1/2)
2h'2	Setting disabled
2h'3	1/4 resizing (x 1/4)
2h'4	Setting disabled

Table 74 Surplus pixels

Vertical direction

RCV[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

1 pixel = 1 RGB

horizontal direction

RCH[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

1 pixel = 1 RGB

Notes to Resizing function

1. Set the resizing instruction (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), make sure RCH = RCV = 2'h0.

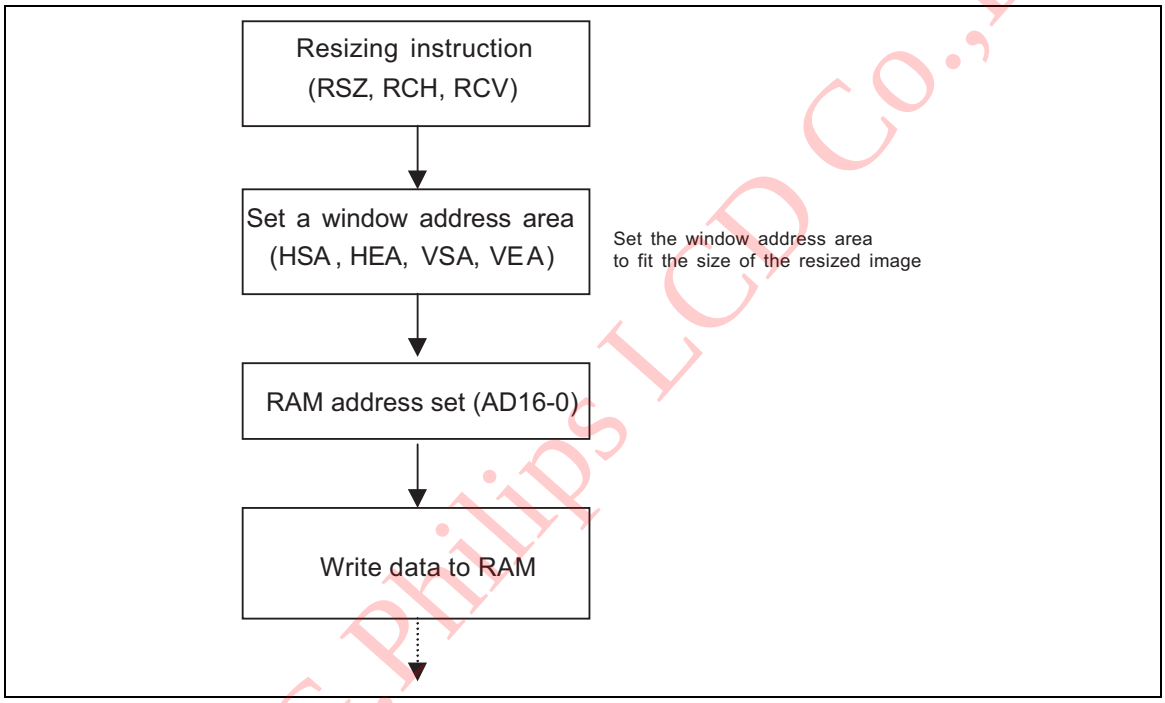


Figure 63 RAM write with resizing

High-Speed RAM Write Function

The R61503B supports high-speed RAM write function to write data to each line of window address area at a time. This function makes the R61503B available with the applications, which require high-speed, low-power-consumption data write operation such as color moving picture display.

When enabling high-speed RAM write function (HWM = "1"), the data is first stored in the internal register of the R61503B in order to rewrite the RAM data in each horizontal line of the window address area at a time. Also, when transferring the data from the internal register to the internal RAM, the data written in the next line of the window address area can be transferred to the internal register of the R61503B. The high-speed write function minimizes the number of RAM access in write operation and enables high-speed consecutive RAM write operation required for moving picture display with low power consumption.

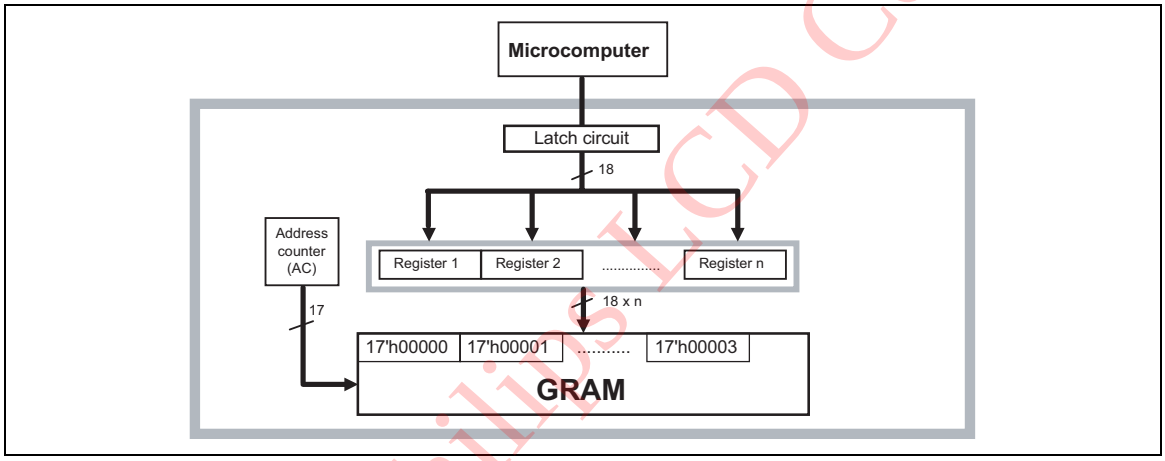


Figure 64 High speed RAM write operation

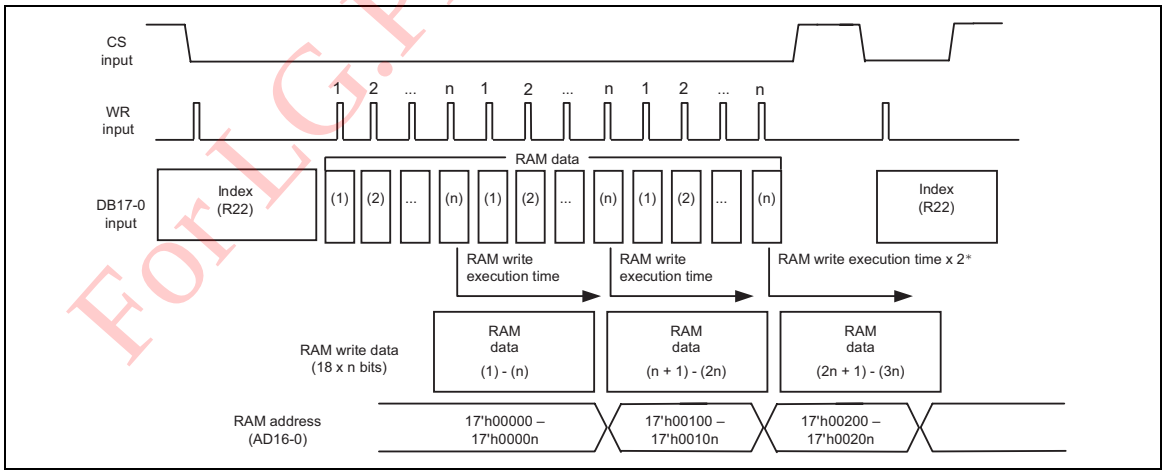


Figure 65 High speed RAM write operation timing relationship

Note: When switching from high-speed RAM write operation to index write operation, wait at least for 2 bus cycle periods (2 x t_{cycw}) for normal RAM write operation before executing next instruction.

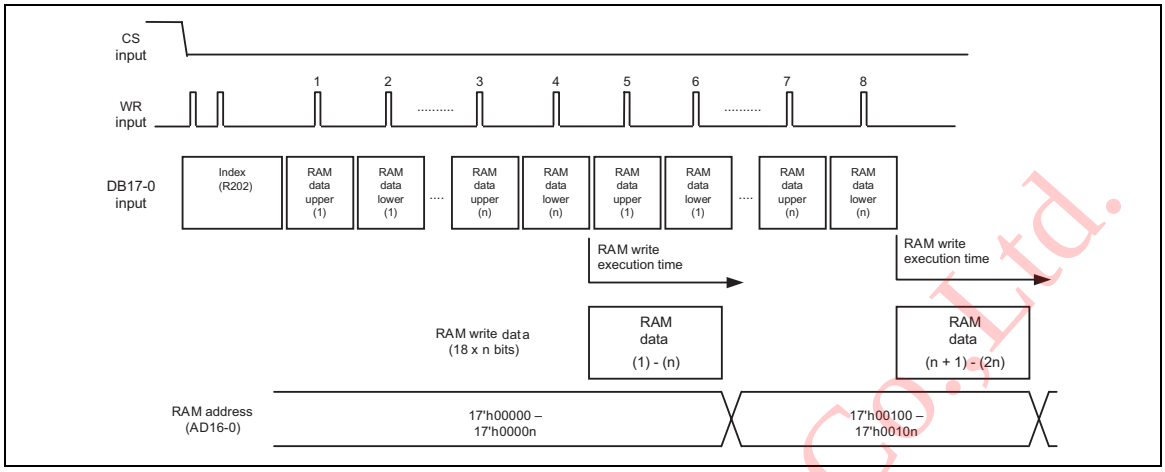


Figure 66 High speed RAM write operation via 9-bit interface

Note: In high-speed RAM write operation, the R61503B writes data in units of n words. When using 9-bit interface, the R61503B performs write operation 2 x n times in the internal register before writing the data in each line of the window address area.

Notes to high-speed RAM write function

1. In high-speed RAM write mode, the R61503B performs write operation to the internal RAM in units of lines. If the data inputted to the internal write register is not enough to rewrite the data in the horizontal line of the window address area, the data is not written correctly in that line address.

2. If the IR is set to 22h when HWM = "1", the R61503B always performs RAM write operation. With this setting, the R61503B does not perform RAM read operation. Make sure to set HWM = 0, when performing RAM read operation.

3. The high-speed RAM write function cannot be used when writing data in normal RAM write function mode. When switching form one write mode to the other, change the mode first and set AD16-0 (RAM address set) before starting write operation.

Table 75

	Normal RAM Write (HWM=0)	High-Speed RAM Write (HWM=1)
BGR function	Available	Available
RAM address set	In units of words	In units of words
RAM read	In units of words	Not Available
RAM write	In units of words	In units of horizontal lines
Window address	In units of words (minimum window address area: 1 word x 1 line)	In units of words (minimum window address area: 8 words x 1 line)
External display interface	Available	Available
AM	AM = 1/0	AM = 0

High-speed RAM data write in a window address area

The R61503B can perform consecutive high-speed data rewrite operation within a rectangular area (minimum: 8 words x 1 line) made in the internal RAM with the following settings.

When writing data to the internal RAM using high-speed RAM write function, make sure each line of the window address area is overwritten at a time. If the data buffered in the internal register of the R61503B is not enough to overwrite the horizontal line in the window address area, the data is not written correctly in that line.

The following is an example of writing data in the window address area using high-speed write function when a window address area is made by setting HSA = 8'h12, HEA = 8'hA7, VSA = 9'h020, VEA = 9'h05B.

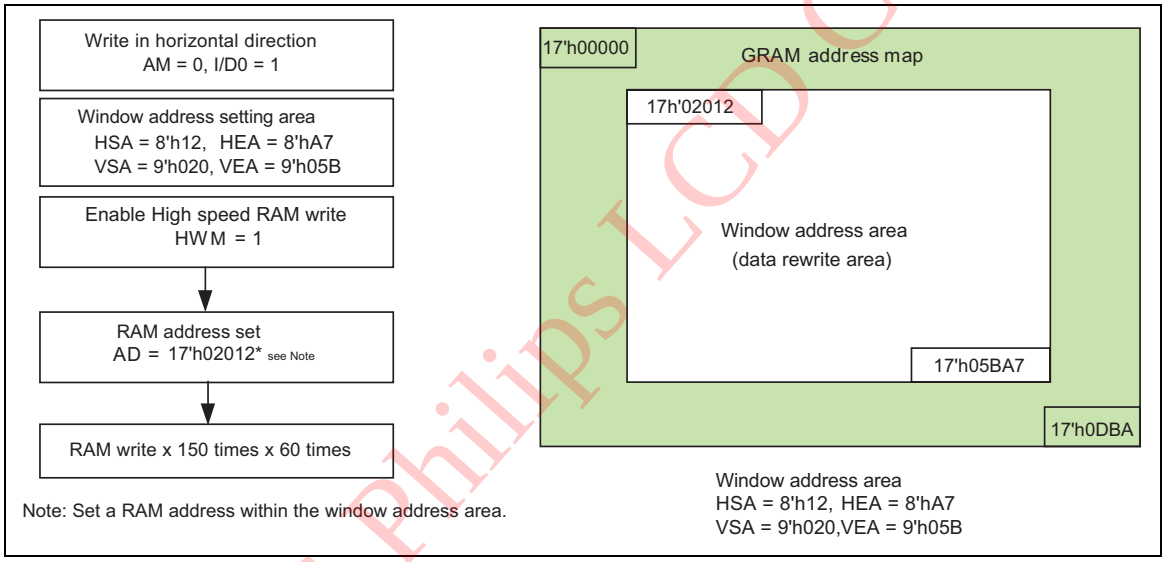


Figure 67

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61503B to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area]
(horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hAF
(vertical direction) 9'h000 ≤ VSA ≤ VEA ≤ 9'h0DB

[RAM address (AD16-0)]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD16-8 ≤ VEA

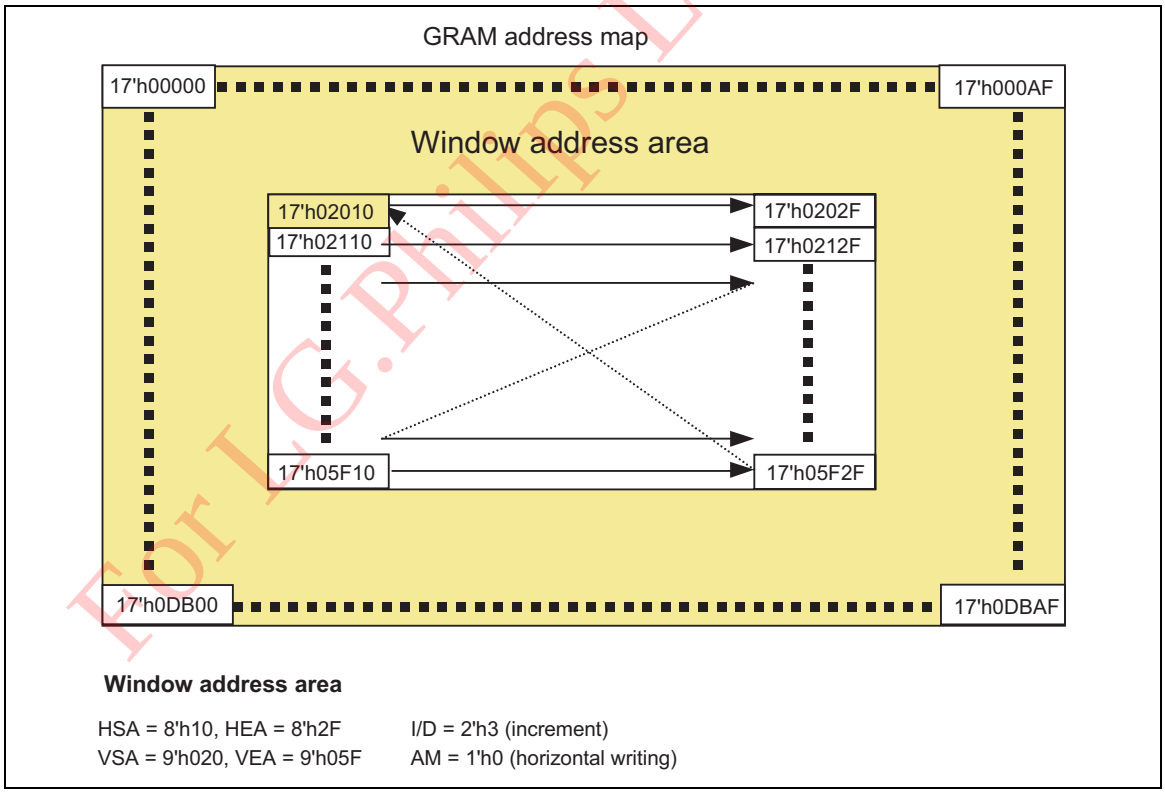


Figure 68 Automatic address update within a Window Address Area

Scan Mode Setting

The R61503B allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the R61503B and the LCD panel.

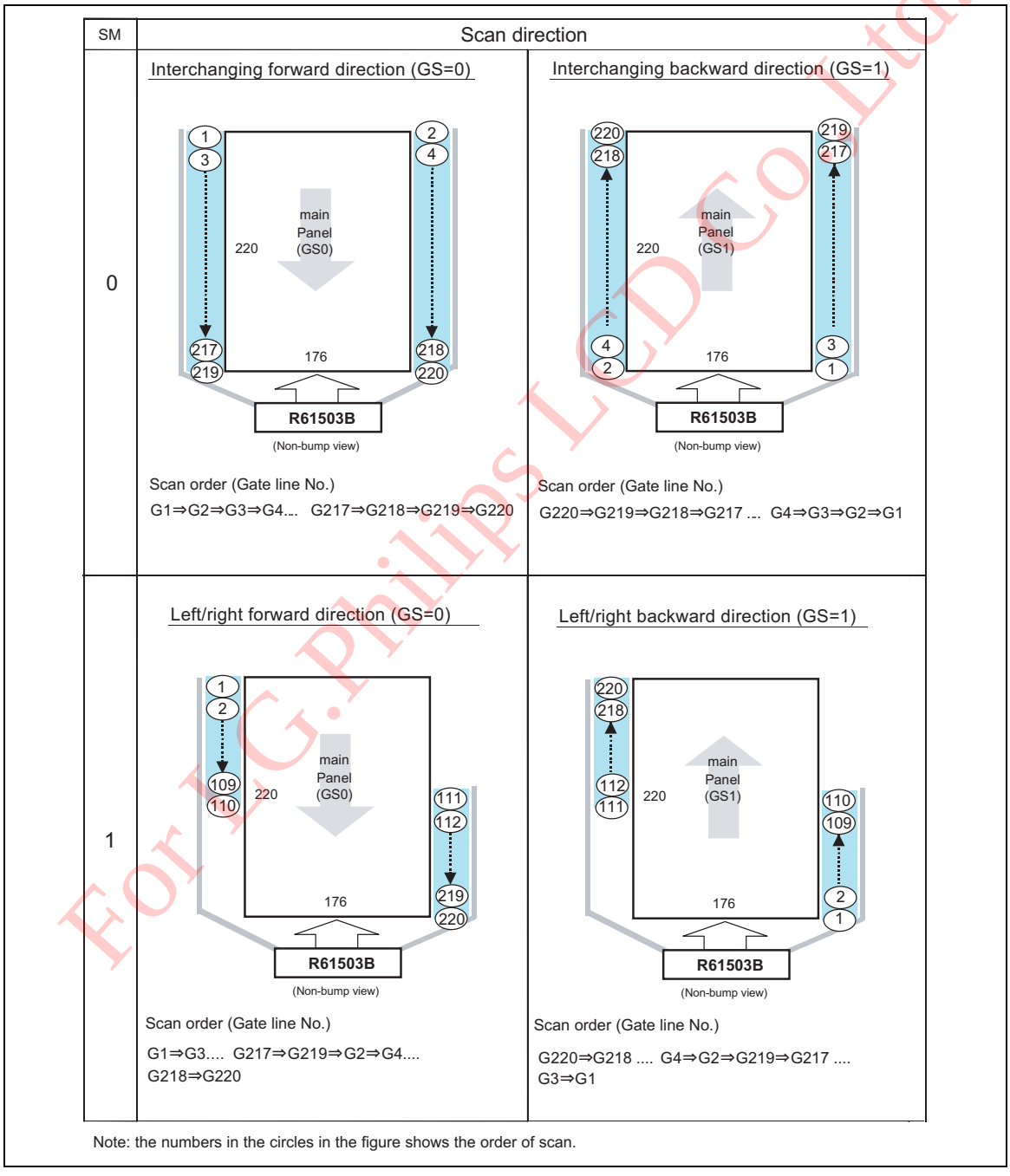


Figure 69

8-color Display Mode

The R61503B has a function to display in eight colors. In this display mode, only V0 and V31 are used and power supplies to other grayscales (V1 to V30) are turned off to reduce power consumption.

In 8-color display mode, the γ-adjustment registers P0KP0-P0KP5, P0KN0-P0KN5, P0RP0, P0RP1, P0RN0, P0RN1 are disabled and the power supplies to V1 to V30 are halted. The R61503B does not require GRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

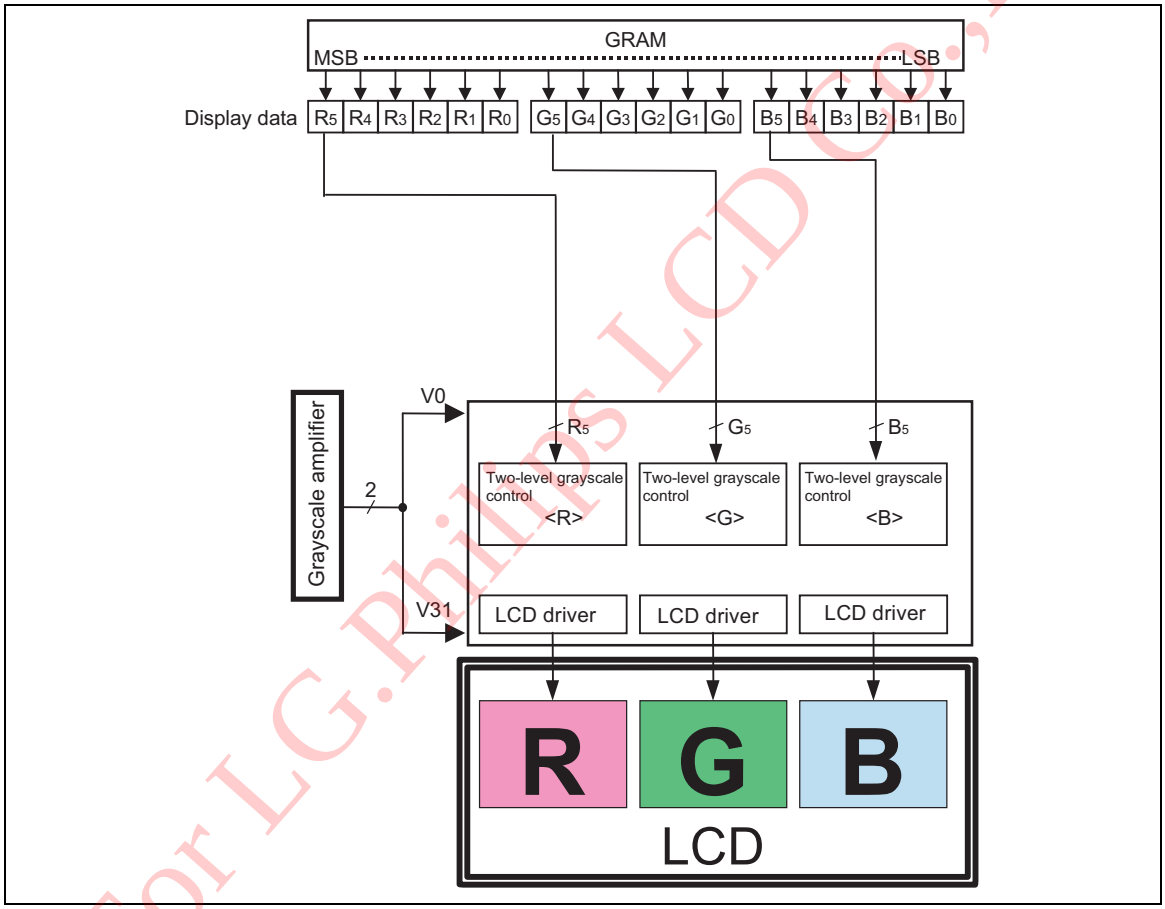
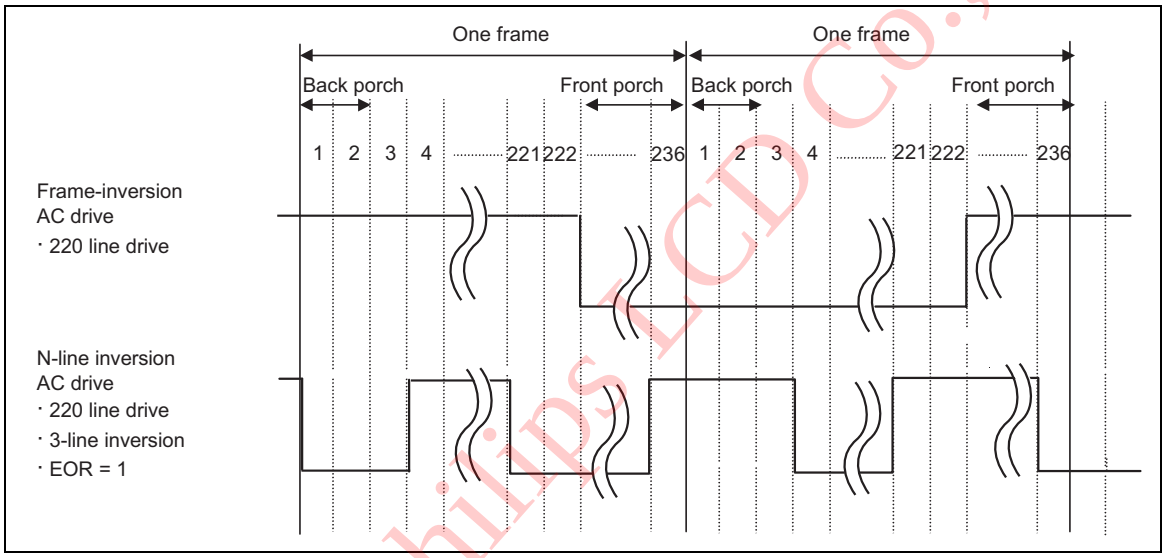


Figure 70

n-line Inversion AC Drive

The R61503B, in addition to the frame-inversion liquid crystal alternating current drive, supports the n-line inversion alternating current drive to invert the polarity of liquid crystal in every n-line periods, where n takes a number from 1 to 64. The n-line inversion can provide a solution when there is a need to improve the display quality.

In determining "n"(the value represented by NW bits +1), check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.



Notes: 1. Make sure to set EOR = "1" to prevent direct bias on liquid crystal when selecting n-line inversion drive.

2. The n-line inversion is halted in blank period (back, front porch periods) and restarted at the first line of the display area.

Figure 71

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61503B draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of n-line inversion AC drive, polarity is inverted as the R61503B draws n line, and a blank period lasting for (BP+FP) periods is inserted when the R61503B draws one frame.

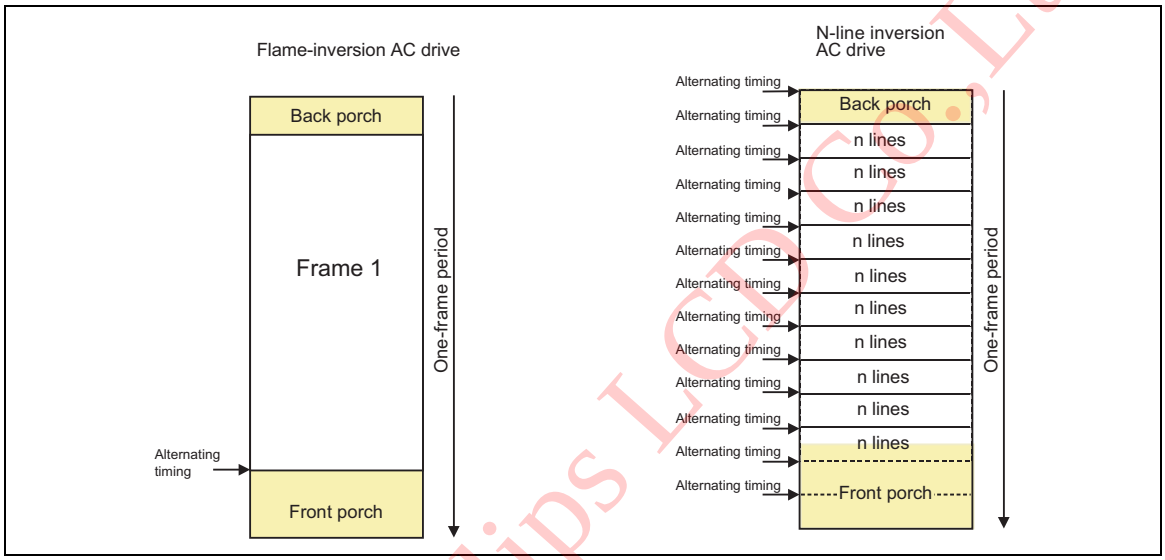


Figure 72

Frame-Frequency Adjustment Function

The R61503B supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIVI, RTNI bits without changing the oscillation frequency.

The R61503B allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the R61503B can operate at high frame frequency when displaying a moving picture, which requires the R61503B to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between liquid crystal drive duty and frame frequency

The following equation represent the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

(Formula to calculate frame frequency)

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line+BP+FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
Line: number of lines to drive a panel (NL bits)
Clock cycles per line: RTNI bits
Division ratio: DIVI bits
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive a panel: 220 lines
1H period: 16 clock cycles (RTNI3-0 = “0000”)
Operation clock division ratio: 1/1
Front porch (FP): 2 line periods
Back porch (BP): 14 line periods

$$\text{fosc} = 60\ (\text{Hz}) \times (0+16)\ (\text{clocks}) \times 1/1 \times (220 + 16)\ (\text{lines}) = 218\ (\text{kHz})$$

In this case, the RC oscillation frequency is 218kHz. Adjust the external resistor connected to the internal RC oscillator to set the frequency to 218kHz.

Partial Display Function

The partial display function allows the R61503B to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

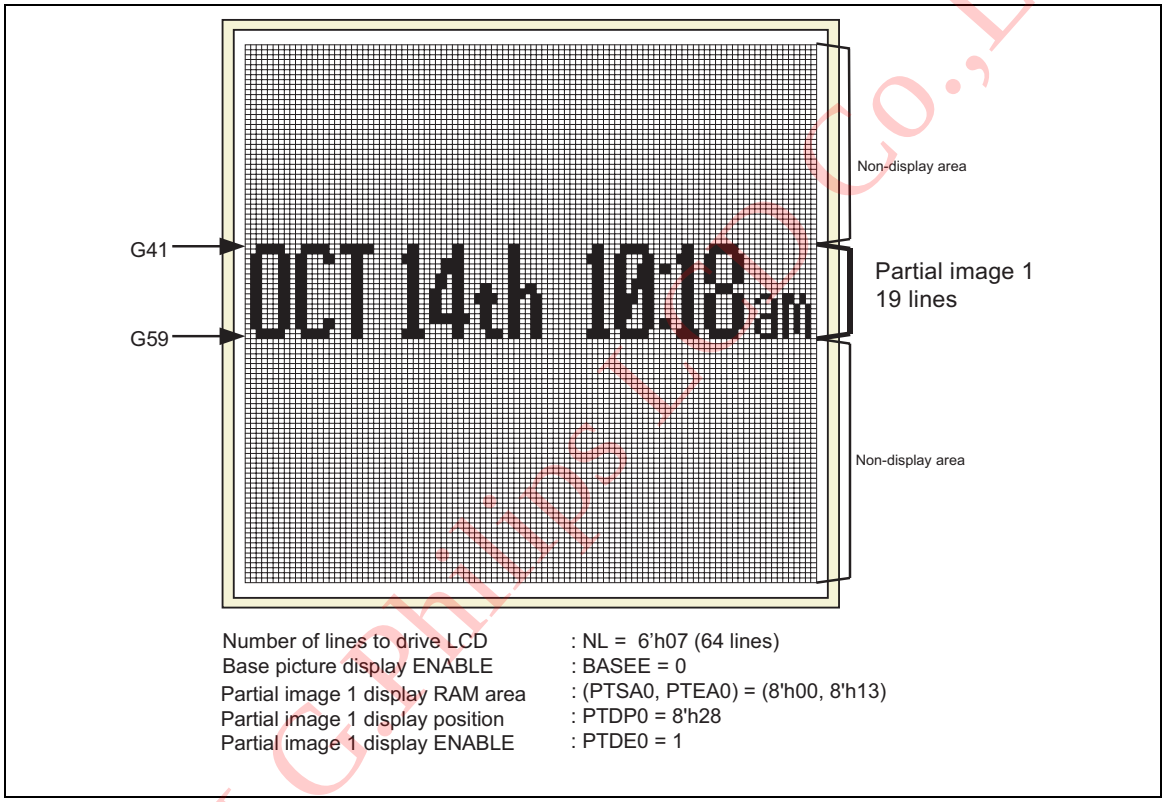


Figure 73

Note: See the "RAM Address and Display Position on the Panel" for details on the relationship between the display position on the panel and the RAM area setting for partial image.

Low power consumption drive settings

The R61503B supports the following low power consumption drive methods to drive the panel with less power requirement. Generally, there is a trade-off between power efficiency and quality of display. Also, the power efficiency depends on the characteristics of the panel. Check which of the following methods can achieve the optimal balance between power consumption and display quality.

1. 8-color display mode (COL)

In this mode (CL = "1"), the R61503B halts grayscale voltage generation except for V0 and V31. In this mode, the R61503B display in 8 colors to save power.

2. Partial display

In this mode, the data is displayed as partial image and the base image is turned off (BASEE = 0). The normal display operation is limited to the partial display area to save power.

The source output level in non-display area can be changed by instruction (PTS[2:0]). By setting PTS[2:0], it becomes possible to halt the amplifiers for generating grayscale voltage except for V0 and V31 and slow down the clock frequency for step-up operation to half the normal frequency.

Table 76 Source outputs in non-display area

PTS[2:0]	Source output in non-display area		Non-display area	Non-display area
	Positive polarity	Negative polarity	Grayscale amp operation	Step-up clock frequency
3'h0	V31	V0	V0 to V31	Set by DC0, DC1 bits
3'h1	Setting disabled	Setting disabled	-	-
3'h2	GND	GND	V0 to V31	Set by DC0, DC1 bits
3'h3	Hi-Z	Hi-Z	V0 to V31	Set by DC0, DC1 bits
3'h4	V31	V0	V0, V31	1/2 the frequency set by DC0, DC1 bits
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0, V31	1/2 the frequency set by DC0, DC1 bits
3'h7	Hi-Z	Hi-Z	V0, V31	1/2 the frequency set by DC0, DC1 bits

See also "Partial Display Function" for details.

3. Frame frequency setting

The R61503B allows changing the liquid crystal polarity inversion cycle by changing the frame frequency by setting DIVI, RTNI bits. To improve power efficiency, set a lower frequency in partial display operation, which requires small power consumption. See also “Frame-Frequency Adjustment Function” for details.

Generally, there is a trade-off between power efficiency and quality of display. The power efficiency also depends on the characteristics of the panel. Check the optimal balance between the quality of display on the panel and the power efficiency before use.

4. Liquid crystal inversion drive

The R61503B allows selecting liquid crystal inversion drive method from frame-inversion AC drive or line-inversion AC drive by setting B/C, NW bits. Select the optimal driving method according to the state of display. Also, see “n-line Inversion AC Drive” for details.

Generally, there is a trade-off between the power efficiency and the quality of display. The power efficiency also depends on the characteristics of the panel. Check the quality of display before use.

5. Optimizing step-up factor

There are cases that power loss in driving liquid crystal can be minimized by optimizing the step-up factor. Whether this method proves to be power-efficient or not depends on the characteristics of the liquid crystal panel. The step-up factor is set by BT[2:0].

LCD panel interface timing

The following are the relationships between RGB interface signals and LCD panel signals when the display operation is synchronized with the internal clock signal and RGB interface signals respectively.

Internal clock operation

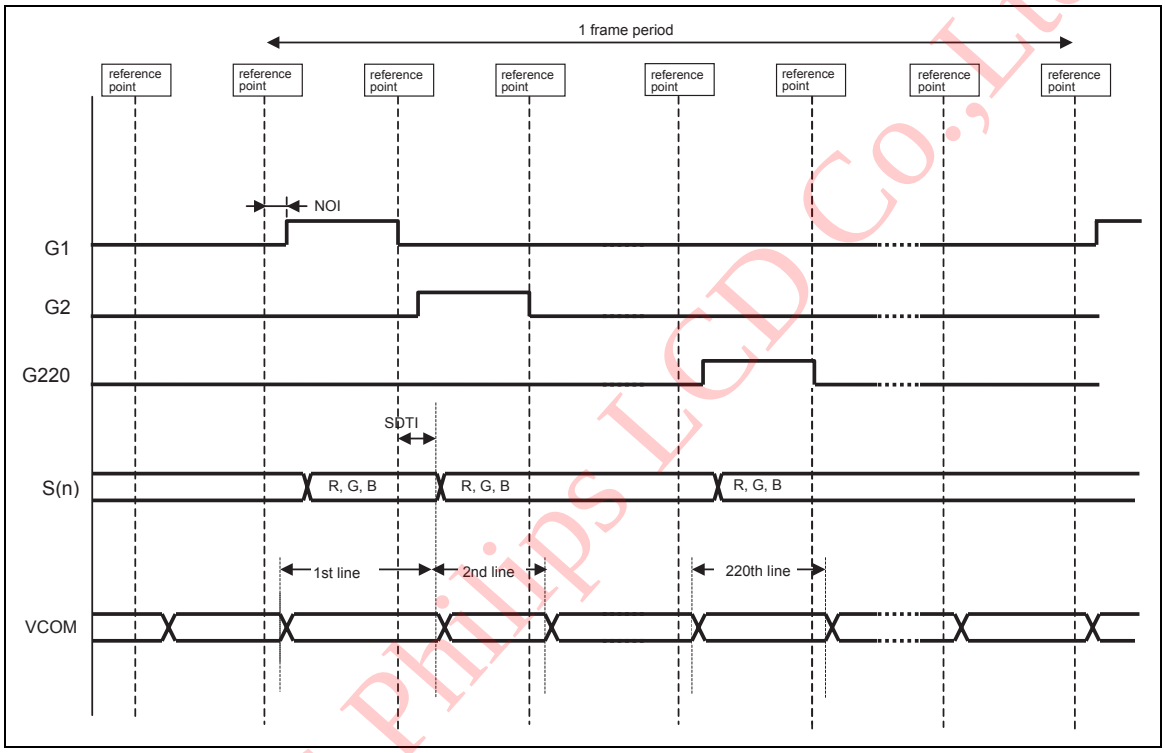


Figure 74

RGB interface signals

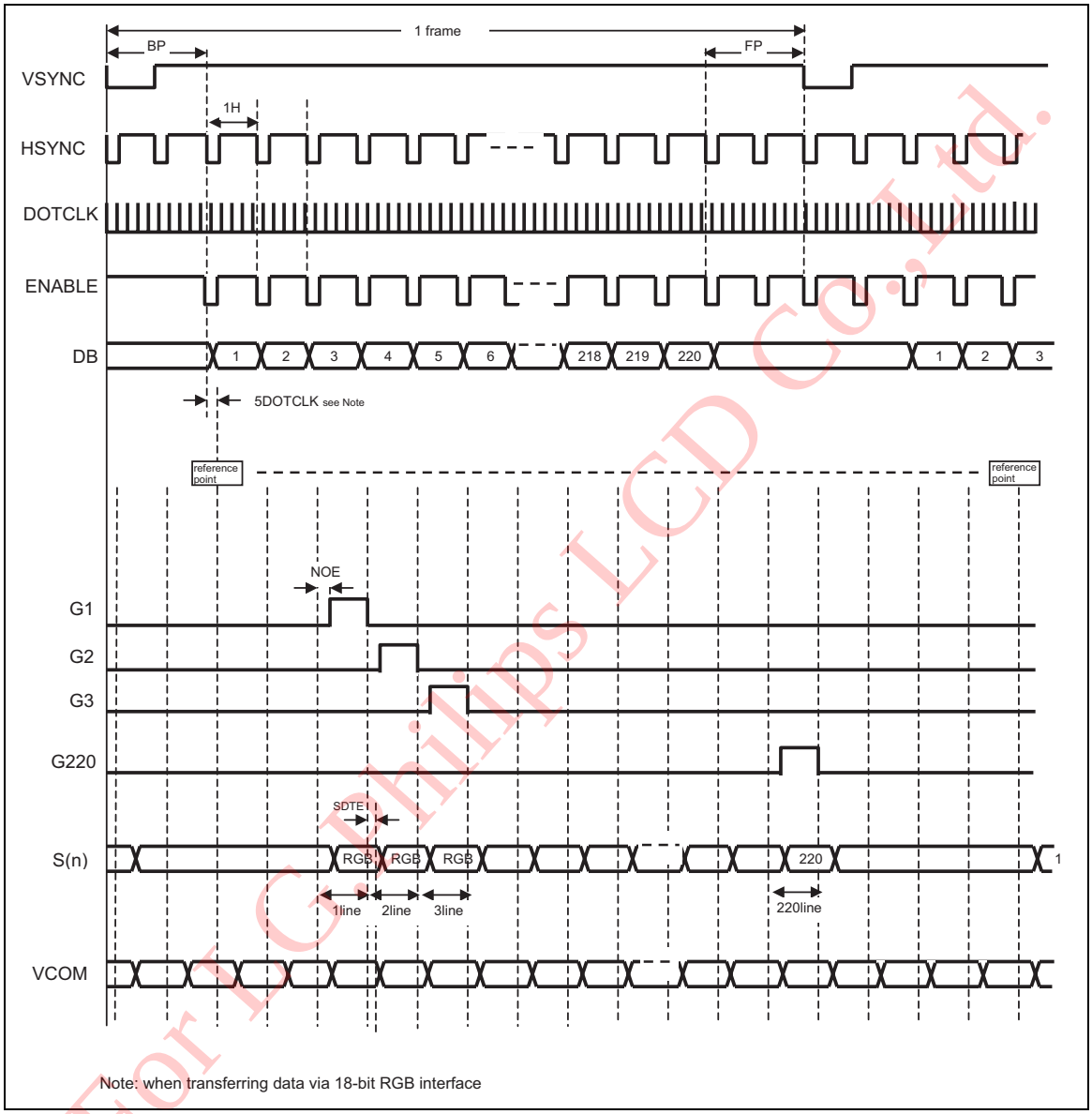


Figure 75

Oscillator

The R61503B generates RC oscillation using the internal RC oscillator to which an external oscillation resistor is connected between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the value of external resistor, wiring length, operating power supply voltage. For example, the oscillation frequency can be lowered by connecting an external resistor of a larger resistance, or lowering supply voltage. See “Notes to electrical characteristics” for details on the relationship between Rf resistance and oscillation frequency (OSC).

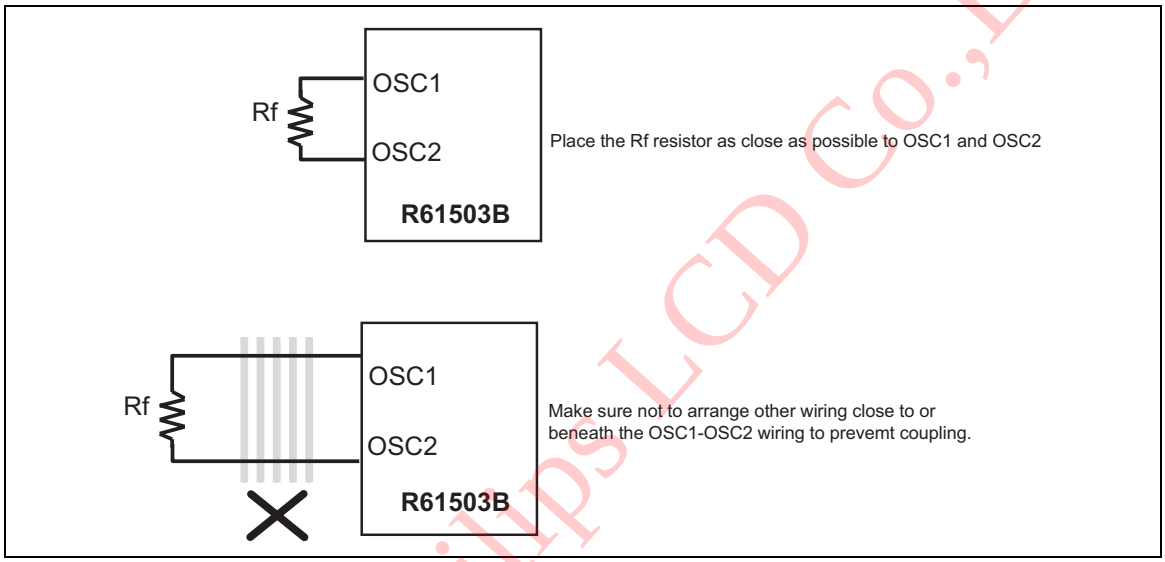


Figure 76

γ Correction function

The R61503B supports γ-correction function to display in 262,144 colors simultaneously using gradient-adjustment, amplitude-adjustment, fine-adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow different settings for positive and negative polarities and make the optimal gamma correction setting for the characteristics of the panel.

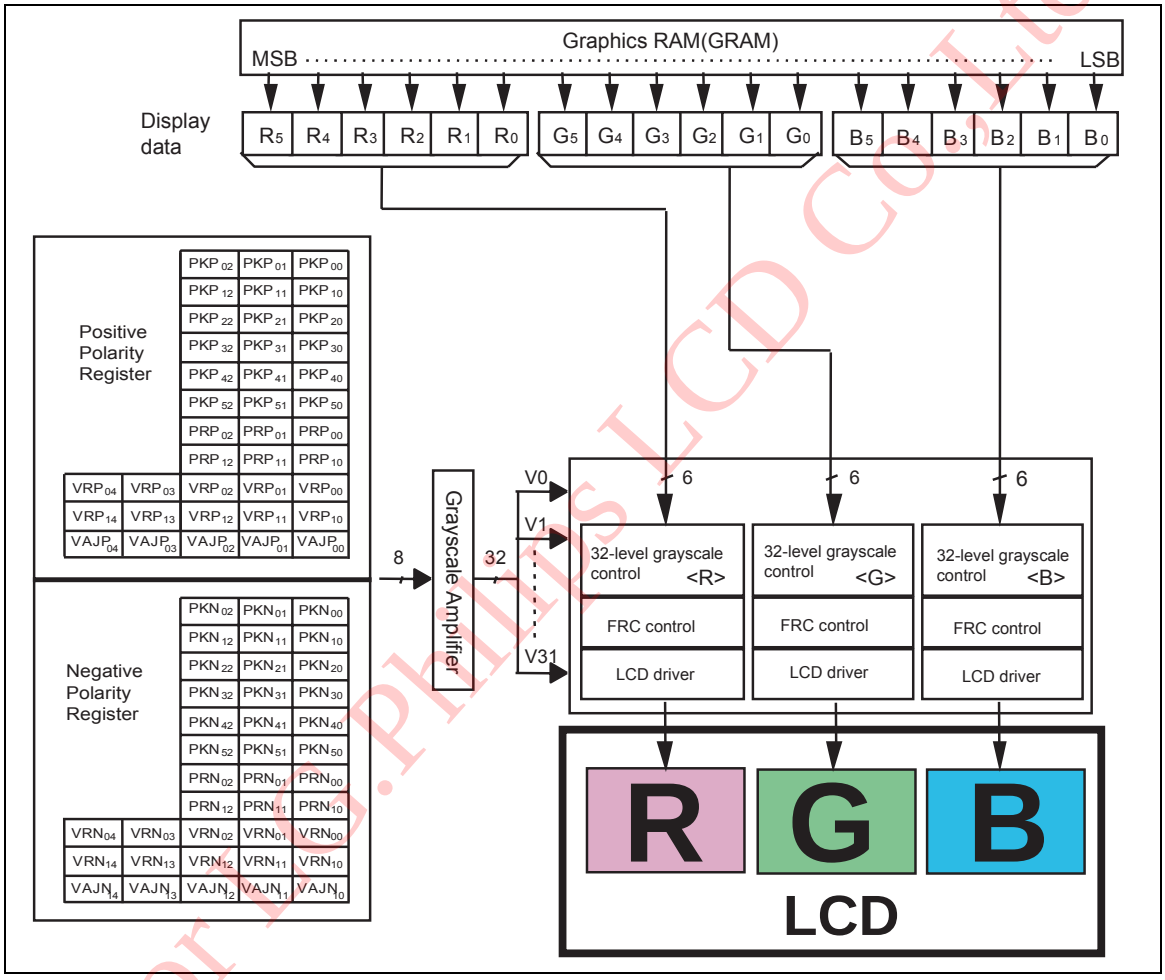


Figure 77

Grayscale amplifier unit

In grayscale amplifier unit, 8 levels VIN0 ~ VIN7 are determined by gradient and fine adjustment registers. Then, the 8 levels are divided by the internal ladder resistors between grayscale amplifiers and 32 grayscale levels (V0 ~ V31) are generated.

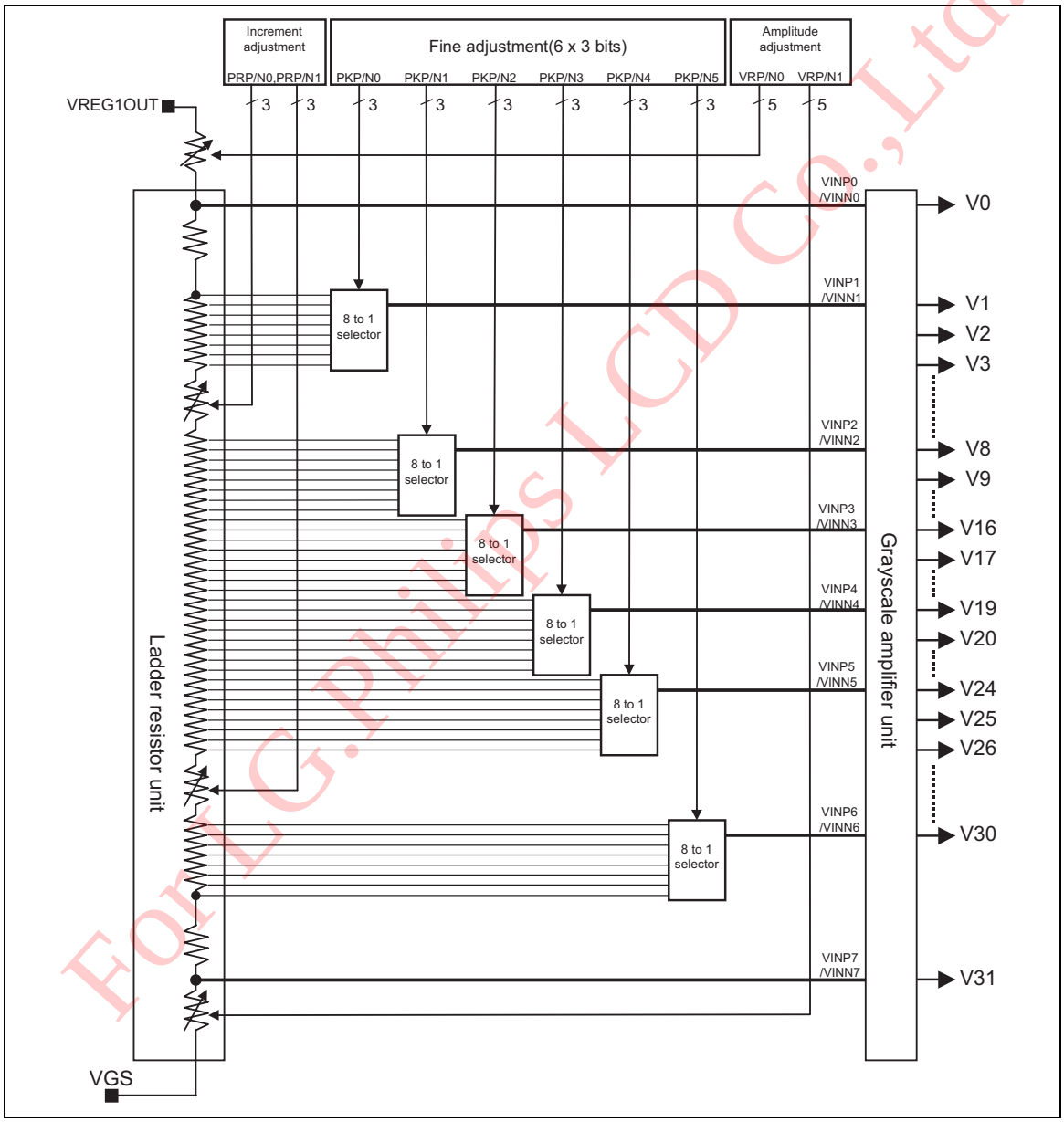


Figure 78

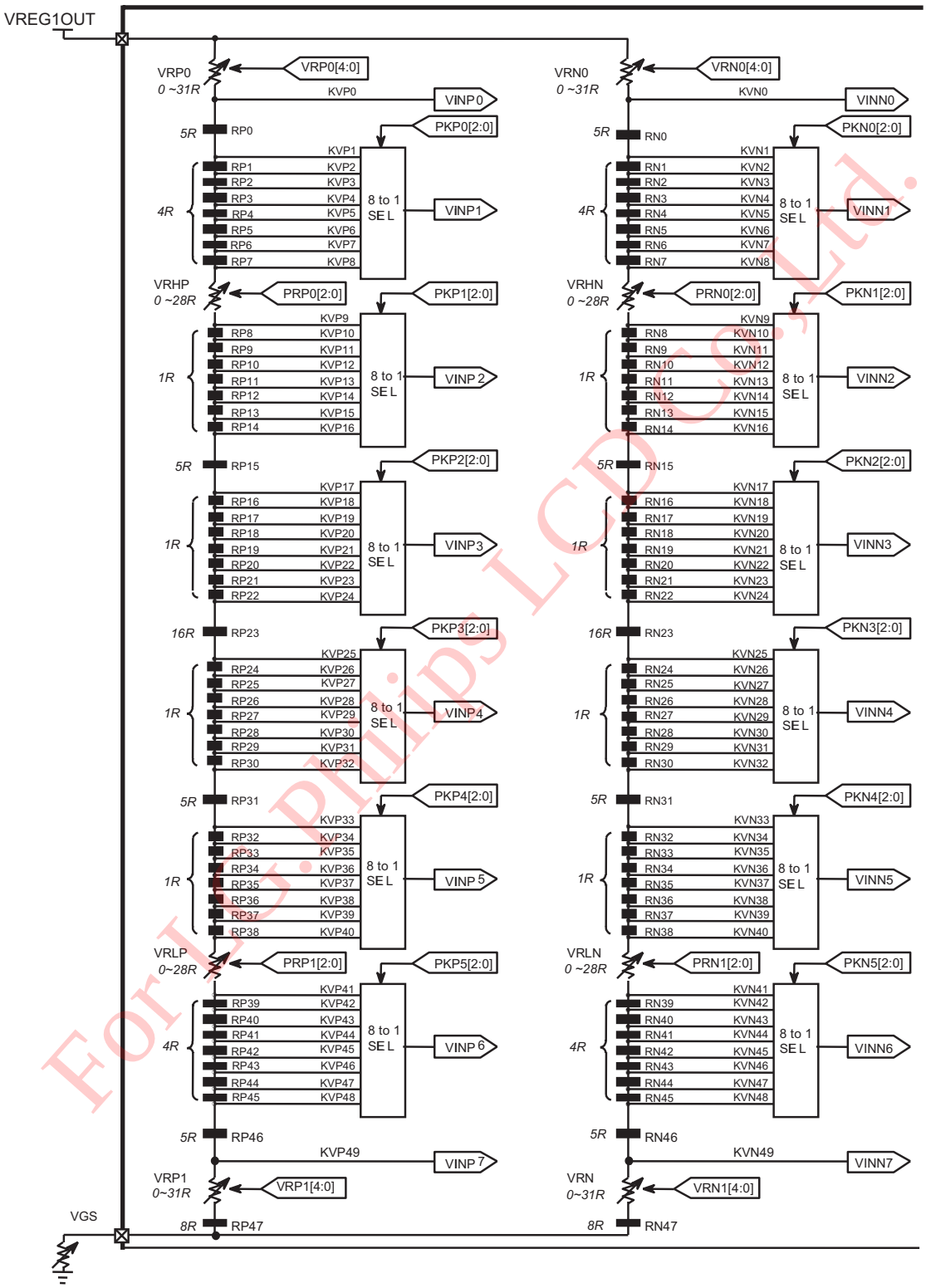


Figure 79 Reference voltage generating block (Ladder resistor units and 8-to-1 selectors)

γ Correction registers

The γ-correction registers of the R61503B consists of gradient-adjustment, amplitude-adjustment, fine-adjustment registers to correct grayscale voltage levels according to the gamma characteristics of the liquid crystal panel. These register settings make adjustments to the relationship between the grayscale number and its corresponding grayscale voltage level and the setting can be made differently for positive and negative polarities (the reference level and the register settings are the same for all RGB dots). The function of each register is as follows.

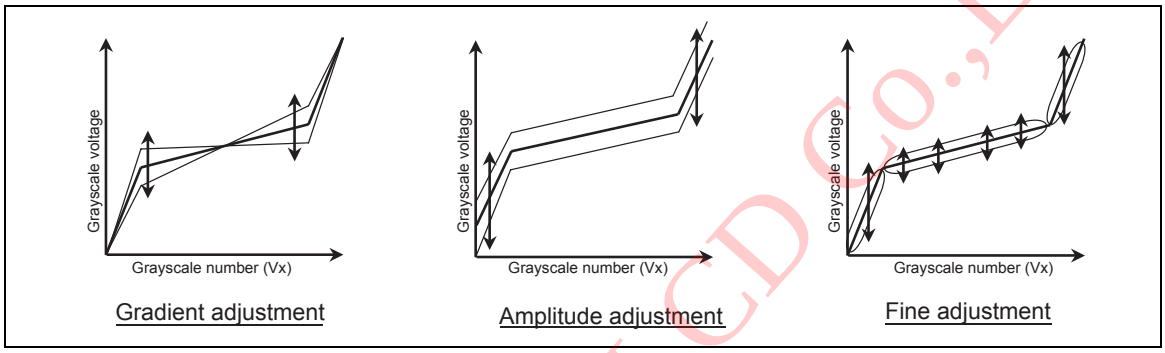


Figure 80

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradients in the middle grayscale range without changing the dynamic range. Adjustments are made by changing the resistance values of the resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit. The gradient adjustment registers consist of positive and negative polarity registers to allow asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage by changing the resistance values of the resistors (VRP(N)1/0) at both ends of the ladder resistor unit. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used for minute adjustment of grayscale voltage. The fine adjustment register represent one voltage level to be selected in the 8-to-1 selector among 8 levels generated from the ladder resistor unit. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 77 γ correction register

Register	Positive	Negative	Function
Gradient	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8 to1 selector (grayscales1-3 voltage levels)
	PKP1[2:0]	PKN1[2:0]	8 to1 selector (grayscale 4 voltage level)
	PKP2[2:0]	PKN2[2:0]	8 to1 selector (grayscale 10 voltage level)
	PKP3[2:0]	PKN3[2:0]	8 to1 selector (grayscale 21 voltage level)
	PKP4[2:0]	PKN4[2:0]	8 to1 selector (grayscale 27 voltage level)
	PKP5[2:0]	PKN5[2:0]	8 to1 selector (grayscale 28-30 voltage levels)

Reference voltage generating block (Ladder resistor units and 8-to-1 selectors)

Block configuration

The ladder resistor and 8-to-1 selector unit shown in page 155 consists of two ladder resistor unit including variable resistors and 8-to-1 selectors which selects a voltage generated by the ladder resistor unit and output the reference voltage from which grayscale voltages are generated. The γ correction registers represent the resistance values of these resistors in the ladder resistor unit and the reference levels selected in the 8-to-1 selectors (see Table 77 γ correction register).

Variable resistors

The R61503B uses variable resistors for the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and amplitude adjustment (2) (VRP(N)1). The resistance values are determined by gradient adjustment and amplitude adjustment registers as below.

Table 78
Gradient adjustment

Register PRP(N) 0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 79
Amplitude adjustment (1)

Register VRP(N)0[4:0]	Resistance VRP(N)0
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

Table 80
Amplitude adjustment (2)

Register VRP(N)1[4:0]	Resistance VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selector

The 8-to-1 selector selects one voltage level according to the fine adjustment register setting among the voltages generated by ladder resistors, and outputs the selected level as one of the reference voltages (VINP(N)1~6). The following table shows the correspondence between the selected voltage levels and the fine-adjustment register settings for respective reference voltage levels (VINP(N)1~6).

Table 81 Fine adjustment registers and selected voltage

Register bits	Selected Voltage level (reference grayscale voltage level)					
PKP(N)0/1[2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels V1 ~ V 31 is calculated from the following formula.

Table 82 Grayscale voltage calculation formula (positive polarity)

Pin	Formula	Fine-adjustment register	Reference voltage
KVP0	VREG1OUT-ΔV*VRP0/SUMRP	–	VINP0
KVP1	VREG1OUT-ΔV*(VRP0+5R)/SUMRP	PKP02-00="000"	VINP1
KVP2	VREG1OUT-ΔV*(VRP0+9R)/SUMRP	PKP02-00="001"	
KVP3	VREG1OUT-ΔV*(VRP0+13R)/SUMRP	PKP02-00="010"	
KVP4	VREG1OUT-ΔV*(VRP0+17R)/SUMRP	PKP02-00="011"	
KVP5	VREG1OUT-ΔV*(VRP0+21R)/SUMRP	PKP02-00="100"	
KVP6	VREG1OUT-ΔV*(VRP0+25R)/SUMRP	PKP02-00="101"	
KVP7	VREG1OUT-ΔV*(VRP0+29R)/SUMRP	PKP02-00="110"	
KVP8	VREG1OUT-ΔV*(VRP0+33R)/SUMRP	PKP02-00="111"	
KVP9	VREG1OUT-ΔV*（VRP0+33R+VRHP）/SUMRP	PKP12-10="000"	VINP2
KVP10	VREG1OUT-ΔV*（VRP0+34R+VRHP）/SUMRP	PKP12-10="001"	
KVP11	VREG1OUT-ΔV*（VRP0+35R+VRHP）/SUMRP	PKP12-10="010"	
KVP12	VREG1OUT-ΔV*（VRP0+36R+VRHP）/SUMRP	PKP12-10="011"	
KVP13	VREG1OUT-ΔV*（VRP0+37R+VRHP）/SUMRP	PKP12-10="100"	
KVP14	VREG1OUT-ΔV*（VRP0+38R+VRHP）/SUMRP	PKP12-10="101"	
KVP15	VREG1OUT-ΔV*（VRP0+39R+VRHP）/SUMRP	PKP12-10="110"	
KVP16	VREG1OUT-ΔV*（VRP0+40R+VRHP）/SUMRP	PKP12-10="111"	
KVP17	VREG1OUT-ΔV*（VRP0+45R+VRHP）/SUMRP	PKP22-20="000"	VINP3
KVP18	VREG1OUT-ΔV*（VRP0+46R+VRHP）/SUMRP	PKP22-20="001"	
KVP19	VREG1OUT-ΔV*（VRP0+47R+VRHP）/SUMRP	PKP22-20="010"	
KVP20	VREG1OUT-ΔV*（VRP0+48R+VRHP）/SUMRP	PKP22-20="011"	
KVP21	VREG1OUT-ΔV*（VRP0+49R+VRHP）/SUMRP	PKP22-20="100"	
KVP22	VREG1OUT-ΔV*（VRP0+50R+VRHP）/SUMRP	PKP22-20="101"	
KVP23	VREG1OUT-ΔV*（VRP0+51R+VRHP）/SUMRP	PKP22-20="110"	
KVP24	VREG1OUT-ΔV*（VRP0+52R+VRHP）/SUMRP	PKP22-20="111"	
KVP25	VREG1OUT-ΔV*（VRP0+68R+VRHP）/SUMRP	PKP32-30="000"	VINP4
KVP26	VREG1OUT-ΔV*（VRP0+69R+VRHP）/SUMRP	PKP32-30="001"	
KVP27	VREG1OUT-ΔV*（VRP0+70R+VRHP）/SUMRP	PKP32-30="010"	
KVP28	VREG1OUT-ΔV*（VRP0+71R+VRHP）/SUMRP	PKP32-30="011"	
KVP29	VREG1OUT-ΔV*（VRP0+72R+VRHP）/SUMRP	PKP32-30="100"	
KVP30	VREG1OUT-ΔV*（VRP0+73R+VRHP）/SUMRP	PKP32-30="101"	
KVP31	VREG1OUT-ΔV*（VRP0+74R+VRHP）/SUMRP	PKP32-30="110"	
KVP32	VREG1OUT-ΔV*（VRP0+75R+VRHP）/SUMRP	PKP32-30="111"	
KVP33	VREG1OUT-ΔV*（VRP0+80R+VRHP）/SUMRP	PKP42-40="000"	VINP5
KVP34	VREG1OUT-ΔV*（VRP0+81R+VRHP）/SUMRP	PKP42-40="001"	
KVP35	VREG1OUT-ΔV*（VRP0+82R+VRHP）/SUMRP	PKP42-40="010"	
KVP36	VREG1OUT-ΔV*（VRP0+83R+VRHP）/SUMRP	PKP42-40="011"	
KVP37	VREG1OUT-ΔV*（VRP0+84R+VRHP）/SUMRP	PKP42-40="100"	
KVP38	VREG1OUT-ΔV*（VRP0+85R+VRHP）/SUMRP	PKP42-40="101"	
KVP39	VREG1OUT-ΔV*（VRP0+86R+VRHP）/SUMRP	PKP42-40="110"	
KVP40	VREG1OUT-ΔV*（VRP0+87R+VRHP）/SUMRP	PKP42-40="111"	
KVP41	VREG1OUT-ΔV*（VRP0+87R+VRHP+VRLP）/SUMRP	PKP52-50="000"	VINP6
KVP42	VREG1OUT-ΔV*（VRP0+91R+VRHP+VRLP）/SUMRP	PKP52-50="001"	
KVP43	VREG1OUT-ΔV*（VRP0+95R+VRHP+VRLP）/SUMRP	PKP52-50="010"	
KVP44	VREG1OUT-ΔV*（VRP0+99R+VRHP+VRLP）/SUMRP	PKP52-50="011"	
KVP45	VREG1OUT-ΔV*（VRP0+103R+VRHP+VRLP）/SUMRP	PKP52-50="100"	
KVP46	VREG1OUT-ΔV*（VRP0+107R+VRHP+VRLP）/SUMRP	PKP52-50="101"	
KVP47	VREG1OUT-ΔV*（VRP0+111R+VRHP+VRLP）/SUMRP	PKP52-50="110"	
KVP48	VREG1OUT-ΔV*（VRP0+115R+VRHP+VRLP）/SUMRP	PKP52-50="111"	
KVP49	VREG1OUT-ΔV*（VRP0+120R+VRHP+VRLP）/SUMRP	–	VINP7

SUMRP : Sum of positive polarity ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
ΔV : Electrical potential between VREG1OUT and VGS

Table 83 Grayscale voltage calculation formula (positive polarity)

Grayscale	Formula
V0	VINP0
V1	V4+(VINP1-V4)*(15/24)
V2	V4+(VINP1-V4)*(8/24)
V3	V4+(VINP1-V4)*(4/24)
V4	VINP2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V10+(V4-V10)*(4/24)
V10	VINP3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINP4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINP5
V28	VINP6+(V27-VINP6)*(20/24)
V29	VINP6+(V27-VINP6)*(16/24)
V30	VINP6+(V27-VINP6)*(9/24)
V31	VINP7

Make sure DDVDH – V0 > 0.5V and DDVDH – V8 >1.1V.

Table 84 Grayscale voltage calculation formula (negative polarity)

Pin	Formula	Fine-adjustment register	Reference voltage
KVN0	VREG1OUT-ΔV*VRN0/SUMRN	—	VINN0
KVN1	VREG1OUT-ΔV*(VRN0+5R)/SUMRN	PKN02-00="000"	VINN1
KVN2	VREG1OUT-ΔV*(VRN0+9R)/SUMRN	PKN02-00="001"	
KVN3	VREG1OUT-ΔV*(VRN0+13R)/SUMRN	PKN02-00="010"	
KVN4	VREG1OUT-ΔV*(VRN0+17R)/SUMRN	PKN02-00="011"	
KVN5	VREG1OUT-ΔV*(VRN0+21R)/SUMRN	PKN02-00="100"	
KVN6	VREG1OUT-ΔV*(VRN0+25R)/SUMRN	PKN02-00="101"	
KVN7	VREG1OUT-ΔV*(VRN0+29R)/SUMRN	PKN02-00="110"	
KVN8	VREG1OUT-ΔV*(VRN0+33R)/SUMRN	PKN02-00="111"	
KVN9	VREG1OUT-ΔV*（VRN0+33R+VRHN）/SUMRN	PKN12-10="000"	VINN2
KVN10	VREG1OUT-ΔV*（VRN0+34R+VRHN）/SUMRN	PKN12-10="001"	
KVN11	VREG1OUT-ΔV*（VRN0+35R+VRHN）/SUMRN	PKN12-10="010"	
KVN12	VREG1OUT-ΔV*（VRN0+36R+VRHN）/SUMRN	PKN12-10="011"	
KVN13	VREG1OUT-ΔV*（VRN0+37R+VRHN）/SUMRN	PKN12-10="100"	
KVN14	VREG1OUT-ΔV*（VRN0+38R+VRHN）/SUMRN	PKN12-10="101"	
KVN15	VREG1OUT-ΔV*（VRN0+39R+VRHN）/SUMRN	PKN12-10="110"	
KVN16	VREG1OUT-ΔV*（VRN0+40R+VRHN）/SUMRN	PKN12-10="111"	
KVN17	VREG1OUT-ΔV*（VRN0+45R+VRHN）/SUMRN	PKN22-20="000"	VINN3
KVN18	VREG1OUT-ΔV*（VRN0+46R+VRHN）/SUMRN	PKN22-20="001"	
KVN19	VREG1OUT-ΔV*（VRN0+47R+VRHN）/SUMRN	PKN22-20="010"	
KVN20	VREG1OUT-ΔV*（VRN0+48R+VRHN）/SUMRN	PKN22-20="011"	
KVN21	VREG1OUT-ΔV*（VRN0+49R+VRHN）/SUMRN	PKN22-20="100"	
KVN22	VREG1OUT-ΔV*（VRN0+50R+VRHN）/SUMRN	PKN22-20="101"	
KVN23	VREG1OUT-ΔV*（VRN0+51R+VRHN）/SUMRN	PKN22-20="110"	
KVN24	VREG1OUT-ΔV*（VRN0+52R+VRHN）/SUMRN	PKN22-20="111"	
KVN25	VREG1OUT-ΔV*（VRN0+68R+VRHN）/SUMRN	PKN32-30="000"	VINN4
KVN26	VREG1OUT-ΔV*（VRN0+69R+VRHN）/SUMRN	PKN32-30="001"	
KVN27	VREG1OUT-ΔV*（VRN0+70R+VRHN）/SUMRN	PKN32-30="010"	
KVN28	VREG1OUT-ΔV*（VRN0+71R+VRHN）/SUMRN	PKN32-30="011"	
KVN29	VREG1OUT-ΔV*（VRN0+72R+VRHN）/SUMRN	PKN32-30="100"	
KVN30	VREG1OUT-ΔV*（VRN0+73R+VRHN）/SUMRN	PKN32-30="101"	
KVN31	VREG1OUT-ΔV*（VRN0+74R+VRHN）/SUMRN	PKN32-30="110"	
KVN32	VREG1OUT-ΔV*（VRN0+75R+VRHN）/SUMRN	PKN32-30="111"	
KVN33	VREG1OUT-ΔV*（VRN0+80R+VRHN）/SUMRN	PKN42-40="000"	VINN5
KVN34	VREG1OUT-ΔV*（VRN0+81R+VRHN）/SUMRN	PKN42-40="001"	
KVN35	VREG1OUT-ΔV*（VRN0+82R+VRHN）/SUMRN	PKN42-40="010"	
KVN36	VREG1OUT-ΔV*（VRN0+83R+VRHN）/SUMRN	PKN42-40="011"	
KVN37	VREG1OUT-ΔV*（VRN0+84R+VRHN）/SUMRN	PKN42-40="100"	
KVN38	VREG1OUT-ΔV*（VRN0+85R+VRHN）/SUMRN	PKN42-40="101"	
KVN39	VREG1OUT-ΔV*（VRN0+86R+VRHN）/SUMRN	PKN42-40="110"	
KVN40	VREG1OUT-ΔV*（VRN0+87R+VRHN）/SUMRN	PKN42-40="111"	
KVN41	VREG1OUT-ΔV*（VRN0+87R+VRHN+VRLN）/SUMRN	PKN52-50="000"	VINN6
KVN42	VREG1OUT-ΔV*（VRN0+91R+VRHN+VRLN）/SUMRN	PKN52-50="001"	
KVN43	VREG1OUT-ΔV*（VRN0+95R+VRHN+VRLN）/SUMRN	PKN52-50="010"	
KVN44	VREG1OUT-ΔV*（VRN0+99R+VRHN+VRLN）/SUMRN	PKN52-50="011"	
KVN45	VREG1OUT-ΔV*（VRN0+103R+VRHN+VRLN）/SUMRN	PKN52-50="100"	
KVN46	VREG1OUT-ΔV*（VRN0+107R+VRHN+VRLN）/SUMRN	PKN52-50="101"	
KVN47	VREG1OUT-ΔV*（VRN0+111R+VRHN+VRLN）/SUMRN	PKN52-50="110"	
KVN48	VREG1OUT-ΔV*（VRN0+115R+VRHN+VRLN）/SUMRN	PKN52-50="111"	
KVN49	VREG1OUT-ΔV*（VRN0+120R+VRHN+VRLN）/SUMRN	—	VINN7

SUMRN : Sum of negative polarity ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV : Electrical potential between VREG1OUT and VGS

Table 85 Grayscale voltage calculation formula (negative polarity)

Grayscale	Formula
V0	VINN0
V1	V4+(VINN-V4)*(15/24)
V2	V4+(VINN-V4)*(8/24)
V3	V4+(VINN-V4)*(4/24)
V4	VINN2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V10+(V4-V10)*(4/24)
V10	VINN3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINN4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINN5
V28	VINN6+(V27-VINN6)*(20/24)
V29	VINN6+(V27-VINN6)*(16/24)
V30	VINN6+(V27-VINN6)*(9/24)
V31	VINN7

Make sure DDVDH – V0 > 0.5V and DDVDH – V8 >1.1V.

RAM data (RGB dot data bits) and the source output level

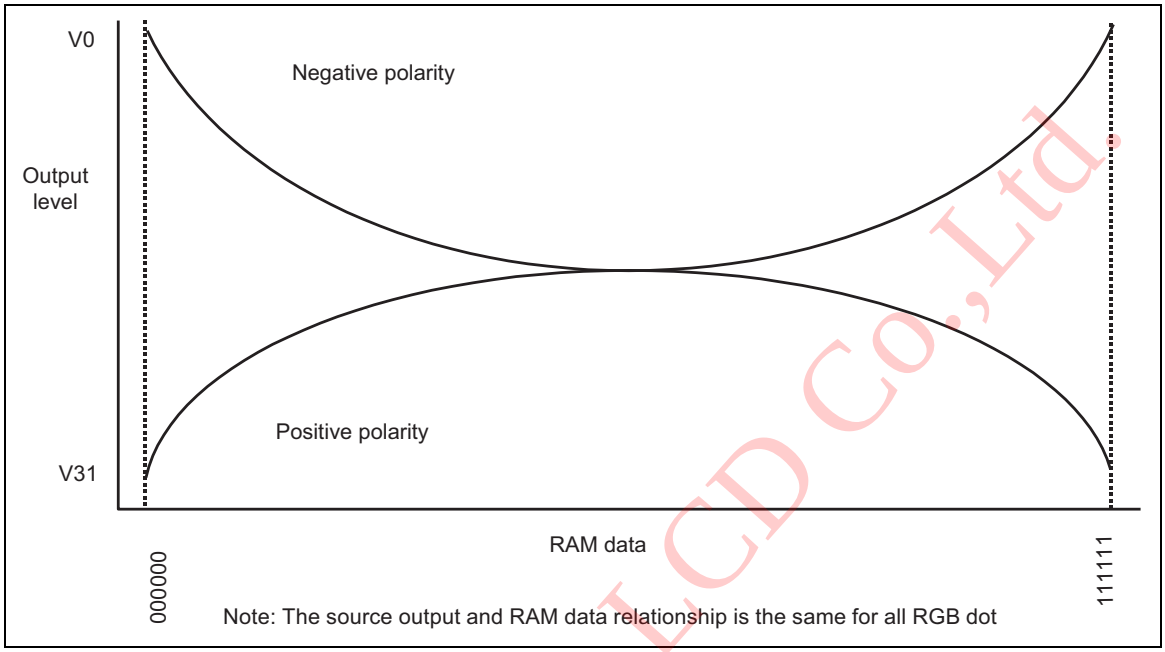


Figure 81

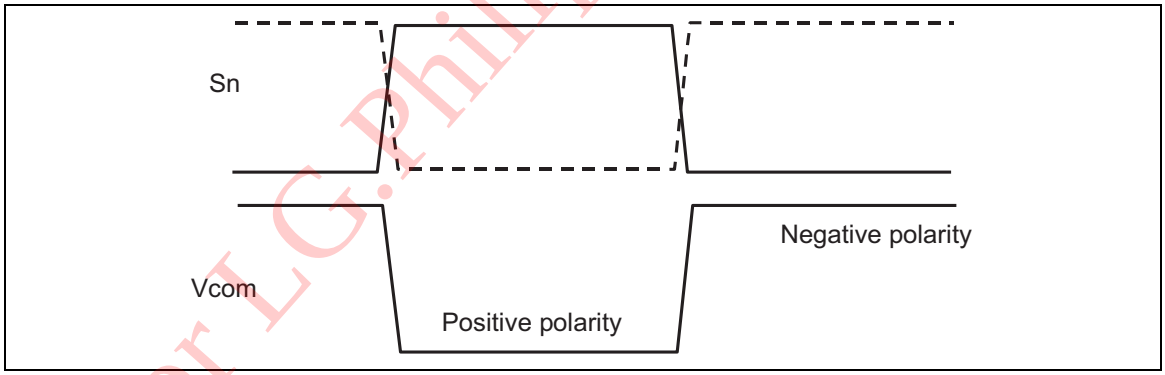


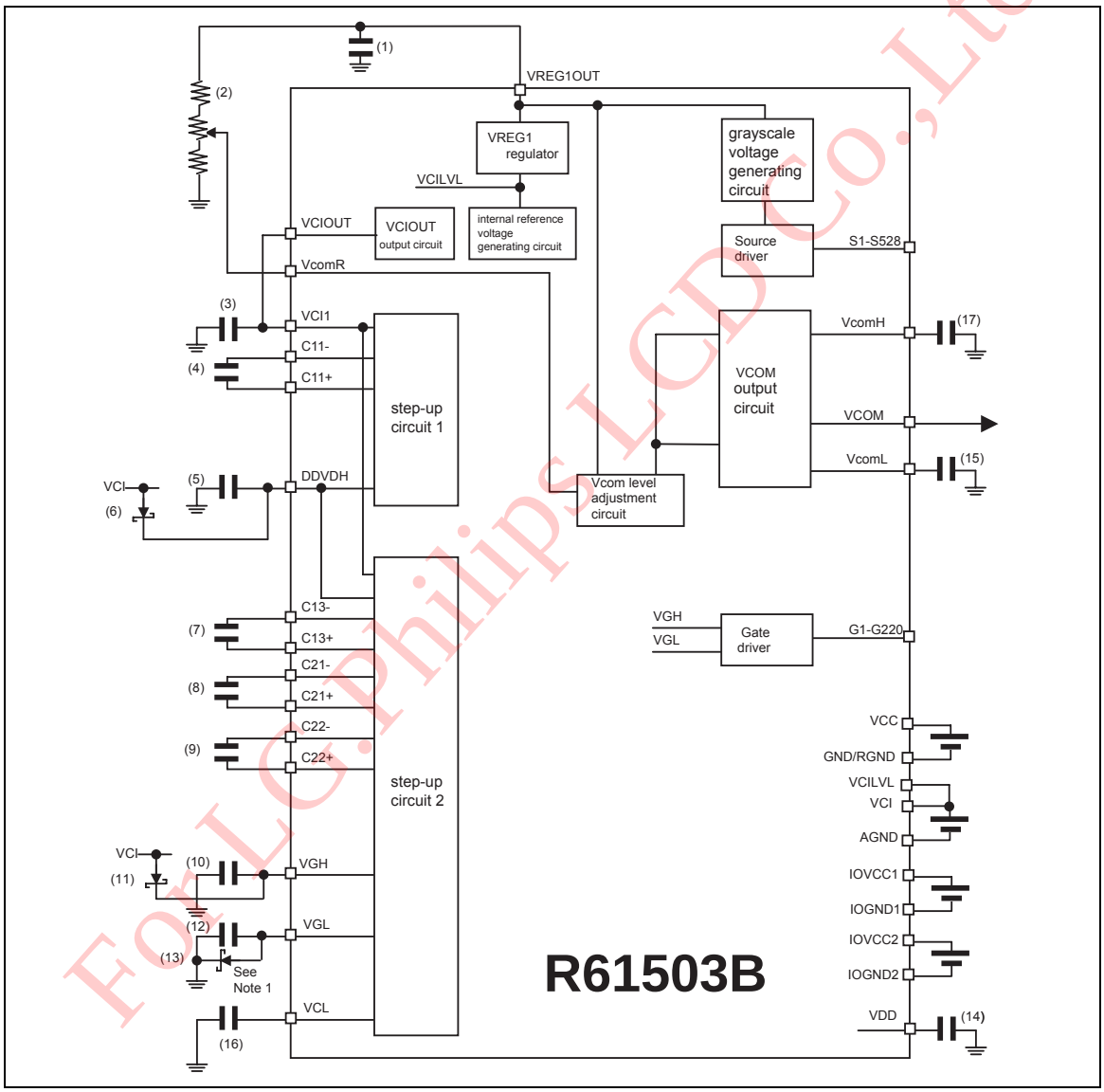
Figure 82 Source output waveform and Vcom polarity

Power Supply Generating Circuit

The following is the configuration of LCD drive voltage generating circuit of the R61503B.

Power supply circuit connection example1 (Vci1=VciOUT)

The VciOUT output circuit changes the VciOUT level in this example.

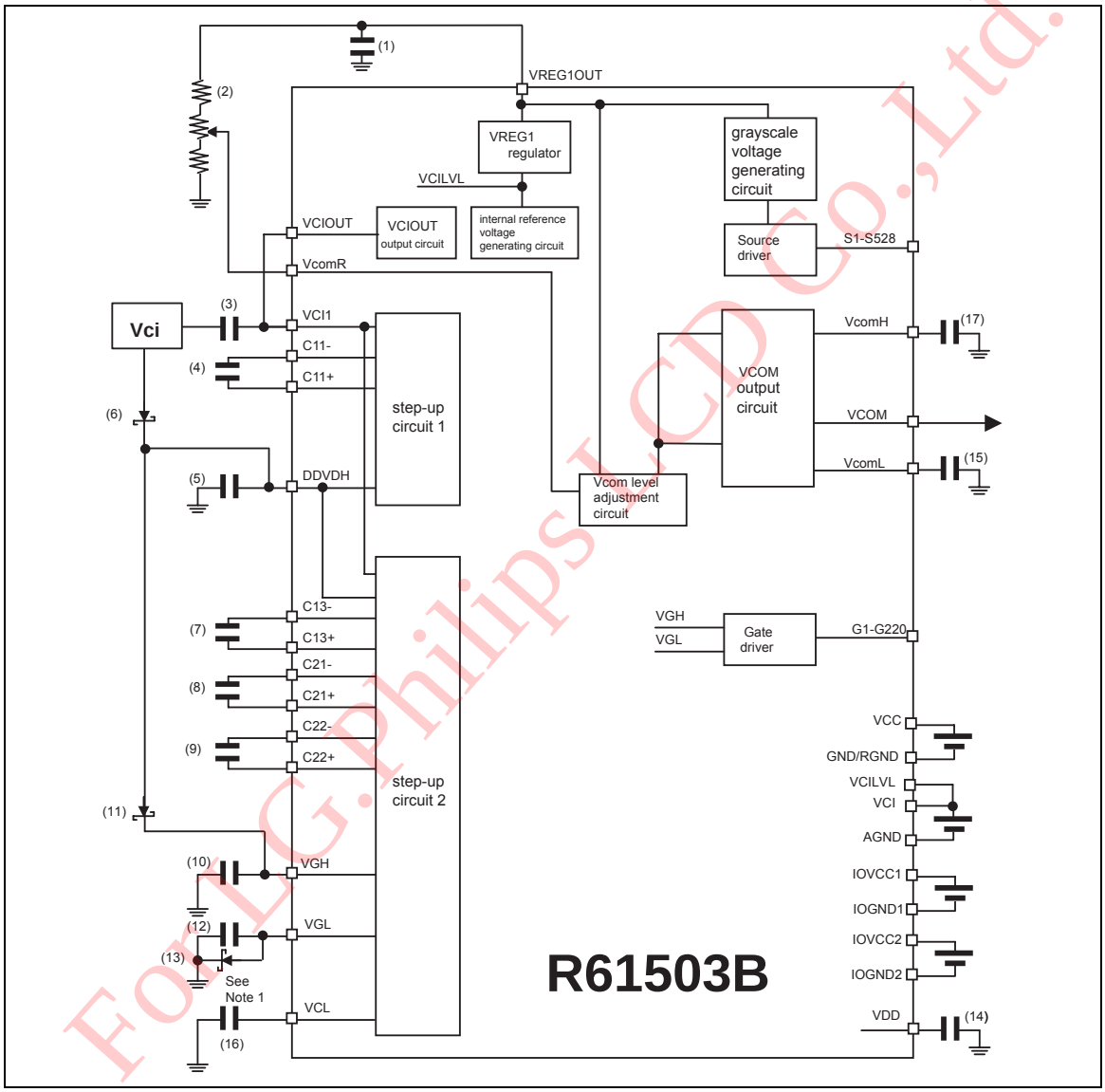


Note: The wiring resistances between GND/VGL to the schottky diodes must be 10Ω or less.

Figure 83

Power supply circuit connection example 2 (Vci1=Vci direct input)

This connection example allows directly applying the Vci electrical potential to Vci1. In this case, the VciOUT adjustment circuit is not available* see Note 2, but the efficiency of the step-up operation can be enhanced.



Notes: 1. The wiring resistances between GND/VGL and the schottky diodes must be 10Ω or less.

2. When directly applying Vci to Vci1, set VC=3'h7. Capacitor connection is not required for VciOUT output.

Figure 84

Specifications of external elements for the power supply circuit

The specifications of external elements connected to the power supply circuit of the R61503B are as follows.

Table 86 Capacitor

Capacitance	Upper voltage limit	Pin connection
1μF Characteristics B	6V	(3) VciOUT, (4) C11-/+ (7) C13-/+, (14) VDD, (15) VcomL, (16) VCL
	10V	(1) VREG1OUT, (5) DDVDH, (8) C21-/+, (9) C22-/+, (17) VcomH
	25V	(10) VGH, (12) VGL

Notes: 1. Check the capacitor by connecting it on the LC module.
2. The numbers in the parentheses correspond to the numbers in Figure 83 and Figure 84.

Table 87 Schottky diode

Specification	Pin connection
VF ＜ 0.4V/20mA@25℃, VR≧25V (Recommended diode: HSC226)	(13) GND-VGL (11) Vci-VGH (6) Vci-DDVDH

Table 88 Variable resistor

Specification	Pin connection
＞200kΩ	(2) VcomR

Table 89 Internal logic power supply

Capacitor	Recommended voltage proof	Pin connection
IμF (B characteristics)	3V	VDD

Table 90 Oscillator

Resistance	Condition of usage	Pin connection
Rf	Rf ≥ 1mW ≥ ± 1%	OSC1-OSC2

Voltage generation diagram

The following are the diagrams of voltage generation in the R61503B and the TFT display application voltage waveforms and electrical potential relationship.

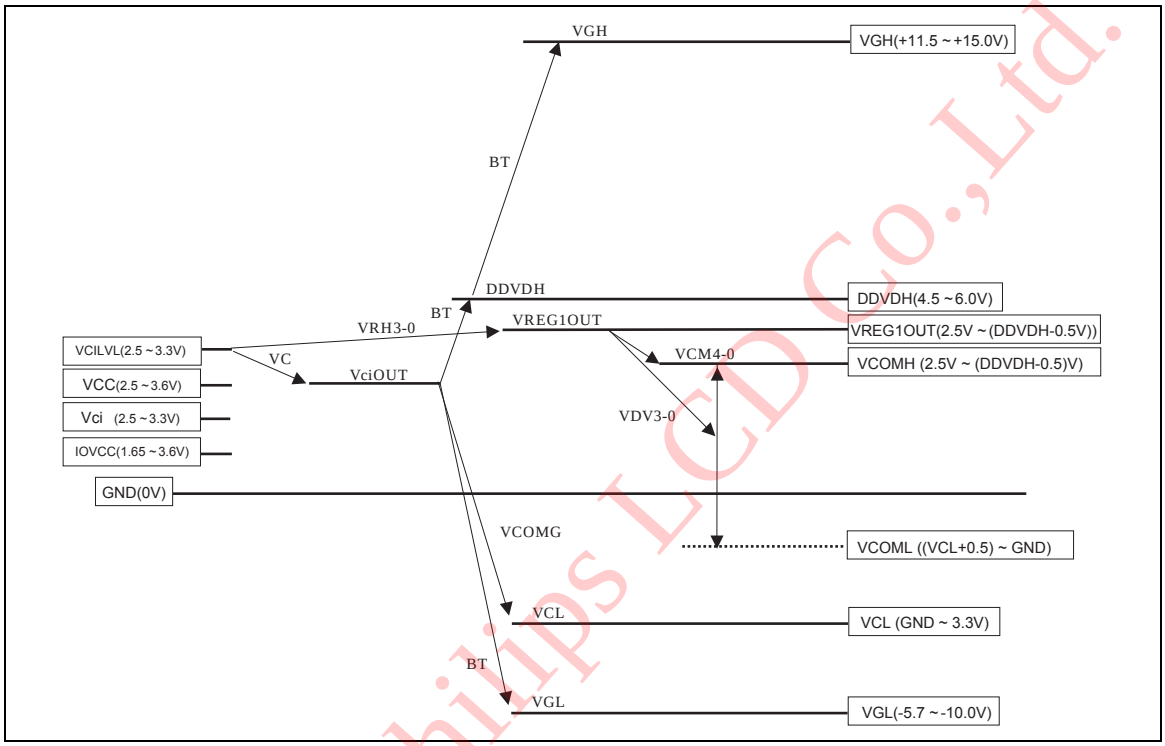


Figure 85 Pattern diagram for voltage setting

Notes: 1. The DDVDH, VGH, VGL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at respective outputs. Make sure that output voltage levels in operation do not conflict with the following conditions: (DDVDH – VREG1OUT) > 0.5V, (DDVDH – VcomH) > 0.5V, (VcomL – VCL) > 0.5V. When the alternating cycle of Vcom is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges are recommended.

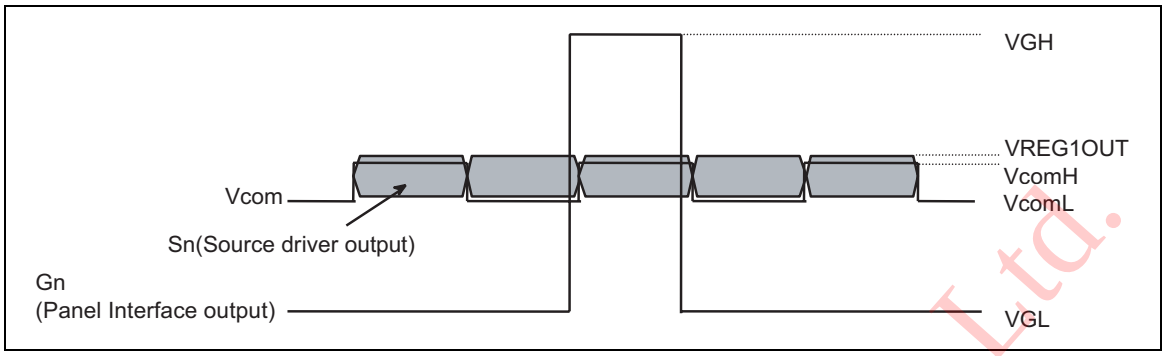


Figure 86 TFT display application voltage waveform and electrical potential

Power Supply Setting sequence

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences.

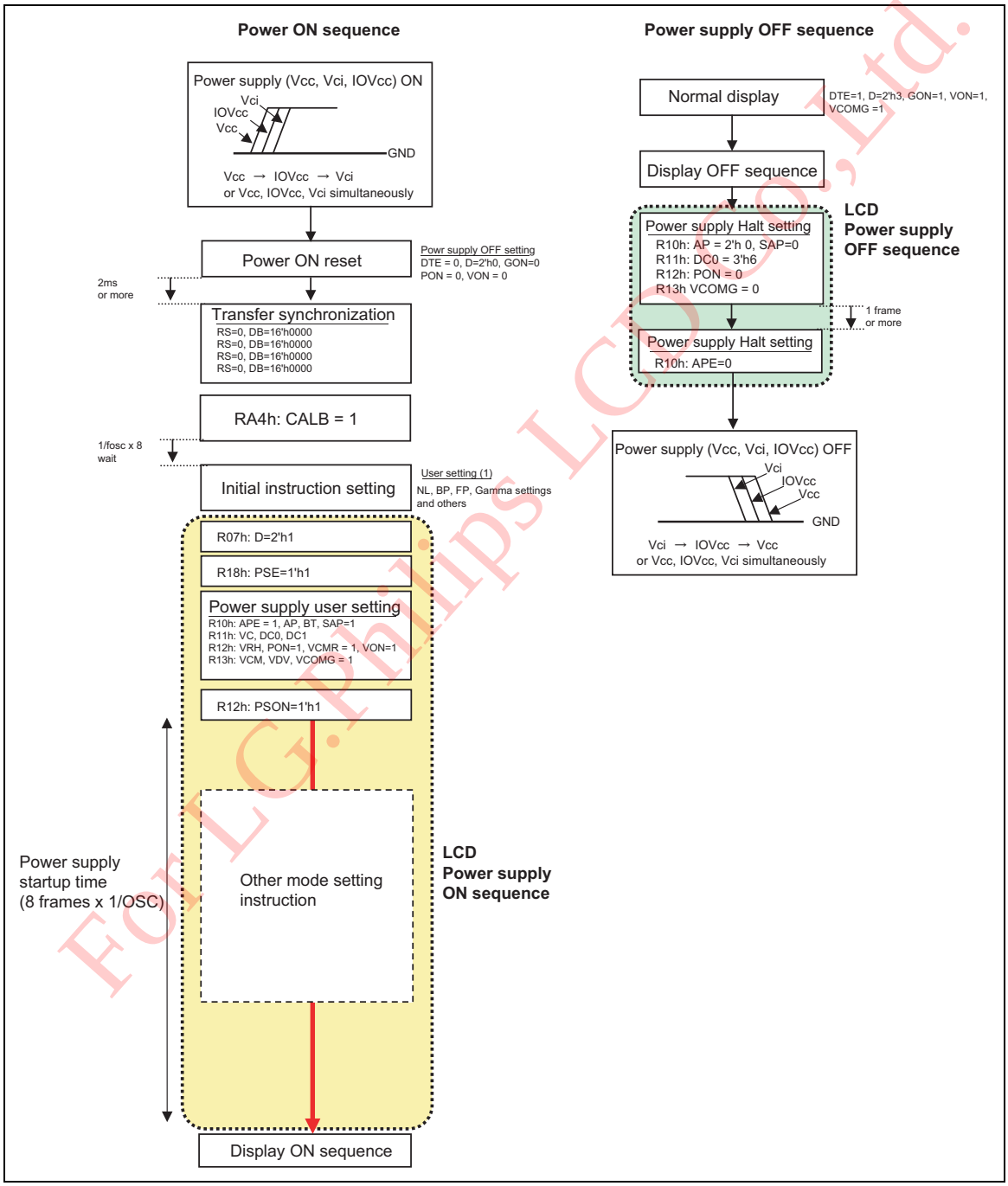


Figure 87

Instruction Setting

The following are the sequences for various instruction settings. When setting instruction in the R61503B, follow the sequence below.

Display ON/OFF

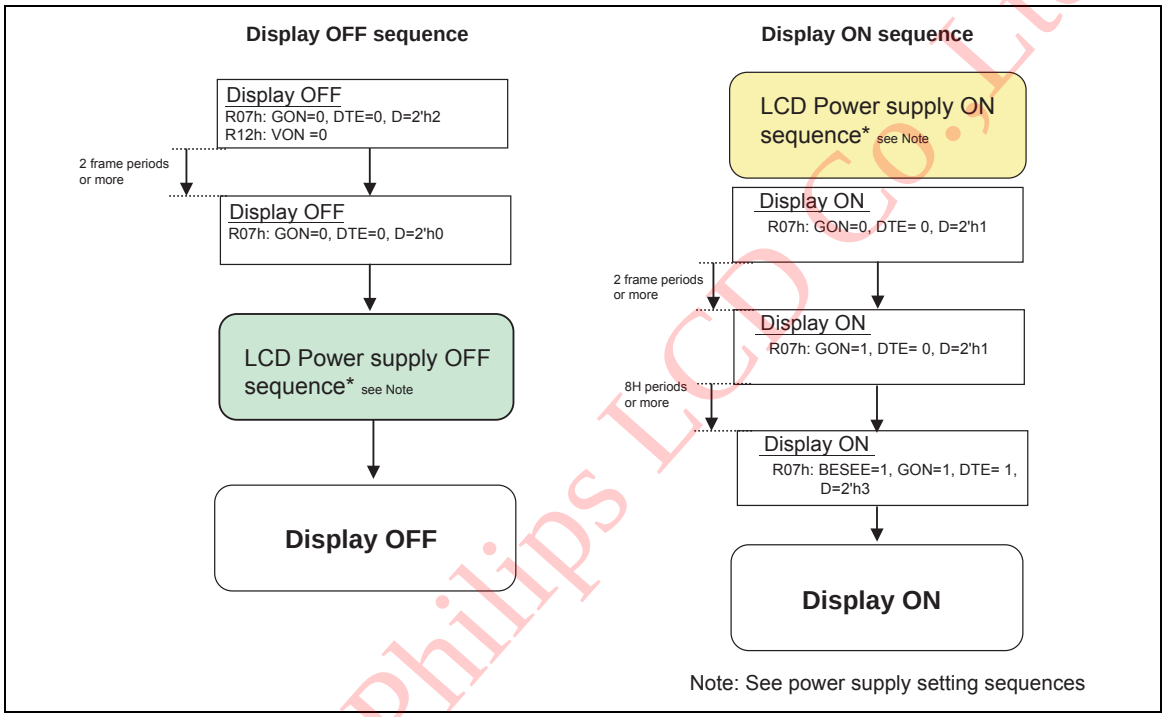


Figure 88

Sleep/Standby mode

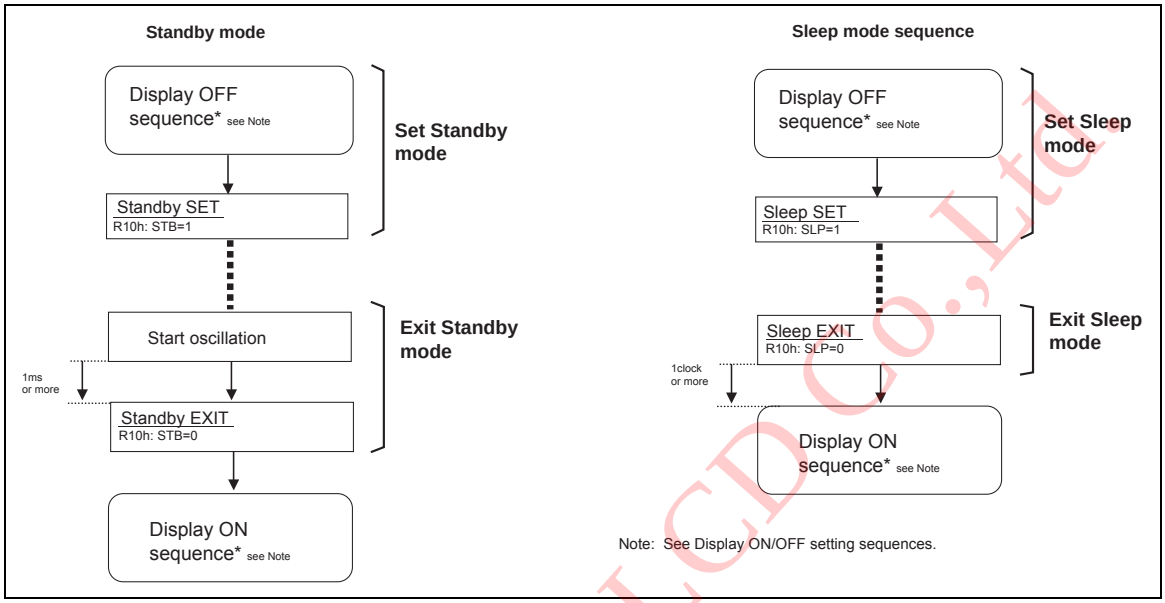


Figure 89

Deep standby mode

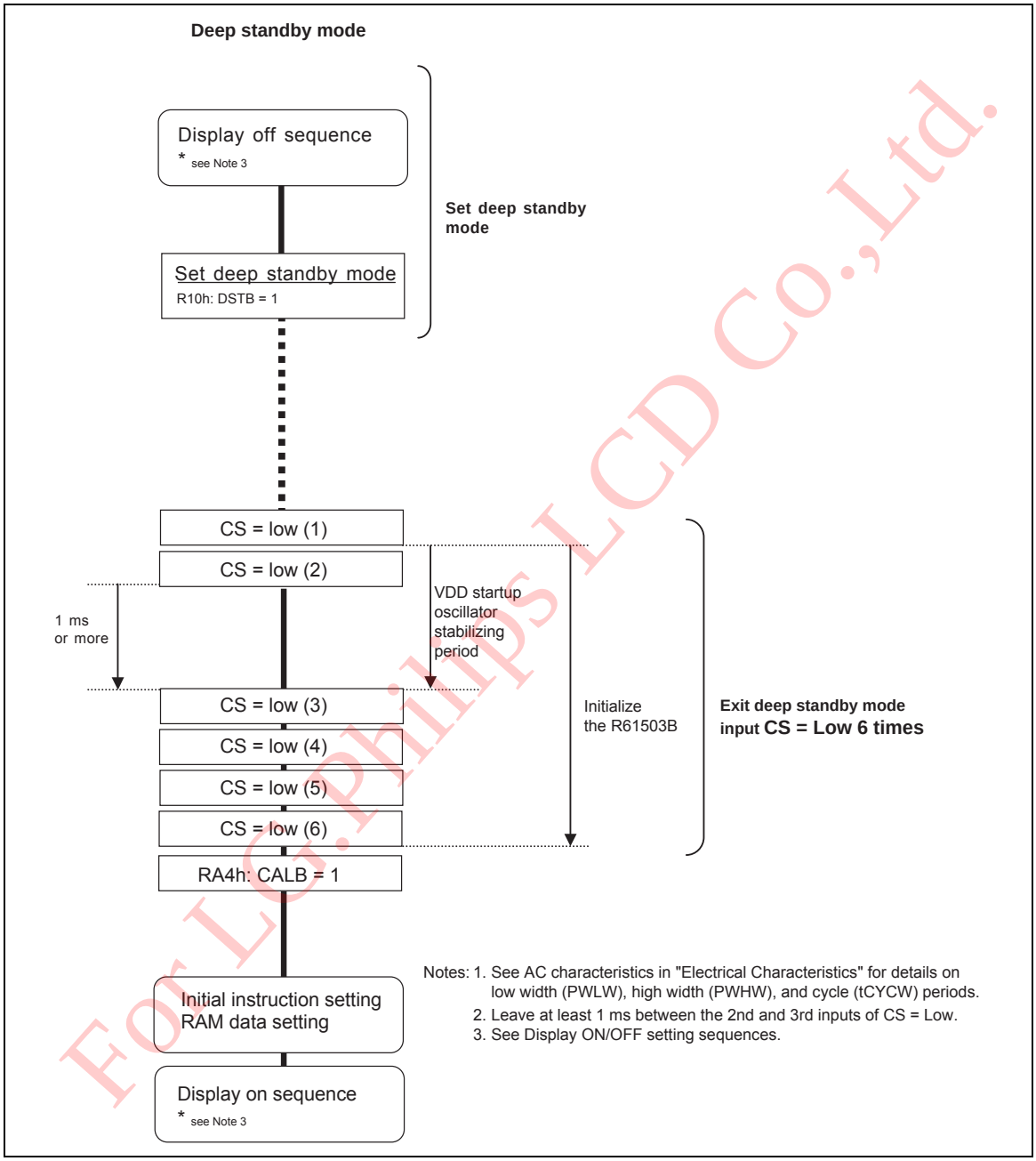


Figure 90

EPROM control

The R61503B incorporates 8-bits x 3 address EPROM. User identification code is written in the EPROM address 0'h. VcomH setting instruction is written in the EPROM addresses 1'h, 2'h. The R61503B's EPROM has two addresses for VcomH setting to allow changing the VcomH setting. When writing the VcomH setting for the first time, write the setting in the address 1'h. Write the setting in the address 2'h when writing the setting for the second time. Make sure to write "1" to EVCM0 and EVCM1 bits. When the second VcomH setting is written in the address 2'h, the second setting is enabled.

The VCMSEL bit in the R13h register determines whether the setting in the EPROM or the VCM[4:0] setting (externally inputted instruction) is enabled to set the VcomH level. Set VCMSEL = 1, when enabling the EPROM setting. Set VCMSEL = 0, when not using the EPROM setting.

When writing the setting to the EPROM, make sure to follow the EPROM write sequence.

By performing an EPROM read operation, the setting written in EPROM is read out. In this case, follow the EPROM read sequence. In case of setting CALB = 1 (RA4h: calibration to internal operation) after power-on reset, the data written in the EPROM is stored in the EPROM read register.

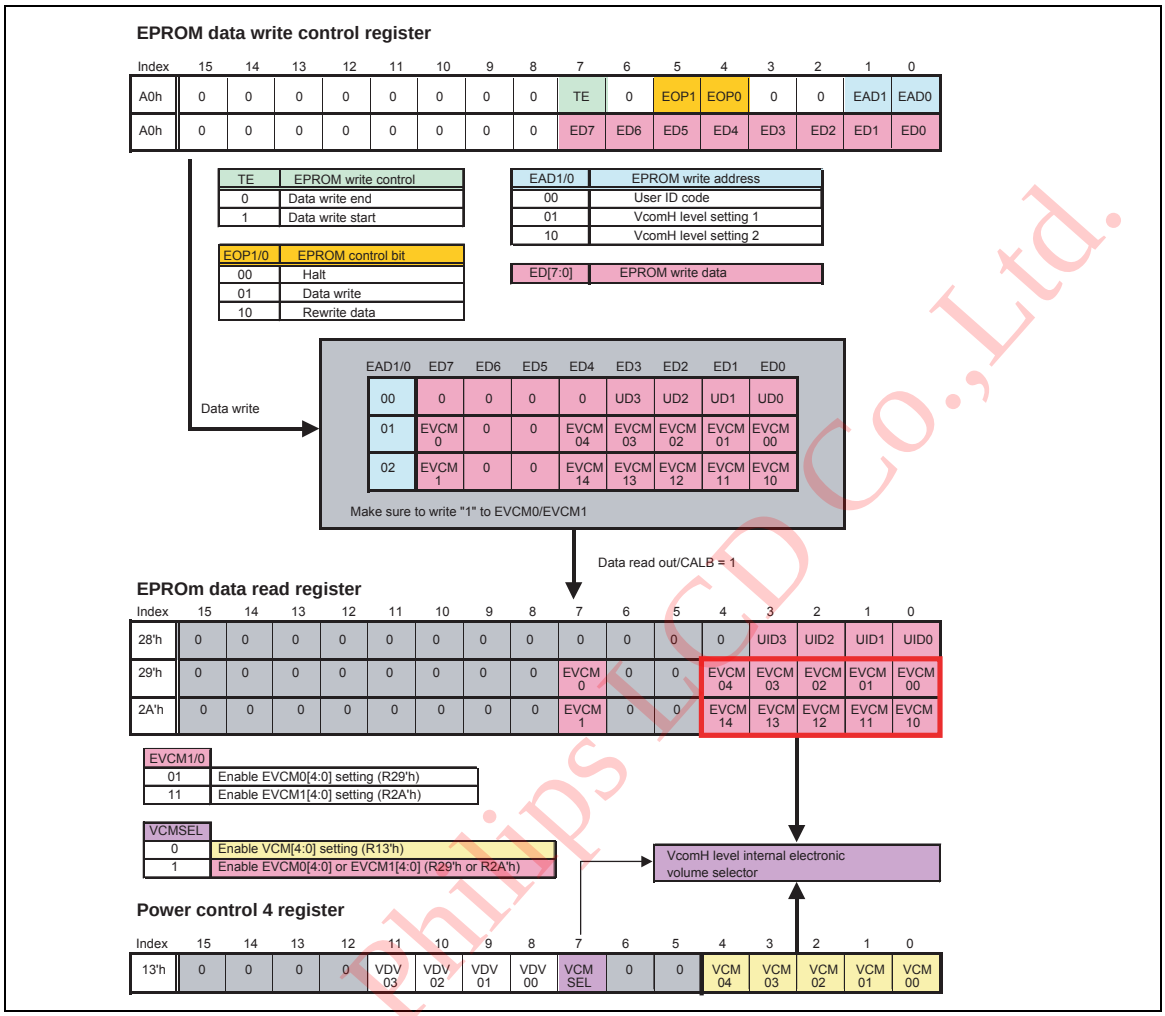


Figure 91 EPROM system configuration

EPROM write/read sequence

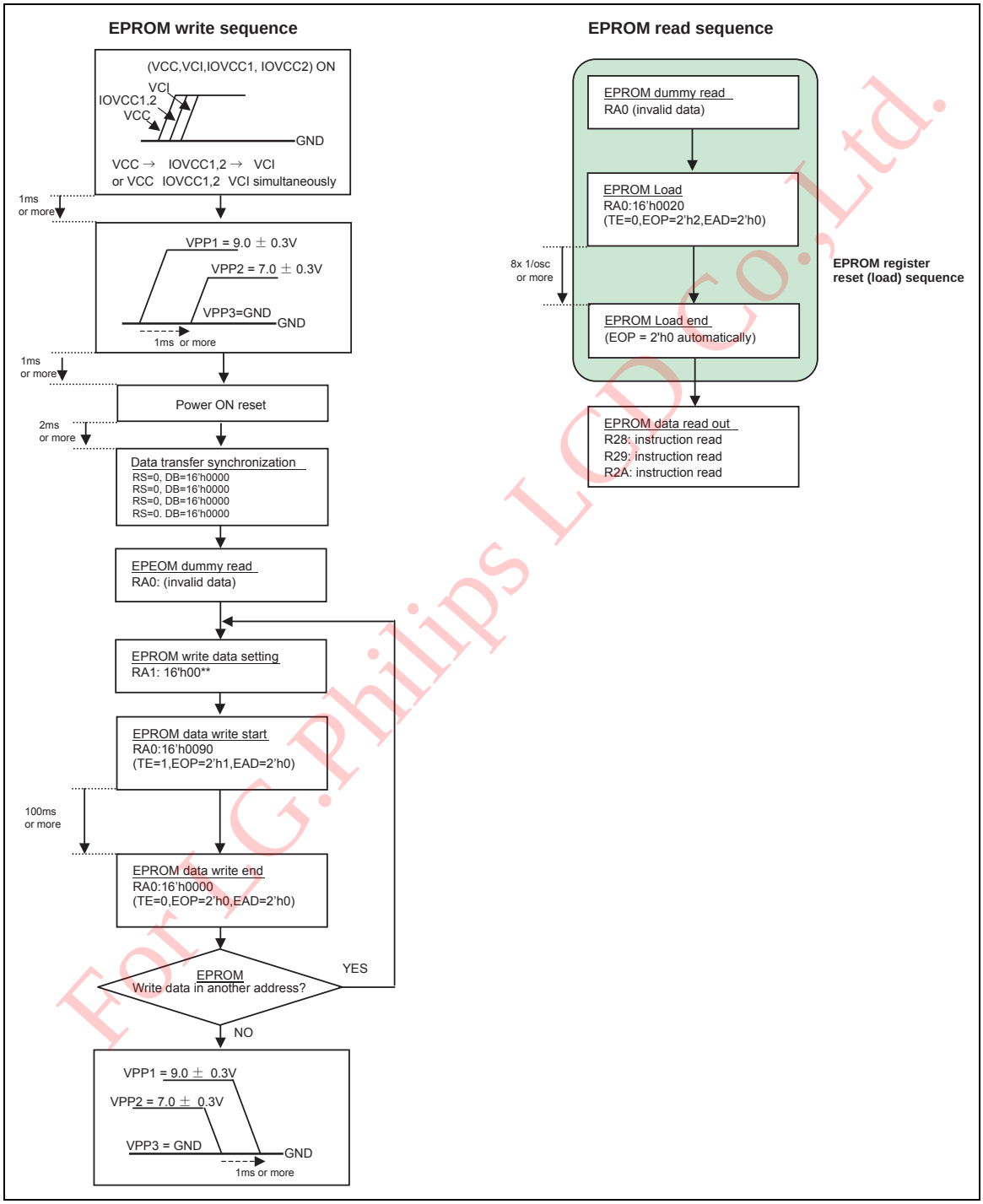


Figure 92 EPROM write sequence

R61503B recommended resistance and connection example

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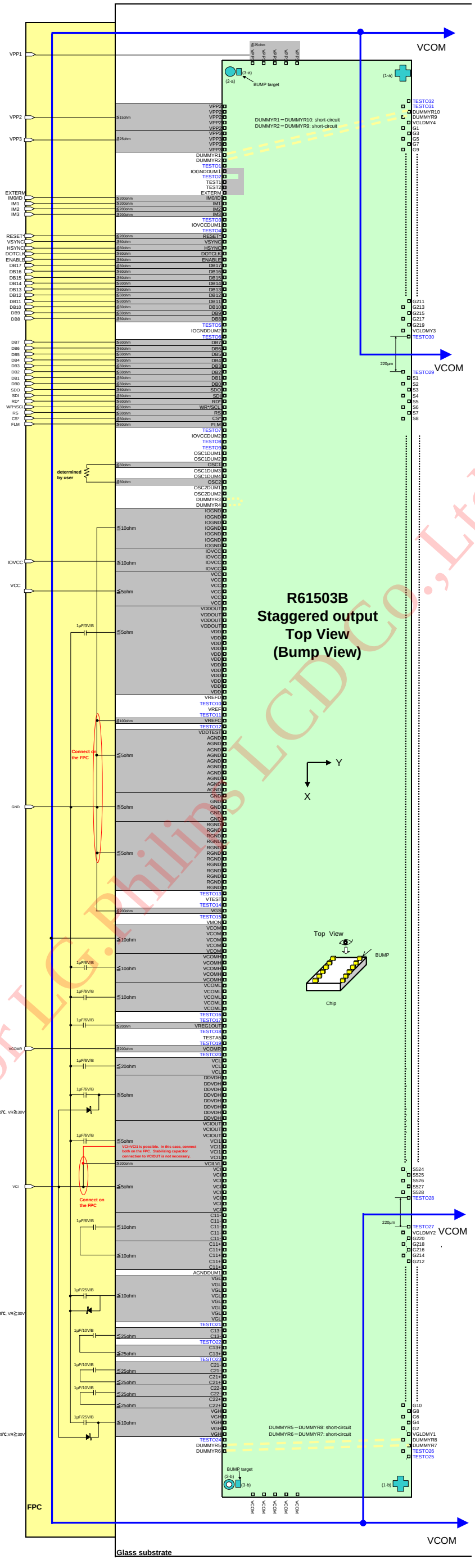


Absolute Maximum Ratings

Table 91

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci - AGND	V	-0.3 ~ + 4.6	1, 3
Power supply voltage (3)	DDVDH - AGND	V	-0.3 ~ + 6.5	1, 4
Power supply voltage (4)	VGH - VGL	V	+11.0 ~ + 30.0	1, 4
Power supply voltage (5)	AGND - VGL	V	+3.0 ~ +13.0	1, 7
Power supply voltage (6)	DDVDH - VGL	V	+7.0 ~ +19.0	1, 5
Power supply voltage (7)	Vci - VGL	V	+5.5 ~ +16.8	1, 7
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 8
Storage temperature	Tstg	°C	-55 ~ + 110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure Vcc (high) ≥ GND (low) and IOVcc (high) ≥ GND (low).
3. Make sure Vci (high) ≥ AGND (low).
4. Make sure DDVDH (high) ≥ AGND (low).
5. Make sure DDVDH (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ AGND (low).
7. Make sure AGND (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

Electrical Characteristics

DC Characteristics

Table 92 (Vcc = 2.4V ~ 3.6V, IOVcc = 1.65V ~ 3.6V, Ta = -40°C ~ 85°C) see Note 1

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
Input high-level voltage	V_{IH}	V	IOV_{CC} = 1.65V ~ 3.3 V	0.8 x IOV_{CC}	—	IOV_{CC}	2, 3
Input low-level voltage	V_{IL}	V	IOV_{CC} = 1.65V ~ 3.3 V	– 0.3	—	0.2 x IOV_{CC}	2, 3
Output high voltage (DB0-17 pins, FLM)	V_{OH}	V	IOV_{CC} = 1.65V ~ 3.3 V I_{OH} = -0.1mA	0.8 x IOVcc	—	—	2
Output low voltage (DB0-17 pins, FLM)	V_{OL}	V	IOV_{CC} = 1.65 ~ 3.3 V I_{OL} = 0.1mA	—	—	0.2 x IOVcc	2
I/O leak current	I_{Li}	µA	Vin = 0 ~ IOVcc	–1	—	1	4
Current consumption: (IOVcc-GND)+(Vcc-GND) Normal operation mode	I_{OP1}	µA	fosc = 218kHz (220 line drive), IOVcc=Vcc=RVcc=3.0V, Ta=25°C, RAM data: “0000”h	—	90	130	5, 6
Current consumption: (IOVcc-GND)+(Vcc-GND) 8-color mode, 26-line partial display	I_{OP2}	µA	fosc = 218kHz (24 line partial drive), IOVcc=Vcc=RVcc=3.0V, Ta=25°C, RAM data: “0000”h	—	80	—	5, 6
Current consumption: (IOVcc-GND)+(Vcc-GND) RAM access mode 1 normal operation mode (HWM= “0”)	I_{RAM1}	µA	tCYCW=250ns, IOVcc=2.40V, Vcc=RVcc= 2.4V, Ta=25°C, 80-8bit I/F, TRI=0, Consecutive RAM access during display	—	5	—	6
Current consumption: (IOVcc-GND)+(Vcc-GND) RAM access mode 2 high-speed write function (HWM= “1”)	I_{RAM2}	µA	tCYCW=250ns, IOVcc=2.40V, Vcc=RVcc= 2.4V, Ta=25°C, 80-8bit I/F, TRI=0, Consecutive RAM access during display	—	1.2	—	6
Current consumption: (IOVcc-GND)+(Vcc-GND) Standby mode	I_{ST}	µA	IOVcc=Vcc=RVcc=Vci=3.0V, Ta≤50°C	—	20	100	5
			IOVcc=Vcc=RVcc=Vci=3.0V, Ta>50°C	—	0.1	1.0	5
LCD power supply current (VCI-GND) 260k color display	I_{ci1}	mA	IOVcc=Vcc=RVcc=3.0V, Vci=3.0V fosc =218kHz (220 lines), fFLM=70Hz, Ta=25°C, RAM data:”0000”h, REV=0, SAP=100, AP=100, DC0=000, DC1=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 B/C=0, BT=001, VC=001, VRH=0011, VCM=10011, VDV=10000, CL=0 No load on the panel	—	0.7	1.2	5, 6

LCD power supply current (VCI-GND) 8-color mode	I_{ci2}	mA	IOVcc=Vcc=RVcc=3.0V, Vci=3.0V fosc =218kHz fFLM=40Hz, Ta=25°C, RAM data:"0000"h, REV=0, SAP=010, AP=010, DC0=001, DC1=011, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 B/C=0, BT=001, VC=001, VRH=0011, VCM=10011, VDV=01110, CL=1, PTG=10, ISC=0111 No load on the panel	—	0.2	—	5, 6
Output voltage dispersion	ΔVo	mV	—	—	5	—	7
Average output voltage variance	ΔV	mV	—	—	—	35	8

Step-up circuit Characteristics

Table 93

Item		Unit	Test Condition	Min	Typ	Max	Notes
Step-up output voltage	DDVDH	V	IOVcc=Vcc=RVcc=3.0V, Vci=3.0V fosc =218kHz, Ta=25°C, VC=001, AP=100, SAP=100, BT=000, DC0=001 C11=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=1[μF] / B Characteristics, No load on the panel, I_{load1} = -1[mA]	4.0	4.2	—	10
	VGH	V	IOVcc=Vcc=RVcc=3.0V, Vci=3.0V fosc =218kHz, Ta=25°C, VC=001, AP=100, SAP=100, BT=000, DC0=000, DC1=010 C11=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=1[μF] / B Characteristics, No load on the panel, I_{load1} = -100[mA]	12.8	13.3	—	10
	VGL	V	IOVcc=Vcc=RVcc=3.0V, Vci=3.0V fosc =218kHz, Ta=25°C, VC=001, AP=100,SAP=100, BT=000, DC0=000 DC1=010 C11=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=1[μF] / B Characteristics, No load on the panel, I_{load1} = +100[mA]	-10.5	-11.1	—	10
Input voltage	Vci	V		2.5	—	3.3	—

AC Characteristics

(Vcc=2.4V ~ 3.6V, IOVcc = 1.65V ~ 3.6V, Ta = – 40°C ~ +85°C*) * see Note 1

Table 94 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
RC oscillation clock	f_{OSC}	kHz	Rf = 260 kΩ Vcc=3.0V	192	226	271	9

80-system Bus Interface Timing Characteristics (18/16-bit I/F)

Table 95 Normal write operation (HWM= "0"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 98	120	—	—
	Read	t_{CYCR}	ns	Figure 98	400	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 98	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 98	200	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 98	50	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 98	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 98	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 98	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 98	2	—	—
Write data setup time		t_{DSW}	ns	Figure 98	25	—	—
Write data hold time		t_{H}	ns	Figure 98	5	—	—
Read data delay time		t_{DDR}	ns	Figure 98	—	—	150
Read data hold time		t_{DHR}	ns	Figure 98	5	—	—

Table 96 High-Speed Write function (HWM= "1"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 98	80	—	—
	Read	t_{CYCR}	ns	Figure 98	400	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 98	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 98	200	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 98	50	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 98	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 98	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 98	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 98	2	—	—
Write data setup time		t_{DSW}	ns	Figure 98	25	—	—
Write data hold time		t_{H}	ns	Figure 98	5	—	—
Read data delay time		t_{DDR}	ns	Figure 98	—	—	150
Read data hold time		t_{DHR}	ns	Figure 98	5	—	—

80-system Bus Interface Timing Characteristics (9/8-bit I/F)

Table 97 Normal/High-speed Write function (HWM= "0/1"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 98	70	—	—
	Read	t_{CYCR}	ns	Figure 98	400	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 98	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 98	200	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 98	30	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 98	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 98	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 98	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 98	2	—	—
Write data setup time		t_{DSW}	ns	Figure 98	25	—	—
Write data hold time		t_{H}	ns	Figure 98	5	—	—
Read data delay time		t_{DDR}	ns	Figure 98	—	—	150
Read data hold time		t_{DHR}	ns	Figure 98	5	—	—

Serial interface Timing Characteristics

Table 98 IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	Figure 99	100	-	20,000
	Read (transmitted)	t_{SCYC}	ns	Figure 99	350	-	20,000
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 99	40	-	-
	Read (transmitted)	t_{SCH}	ns	Figure 99	150	-	-
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 99	40	-	-
	Read (transmitted)	t_{SCL}	ns	Figure 99	150	-	-
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure 99	-	-	20
Chip select setup time		t_{CSU}	ns	Figure 99	20	-	-
Chip select hold time		t_{CH}	ns	Figure 99	60	-	-
Serial input data setup time		t_{SISU}	ns	Figure 99	30	-	-
Serial input data hold time		t_{SIH}	ns	Figure 99	30	-	-
Serial output data delay time		t_{SOD}	ns	Figure 99	-	-	130
Serial output data hold time		t_{SOH}	ns	Figure 99	5	-	-

Reset Timing Characteristics

Table 99 (IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 100	1	—	—
Reset rise time	t_{rRES}	µs	Figure 100	—	—	10

RGB Interface timing characteristics

Table 100 18/16-bit I/F, High-speed Write function (HWM= "1"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 101	0	—	1
ENABLE setup time	tENS	ns	Figure 101	10	—	—
ENABLE hold time	tENH	ns	Figure 101	20	—	—
DOTCLK "Low" level pulse width	PW_{DL}	ns	Figure 101	40	—	—
DOTCLK "High" level pulse width	PW_{DH}	ns	Figure 101	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 101	100	—	—
Data setup time	tPDS	ns	Figure 101	10	—	—
Data hold time	tPDH	ns	Figure 101	40	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 101	—	—	25

Table 101 6-bit I/F, High-speed Write function (HWM= "1"), IOVcc = 1.65V ~ 3.6V, Vcc= 2.5V ~ 3.6V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 101	0	—	1
ENABLE setup time	tENS	ns	Figure 101	10	—	—
ENABLE hold time	tENH	ns	Figure 101	20	—	—
DOTCLK "Low" level pulse width	PW_{DL}	ns	Figure 101	30	—	—
DOTCLK "High" level pulse width	PW_{DH}	ns	Figure 101	30	—	—
DOTCLK cycle time	tCYCD	ns	Figure 101	80	—	—
Data setup time	tPDS	ns	Figure 101	10	—	—
Data hold time	tPDH	ns	Figure 101	30	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 101	—	—	25

LCD driver output Characteristics

Table 102

Item	Symbol	Unit	Test condition	Min	Typ	Max	Note
Driver output delay time	t_{dd1}	µs	Vcc=3.0V, DDVDH=5.5V, VREG1OUT=5.0V, fosc =226kHz, 220 line drive, Ta=25°C REV=0, SAP=010, AP=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 Load resistance R=10kΩ, Load capacitance C=20pF	—	25	—	11
	t_{dd2}	µs	Time to reach the target voltage level ±35mV from the Vcom polarity inversion timing Transition from the same grayscale level at all source pins	—	15	—	11

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.

2. The following figures illustrate the configurations of input, I/O, and output pins.

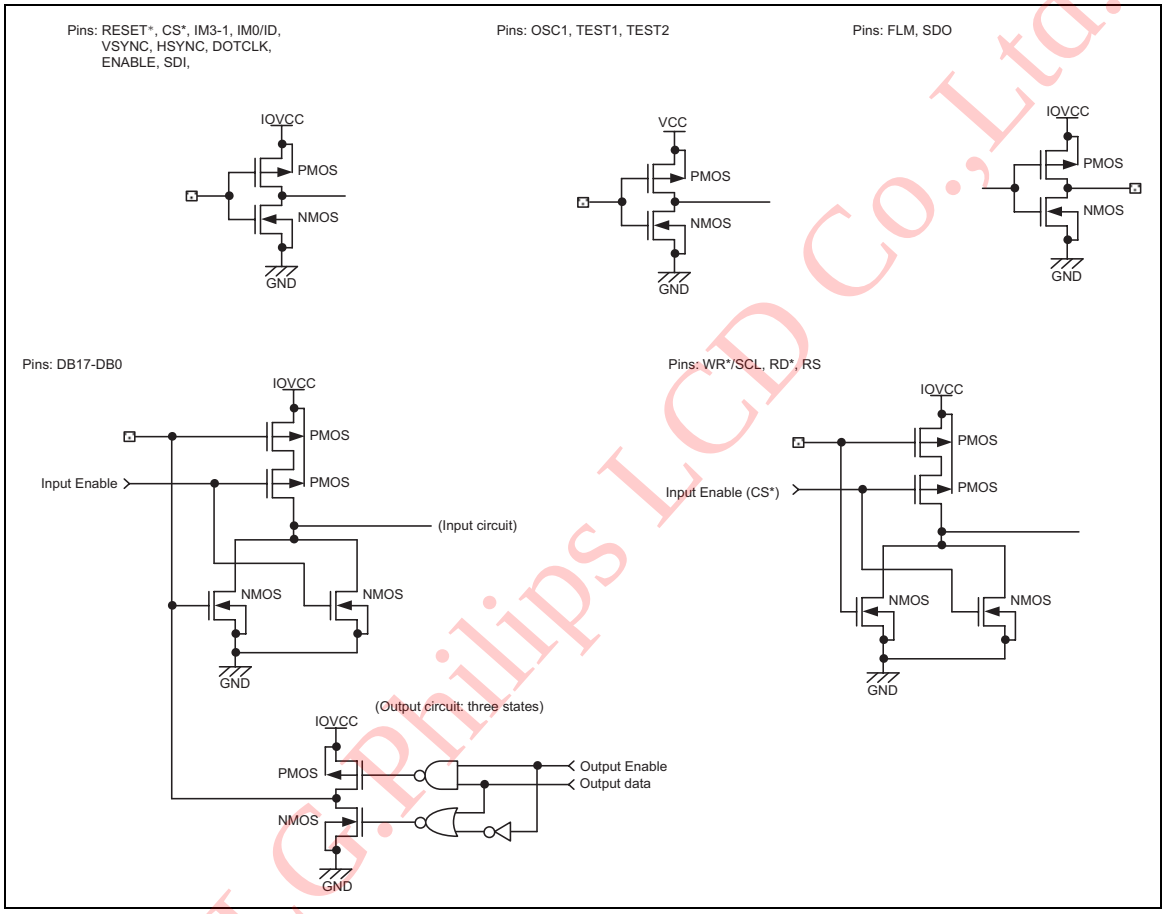


Figure 93

3. The TEST1, TEST2 pins must be grounded (GND). The IM3/2/1 and IM0/ID pins must be fixed at either IOVcc or GND.

4. This excludes the current in the output-drive MOS.

5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CS*pin is “High” or “Low” while not accessing via interface pins.

6. The relationship between voltages and the current consumption is as follows.

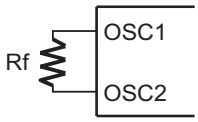
T.B.D.

Figure 94

7. The output voltage deviation is the difference in the voltages from adjacent source pins for the same display data. This value is shown just for reference.

8. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display data.

9. This applies to internal oscillators when using external oscillation resistor Rf.



Oscillation frequency depends on the capacitances OSC1 and OSC2.
Make the wiring between OSC1 and OSC2 as short as possible.

Figure 95

Table 103 Oscillation Resistance and Frequency (Reference Data)

Oscillation Resistance (kΩ)	RC oscillation frequency fOSC(kHz)		
	Vcc=2.4V	Vcc=3.0V	Vcc=3.3V
110			
150			
180		T.B.D	
200			
240			
270			
300			
390			
430			

10. The wiring resistance when the R61503B is mounted on the glass substrate is not taken into consideration. No load is applied on pins except those for measurement. See the reference data “Load current characteristics (T.B.D.)”.

11. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.

T.B.D.

Figure 96

Test Circuits

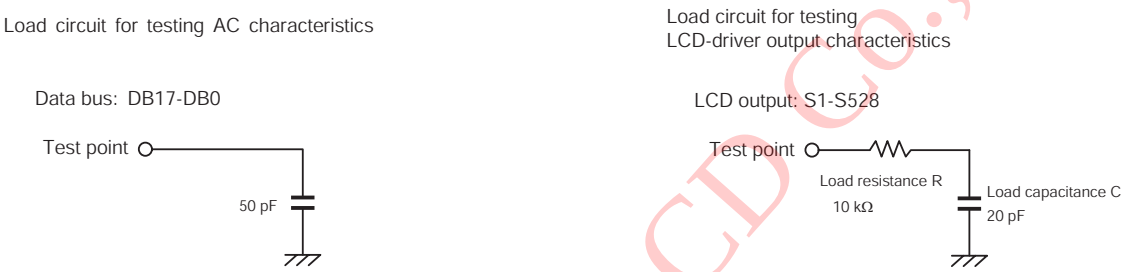


Figure 97

Timing Characteristics

80-system Bus Interface

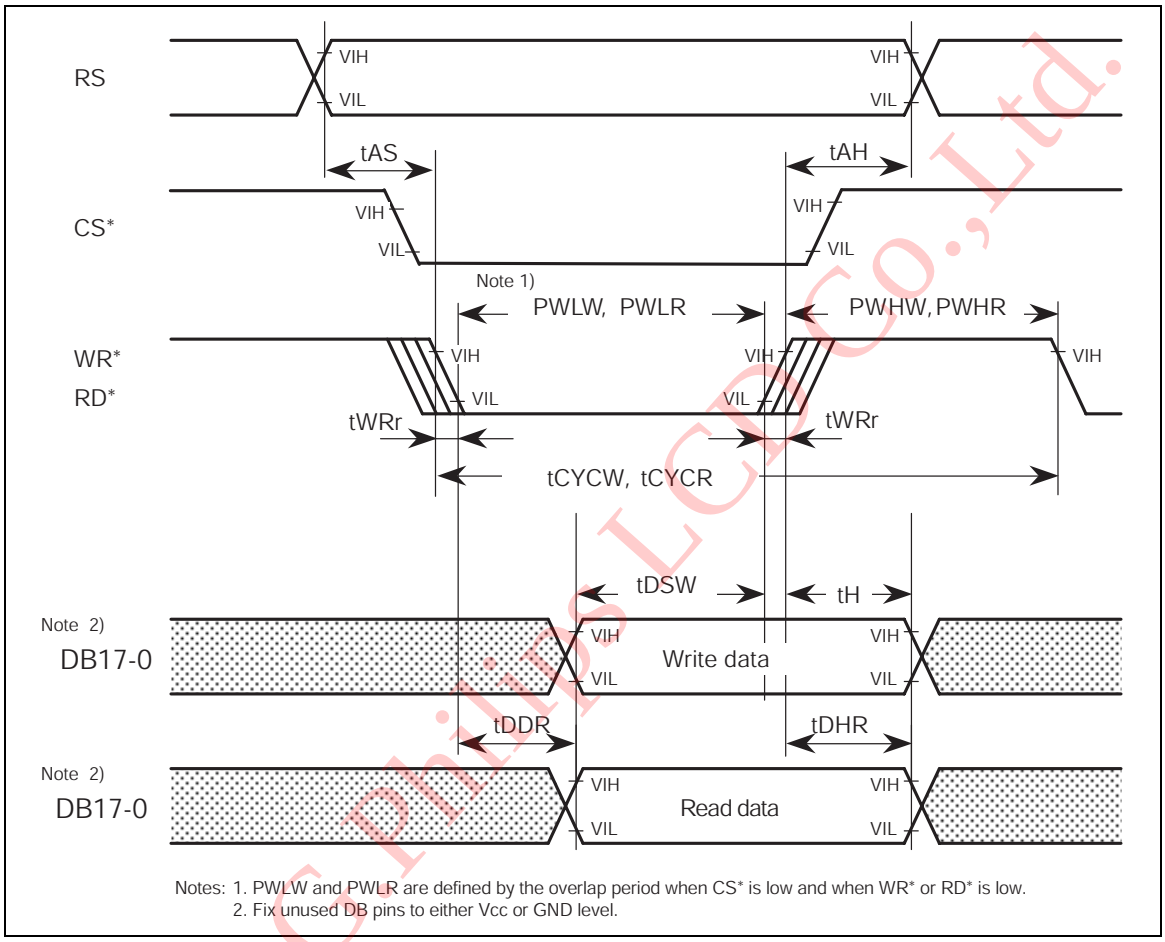


Figure 98

Clock synchronous serial interface

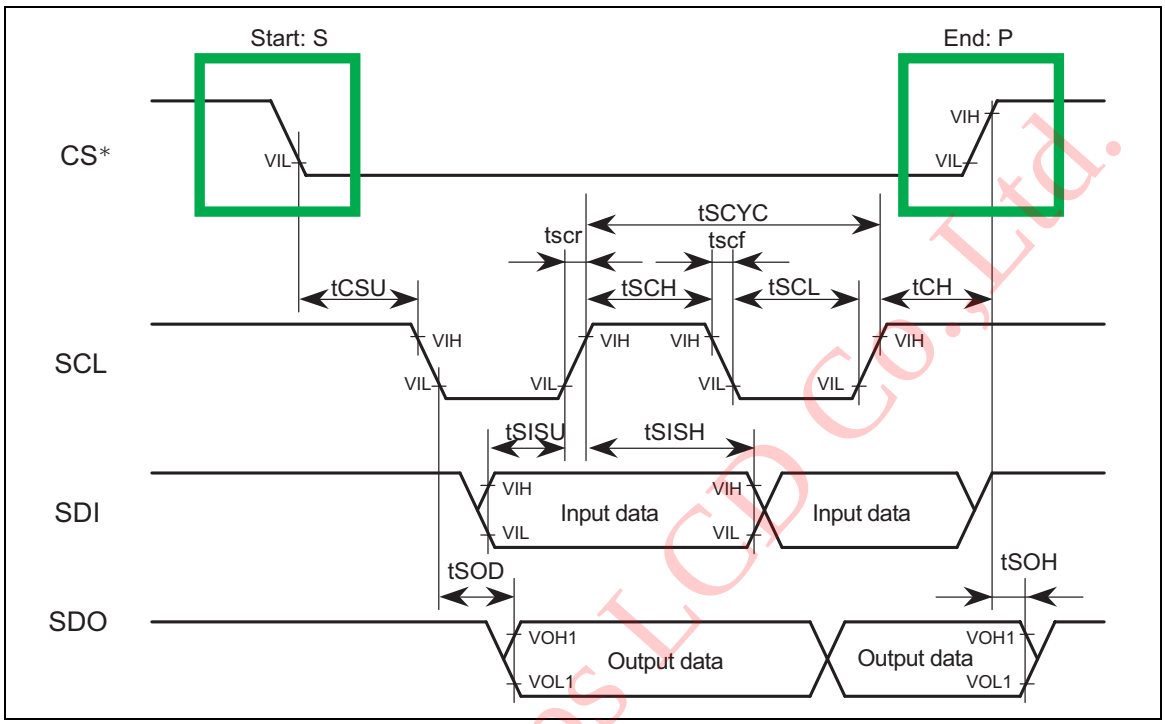


Figure 99

Reset operation

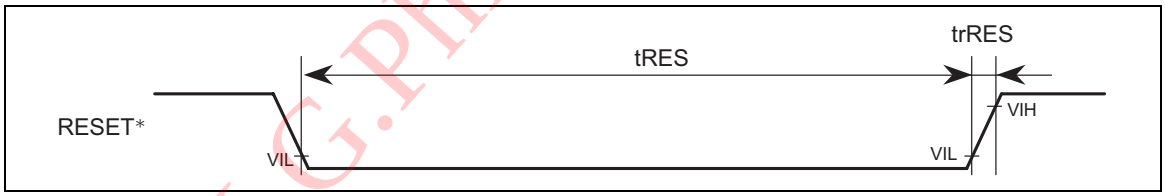


Figure 100

RGB interface

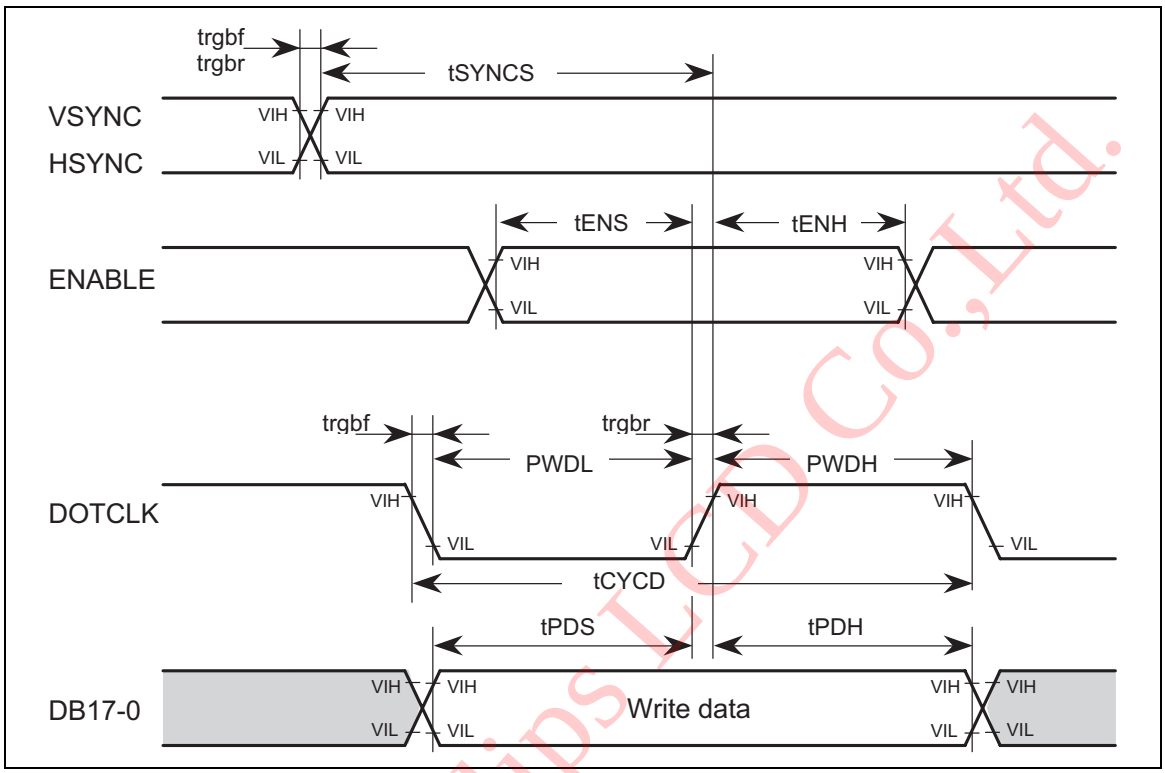


Figure 101

LCD driver output

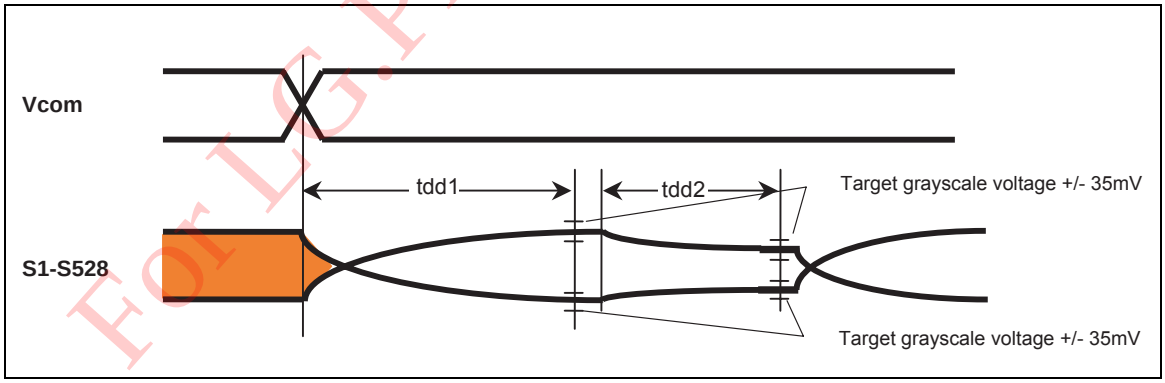


Figure 102

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Nov.09.2005	First issue		
0.11	Nov.25.2005	p.8 Add Vci1 x –2 (VGL), delete FLM (IOVcc) p.9 Add VCL in figure 1 p.13 Error correction (DDVDH). Add VCL p.43 Delete NW[5:0] p.62 Add VCOMG, Change Table 33 p.64 Add VCOMG p.87 Error correction from W to W/R in RA0 to RA4 registers p.88, 89 changes in Instruction List: Add VCOMG and delete NW[5:0] p.126, 149, 150 Delete EQ bits p.157 Error correction in Table 77 p.166 Changes in Figure 84 p.168 Changes in figure 86 (Add VCOMG, VCM setting). p.169 Changes in figure 87 p.170 Error correction in standby sequence		
0.11a	Dec.16.2005	Error corrections. RGB 6-bit interface via DB17-12 (error: DB5-0) Change Figure 5, Figure 8, Figure 49, Figure 50 accordingly.		
0.12	Jan.11.2006	p.31 Add (G1 ~ G220) to LC driver circuit (8) p.63 Table 36 Error correction in Note 1 p.65, 89 Add R14h register (DC5 bit) p.86 Error corrections in Table 56 p.140 Error correction (VEA = 9'h05B) p.144 Add Note 2 p.180 ~ 182 Change Vcc (= 2.5 ~) and delete RVcc		