Core Schematics and Simulation Report

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Contents

1 Top Level Schematics

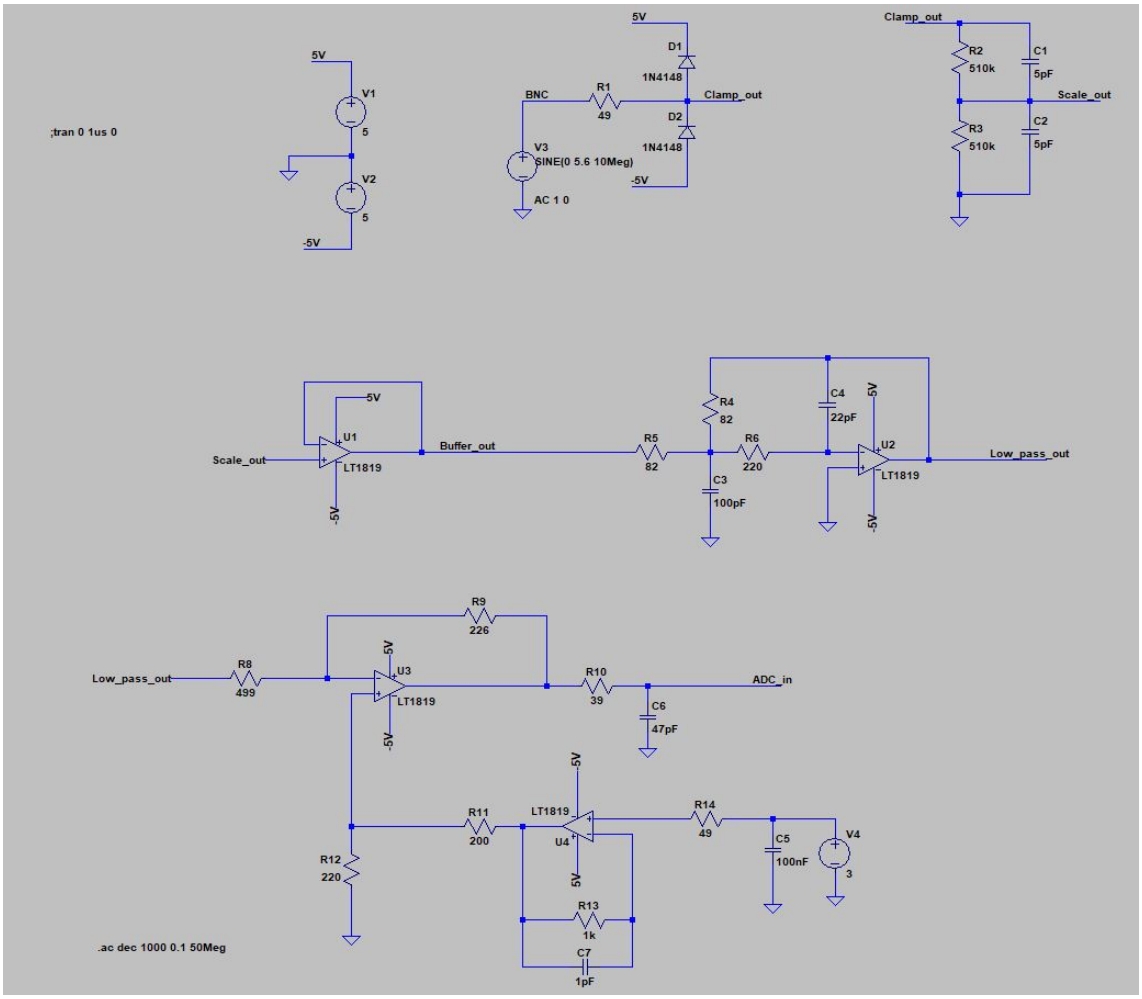

Figure 1: Top level front end LTspice schematics

The corresponding block diagram illustration of the design is as following:

2 Block Level Designs

2.1 Clamp

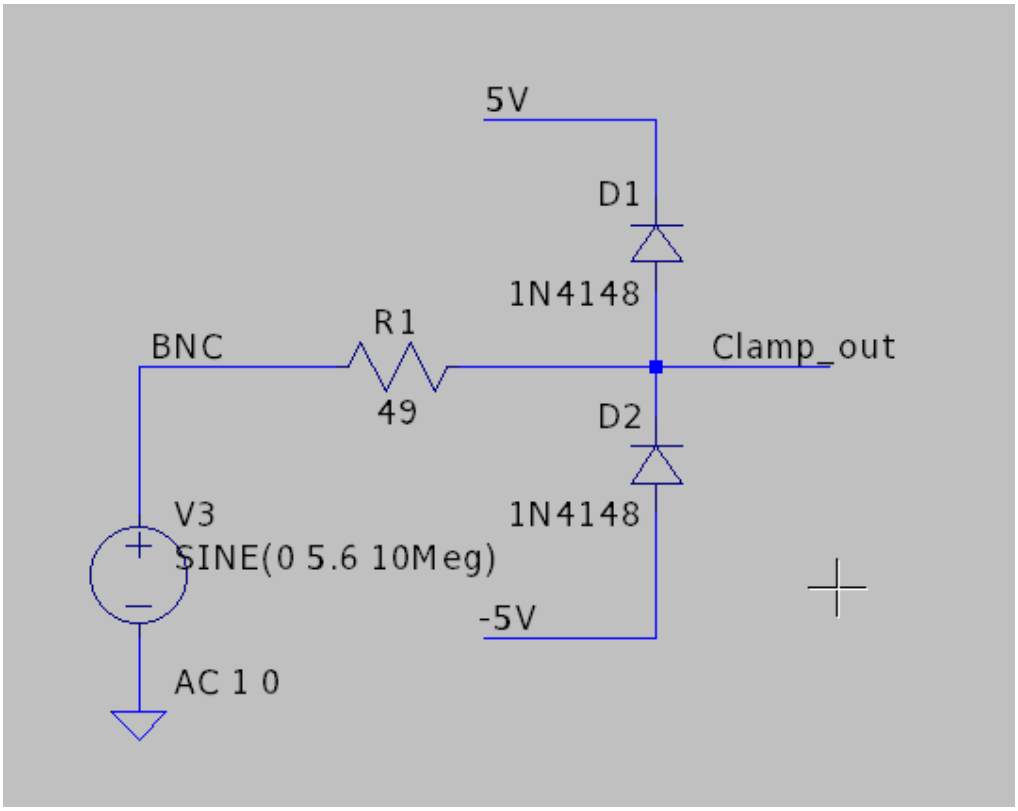

Figure 2: Clamp schematics

Two diodes with forward breakdown voltage of apporoximately 0.6 V are used to limit the input voltage, such that input beyond the range of [-5.6, 5.6] can be clamped. When the input voltage goes beyond this defined range, the upper or the lower diode goes into forward breakdown mode. A small resistor is added to prevent large current through the diodes and potentially damaging the diode.

2.2 Scaling Networks

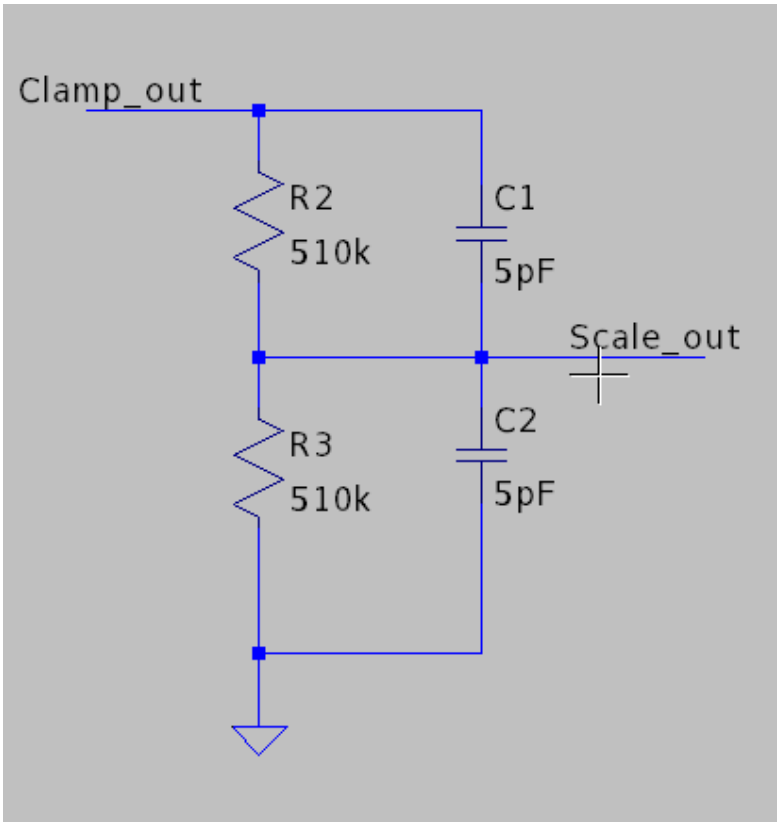

Figure 3: Scaling networks schematics

The reason for including a scaling network in the design is that, the specification requires a 1MΩ impedance at the BNC input in frequency range below 10kHz, while the buffer amplifier only provides up to 750kΩ for differential input. The impedance of the scaling network can be written as,

$$Z = R_1 || \frac{1}{sC_1} + R_2 || \frac{1}{sC_2} || R_{buffer}$$

By asserting $R_1C_1 = R_2C_2$ and ignoring R_{buffer}, we get following expression to guide the design.

$$Z = \frac{R_1 + R_2}{sR_1C_1 + 1}$$

Then we can see that, $R_1 + R_2$ approximates the impedance in the 3dB bandwidth, and the cutoff frequency approximates $\frac{1}{R_1C_1}$, where $s = 2\pi f$. This can give a base value for R_1, R_2, C_1 and C_2, but adjustments are needed to take into account the buffer op amp connected in parallel to the 2nd stage of the scaling networks.

2.3 Buffer

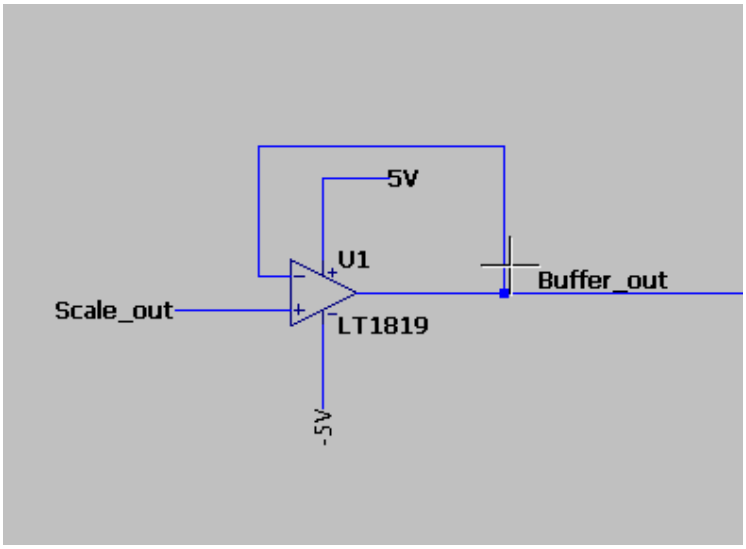

Figure 4: Buffer schematics

A buffer is needed to prevent the input signal at BNC from being affected by currents required by the remaining of front end circuit. Since a dedicated gain stage is also included in the front end, there is no need to provide gain at the buffer stage and it is designed as a simple voltage follower.

2.4 Multi Feedback Lowpass Filter

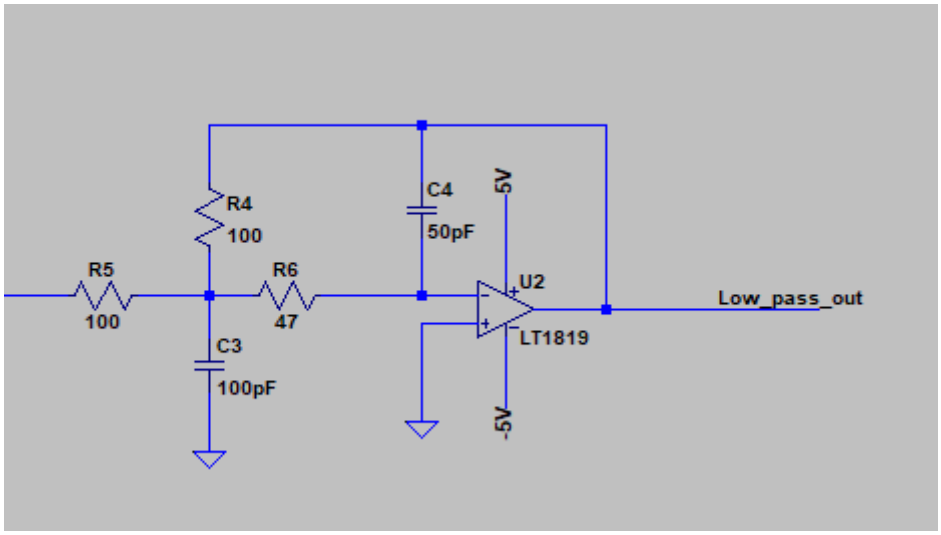

Figure 5: Multi Feedback Lowpass Filter schematics

A low pass filter/ anti-aliasing filter is necessary for any ADC to prevent aliasing. For a sampling frequency of 40MHz at the ADC, signal beyond 20MHz needs to be removed. A second stage filter is deemed sufficient to provide a sharp transient and is more economic due to the limited number of op-amps provided for the design. By comparison between Sallen-Key filter and multi feedback filter, the multi feedback filter appears to be more stable at high frequency and provides sharper roll-off(Sallen-key filter has a kick up at high frequency due to op-amp limitation). Butterworth filter type is chosen to mitigate passband ripple, which is a design specification.

2.5 Gain Stage & Level Shifter

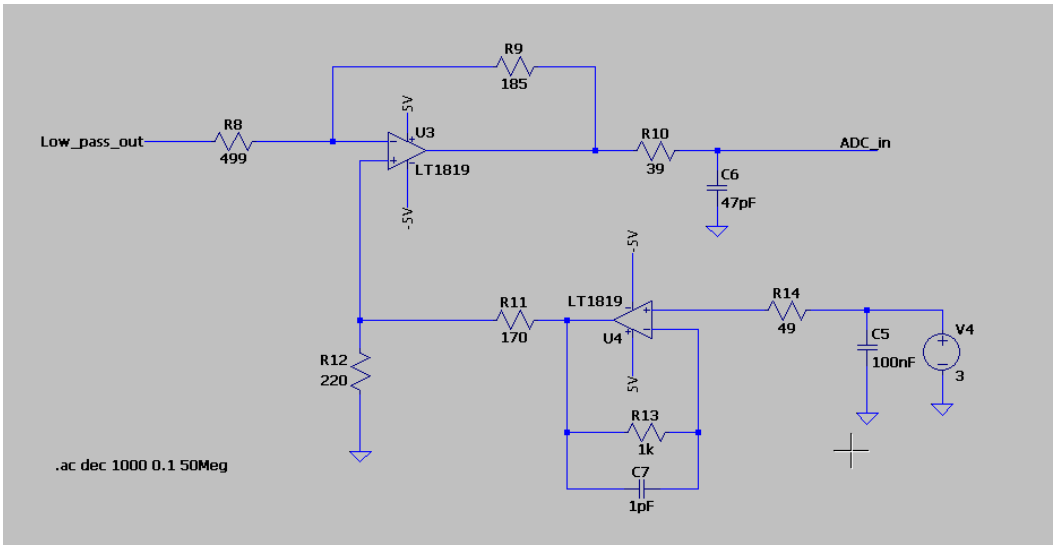

Figure 6: Gain Stage & Level Shifter schematics

The front end is designed to accept input voltage from the range of [-5.6V, 5.6V], but the ADC only has an input range of [1.5, 3.5]. Therefore, a gain stage and level shifter is required to map the BNC input to the ADC input. A DC coupled design is provided by the ADS830 ADC datasheet, the upper part is the gain stage and the lower part is the level shifter. The following relationship at the gain stage(U3) can be obtained to help find the value of R9 and R11.

KCL and virtual short,

$$\frac{V_{DC} - V_{in}}{R8} + \frac{V_{DC} - V_{out}}{R9} = 0$$

$$V_{out} = (1 + G)V_{DC} - GV_{in}$$

where $G = \frac{R9}{R8}$ and V_{DC} is provided by the level shifter. Note this is an inverting amplifer. Ripples were observed on the time-domain output waveform and a 1pF capacitor is added in the level shifter to smooth out the waveform. In the actual implementation, R9 and R11 will be replaced by variable resistor for flexible tuning.

3 Power Consumption

Block	Component	Power(W)	DC current bias(A)	Output port	DC voltage bias at output(V)	Block power(W)
	R1	4.65E-11	9.75E-07			
	D1	1.26E-11	-2.53E-09			
Clamp	D2	1.26E-08	2.53E-09	Clamp_out	4.78E-05	1.27E-08
	R2	4.84E-07	-9.75E-07			
Scaling Network	R3	4.85E-07	9.75E-07	Scale_out	4.97E-01	9.69E-07
Buffer	U1	9.74E-02		Buffer_out	4.97E-01	9.74E-02
	R5	2.47E-03	-4.97E-03			
	R4	2.47E-03	-4.97E-03			
	R6	1.88E-10	2.00E-06			
Low Pass Filter	U2	1.14E-01		Low_pass_out	-4.97E-01	1.19E-01
	R8	8.55E-03	4.14E-03			
	U3	8.68E-02				
	R9	3.87E-03	4.14E-03			
	R10	0.00E+00	0			
	R12	1.12E-02	-7.14E-03			
	R11	1.02E-02	7.13E-03			
	U4	8.73E-02				
	R13	2.89E-12	-1.70E-06			
Gain & Level Shifter	R14	1.41E-10	1.70E-06	ADC_in	2.5041	2.08E-01
					Total power(W)	0.424231682

4 Design Specifications Validation

4.1 Response at ADC input

Figure 7: Frequency and phase response at the ADC input

The designed circuit achieves a 3dB cut-off frequency at around 18.3MHz, this is smaller than the required 20MHz from design specification. However, because the transition from passband to stopband is not instantaneous, having a smaller bandwidth allows a more thorough removal of unwanted frequency component, thus achieves better anti-aliasing performance. No ripple is observed due to the choice of Butterworth filter type. The drop in the passband from 10kHz to 10MHz is around -1dB, still meeting the tolerance for ripple or fluctuation in the passband.

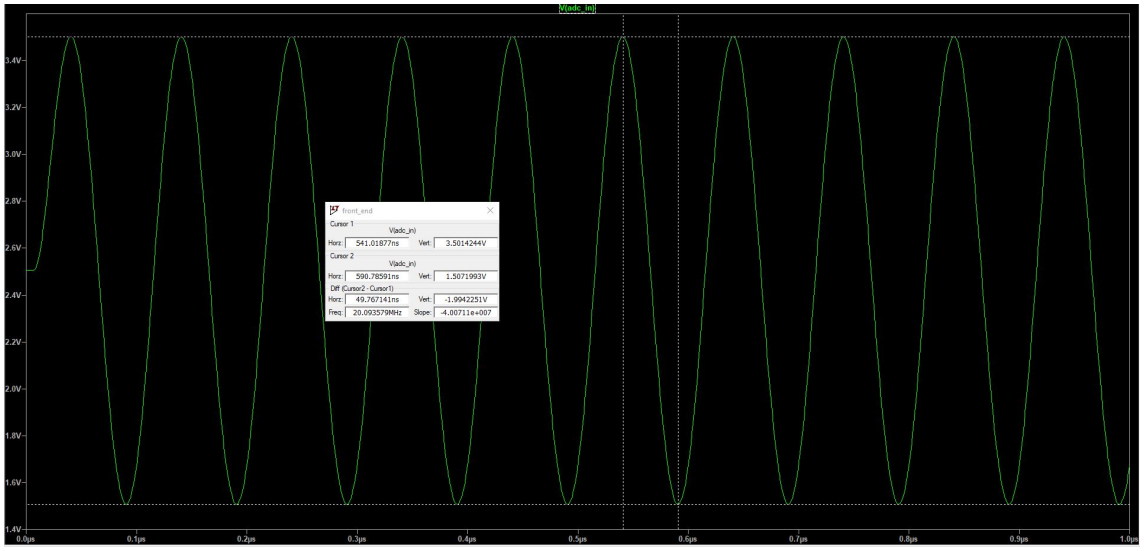

Figure 8: Time response at the ADC input with 10MHz 5.6V amplitude input signal

The maximum BNC input amplitude is mapped to the maximum input range of the ADC input, the specification is met.

4.2 Response at BNC Input

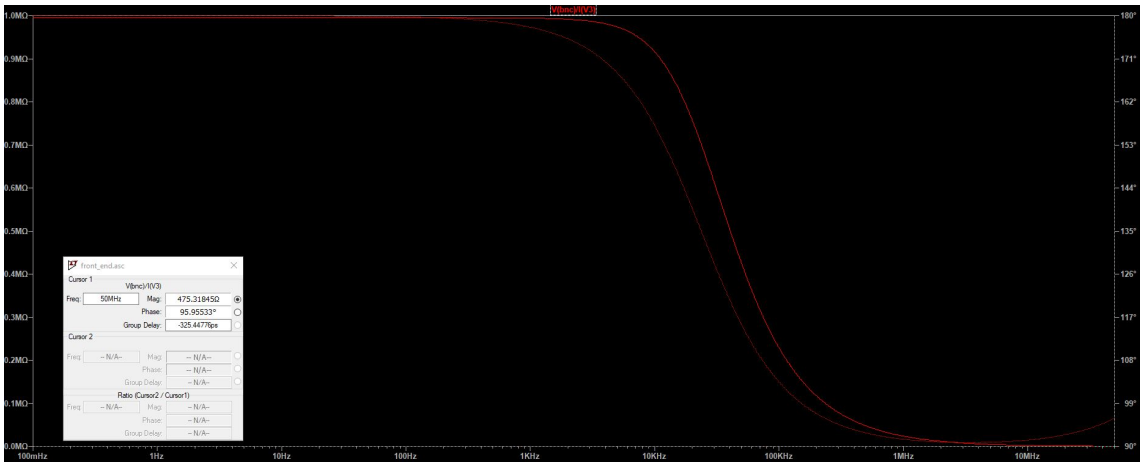

Figure 9: Impedance vs. frequency plot seen at BNC

The input signal at BNC sees an impedance close to 1MΩ from 0 to 10kHz and the minimum impedance across the frequency range of 30MHz is 475 Ω. The specification is met.

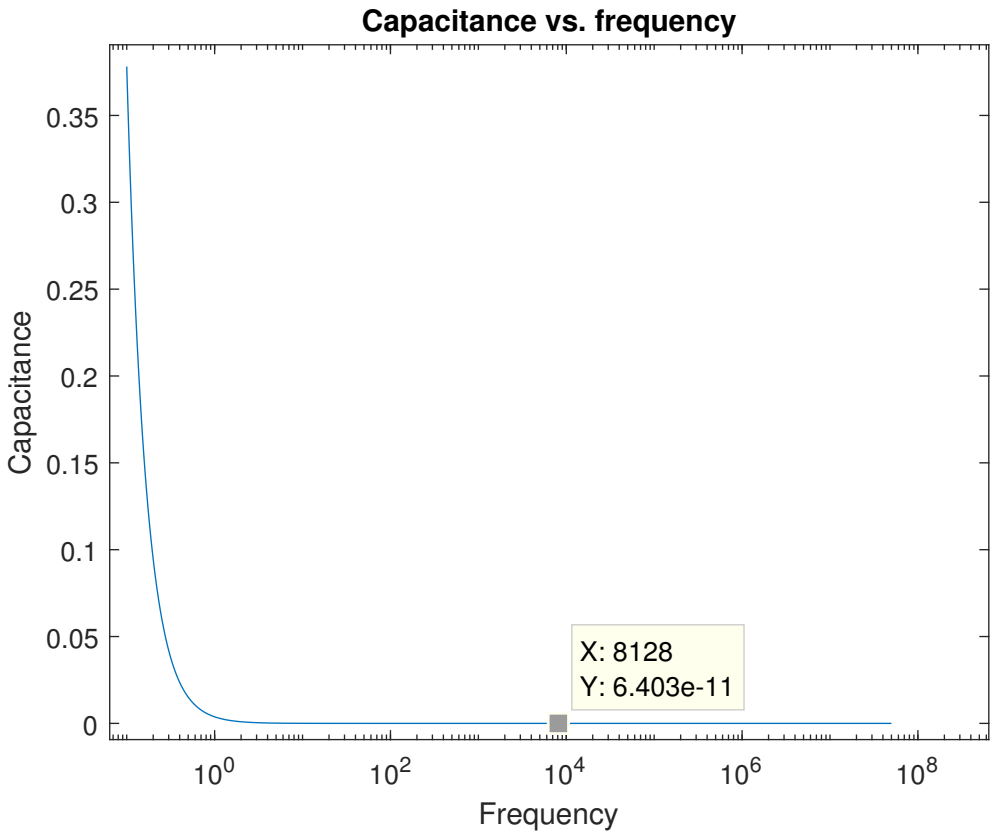

Figure 10: Capacitance vs. frequency plot seen at BNC

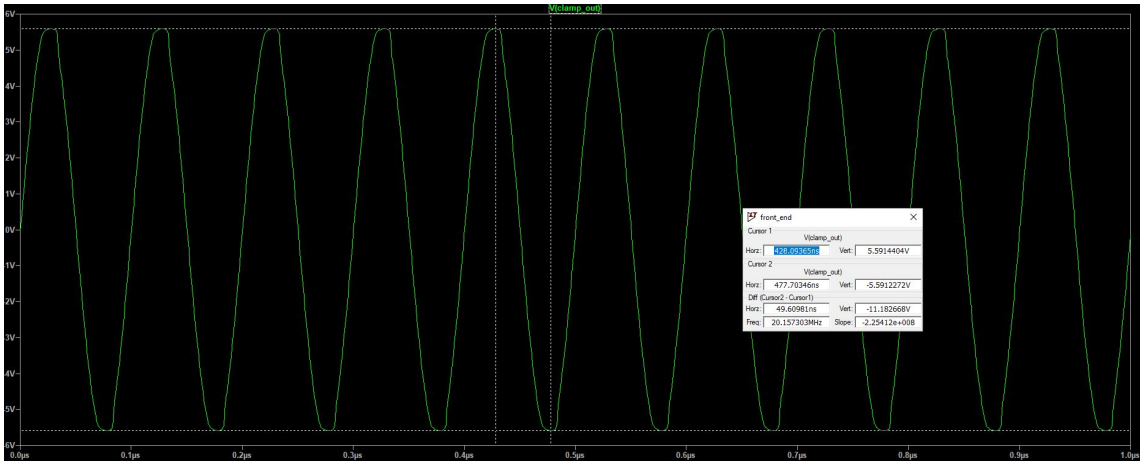

Figure 11: Time response of a 5.8V amplitude sine wave input after clamp

It can be seen that the clamp successfully clamping the input at ± 5.6, the specification is met.

4.3 Response after Buffer

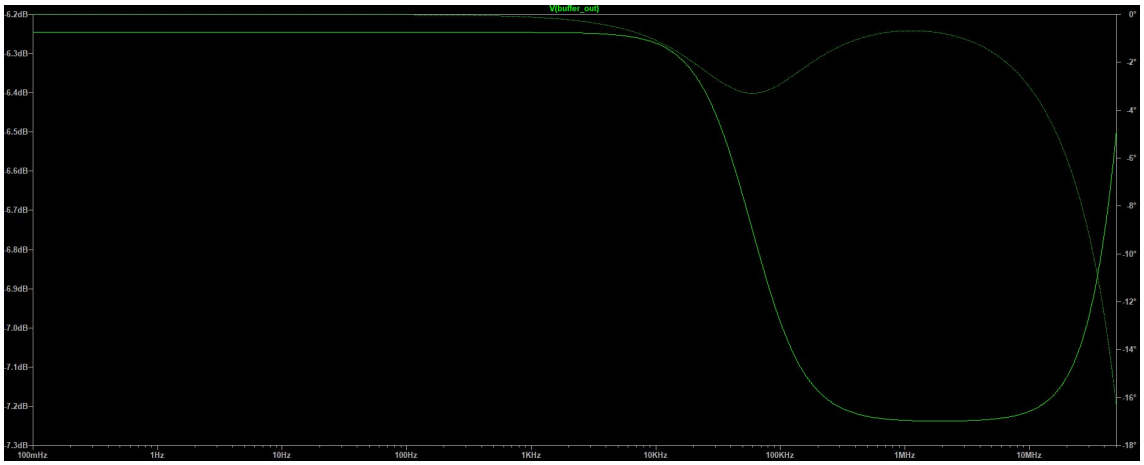

Figure 12: Frequency response after buffer stage

5 Summary

To summarize, the designed front end fully meets the design specification.
At BNC input, it is able to limit the input signal to ±5.6 V. It has an input impedance close to 1MΩ at the frequency range from 0 to 10kHz and minimum impedance of 475 Ω before 50MHz. It has an equivalent capacitance smaller than 60pF. The front end is DC coupled.
The anti-aliasing filter has a cut-off frequency of 18.3MHz, which is close to the specified 20MHz while leaving enough transition region. In passband, the filter has fluctuation less than 2dB due to the choice of Butterworth filter type.
At ADC input, a 10MHz ±5.6 V sine input is mapped to the full [1.5V,3.5V] range, fully utilizing the ADC input range.