RMIT UNIVERSITY

SCHOOL OF ENGINEERING

EEET2162/2035 – ADVANCED DIGITAL DESIGN 1 / DESIGN WITH HARDWARE DESCRIPTION LANGUAGES

MAJOR PROJECT

TOPIC LIST - 2018

1 AIMS

(i) To design, simulate, implement and test a digital circuit using the Quartus Prime toolchain.

(ii) To demonstrate the workflow when using the Verilog HDL to construct a design for a physical Field Programmable Gate Array (FPGA) target.

(iii) To develop a hierarchical design where an emphasis is placed on the development of small sub-modules which can be replicated to form a complete system.

(iv) To develop a large-scale Verilog HDL project that will require numerous sub-modules that are required to work together to achieve a common complex task.

2 INTRODUCTION

Students are expected to work in pairs and submit a combined report which will be assessed by the course coordinator and laboratory demonstrator. The projects will run for four weeks (weeks 8, 9, 10, 11), however the submissions and demonstration will occur at the end of week 12. Note that the aim will be to demonstrate the projects in week 12, however depending on student progress this may be moved to the week 13 at the discretion of the course coordinator.

The aim of the projects is to allow groups of students to build relatively complex designs in Verilog HDL that can be deployed on the DE-10 Nano Development Platform. All work must be original and plagiarism will be taken very seriously. The projects are expected to require approximately 36 hours per student to be completed successfully.

The topics have also been devised to allow students with varying skill levels to select a project that is suitable for their knowledge. As the semester is not yet complete, not all relevant material has been presented, however all students should have enough knowledge to begin working on the actual topic as of week 8. More details will be presented during the remainder of the lecture series.

The topics and outcomes presented in Section 3.0 are non-negotiable and students must select from the provided list unless a prior arrangement has been made with the course coordinator. Furthermore, students are required to inform their laboratory demonstrator as to which project they have selected.

Please note that more details will be added to this document as the project progresses and the assessment schedule is further developed. Furthermore, where possible the designs should be constructed from the 'fundamental units'. As example, where possible a full-adder should be built (as demonstrated in Lecture 7) rather than the "+1'b1" code segment be utilised as this would allow the design to be further developed into an Application Specific Integrated Circuit (ASIC).

3 TOPIC LIST 2018

a) HDMI processing and overlay (on-screen display) using the Cyclone V

Difficulty Level: Distinction.

The DE-10 Nano Development Platform contains an Analog Devices ADV7513 HDMI Transmitter. This particular device is connected to the FPGA using a 24-bit wide bus as well as an array of control signals. The aim of this project is to utilise both the FPGA and the ADV7513 to produce an on-screen display.

As an example, an image can be loaded into the onboard RAM (DDR3 RAM) and then displayed over the HDMI interface. Once that particular image has been loaded an onscreen overlay should present some user-configurable text over the image. Whilst a static image is acceptable, higher marks will be awarded to students who can display a moving image loaded from one of the other interfaces available on the development platform.

The ADV7513 also contains a series of configuration registers which will need to be made accessible over an interface such as I2C.

b) QSYS (System Integrator) implementation of an SPI communication interface

Difficulty Level: High Distinction.

One issue with the DE-10 Nano Development Platform is that it is quite difficult to interface with other standardised interfaces such as SPI or I2C. This is due to the fact that the FPGA needs to be configured with a block that contains the required functionality. In this project, students will need to develop a configurable width (minimum 1-bit, maximum 32-bits) SPI interface that can be used to transmit data / receive data. A maximum serial clock of 25MHz is required.

It is suggested that the interface is modelled on a standard ARM processor such as the STM32F4. Note that IP Blocks (with the exception of a PLL) are not permitted in this project. The system is also required to interface with the Hard Processor System (HPS) embedded in the Cyclone V. Additional material will be made available that discusses the software drivers required to communicate with an Avalon Memory Mapped Slave via QSYS.

At a minimum, the developed SPI peripheral should be able to have the clock phase and polarity configured, the number of bits transmitted / received configurable and have the ability to act as a master or slave device.

c) Audio signal capture and processing using the onboard ADC.

Difficulty Level: High Distinction.

As the need for real-time processing of multiple channels of audio data increases with more advanced musical instruments many manufacturers are beginning to utilise FPGAs to perform data processing. This is mainly due to the fact that FPGAs can have multiple parallel data paths

that can process each signal independently. If signals need to be combined, then a final stage can be utilised to synchronise the audio sources as well as perform and further processing such as equalisation.

The aim of this project will to be capture four channels of audio data using the onboard LTC2308 produced by Analog Devices. A Fast Fourier Transform (using an IP Block) is to then be used on the incoming data and an audio level spectrum analyser developed. The audio signal FFT is to be displayed over the HDMI interface.

Additional hardware will be required to interface the audio sources to the LTC header on the DE-10 Nano Development Platform. Please see the course coordinator for the additional resources if this project is selected.

d) PIC 12C508A Emulation.

Difficulty Level: Distinction.

This project requires students to develop a functionally equivalent micro-controller design that executes a reduced version of the instruction set of the PIC 12C508A. For the complete instruction set please see the Microchip website (www.microchip).

For simplicity, the design does not have to maintain the 4-state timing of the PIC processors but the implementation must maintain its single level pipelining characteristic. Students will need to investigate techniques to implement the program and data memories.

Omit the reset timer and power-on reset and watchdog circuits. A suggested partitioning is shown below:

Sub-task 1 = Memory and I/O section (includes program memory I-reg & RAM)

Sub-task 2 = All timing functions (includes Timer0 and watchdog – omit power-on reset)

Sub-task 3 = CPU functions.

e) Floating-point Unit Development

Difficulty Level: Credit.

In this project, students are required to develop a structural Floating-Point Unit (FPU) for use with a microprocessor. The processor needs to be capable of floating point addition and multiplication. The numbers are to be encoded into IEEE 754 single precision 32-bit format. The FPU should also be able to detect and flag the 'NaN' cases.

For the project demonstration, interface the FPU to the DE-10 RAM and perform the operation A*B+C on 1000 data triplets (A, B, C). Transfer the results back to the RAM, then upload to the PC for display. Verify the results by comparing them with another method (e.g., C program, spreadsheet etc.).

4 REPORT

a) The report / demonstration requirements of the major project will be released in the upcoming weeks. Please ensure that you read all announcements on the course Canvas page to ensure that you download the latest version of this document once the assessment schedule is released.