

Introduction

Electrical & Electronic Circuits and Elements

Embedded Systems & Embedded Programming

Fundamentals of Electronic Circuits (Field Effect Transistors)

Field Effect Transistor (FET)

- Has three terminals (Source, Gate and Drain)
- Can be used as switch, amplifire, resistor, capacitor and etc.
- > Is high efficiency and robust and can be used in most applications to replace **BJT**s
- ➤ Is a unipolar semiconductor device (charge carriers are electrons **or** holes)
- Unlike Bipolar Junction Transistor, it is controlled by an electric field (Gate Voltage)
- > Two basic classifications: the **N-channel FET** and the **P-channel FET**
- \rightarrow Has a very high input impedance (more than $10^9\Omega$)
 - Very sensitive to input voltage signal and can be easily damaged by static electricity
 - Lower power consumption and smaller than an equivalent BJT transistor
 - Very low gate leakage current (less than 10⁻⁹A)
- > Types of FETs: **JFET**, **MOSFET**, MESFET, FinFET and etc.





Fundamentals of Electronic Circuits (Field Effect Transistors)

Field Effect Transistor (FET)

- It has a high power gain and It can deliver more power than BJT
- > It is less noisy and has a higher frequency response in compare with BJT
- ➤ Has a very low "ON" resistance and have a high "OFF" resistance
- It can dissipate large amounts of power while switching
- It provides more thermal stability
- Applications
 - FETs are widely used in analog and digital circuits
 - Power converters and suppliers, RF power amplifiers and etc.
 - Integrated circuits like processors such as the **CMOS** range of digital logic chips
 - Sensors; like pressure and image sensors
 - Volatile and non-volatile memories

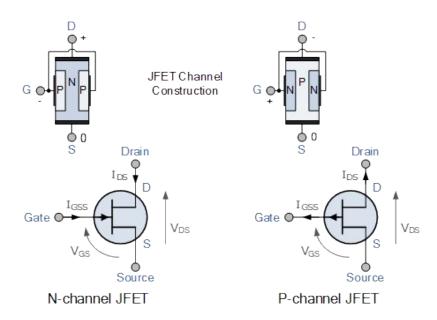


Field Effect Transistor Types & Technology





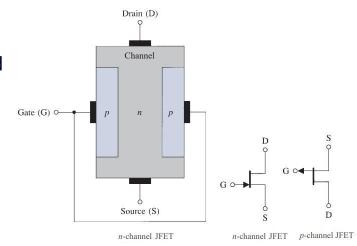
- Junction Field Effect Transistors (JFETs)
 - Two types: P-channel and N-channel
 - They are depletion type transistors only
 - \rightarrow They typically offer about 10⁹ Ω of input impedance
 - The gate-channel junctions are reverse-biased
 - Otherwise whole the current from source will flow to the gate and the device gets damaged
 - Can operate in four regions
 - Cut-off or pinch-off region
 - Ohmic or triode region
 - Saturation or active region
 - Breakdown region

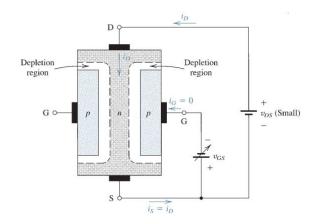






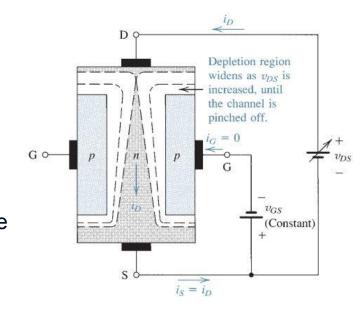
- ❖ JFETs are specified in term of loss and Vp; i.e Vgs(off)
 - ➤ Pinch-off voltage (**VP**) is the voltage at which the channel is closed
 - Drain to source saturation current (IDSS) when VGS = 0
 - ➤ **VP** for N-channel is negative and for P-channel is positive
- Biasing of an N-channel JFET
 - With V_{GS} = 0 and small V_{DS}
 - Maximum saturation current (IDSS) will flow through the channel from the drain to the source restricted only by the small depletion region around the junctions and RDS(on) is about 0.05 Ω
 - By decreasing the VGS, the width of the depletion region is increased which in turn reduces the conduction of the channel
 - When the V_GS ≤ V_P, the channel will be closed and no more current flows between the drain and the source (I_D = 0)







- Biasing of an N-channel JFET
 - ightharpoonup With $V_P \le V_{GS} \le 0$ and increasing the V_{DS} from Zero
 - The most-depleted portion of the depletion region is in between the gate and the drain, while the least-depleted area is between the gate and the source
 - The depleted portion of the depletion region between gate and drain increases and therefore the conduction of the channel reduces
 - When VDS ≥ VGS VP, then the channel gets saturated and
 - The drain current ID no longer increases with increasing of VDS
 - The drain current ID remains fairly constant
 - If VDS is continuously increased, the junctions are broken and the JFET may be destroyed



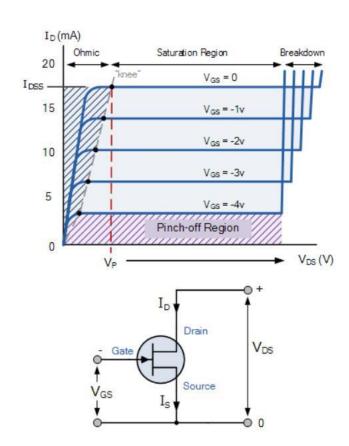


Characteristics of JFETS



Fundamentals of Electronic Circuits (N-channel JFET)

- Four different regions of operation for a JFET
 - Cut-off (VGS ≤ VP)
 - Where VGs is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum (ID = 0)
 - \triangleright Ohmic or triode ($V_P < V_{GS} \le 0$ and $V_{DS} \le V_{GS} V_P$)
 - The depletion layer of the channel is small and the JFET acts like a voltage controlled resistor
 - Saturation or active (V_P < V_Gs ≤ 0 and V_Ds > V_Gs − V_P)
 - It becomes a good conductor controlled by Vcs
 - VDs has little or no effect and the device is used as an amplifier
 - Breakdown
 - Vos is high enough to causes the channel to break down and pass uncontrolled maximum current



KVL: VDS = VDG + VGS, KCL: IG = 0, ID = IS



Fundamentals of Electronic Circuits (N-channel JFET)

❖ The drain-source current in ohmic region is

$$i_D = I_{DSS} \left[2 \left(1 - \frac{\mathbf{v}_{GS}}{V_P} \right) \left(\frac{\mathbf{v}_{DS}}{-V_P} \right) - \left(\frac{\mathbf{v}_{DS}}{V_P} \right)^2 \right]$$

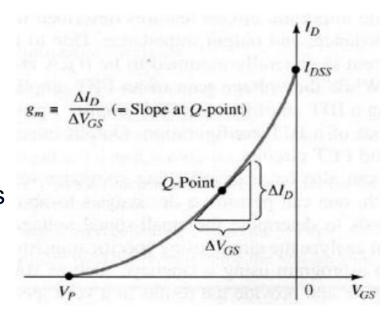
The drain-source current in saturation region is

$$i_D = I_{DSS} \left(1 - \frac{\mathbf{v}_{GS}}{V_P} \right)^2$$

Transconductance gain of the JFET in active mode is

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right) \left(1 - \frac{V_{GS}}{V_P}\right)$$

- Where \mathbf{g}_{m} is the ratio of change in drain current, $\Delta \mathbf{l} \mathbf{D}$, to the change in gate-source voltage, $\Delta \mathbf{V} \mathbf{c} \mathbf{s}$.
- \triangleright Its unit is 1/Ω (mho or Siemens)



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How FETs Function - The Learning Circuit



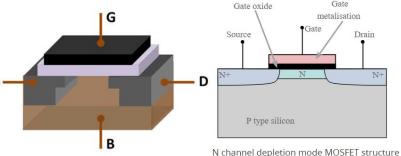
- Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
 - The gate is physically insulated from the channel by an oxide layer (SiO₂)
 - Voltage applied to the gate controls the conductivity of the channel
- Working of Transistors | MOSFET

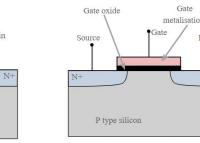
Enhancement

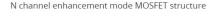
no bulk semi

Enhancement

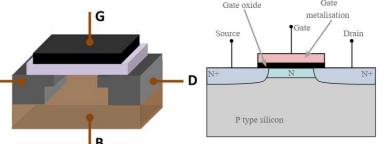
- As a result of the electric field induced capacitively across the insulating dielectric layer
- Both N-channel (NMOS) and P-channel (PMOS) variants are available
- Both enhancement and depletion types are available
- Typically offers more than $10^{14} \Omega$ of input impedance
- Is the most manufactured device in history
 - 1.3×10^{22} MOSFETs between 1960 and 2018
- Three terminals
 - Gate, Drain, Source
 - Bulk/Body is connected to source or has no effect (in no bulk E-MOSFET)







Depletion





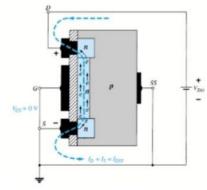
Depletion MOSFET

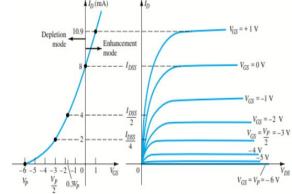
- it consists of a channel diffused between the drain to source terminal
- > It requires the Gate-Source voltage, (VGS) to switch the device "OFF"
- It is equivalent to a "Normally Closed" switch



Depletion Type MOSFET: What is it?

- > Its behaviour is almost like a JFET but because of the insulated gate
 - it is possible to bias its gate in either polarity, positive or negative
 - For example in a N-channel MOSFET
 - More +Vgs means more current
 - While more -Vgs means less current
- Operate within three different regions
 - Cut-off, Linear (Ohmic) and Saturation
- > Is less common than the enhancement mode types
- ➤ Like a JFET, it is specified in term of loss and VP

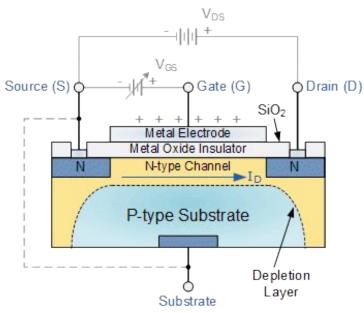




$$i_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$



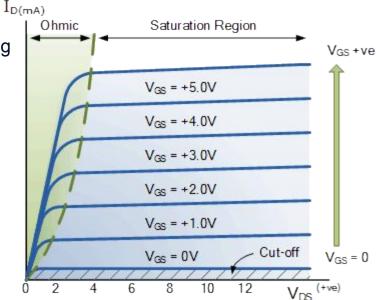
- Enhancement MOSFET (eMOSFET)
 - The conducting channel is lightly doped or even undoped
 - ➤ The device is normally "OFF" when VGS is 0V
 - > It requires a Gate-Source voltage to switch the device "ON"
 - ➤ It is equivalent to a "Normally Open" switch
 - For an n-channel eMOSFET
 - + Vgs turns it "ON", while a zero or Vgs turns it "OFF"
 - Increasing the + VGS will decrease the channel resistance
 - A drain current will only flow when VGs greater than the threshold voltage (Vтн)
 - It is an excellent electronics switch due to its
 - Infinitely high input impedance
 - Low "ON" and extremely high "OFF" output impedances
 - eMOSFETs are used in ICs to produce CMOS type Logic Gates and power switching circuits

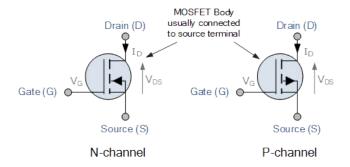


MOSFET Transistor Basics & Working Principle



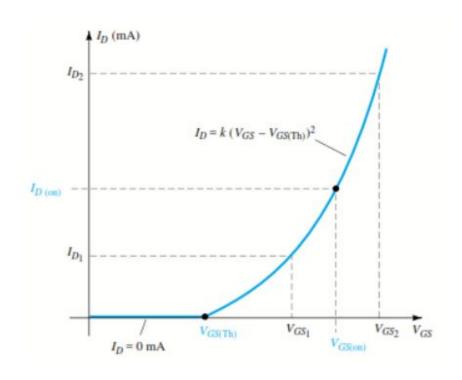
- ♣ An eMOSFET is specified in term of (Vth) and Kn
 - > Vth (threshold) is the minimum required VGS to make the device conducting
 - **K**_n is the conductance coefficient and it can be calculated form
 - ID(on) and VGS(on) form its datasheet
- eMOSFET operation modes
 - Cut-off Region (Vgs ≤ Vth):
 - It is "fully-OFF" thus, $I_D = 0$
 - It acts like an open switch regardless of the value of **V**_{DS}
 - Ohmic Region (Vgs > Vth and Vps ≤ Vgs Vth):
 - It acts like a voltage-controlled resistance
 - ➤ Saturation Region (Vgs > Vth and Vps > Vgs Vth):
 - It is "fully-ON" and the drain current is maximum
 - It acts like a closed switch







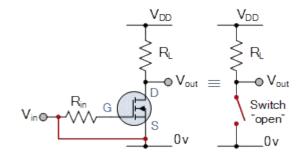
- The conductance coefficient is $k_n = \mu_n C_{ox} \frac{W}{L}$
 - > µn is the charge-carrier effective mobility, Cox is the gate oxide capacitance per unit area
 - > W is the gate width and L is the gate length
- The drain current in ohmic mode is
 - \rightarrow ID = Kn(VGS Vth 0.5VDS)VDS
- The drain current in saturation mode is
 - \rightarrow ID = 0.5 x Kn(VGS Vth)²
- The gain of an eMOSFET in saturation mode is
 - \rightarrow gm = 2×Kn×(VGS Vth)
 - MOSFETs and How to Use Them | AddOhms
 - Power Electronics MOSFET Power Losses



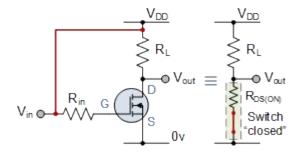


MOSFET as a switch

- > OFF State
 - VGS = 0V and VGS < VTH
 - MOSFET is "OFF" and ID = 0A
 - MOSFET operates as an "open switch"
 - Vout = Vds = Vdd == HIGH
- > ON State
 - Vgs = Vdd and Vgs > Vth
 - MOSFET is "ON" and ID = VDD / RL
 - VDS = 0V (ideal saturation) and channel resistance $RDS(on) < 0.1\Omega$
 - MOSFET operates as a low resistance "closed switch"
 - Vout = Vds \approx 0.2V due to Rds(on)



The MOSFET is in the cut-off mode



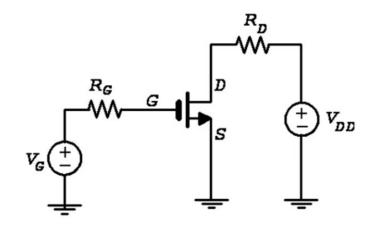
The MOSFET is in saturation mode



- Example: Calculate Vgs, Vps and Ip
- Known values
 - ightharpoonup V_{GG} = 1.5V, V_{DD} = 7V, V_{th} = 1V, K_n = 1.2mA/V² and R_D = 7 k Ω
- Answer
 - \rightarrow Ig = 0, Vgs = Vgg = Vg Vs = 1.5V
 - > V_{GS} > V_{th}, we assume that the MOSFET is in saturation mode
 - > I_D = 150 µA and V_{DS} = 5.95V
 - \triangleright V_{DS} > V_{GS} V_{th} => 5.95 > 1.5 1 \bigvee so the transistor is in the saturation mode





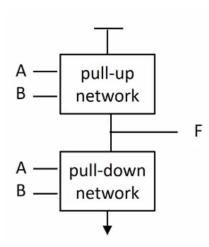




- CMOS (Complementary MOS)
 - Is a type of MOSFET fabrication process
 - Uses complementary and symmetrical pairs of NMOS and PMOS for logic function

Features

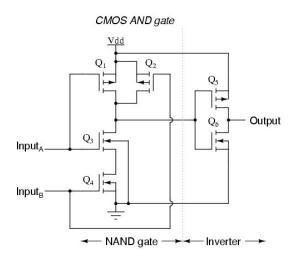
- Dissipates low power
 - At 1 MHz and 50 pF load, the power dissipation is typically 10 nW per gate
 - Power consumption increases with higher clock speeds
- Short propagation delays (around 25 ns)
- Good noise immunity (50% or 45% of the full logic)
 - NMH = NML = 3(VDD + 2Vth/3)/8
- ➤ Levels of the logic signal will be equal to VDD since the input impedance is so high.
- ➤ Voltage levels range from 0 to VDD
- ➤ A low level is between 0 and 1/3 VDD while a high level is between 2/3 VDD and VDD



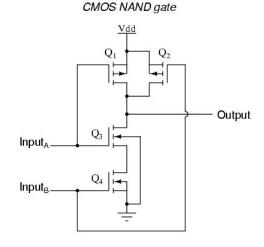
Pull-up: PMOS only Pull-down: NMOS only

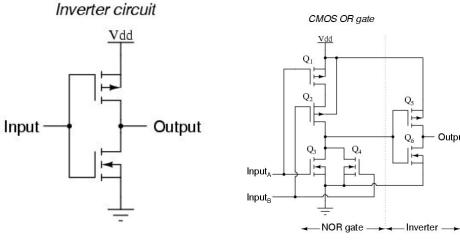


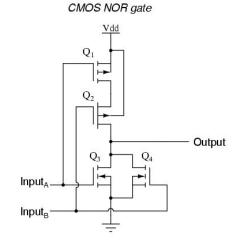
- **Basic Logic Gates**
- Useful links
 - **CMOS Gate Circuitry**
 - **CMOS Logic Gates**
 - **CMOS Transistors**
 - **CMOS Introduction**



Output









Fundamentals of Electronic Circuits

Some useful links

- ➤ MOSFET BJT or IGBT Brief comparison Basic components
- ➤ The FET (field effect transistor)
- How FETs Function The Learning Circuit
- > What is Field Effect Transistor FET JFET MOSFET Applications of MOSFET
- ➤ The MOSFET (part 1, part 2 and part 3)
- ➤ MOSFET
- ➤ Field Effect Transistor (FET)
- Depletion MOSFETs
- Understanding The FinFet Semiconductor Process
- Investing in FinFET Technology Leadership Presented by ARM
- Samsung Foundry's New Transistor Structure
- Using Power MOSFETS with Arduino

