

## Integrated Systems Architectures

### Lab 2

Design with TCE an Application Specific Instruction-set Processor (ASIP) for the Discrete Cosine Transform (DCT). Download the C code available on “Portale della didattica” and analyze it to implement an optimized ASIP.

**Step 1** Follow the tutorial steps to understand the tool feature and characteristics.

**Step 2** Design an optimized ASIP for the DCT, simulate and verify it. Synthesize the VHDL code for a 100 MHz target clock frequency. Verify the target clock frequency is met and collect area results.

**Optional** Find the maximum clock frequency achieved by your ASIP and complete the design flow with place and route for a target clock frequency of 100 MHz.