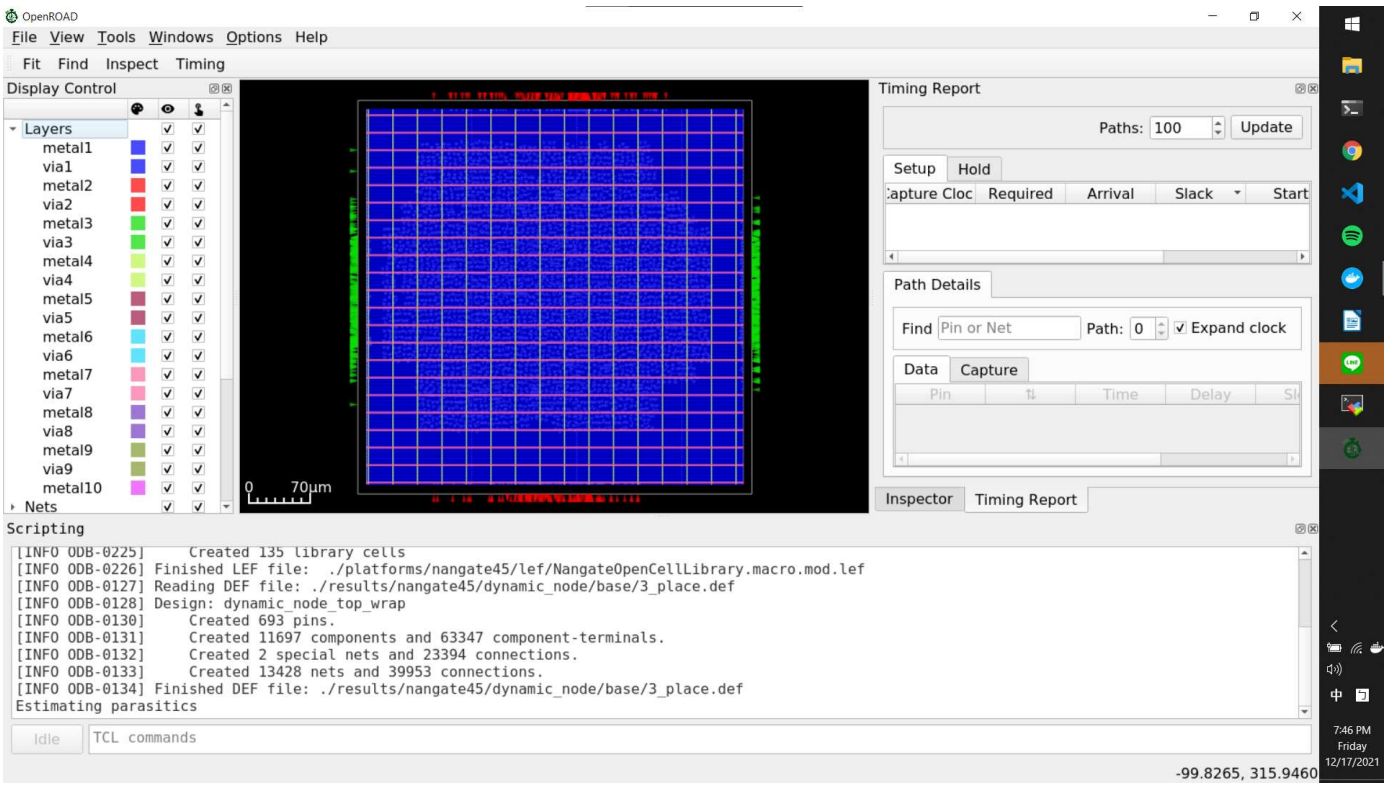
DDLab pj 11

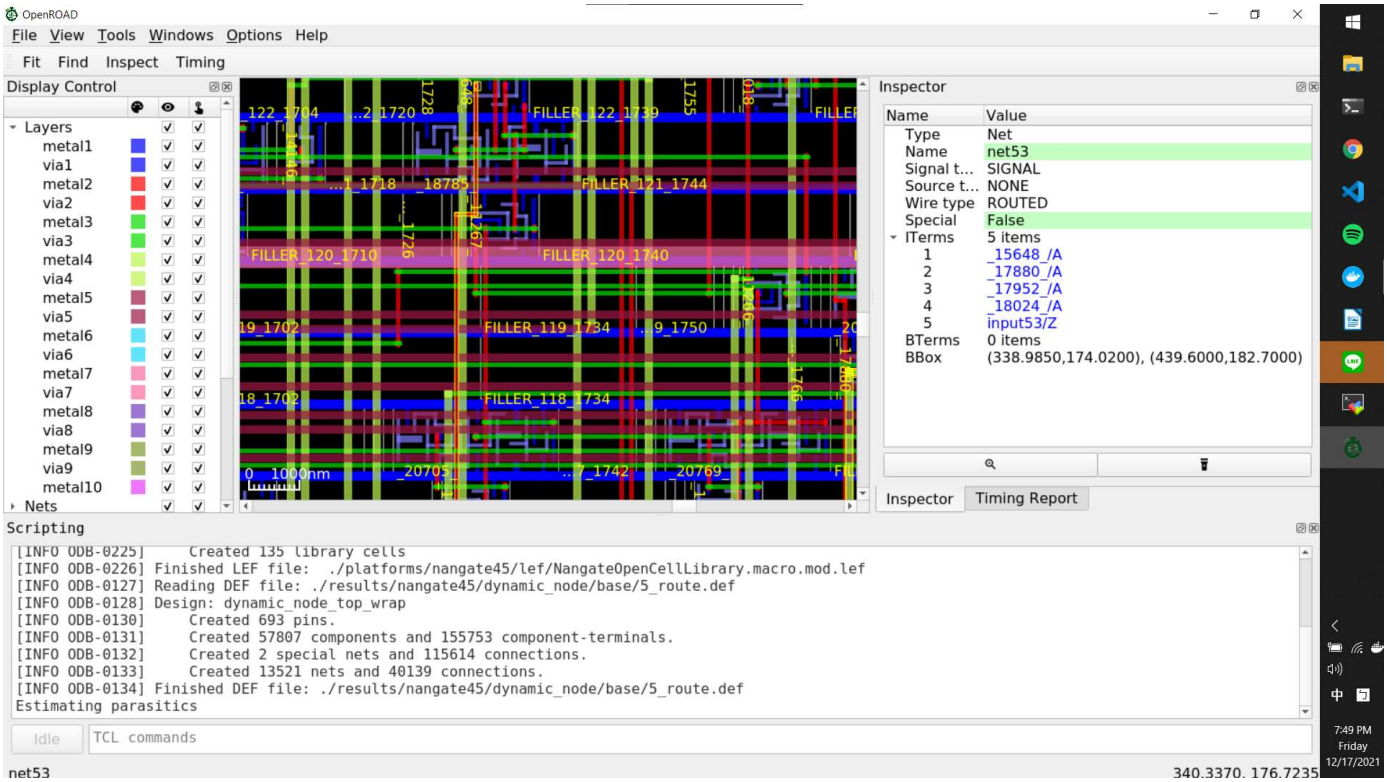
Several screenshots of the selected designs in various design stages

Design 1 - dynamic node

3_place

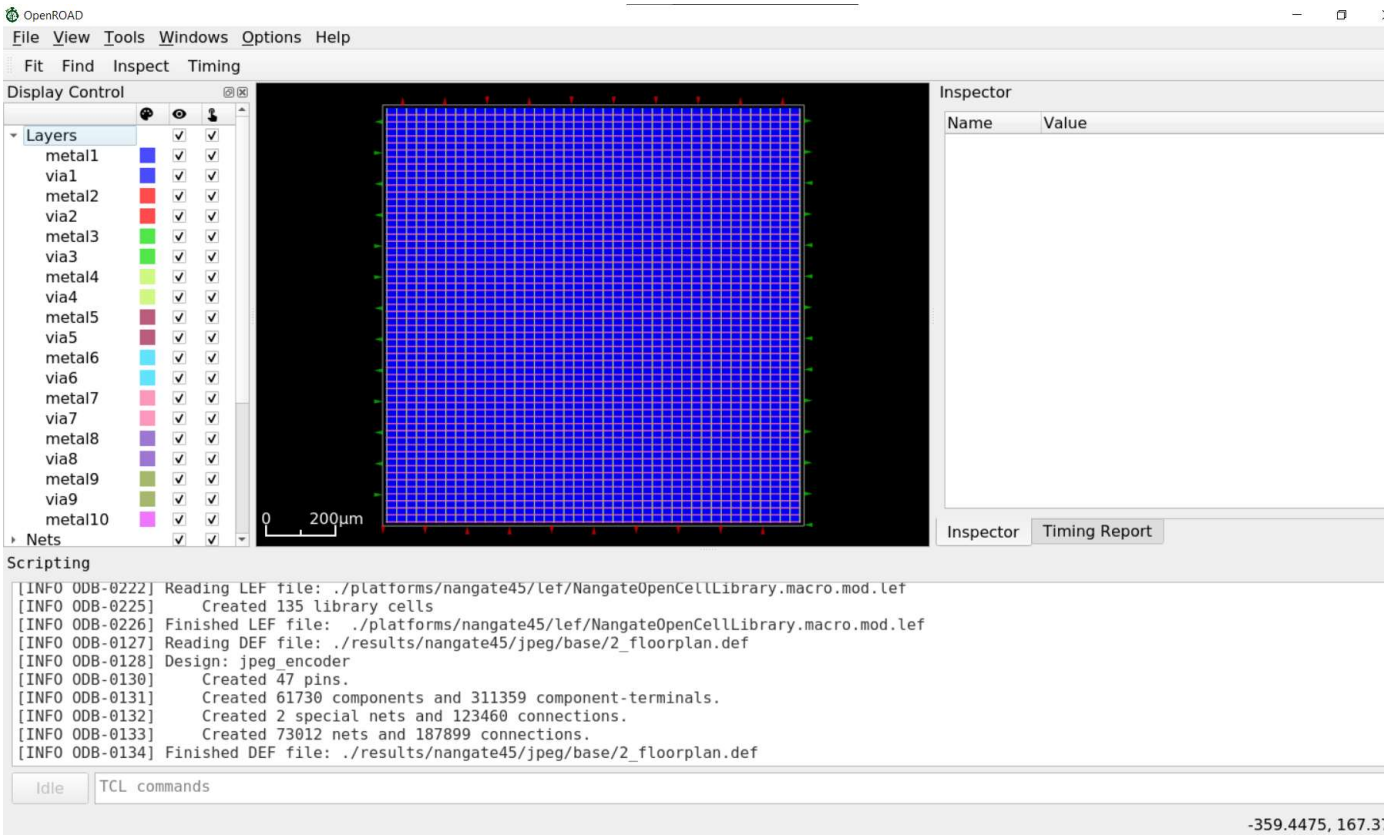


5_route

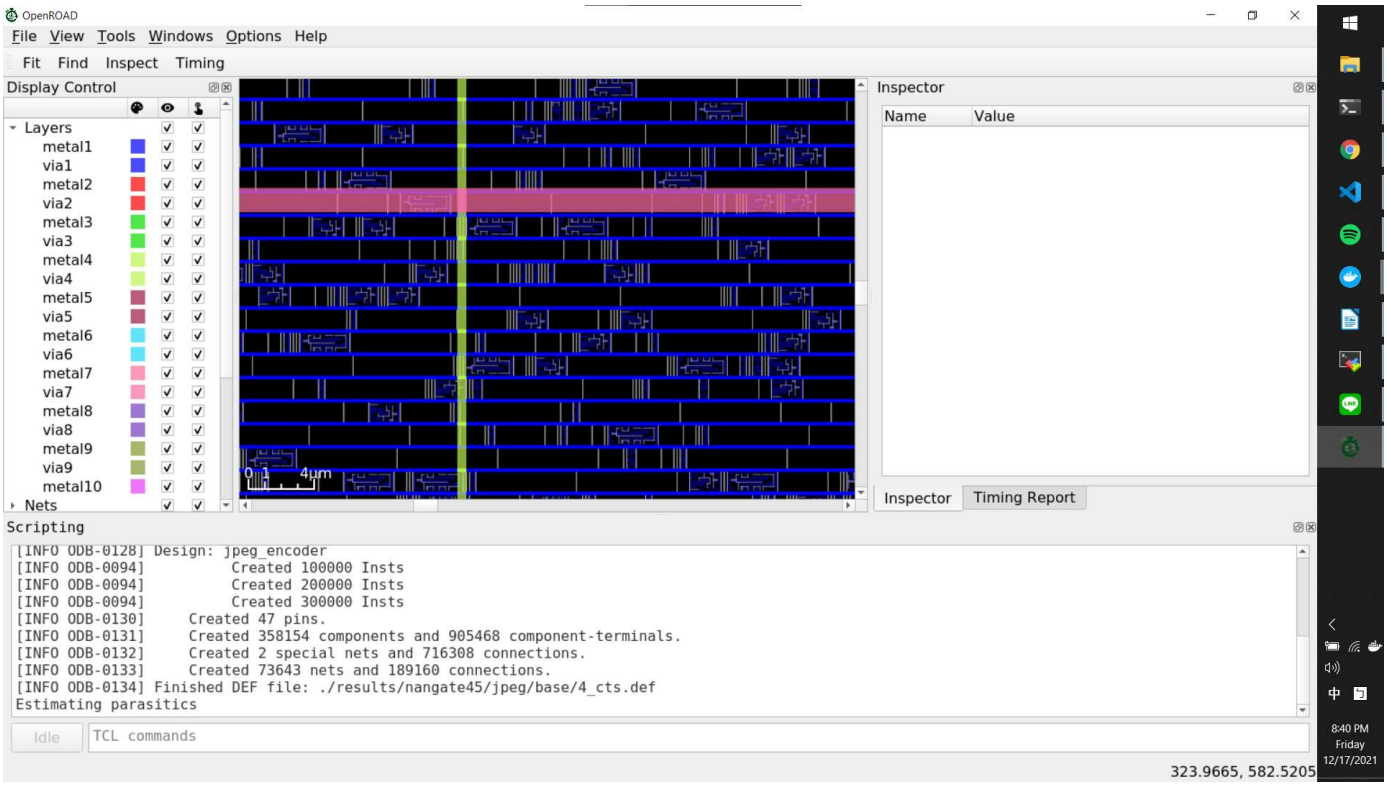


Design 2 - jpeg

2_floorplan



4_cts



Compare and discuss 2 Verilog files generated from consecutive steps.

在第二步 floorplan 中，會把一些原本接到 wire 的邏輯閘改接到 IO 腳位。

Compare and discuss 2 DEF files generated from consecutive steps.

步驟 5 route 會開始規劃訊號線及時脈線的 layout。

Overall discussion and comments about the EDA tool

我覺得使用起來很流暢，每個步驟都有對應的輸出可以用軟體檢視，非常清楚，對製程中各步驟的分工可以有更清楚的認識。