DDLab project 4

```
module ALU(
    output reg [7:0] y,
    input [2:0] sel,
    input [7:0] a,b
);
    always @(sel,a,b) begin
        case (sel)
            3'b0: y = 8'b0;
            3'b1: y = a & b;
            3'b10: y = a | b;
            3'b11: y = a ^ b;
            3'b100: y = ~a;
            3'b101: y = a - b;
            3'b110: y = a + b;
            3'b111: y = 8'hFF;
            default:
                y = 8'b0;
        endcase
    end
endmodule

module t_ALU;
    wire [7:0] y;
    reg [2:0] sel;
    reg [7:0] a,b;

    ALU alu(y,sel,a,b);

    initial begin
        a = 8'b10101010; b = 8'b11110000;
        sel = 3'b0;
        $display("time = %d, sel = %b, a = %h, b = %h, y = %h", $time, sel, a, b, y);

        repeat(7)
            #100 sel = sel + 3'b1;
    end
    initial #800 $finish;
    initial $dumpvars;
    initial begin
        $monitor("time = %d, sel = %b, a = %h, b = %h, y = %h", $time, sel, a, b, y);
    end


endmodule
```

```
PS C:\data\MyNTUST\Lab-of-Digital-Logic-Design\4> iverilog.exe .\alu.v
PS C:\data\MyNTUST\Lab-of-Digital-Logic-Design\4> vvp .\a.out -lxt2
time =                    0, sel = 000, a = aa, b = f0, y = xx
LXT2 info: dumpfile dump.lx2 opened for output.
time =                    0, sel = 000, a = aa, b = f0, y = 00
time =                  100, sel = 001, a = aa, b = f0, y = a0
time =                  200, sel = 010, a = aa, b = f0, y = fa
time =                  300, sel = 011, a = aa, b = f0, y = 5a
time =                  400, sel = 100, a = aa, b = f0, y = 55
time =                  500, sel = 101, a = aa, b = f0, y = ba
time =                  600, sel = 110, a = aa, b = f0, y = 9a
time =                  700, sel = 111, a = aa, b = f0, y = ff
.\alu.v:37: $finish called at 800 (1s)
PS C:\data\MyNTUST\Lab-of-Digital-Logic-Design\4>
```