UTRON

UT6264C

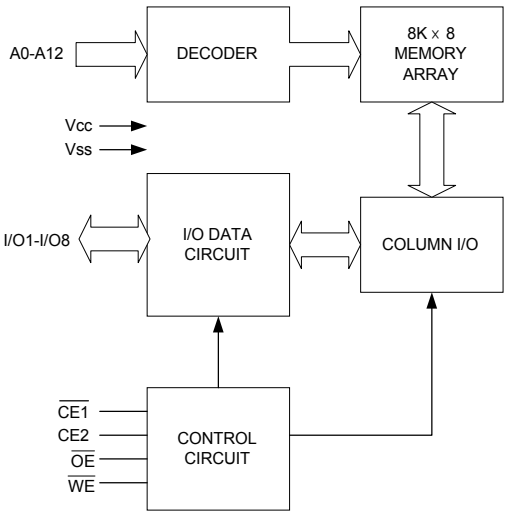
Rev. 1.1

8K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time : 35/70ns (max.)
- Low power consumption :
  Operating : 45/30 mA (typ.)
  CMOS Standby : 2mA (typ.) normal
  2 μA (typ.) L-version
  1 μA (typ.) LL-version
- Single 4.5V~5.5V power supply
- Operating temperature :
  Commercial : 0℃~70℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 28-pin 600 mil PDIP
  28-pin 330 mil SOP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE1}$,CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No connection

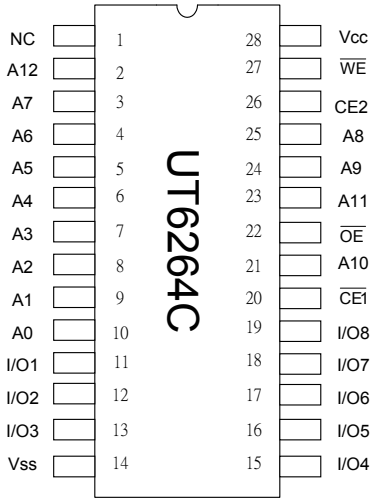
GENERAL DESCRIPTION

The UT6264C is a 65,536-bit low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

Easy memory expansion is provided by using two chip enable input.($\overline{CE1}$,CE2) ,and supports low data retention voltage for battery back-up operation with low data retention current.

The UT6264C operates from a single 4.5V~5.5V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



PDIP/SOP

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to +7.0	V
Operating Temperature	Commercial	T_A	0 to +70	℃
Storage Temperature		T_{STG}	-65 to +150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 sec)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	ISB, ISB1
Standby	X	L	X	X	High - Z	ISB, ISB1
Output Disable	L	H	H	H	High - Z	Icc,Icc1,Icc2
Read	L	H	L	H	D_{OUT}	Icc,Icc1,Icc2
Write	L	H	X	L	D_{IN}	Icc,Icc1,Icc2

note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5V~5.5V, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	Vcc			4.5	5.0	5.5	V
Input High Voltage	V_{IH}			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$; $\overline{CE1}$=V_{IH};or CE2=V_{IL}; or $\overline{OE}$ = V_{IH} ;or $\overline{WE}$ = V_{IL}		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 4mA		-	-	0.4	V
Operating Power Supply Current	Icc	Cycle time=Min,$I_{I/O}$ = 0mA; $\overline{CE1}$= V_{IL} , CE2= V_{IH}	- 35	-	45	60	mA
			- 70	-	30	45	mA
	Icc1	Cycle time=1us; $I_{I/O}$ = 0mA ; $\overline{CE1}$=0.2V; CE2=Vcc-0.2V; other pins at 0.2V or Vcc-0.2V		-	20	30	mA
	Icc2	Cycle time=500ns;$I_{I/O}$ = 0mA; $\overline{CE1}$=0.2V; CE2=Vcc-0.2V; other pins at 0.2V or Vcc-0.2V		-	10	15	mA
Standby Current (TTL)	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2= V_{IL}	Normal	-	1	10	mA
			- L/- LL	-	0.3	3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE1} \geqq$ VCC-0.2V ; or CE2 $\leqq$ 0.2V; other pins at 0.2V or Vcc-0.2V	Normal	-	2	5	mA
			- L	-	2	100	µA
			- LL	-	1	50	µA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF, I_{OH}/I_{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5V~5.5V, T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT6264C-35		UT6264C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ1}*, t_{CLZ2}*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}*, t_{CHZ2}*	-	25	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

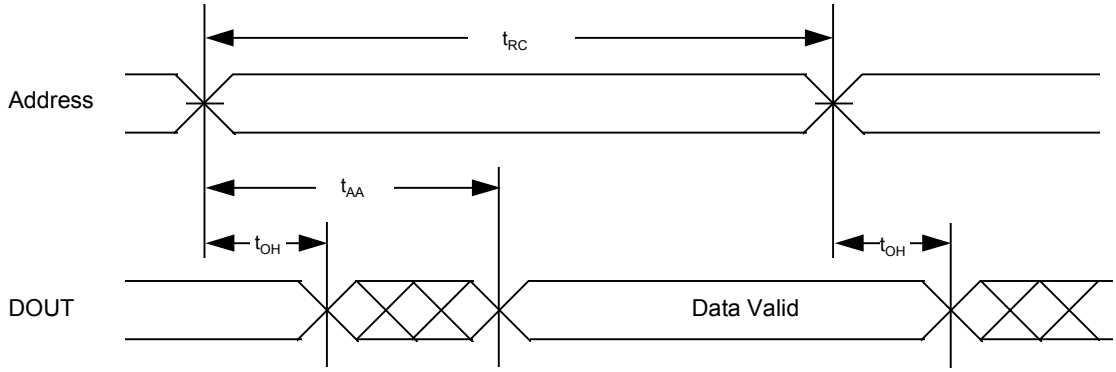
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT6264C-35		UT6264C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	50	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	25	ns

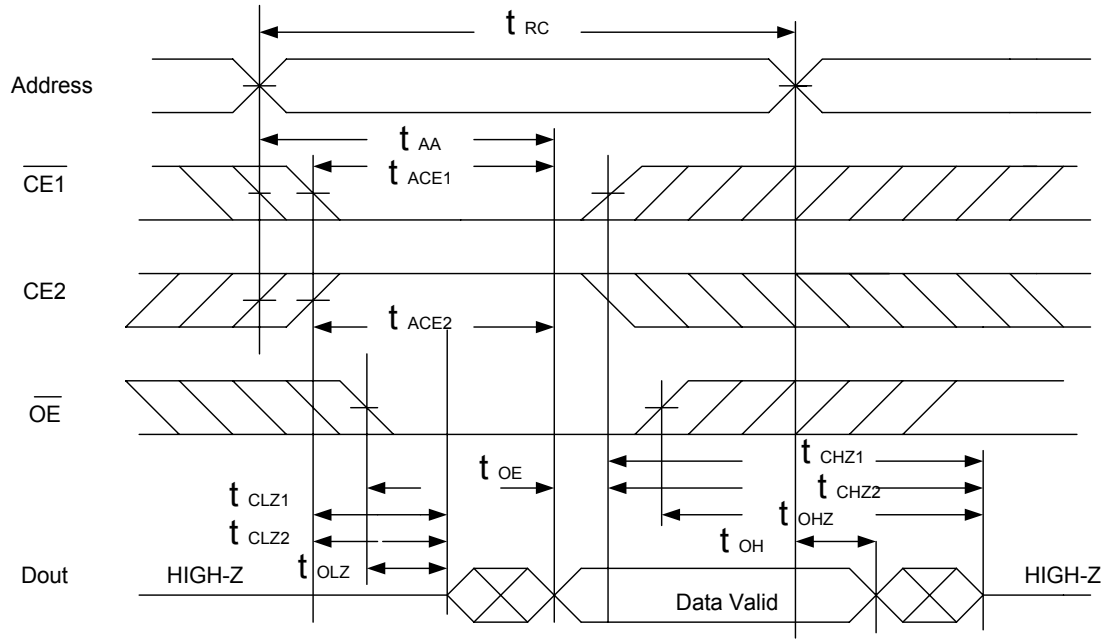
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



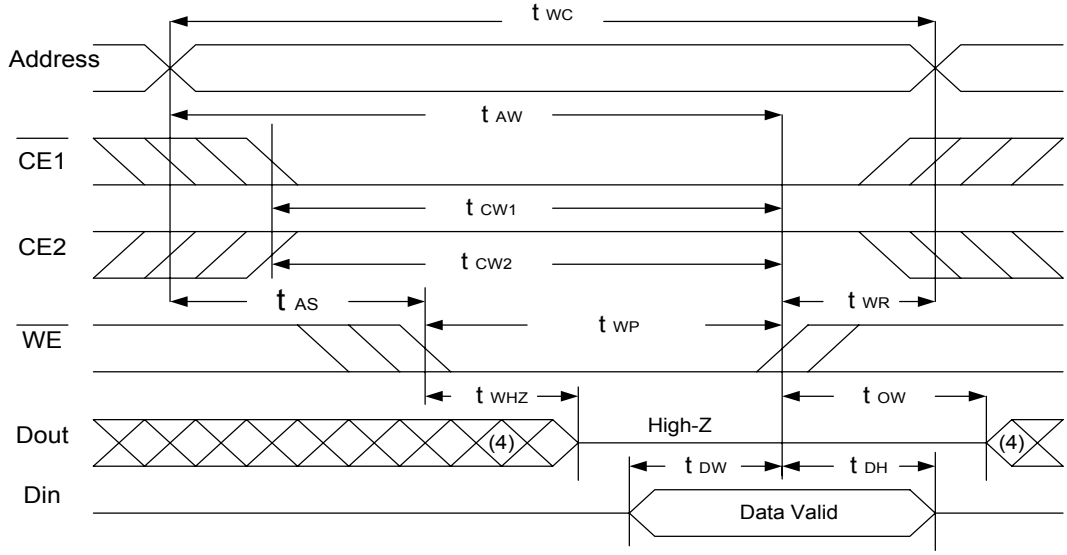
READ CYCLE 2 ($\overline{CE1}$, CE2 and $\overline{OE}$ Controlled) (1,3,5,6)



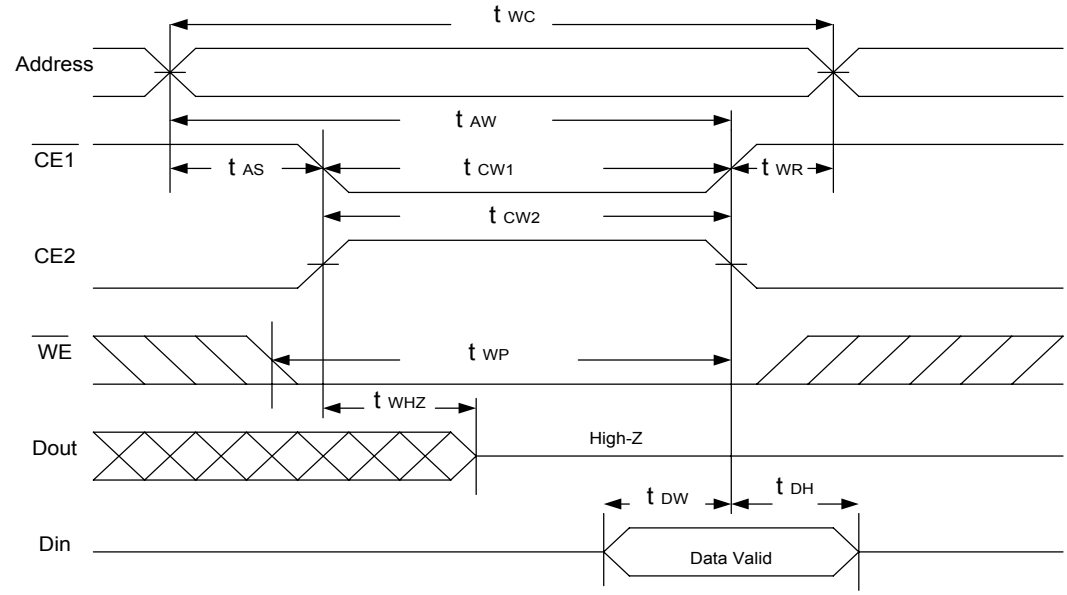
Notes :

1. $\overline{WE}$ is HIGH for a read cycle.
2. Device is continuously selected $\overline{OE}$, $\overline{CE1}$ =V_{IL} and CE2=V_{IH}.
3. Address must be valid prior to or coincident with $\overline{CE1}$ low and CE2 high transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)



Notes :

1. $\overline{WE}$ or $\overline{CE1}$ must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high Impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.

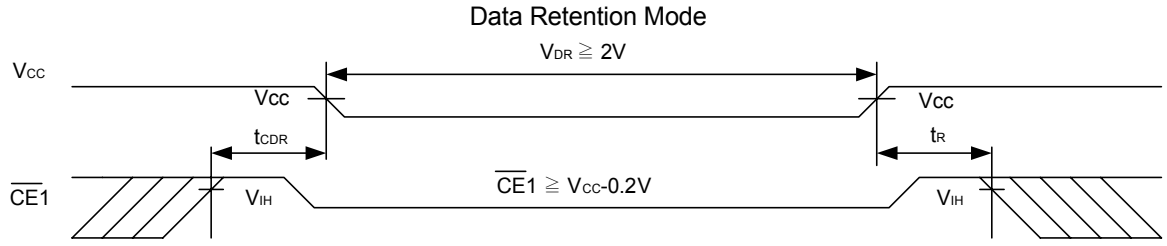
DATA RETENTION CHARACTERISTICS (TA = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V		2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc=2V	-L	-	1	50	μA
		$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V	-LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data RetentionWaveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

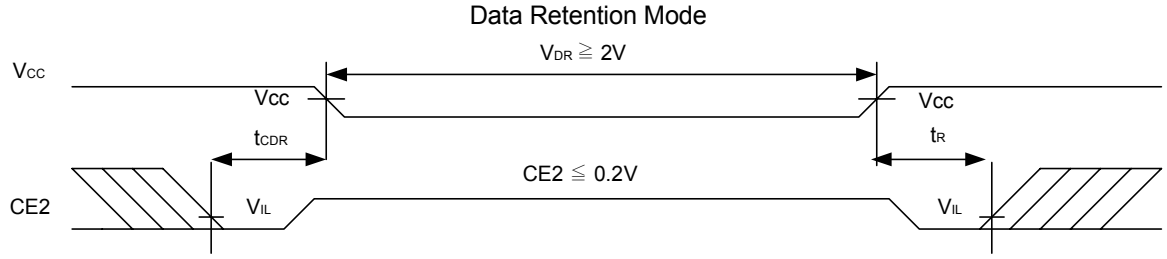
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE1}$ controlled)

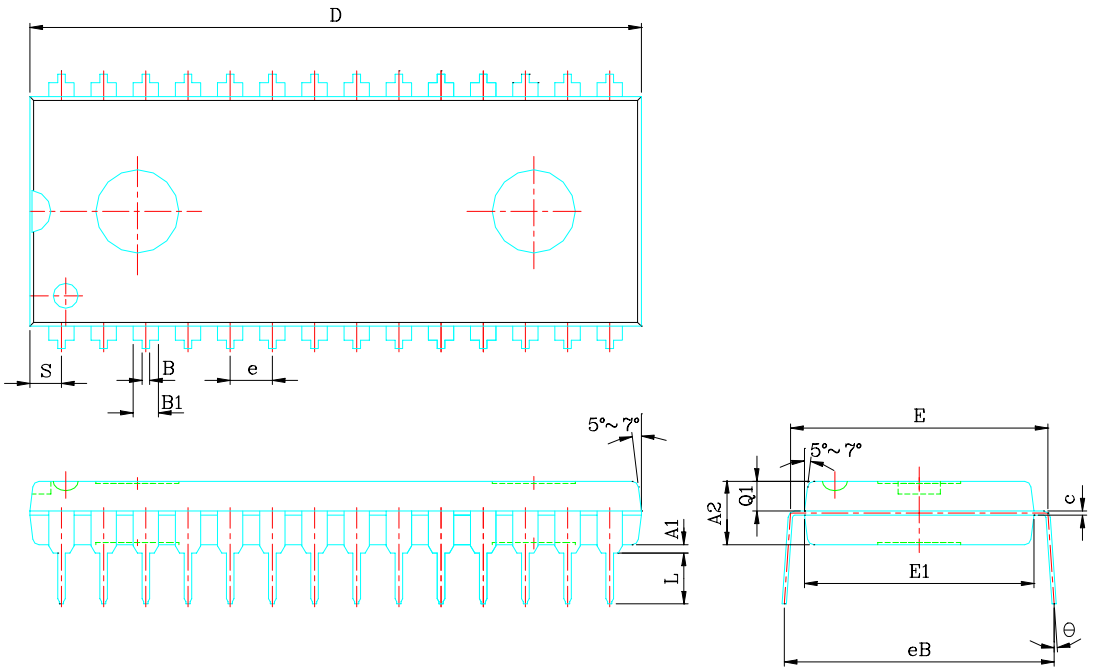


Low Vcc Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



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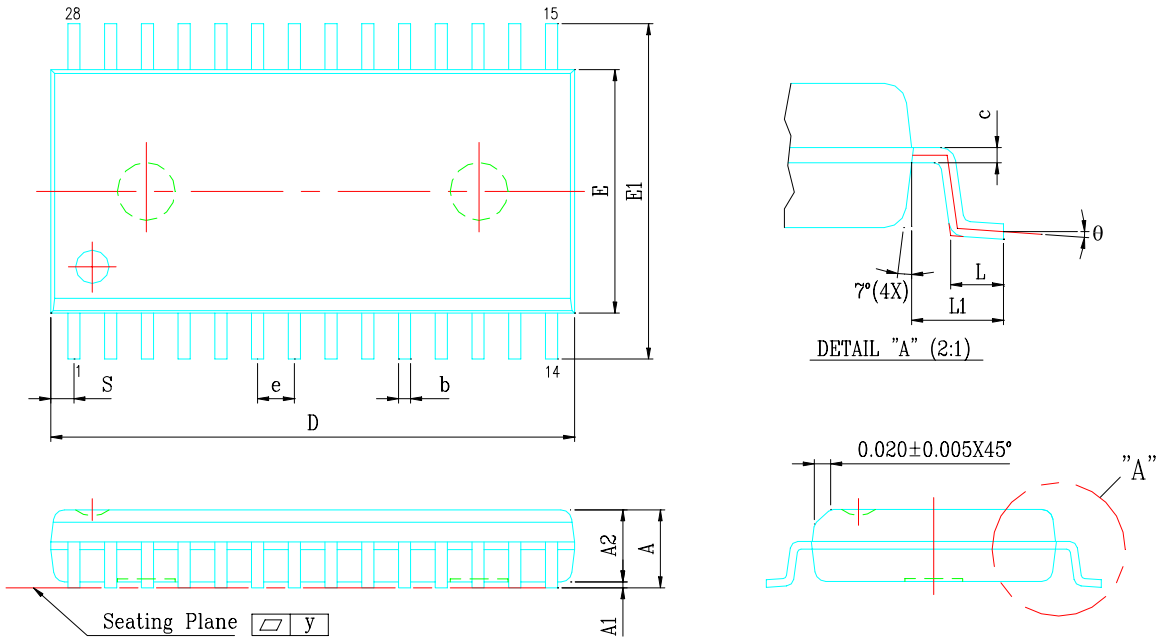
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150± 0.005	3.810± 0.127
B	0.020 (MAX)	0.508(MAX)
B1	0.055 (MAX)	1.397(MAX)
c	0.012 (MAX)	0.304 (MAX)
D	1.430 (MAX)	36.322 (MAX)
E	0.625 (MAX)	15.87 (MAX)
E1	0.52 (MAX)	13.208 (MAX)
e	0.100 (TYP)	2.540(TYP)
eB	0.6 (TYP)	15.24 (TYP)
L	0.180(MAX)	4.572(MAX)
S	0.06 (MAX)	1.524 (MAX)
Q1	0.08(MAX)	2.032(MAX)
Θ	15°(MAX)	15°(MAX)

28 pin 330 mil SOP Package Outline Dimension



SYMBOL \ UNIT	INCH(REF)	MM(BASE)
A	0.112(max)	2.845(max)
A1	0.004(MIN)	0.102(MIN)
A2	0.098±0.005	2.489±0.127
b	0.016(TYP)	0.406(TYP)
c	0.010(TYP)	0.254(TYP)
D	0.713±0.005	18.110±0.127
E	0.331±0.005	8.407±0.127
E1	0.465±0.012	11.811±0.305
e	0.050(TYP)	1.270(TYP)
L	0.0404±0.008	1.0255±0.203
L1	0.067±0.008	1.702±0.203
S	0.047(MAX)	1.194(MAX)
y	0.003(MAX)	0.076(MAX)
θ	0°~10°	0°~10°

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (µA) (TYP.)	PACKAGE
UT6264CPC-35	35	2mA	28 PIN PDIP
UT6264CPC-35L	35	2µA	28 PIN PDIP
UT6264CPC-35LL	35	1µA	28 PIN PDIP
UT6264CPC-70	70	2mA	28 PIN PDIP
UT6264CPC-70L	70	2µA	28 PIN PDIP
UT6264CPC-70LL	70	1µA	28 PIN PDIP
UT6264CSC-35	35	2mA	28 PIN SOP
UT6264CSC-35L	35	2µA	28 PIN SOP
UT6264CSC-35LL	35	1µA	28 PIN SOP
UT6264CSC-70	70	2mA	28 PIN SOP
UT6264CSC-70L	70	2µA	28 PIN SOP
UT6264CSC-70LL	70	1µA	28 PIN SOP

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	May 3 ,2001
Rev. 1.0	The timeing waveforms add CE2 control pin.	Jun.4,2001
Rev. 1.1	1. Revised package outline dimension. 2. Revised waveform.	Jan 15,2002