iCE40 sysCLOCK PLL Design and Usage Guide

March 2015 Technical Note TN1251

Introduction

This technical note discusses the clock resources available in the iCE40™ devices (iCE40LP/HX, iCE40LM, iCE40 Ultra™). Details are provided for global buffers and sysCLOCK™ PLLs. The iCE40 devices include an ultra-low power Phase Locked Loop (PLL) to support a variety of display, imaging and memory interface applications. Table 1 shows the number of PLLs in each of the devices in the iCE40 device family. For the performance of the PLLs, please refer to the device family data sheet.

Table 1. Number of PLLs in the iCE40 Device Family

Package	HX1K	HX4K	HX8K
VQ100 100-ball VQFP	0	—	—
CB132 132-ball csBGA	1	2	2
TQ144 144-ball TQFP	1	2	—
CM225 225-ball ucBGA	—	—	2
CT256 256-ball caBGA	—	—	2

Package	LP384	LP640	LP1K	LP4K	LP8K
SQG16 16-ball WLCSP	—	0	—	—	—
SG32 32-ball QFN	0	—	—	—	—
CM36 36-ball ucBGA	0	—	0	—	—
CM49 49-ball ucBGA	0	—	1	—	—
CM81 81-ball ucBGA	—	—	1	1	1
CB81 81-ball csBGA	—	—	0	—	—
QN84 84-ball QFN	—	—	0	—	—
CM121 121-ball ucBGA	—	—	1	2	2
CB121 121-ball csBGA	—	—	1	—	—
CM225 225-ball ucBGA	—	—	—	2	2

Package	LM1K	LM2K	LM4K
SWG25 25-ball WLCSP	0	0	0
CM36 36-ball ucBGA	1	1	1
CM49 49-ball ucBGA	1	1	1

Package	Ultra 1K	Ultra 2K	Ultra 4K
SWG36 36-ball WLCSP	1	1	1

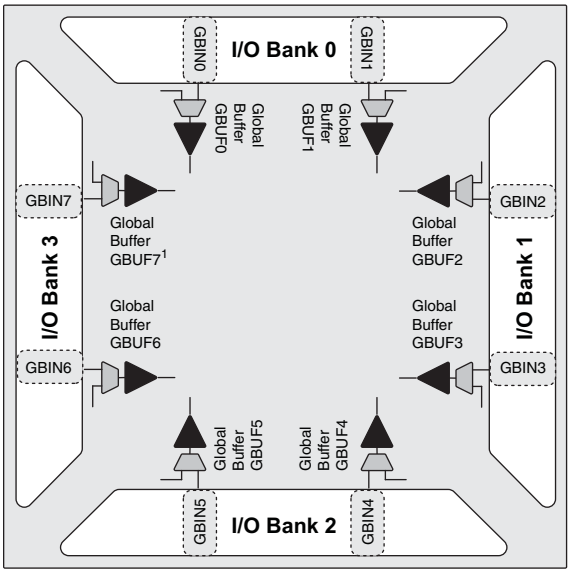
Package	UltraLite 640	UltraLite 1K
SWG16 16-ball WLCSP	1	1
CM36 36-ball ucBGA	1	1

Global Routing Resources

The iCE40 device has eight high drive buffers called global buffers (GBUFx). These are connected to eight low-skew global lines, designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals.

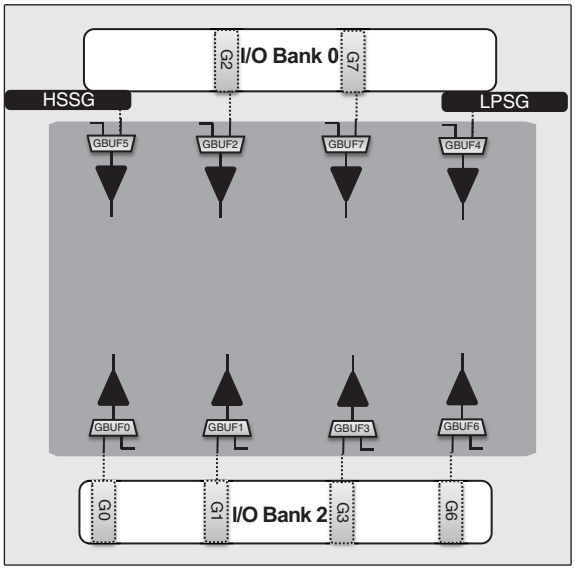
Figure 1. High-drive, Low-skew, High-fanout Global Buffer Routing Resources

iCE40LP/HX



1. GBUF7 and its associted PIO are best for direct differential clock inputs.

iCE40LM/iCE40 Ultra/iCE40 UltraLite



The input (sources) to the GBUFx can be:

- Global buffer inputs (GBINx, Gx)
- Programmable interconnect[1]
- PLL output[1]
- Programmable input/output block (PIO)[1]
- Strobe Generators (HSSG, LPSG on iCE40LM devices.)
- On-chip Oscillator (LFOSC, HFOSC on iCE40 Ultra and iCE40 UltraLite devices.)

1. To use a global buffer along with a user interface or PIO, use the SB_GB primitive if it is not inferred automatically.

The associated GBINx/Gx pin represents the best pin to drive a global buffer from an external source.

Verilog Instantiation

```
SB_GB My_Global_Buffer_i (// required for a user's internally generated FPGA signal that is
heavily loaded and requires global buffering. For example, a user's logic-generated clock.

.USER_SIGNAL_TO_GLOBAL_BUFFER (Users_internal_Clk),

.GLOBAL_BUFFER_OUTPUT ( Global_Buffered_User_Signal) );
```

VHDL Instantiation

```
component SB_GB
   port (
   USER_SIGNAL_TO_GLOBAL_BUFFER:input std_logic;
   GLOBAL_BUFFER_OUTPUT:output std_logic);
end component;

My_Global_Buffer_i: SB_GB
   port map (
   USER_SIGNAL_TO_GLOBAL_BUFFER=>Users_internal_Clk,
   BUFFER=>Global_Buffered_User_Signal);
```

Refer to the iCE Technology Library for more details on device primitives.

If not used in an application, individual global buffers are turned off to save power.

Table 2 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). Refer to the Architecture section of the iCE40 Family Data Sheet for more information on PLBs. All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enabled input.

Table 2. Global Buffer Connections to a Programmable Logic Block

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes		
GBUF1		Yes	Yes	Yes
GBUF2		Yes		
GBUF3		Yes	Yes	Yes
GBUF4		Yes		
GBUF5		Yes	Yes	Yes
GBUF6		Yes		
GBUF7		Yes	Yes	Yes

Table 3 lists the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pins. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

Table 3. Global Buffer Connections to Programmable I/O Pair

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	None (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	

iCE40 sysCLOCK PLL

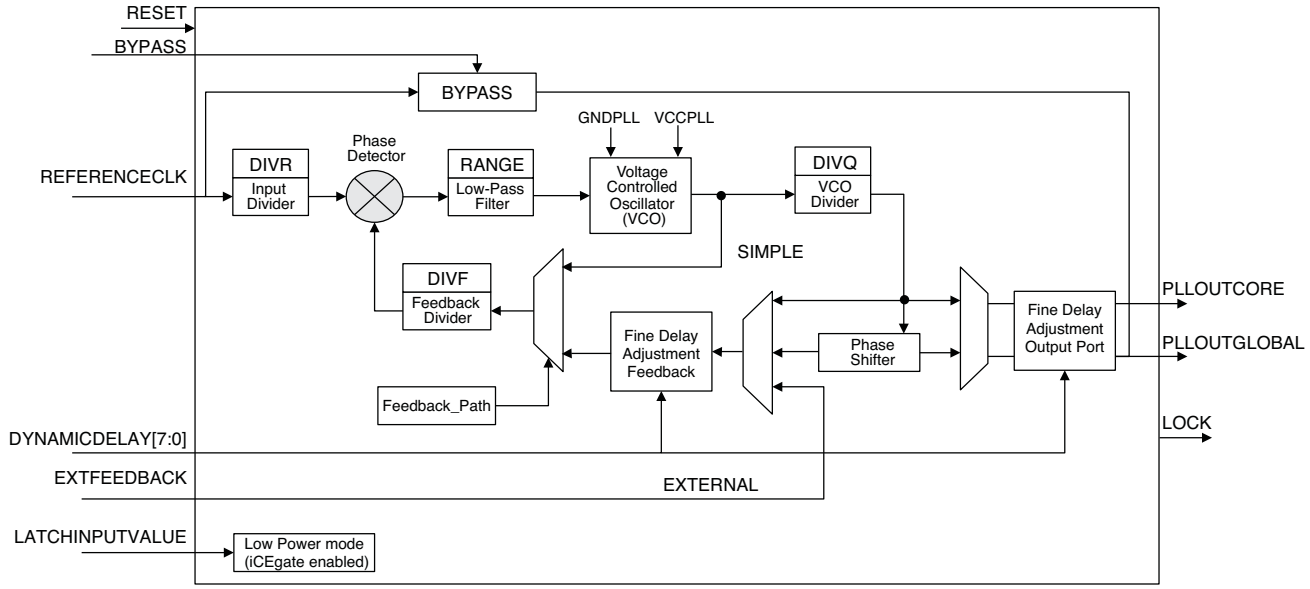
The iCE40 Phase Locked Loop (PLL) provides a variety of user-synthesizable clock frequencies, along with custom phase delays.The PLL in the iCE40 device can be configured and utilized with the help of software macros or the PLL Module Generator. The PLL Module Generator utility helps users to quickly configure the desired settings with the help of a GUI and generate Verilog code which configures the PLL macros. Figure 2 shows the iCE40 sysCLOCK PLL block diagram.

iCE40 sysCLOCK PLL Features

The PLL provides the following functions in iCE40 applications:

- Generates a new output clock frequency
  - Clock multiplication
  - Clock division
- De-skews or phase-aligns an output clock to the input reference clock
  - Faster input set-up time
  - Faster clock-to-output time
- Corrects output clock to have nearly a 50% duty cycle, which is important for Double Data Rate (DDR) applications
- Optionally phase shifts the output clock relative to the input reference clock
  - Optimal data sampling within the available bit period
  - Fixed quadrant phase shifting at 0°, 90°
  - Optional fine delay adjustments of up to 2.5 ns (typical) in 150 ps increments (typical)

Figure 2. iCE40 Phase Locked Loop (sysCLOCK PLL) Block Diagram



Signals

Table 4 lists the signal names, direction, and function of each connection to the PLL. Some of the signals have an associated attribute or property, as listed in Table 4. Table 4 lists the attributes or properties associated with the PLL and the allowable settings for each attribute.

Note: Signals and attribute settings of PLL primitives are for reference only. It is recommended to generate a PLL module with the GUI-based PLL Module Generator as explained in the Generating iCE40 PLL Using PLL Module Generator in iceCube2 Design Software section.

Table 4. PLL Signals

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
RESET	Input	Reset
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

Table 5. PLL Attributes and Settings in PLL Macro [1]

Parameter Name	Description	Parameter Value	Description
FEEDBACK_PATH	Selects the feedback path to the PLL	SIMPLE	Feedback is internal to the PLL, directly from VCO.
		DELAY	Feedback is internal to the PLL, through the Fine Delay Adjust Block.
		PHASE_AND_DELAY	Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block.
		EXTERNAL	Feedback path is external to the PLL and connects to the EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.

Table 5. PLL Attributes and Settings in PLL Macro (Continued)[1]

Parameter Name	Description	Parameter Value	Description
DELAY_ADJUSTMENT_MODE_FEEDBACK	Selects the mode for the Fine Delay Adjust block in the feedback path	FIXED	Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_FEEDBACK parameter setting.
		DYNAMIC	Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins.
FDA_FEEDBACK	Sets a constant value for the Fine Delay Adjust Block in the feedback path	0, 1,…,15	The PLLOUTGLOBAL and PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if DELAY_ADJUSTMENT_MODE_FEEDBACK is set to FIXED.
DELAY_ADJUSTMENT_MODE_RELATIVE	Selects the mode for the Fine Delay Adjust block	FIXED	Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_RELATIVE parameter setting.
		DYNAMIC	Delay of the Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[7:4] pins.
FDA_RELATIVE	Sets a constant value for the Fine Delay Adjust Block	0, 1,…,15	The PLLOUTGLOBALA and PLLOUTCOREA signals are additionally delayed by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE_RELATIVE is set to FIXED.
SHIFTREG_DIV_MODE	Selects shift register configuration	0,1	Used when FEEDBACK_PATH is set to PHASE_AND_DELAY. 0 = Divide by 4 1 = Divide by 7
PLLOUT_SELECT	Selects the signal to be output at the PLLOUTCORE and PLLOUTGLOBAL ports	SHIFTREG_0deg	0° phase shift only if the setting of FEEDBACK_PATH is set to PHASE_AND_DELAY.
		SHIFTREG_90deg	90° phase shift only if the setting of FEEDBACK_PATH is PHASE_AND_DELAY and SHIFTREG_DIV_MODE = 0.
		GENCLK	The internally generated PLL frequency will be output without any phase shift.
		GENCLK_HALF	The internally generated PLL frequency will be divided by 2 and then output. No phase shift.

Table 5. PLL Attributes and Settings in PLL Macro (Continued)[1]

Parameter Name	Description	Parameter Value	Description
DIVR	REFERENCECLK divider	0,1,2,…,15	These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.
DIVF	Feedback divider	0,1,…,63	
DIVQ	VCO divider	0,1,…,7	
FILTER_RANGE	PLL filter range	0,1,…,7	
EXTERNAL_DIVIDE_FACTOR	Divide-by factor of a divider in external feedback path	User specified value. Default = 1	Specified only when there is a user-implemented divider in the external feedback path.
ENABLE_ICEGATE	Enables the PLL power-down control	0	Power-down control disabled.
		1	Power-down controlled by the LATCHINPUTVALUE input.

1. The attributes are automatically configured through the PLL Module Generator.

Clock Input Requirements

Proper operation requires the following considerations:

- A stable monotonic (single frequency) reference clock input
- The reference clock input must be within the input clock frequency range, F_{REF}, specified in the data sheet
- The reference clock must have a duty cycle that meets the requirement specified in the data sheet
- The jitter on the reference input clock must not exceed the limits specified in the data sheet

PLL Output Requirements

The PLL output clock, PLLOUT, has the following restrictions:

- The PLLOUT output frequency must be within the limits specified in the data sheet
- The PLLOUT output is not valid or stable until the PLL LOCK output remains high

Functional Description

The PLL optionally multiplies and/or divides the input reference clock to generate a PLLOUT output clock of another frequency. The output frequency depends on the frequency of the REFERENCLK input clock and the settings for the DIVR, DIVF, DIVQ, RANGE, and FEEDBACK_PATH attribute settings, as indicated in Figure 2.

The PLL's phase detector and Voltage Controlled Oscillator (VCO) synthesize a new output clock frequency based on the attribute settings. The VCO is an analog circuit and has independent voltage supply and ground connections labeled VCCPLL and GNDPLL.

PLLOUT Frequency for All Modes Except FEEDBACK_PATH = SIMPLE

For all the FEEDBACK_PATH modes, except SIMPLE, the PLLOUT frequency calculated as per the equation below.

$$F_{PLLOUT} = \frac{F_{REFERENCECLK} \times (\mathrm{DIVF} + 1)}{\mathrm{DIVR} + 1}$$

PLLOUT Frequency for FEEDBACK_PATH = SIMPLE

In the SIMPLE feedback mode, the PLL feedback signal taps directly from the output of the VCO, before the final divider stage. Consequently, the PLL output frequency has an additional divider step, DIVQ, contributed by the final divider step as shown in equation below. (DIVF, DIVQ and DIVR are binary).

$$F_{PLLOUT} = \frac{F_{REFERENCECLK} \times (\mathrm{DIVF} + 1)}{2^{(DIVQ)} \times (DIVR + 1)}$$

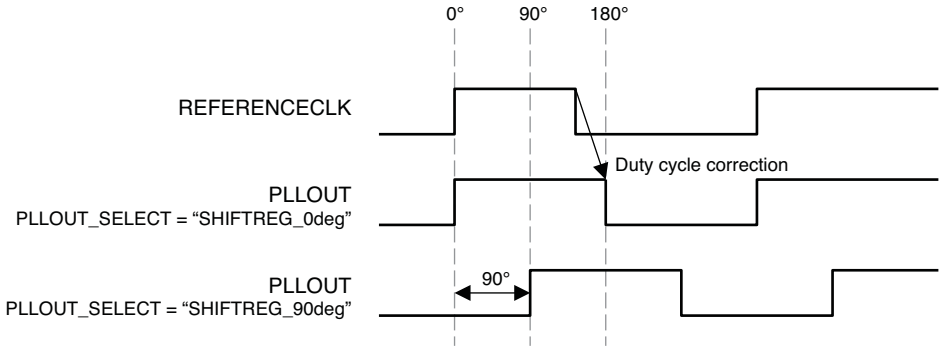
Fixed Quadrant Phase Shift

The PLL optional phase feature shifts the PLLOUT output by a specified quadrant or quarter clock cycle as shown in Figure 3 and Table 6. The quadrant phase shift option is only available when the FEEDBACK_PATH attribute is set to PHASE_AND_DELAY.

Table 6. PLL Phase Shift Options

PLLOUT_SELECT	Duty Cycle Correction	Phase Shift	Fraction Clock Cycle
SHIFTREG_0deg	Yes	0º	None
SHIFTREG_90deg	Yes	90º	Quarter Cycle

Figure 3. Fixed Quadrant Phase Shift Control



Unlike the Fine Delay Adjustment, the quadrant phase shifter always shifts by a fixed phase angle. The resulting phase shift, measured in delay, depends on the clock period and the PLLOUT_PHASE phase shift setting, as shown in the equation below.

$$Delay = \frac{\text{Phase Shift}}{360°} \times \text{Clock\_Period}$$

Fine Delay Adjustment (FDA)

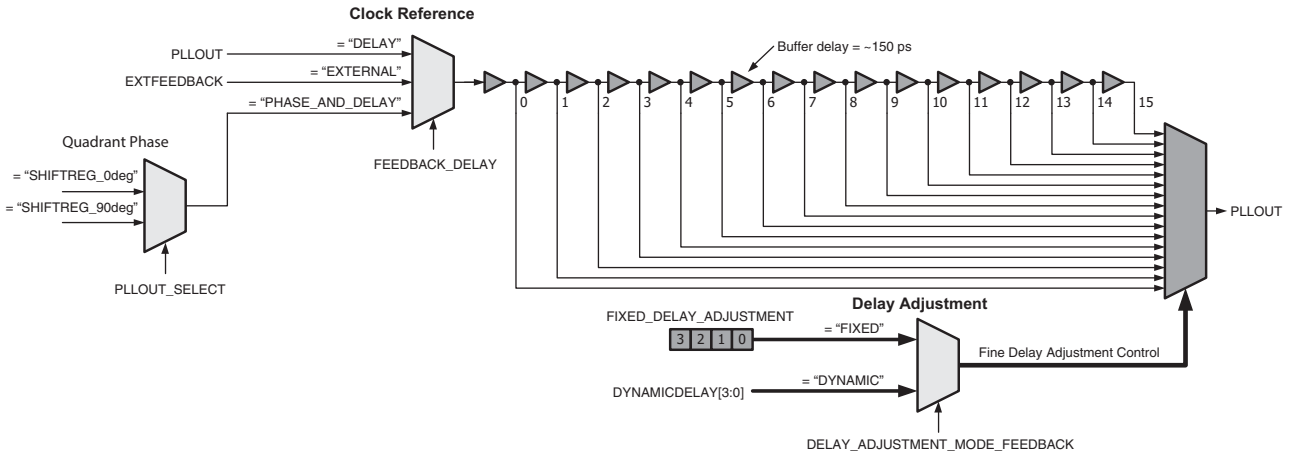
The PLL provides two optional fine delay adjustment blocks that control the delay of the PLLOUT output relative to the input reference clock, to an external feedback signal, or relative to the selected quadrant phase shifted clock. One FDA is placed in the feedback path, while the other FDA provides delay on the output port directly. If a two-port PLL is used, this additional delay is applied only on Port A. Unlike the Feedback FDA, the output port FDA is not dependent on FEEDBACK_PATH, and can be used even if FEEDBACK_PATH = Simple. The PLL Module Generator provides easy selection of the two fine delay adjust blocks. Figure 4 shows the typical first fine delay adjust control block.

The delay is adjusted by selecting one or more of the 16 delay taps inside the fine delay adjustment block. Each tap is approximately 150 ps.

Fine Delay Adjustment (nominal) = (n+1) * 150ps; $0 \leq n \leq 15$, where 'n' is the number of delay taps.

The number of taps can be selected statically (by providing the value within the PLL Module Generator) or dynamically by setting the values in DYNAMICDELAY [7:0]. DYNAMICDELAY [3:0] sets the tap numbers for the feedback path fine delay adjustment block while DYNAMICDELAY [7:0] sets values for the output port FDA. Refer to parameters DELAY_ADJUSTMENT_MODE_FEEDBACK and DELAY_ADJUSTMENT_MODE_RELATIVE in Table 2 for more details.

Figure 4. Fine Delay Adjust Control



Phase Angle Equivalent

The fine delay adjustment feature injects an actual delay value, rather than a fixed phase angle like the Fixed Quadrant Phase Shift feature. Use the equation below to convert the fine adjustment delay to a resulting phase angle.

$$\text{Phase Shift} = \frac{\text{Fine\_Delay\_Adustment}}{\text{Clock Period}} \times 360°$$

Low Power Mode

The iCE40 sysCLOCK PLL has low operating power by default. The PLL can be dynamically disabled to further reduce power. The low-power mode must first be enabled by setting the ENABLE_ICEGATE attribute to '1'. Once enabled, use the LATCHINPUTVALUE to control the PLL's operation, as shown in Table 7. The PLL must reacquire the input clock and LOCK when the LATCHINPUTVALUE returns from '1' to '0', external feedback is used and path goes out into the fabric.

Table 7. PLL LATCHINPUTVALUE Control

ENABLE_ICEGATE Attribute	LATCHINPUTVALUE Input	Function
0	Don't Care	PLL is always enabled.
1	0	PLL is enabled and operating.
	1	PLL is in low-power mode; PLLOUT output holds last clock state.

Generating iCE40 PLL Using PLL Module Generator in iceCube2 Design Software

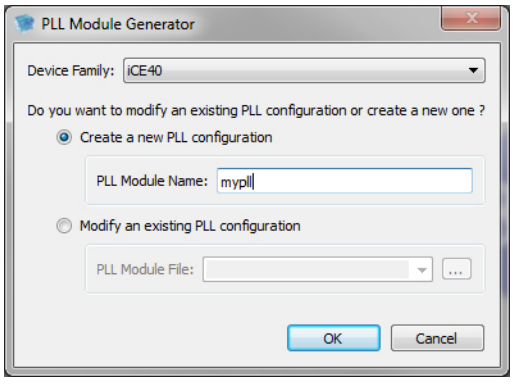
A GUI-based PLL Configuration tool is provided in iceCube2™ design software which configures the iCE40 PLL software macros based on the inputs in the GUI. The resultant HDL code can be used for synthesis.

Figure 5 shows the iceCube2 design software. The PLL module generator GUI can be invoked from the Tool menu as shown.

Figure 5. iceCube2 Design Software

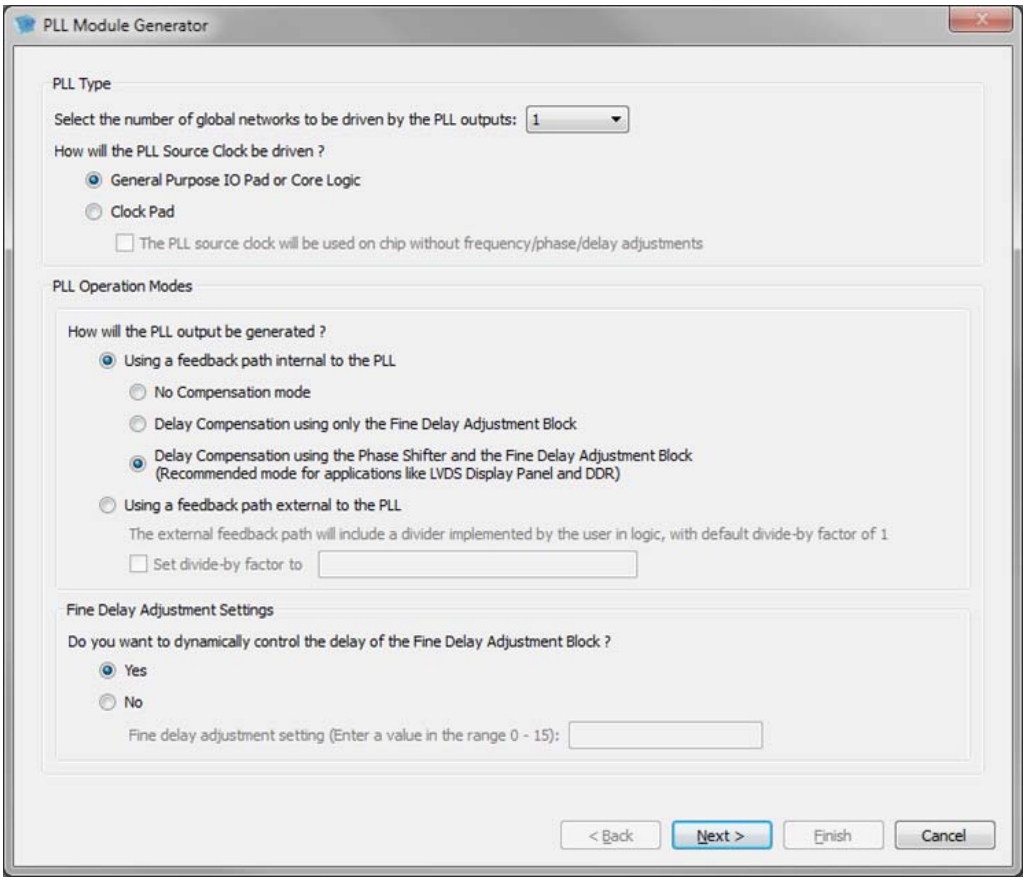
Figure 6 shows the PLL configuration GUI. Select the device (iCE40 in this case) and other desired operations.

Figure 6. PLL Module Generator/Modify Existing PLL Configuration



Click **OK** and the PLL frequency settings window will open up, as shown in Figure 7.

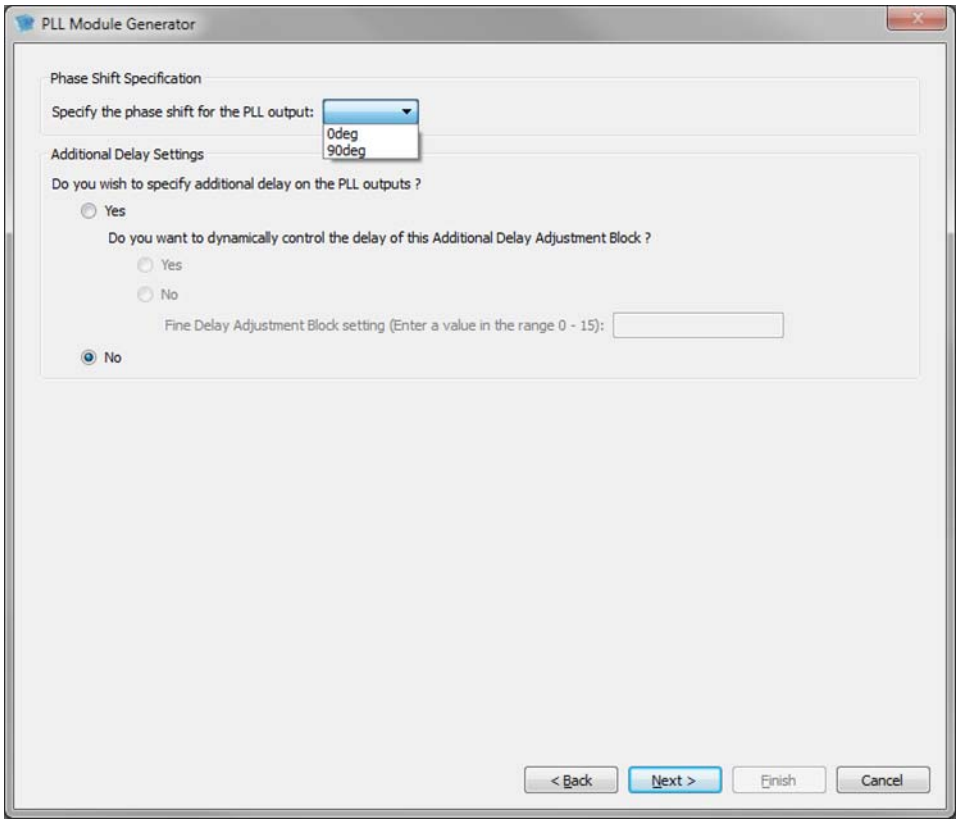
Figure 7. Settings Window 1



Refer to Table 8 for details on user options. Select desired settings which are self-explanatory. Note that some of the options are only activated when other required selections are made. These settings directly modify the PLL signals and attributes of the PLL software macro, as explained in Tables 4 and 5.

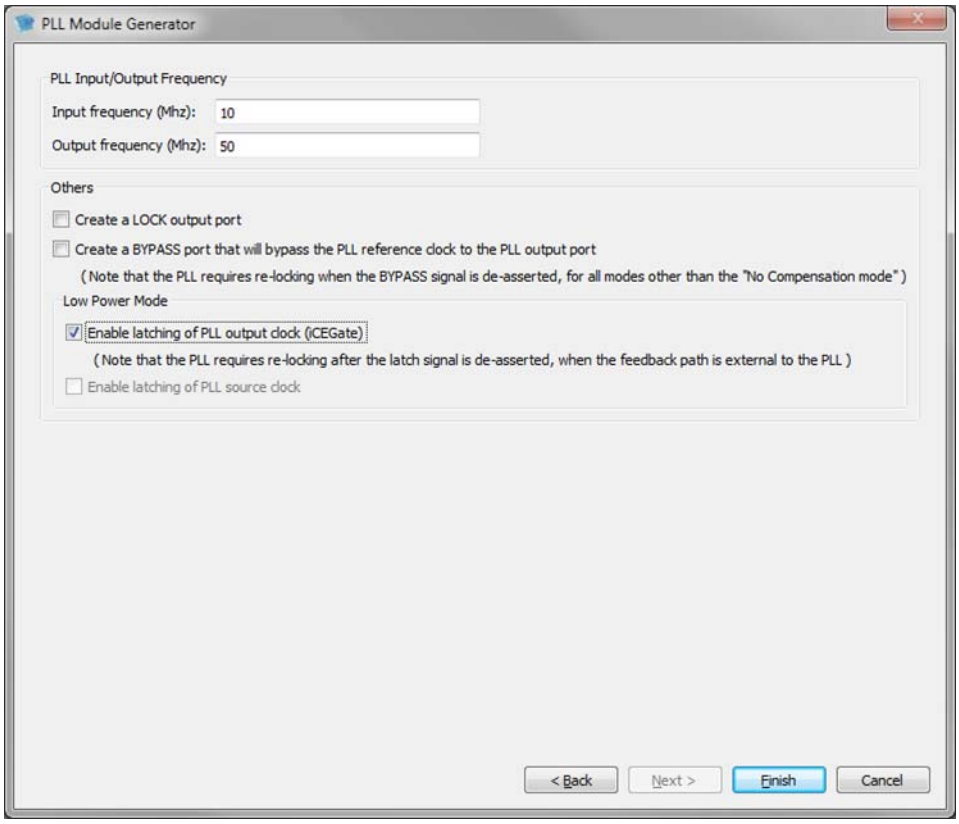
Figure 8 shows the next setting window.

Figure 8. Settings Window 2



Select desired values and click **Next**. The last of the settings windows will open, as shown in Figure 9.

Figure 9. Settings Window 3



After selecting the desired values, the final window the PLL Module Generator opens, as shown in Figure 10. This window shows all the values of the attributes and parameters that were discussed in the previous sections and in Tables 4 and 5. It also shows which PLL Macro type has been selected. The PLL Macro Type used in this example is SB_PLL40_Core.

Figure 10. PLL Configuration – Final Settings

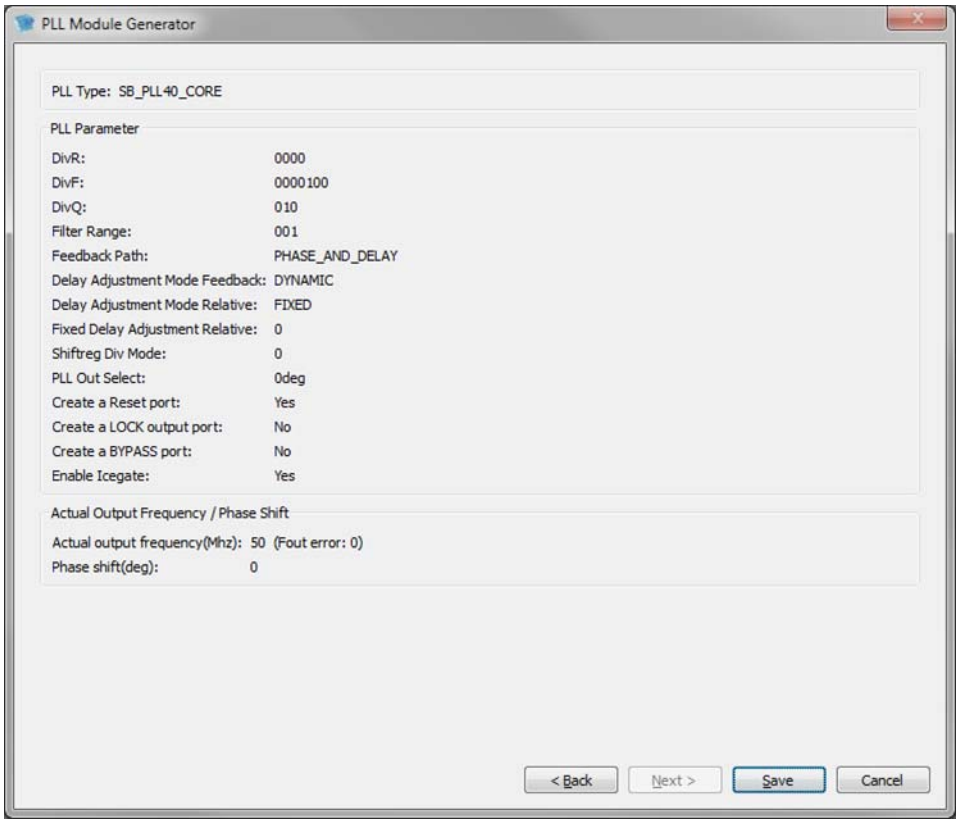


Table 8. PLL Configuration Tool User Parameters

User Parameter	Description	Range	Description
PLL Type			
Select the number of global networks to be driven by the PLL outputs	Setting the value to '1' generates a PLL which drives a single global clock network, as well as regular routing. Setting the value to '2' generates a PLL which drives two global clock networks as well as two regular routing resources.	1	
		2	
How will the PLL Source Clock be driven?		General Purpose I/O Pad or Core Logic	In this scenario, the PLL input (source clock) is driven by a signal from the FPGA fabric. This signal can either be generated on the FPGA core, or it can be an external signal that was brought onto the FPGA using a General Purpose I/O pad.
		Clock Pad	The PLL input clock (source) is driven by a dedicated clock pad located in I/O Bank 2 (bottom bank) or I/O Bank 0 (top bank). If the number of global networks is two, the source clock of the PLL can be used as is (i.e. without any frequency, delay compensation or phase adjustments). It is recommended that if the source clock is required on-chip, this option should not be selected.

Table 8. PLL Configuration Tool User Parameters (Continued)

User Parameter	Description	Range	Description
PLL Operation Modes			
How will the PLL output be generated?	The PLL can be configured to operate in one of multiple modes. An Operation Mode determines the feedback path of the PLL and enables phase alignment of the generated clock with regard to the source clock.	Using a feedback path internal to the PLL	This option is related to the phase delay introduced in the feedback path. The options are: **No Compensation mode** – There is no phase delay in the feedback path. **Delay compensation using only the Fine Delay Adjustment (FDA) Block** – The feedback path traverses through the FDA block, as explained in the section Fine Delay Adjustment (FDA). **Delay compensation using the phase shifter and the Fine Delay Adjustment (FDA) Block** – For single-port PLL types, the Phase Shifter provides two outputs corresponding to a phase shift of 0º and 90º. For two-port PLL types, the Phase Shifter has two modes: Divide-by-4 mode and Divide-by-7 mode. In Divide-by-4 mode, the output of the B port can be shifted either 0º or 90º with regard to A port outputs. In Divide-by-7 mode, the B port output frequency can be set to have a frequency ratio of 3.5:1 or 7:1 with regard to the port A output frequency.
		Using a feedback path external to the PLL	The feedback path traverses through FPGA routing (external to the PLL) followed by the FDA block. In effect, two delay controls are available – the external path for coarse adjustment and the FDA block for fine delay adjustment.
Fine Delay Adjustment Settings			
Do you want to dynamically control the delay of the Fine Delay Adjustment block?	Enabled only when Compensation mode or external Feedback mode is selected. The delay contributed by the FDA block can be fixed or controlled dynamically during FPGA operation. If fixed, it is necessary to provide a number (n) in the range of 0-15 to specify the delay contributed to the feedback path. For further details, see Fine Delay Adjustment (FDA).	Yes	
		No	Enter a value in the range 0-15.
Phase Shift Specification			
Specify the phase shift for the PLL output	Enabled only when delay compensation using the phase shifter is selected. Gives a phase shift of 0º and 90º to the output clock.	0º	
		90º	
Target Application[1]			
LVDS Display Panel	Two different frequencies can be observed on different ports (A and B).	3.5:1	The frequency of port B is 3.5x of Port A.
		7:1	The frequency of Port B is 7x of Port A.
DDR Application	The signal on Port B can be phase shifted by 90º with respect to signal A.	0º	
		90º	

Table 8. PLL Configuration Tool User Parameters (Continued)

User Parameter	Description	Range	Description
Additional Delay Settings			
Do you wish to specify additional delay on the PLL outputs?	In addition to Fine Delay Adjustment in the feedback path, the user can specify additional delay on the PLL output ports.	Yes No	The delay contributed by the delay block can be fixed or controlled dynamically during FPGA operation. If fixed, it is necessary to provide a number (n) in the range 0-15 to specify the delay contributed to the feedback path. The delay for a setting 'n' is calculated as follows : FDA delay = (n+1)*0.15 ps, range of n = 0 to 15. *Note: This additional delay is applied on the output of single-port PLL and port A of two-port PLL Types.*
PLL Input/output Frequency			
Input Frequency (MHz)	Specify input frequency. Refer to the iCE40 Family Data Sheet for the input range.		
Output Frequency (MHz)	Specify desired output frequency. Refer the iCE40 Family Data Sheet for the output frequency range.		
Others			
Create a LOCK output port	A lock signal is provided to indicate that the PLL has locked on to the incoming signal. Lock asserts High to indicate that the PLL has achieved frequency lock with a good phase lock.		
Create a BYPASS port that will bypass the PLL reference clock to the PLL output port	A BYPASS signal is provided which both powers-down the PLL core and bypasses it such that the PLL output tracks the input reference frequency.		
Low Power Mode	A control is provided to dynamically put the PLL into a lower power mode through the iCEGate feature. The iCEGate feature latches the PLL output signal and prevents unnecessary toggling.	Enable latching of PLL clock (iCEGate)	Dynamically controls power by enabling the signal LATCHINPUTVALUE. Refer to the section Low Power Mode.
		Enable latching of PLL source clock	Default setting

1. Enabled when the Number of Global Networks to be Driven by the PLL Outputs option is set to '2'.

PLL Module Generator Output

The PLL module generator generates two HDL files:

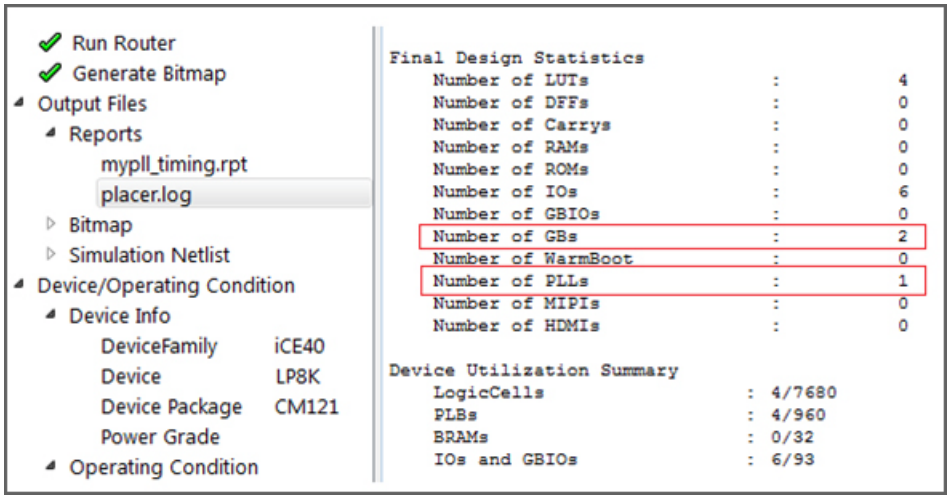
- <module_name>_inst.v
- <module_name>.v

The <module_name>_inst.v is the instantiation template to be used in the custom top level design. The <module_name>.v contains the PLL software macro with the required attributes and signal values, calculated based on the inputs to the GUI.

iCEcube2 Design Software Report File

The placer.log file (Final Design Statistics section) shows the use of PLLs and GBUFs (global buffers) along with other design elements of the iCE40 device. Note that when GBUF is instantiated in the RTL to connect to a PIO, an extra slice will be utilized for connection.

Figure 11. Report File Showing the Use of PLLs and Global Buffers



Hardware Design Considerations

PLL Placement Rules

- If any instance of PLL is placed in the location of the IO cell, then, an instance of SB_GB_IO cannot be placed in that particular IO cell.
- If an instance of ice40_PLL_CORE or ice40_PLL_2F_CORE is placed, an instance of SB_IO in “output-only” mode can be placed in the associated IO cell location.
- If an instance of ice40_PLL_PAD, ice40_PLL_2F_PAD, ice40_PLL_2_PAD is placed, the associated IO cell cannot be used by any SB_IO or SB_GB_IO.
- If an instance of ice40_PLL_2F_CORE, ice40_PLL_2F_PAD, ice40_PLL_2_PAD is placed, an instance of SB_IO in “output-only” mode can be placed in the right neighboring IO cell.

Analog Power Supply Filter for PLL

The iCE40 sysCLOCK PLL contains some analog blocks, On some devices, the PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL. On some devices with low pin count, the PLL is not available.

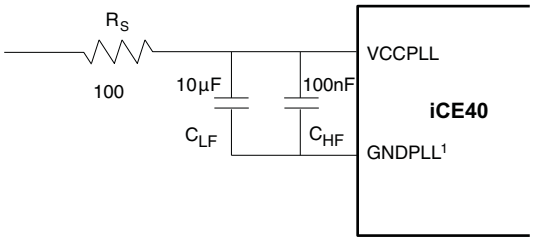
On devices with external power and ground for the PLL, an R-C filter as shown in Figure 12 is used as a power supply filter on the PLL power and ground pins. The series resistor (R_S) limits the voltage drop across the filter. A

high frequency non-electrolytic capacitor (C_{HF}) is placed in parallel with a lower frequency electrolytic capacitor (C_{LF}). C_{HF} is used to attenuate high frequency components while C_{LF} is used for low frequency cut-off.

Board layout around the high frequency capacitor and the path to the pads is critical. The PLL power (V_{CCPLL}) path must be a single wire from the FPGA pin to the high frequency capacitor (C_{HF}), then to the low frequency capacitor (C_{LF}), through the series resistor (R_S) and then to board power $V_{CC.}$ The distance from the FPGA pin to the high frequency capacitor should be as short as possible. Similarly, the PLL Ground (GNDPLL) path should be from the FPGA pin to the high frequency capacitor (C_{HF}) and then to the low frequency capacitor (C_{LF}), with the distance from the FPGA pin to the C_{HF} being as short as possible.

The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground. Figure 12 also includes sample values for the components that make up the PLL power supply filter.

Figure 12. Power Supply Filter for VCCPLL and GNDPLL



1. GNDPLL should not beconnected to the board's ground

Technical Support Assistance

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Revision History

Date	Version	Change Summary
March 2015	1.7	Updated Global Routing Resources section. Updated Table 2, Global Buffer Connections to a Programmable Logic Block to reflect Clock Enable for odd numbered buffers.
January 2015	1.6	Updated Introduction section. Updated Table 1, Number of PLLs in the iCE40 Device Family. Added iCE40 UltraLite devices.
		Updated Global Routing Resources section. — Updated Figure 1, High-drive, Low-skew, High-fanout Global Buffer Routing Resources. Added iCE40 UltraLite in figure label. — Added iCE40 UltraLite on On-chip Oscillator input source.
		Updated Signals section. Updated Table 5, PLL Attributes and Settings in PLL Macro. Changed DIVQ parameter value.
October 2014	1.5	Updated Table 1, Number of PLLs in the iCE40 Device Family. Removed UWG20 20-ball WLCSP.
June 2014	1.4	Added support for iCE40 Ultra.
		Updated Introduction section. Updated Table 1, Number of PLLs in the iCE40 Device Family.
		Updated Table 5, PLL Attributes and Settings in PLL Macro. Changed value for DIVQ parameter.
October 2013	01.3	Added support for iCE40LM
September 2013	01.2	Added PLL Placement Rules section.
		Updated Technical Support Assistance information.
February 2013	01.1	Updated range of DIVQ divider settings.
September 2012	01.0	Initial release.