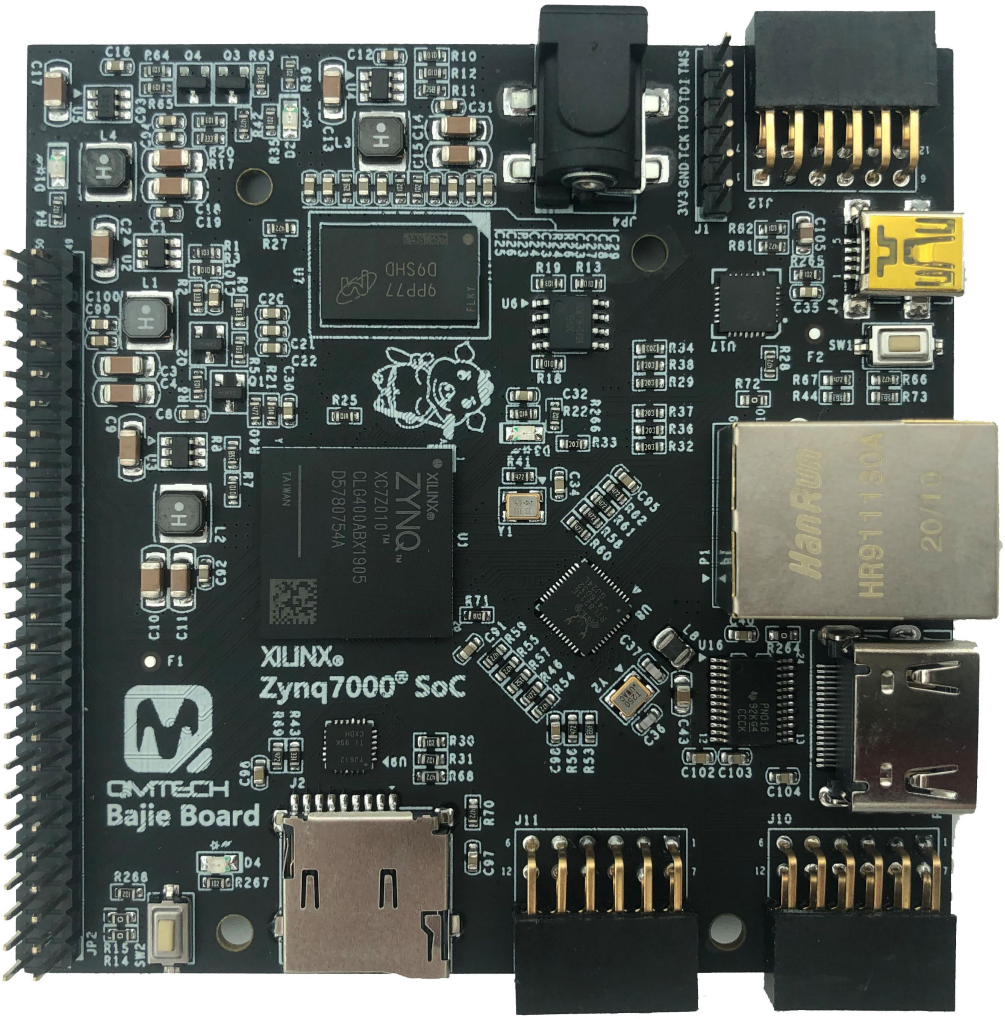
QMTECH ZYNQ7000 BAJIE BOARD

USER MANUAL



Preface

The QMTech® ZYNQ7000 Bajie Board uses Xilinx Zynq®-7000 device which integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of single-core Zynq-7000S and dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performance-per-watt, fully scalable SoC platform for your unique application requirements.

For more information, updates and useful links, please visit QMTECH Official Website:

http://www.chinaqmtech.com

Table of Contents

1. Introduction

1.1 Document Scope

This demo user manual introduces the QMTECH ZYNQ7000 Bajie Board and describes how to setup the development board running with environment Xilinx Vivado 2018.3 and application software Linux. Users may employee the PL side rich logic resource 28K Logic Cells for XC7Z010 to implement various applications. The development board also has 58 non-multiplexed PL IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the Bajie Board:

- On-Board SoC: XC7Z010-1CLG400C;
- On-Board PS side external crystal frequency: 33.333MHz;
- XC7Z010-1CLG400C has rich block RAM resource up to 2.1Mb;
- XC7Z010-1CLG400C has 28K logic cells;
- On-Board 512MB Micron DDR3, MT41K256M16TW-107:P;
- On-Board micro SD slot;
- On-Board power supply for FPGA by using TI TPS563201 wide input range DC/DC;
- On-Board one 50p and two Digilent PMOD compatible, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- On-Board RGMII ethernet interface connected to PS side by using RealTek chip RTL8211E-VL;
- One on-board user switch for PS logical reset;
- Two on-board user LEDs, one connected to PL and the other connected to PS;
- On-board HDMI display interface by using TI chip TPD12S016;
- On-Board JTAG interface, by using 6p, 2.54mm pitch header;
- PCB size is: 8.41cm x 8.41cm;
- Default power source for board is: 2A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

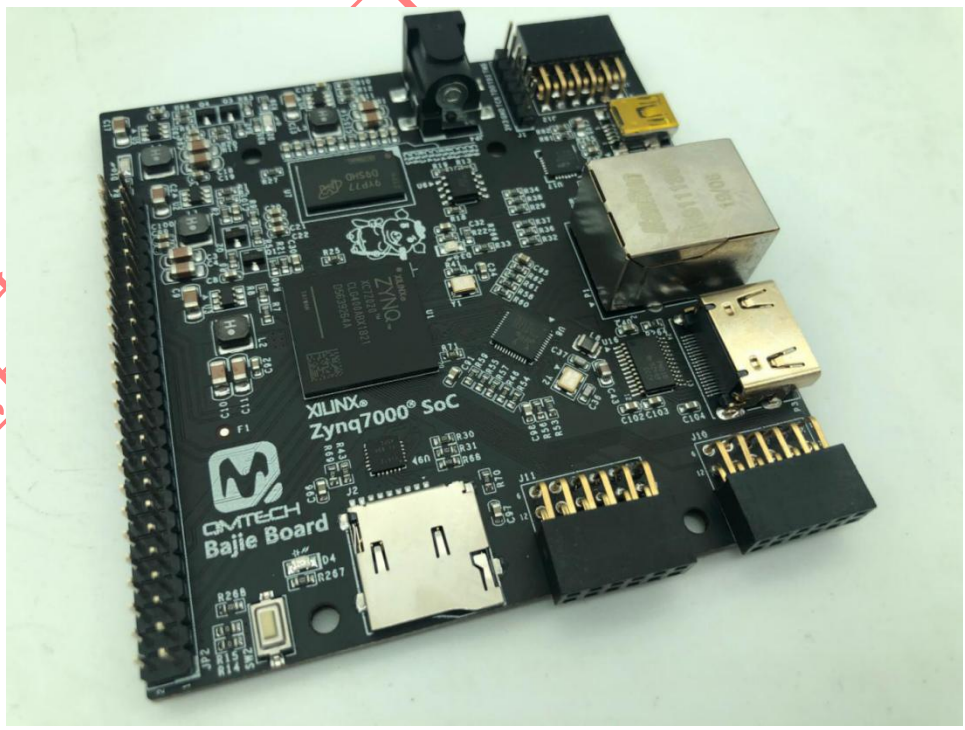


Figure 1-1. QMTECH ZYNQ XC7Z010 Bajie Board Overview

2. Getting Started

Below image shows the dimension of the QMTECH ZYNQ7000 Bajie Board: 8.41cm x 8.41cm. The unit in below image is millimeter(mm).

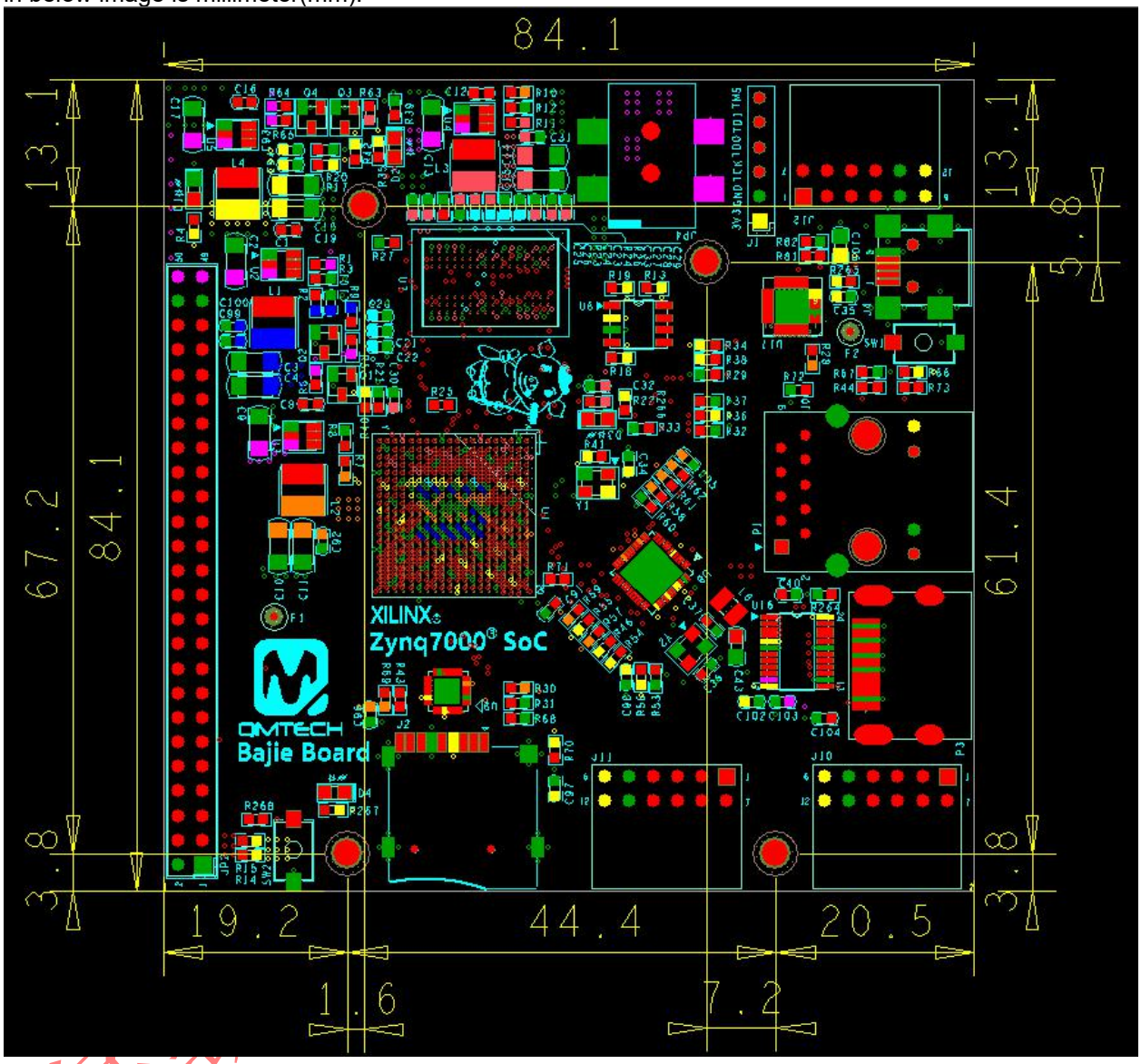


Figure 2-1. QMTECH ZYNQ7000 Bajie Board Dimension

2.1 Install Development Tools

The QMTECH ZYNQ7000 Bajie Board tool chain consists of Xilinx Vivado 2018.3, Xilinx USB platform cable, VMware virtual machine installed with Ubuntu 18.04, ZYNQ Bajie Board and 5V DC power supply. Below image shows the Xilinx Vivado 2018.3 development environment which could be downloaded from Xilinx office website:

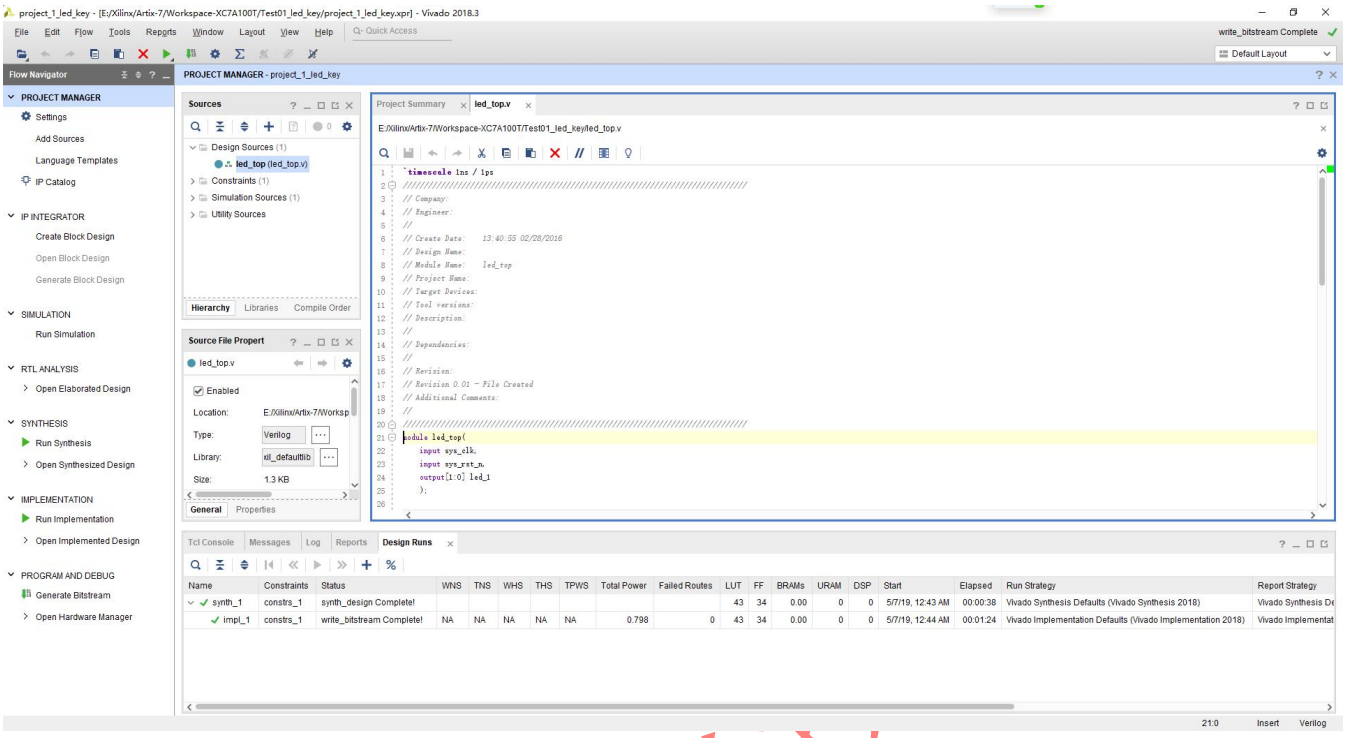


Figure 2-2. Vivado 2018.3

Below image shows the JTAG connection between Xilinx USB platform cable and ZYNQ7000 Bajie Board:

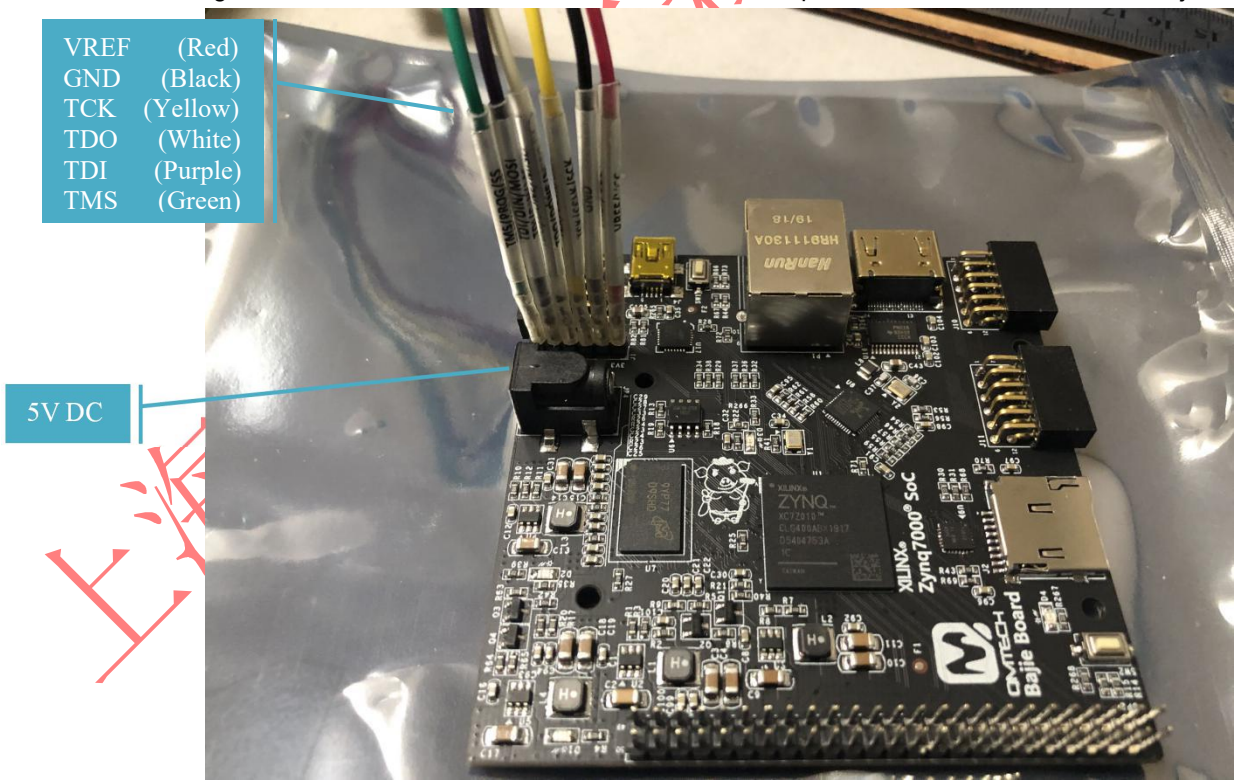


Figure 2-3. JTAG Connection and Power Supply

Below image shows the Ubuntu 18.04 OS:

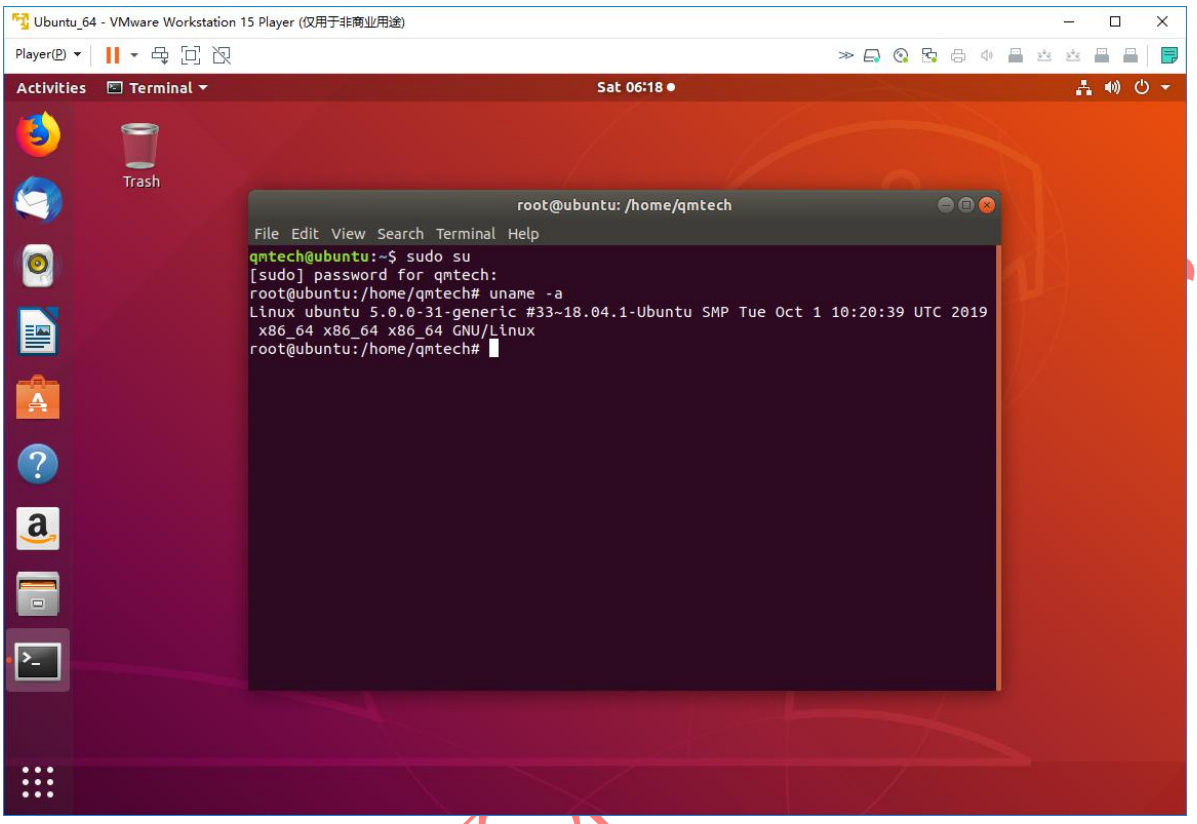


Figure 2-4. Ubuntu 18.04

2.2 QMTECH ZYNQ7000 Bajie Board Hardware Design

2.2.1 Zynq SoC Power Supply

The Bajie Board needs 5V DC input as power supply which could be directly injected from power header or the 50P header JP2. Users may refer to the hardware schematic for the detailed design. The on-board LED D1 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the PL banks' IO power level is 3.3V because bank power supply is 3.3V. However, BANK34 IO's power level could be changed according to detailed custom requirement. There are two 0 ohm resisters could be removed: R14/R15, and instead the BANK34's power supply could be injected from 50P female header JP2. Detailed design refers to hardware schematic.

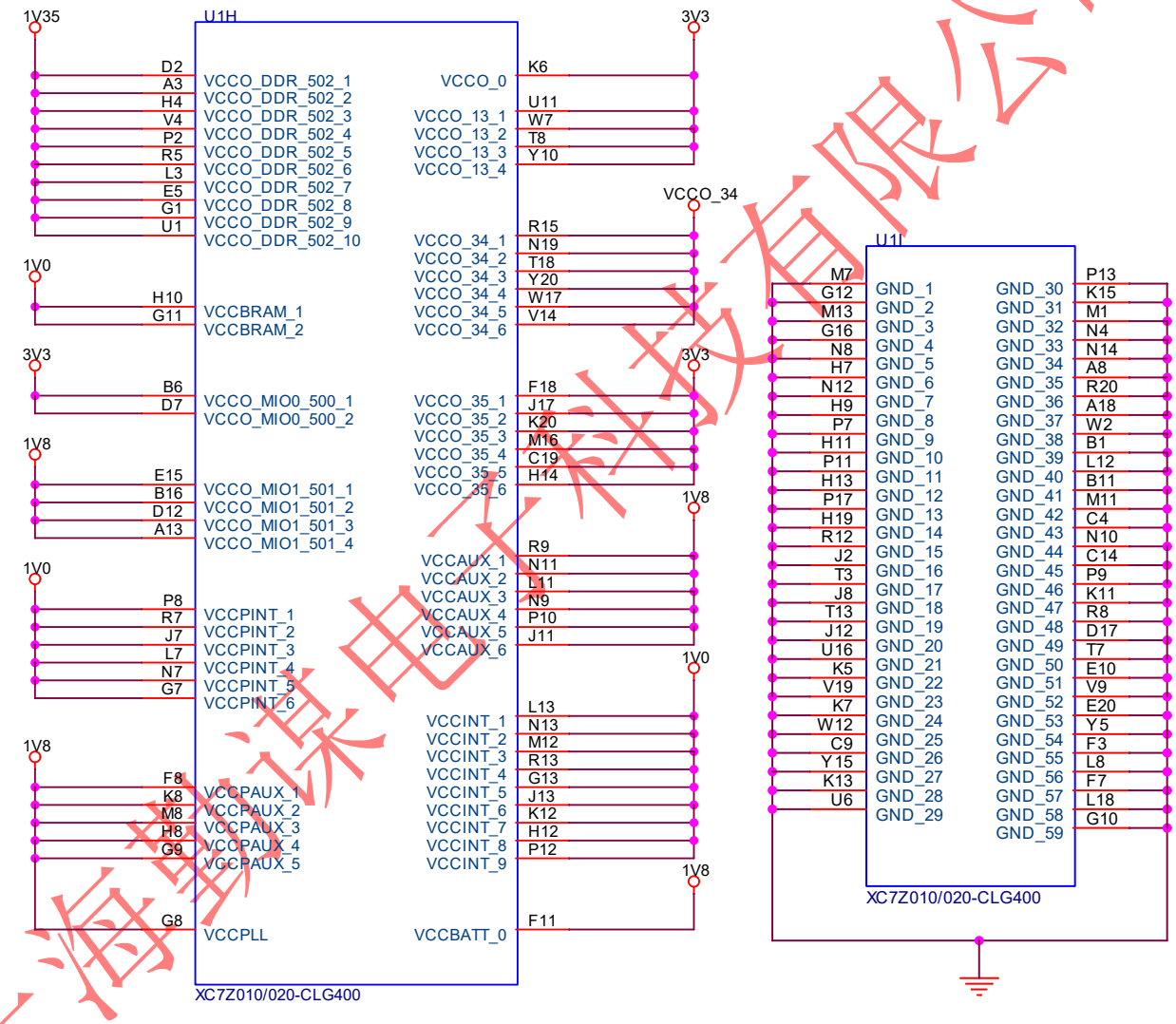


Figure 2-5. Power Supply for the FPGA

2.2.1 3.3V Power Supply

The XC7Z010's power supply are all using high efficiency DC/DC chip TPS563201 provided by TI. The TPS563201 supports wide voltage input range from 4.5V to 17V. In normal use case, 5V DC power supply is suggested to be applied on the board. The power on sequence for the Zynq SoC is 1.0V → 1.8 → 1.35V → 3.3V. Below image shows the TPS563201 hardware design for these power supplies.

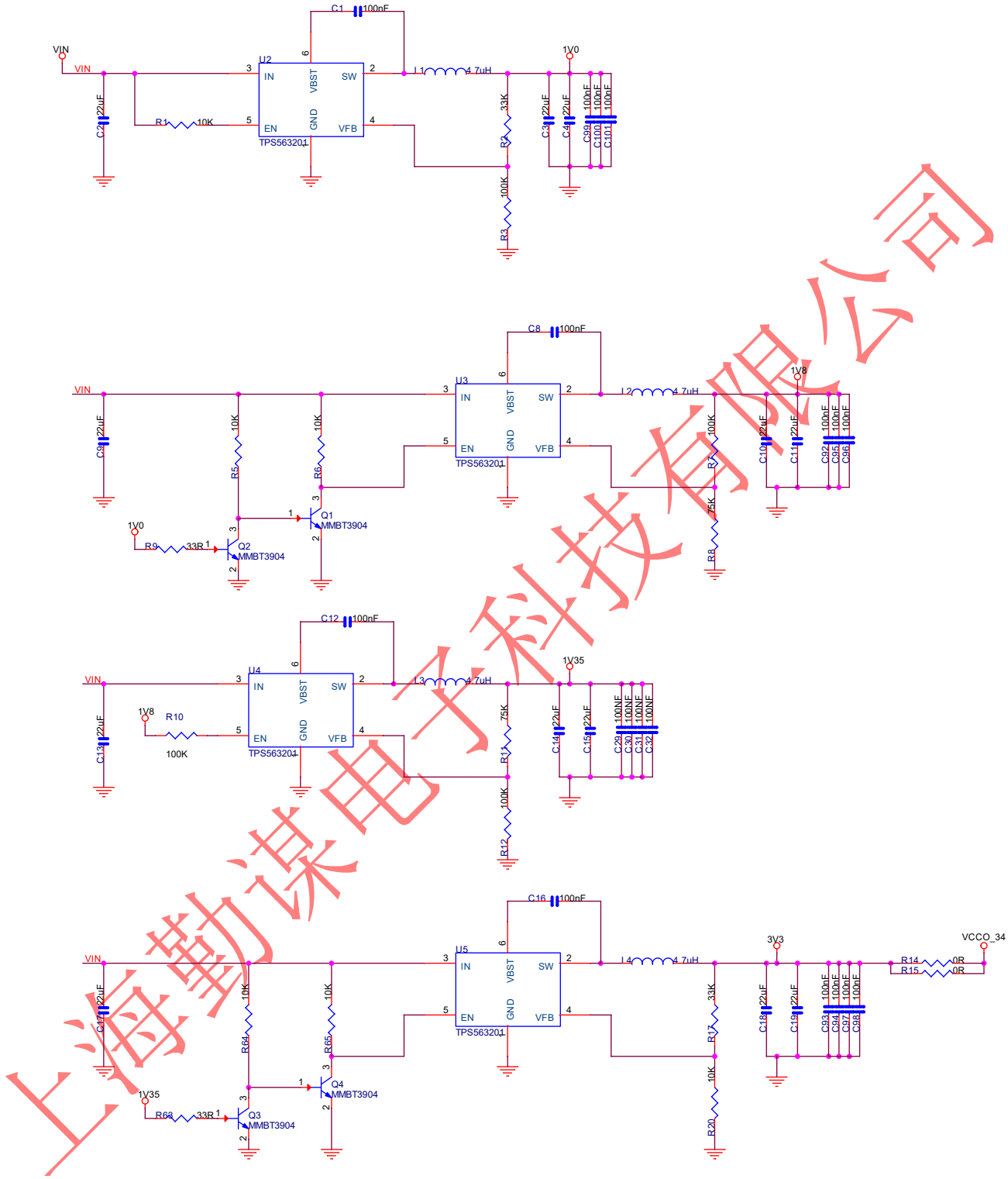


Figure 2-6. TPS563201 Hardware Design

2.2.2 Boot Mode

In default, the PS side ARM core boots from external SD card through SDIO 0 interface, detailed hardware design is shown in below figure.

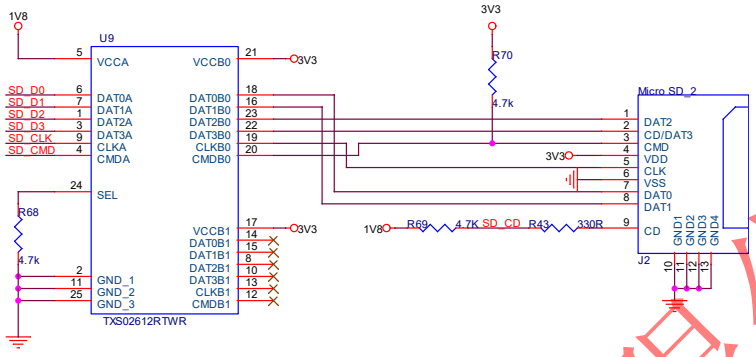


Figure 2-7. SD Card

The boot sequence setting MIO[2:8] is configured as below image.

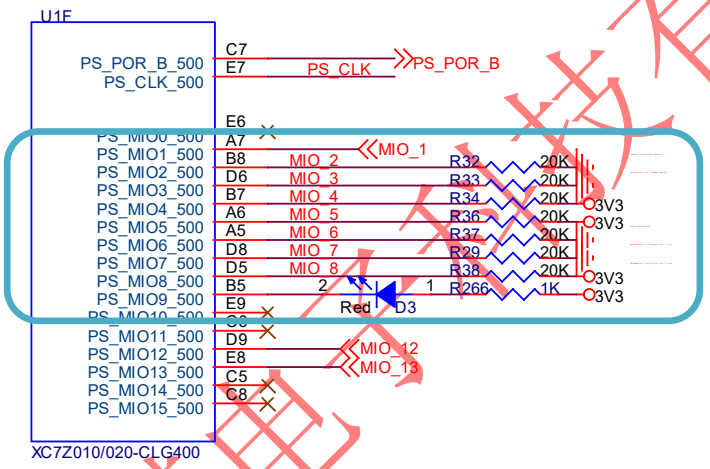


Figure 2-8. MIO[2:8] Hardware Settings

Below image copied from ug585-Zynq-7000-TRM.pdf shows the detailed hardware settings for the boot mode:

Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common(1)				0	0	0	JTAG Chain Routing(2) 0: Cascade mode 1: Independent mode
NOR Boot(3)				0	0	1	
NAND				0	1	0	
Quad-SPI(3)				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage(4)							
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

Figure 2-9. MIO[2:8] Hardware Settings

2.2.3 System Clock

The PS side has system clock frequency 33.333MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

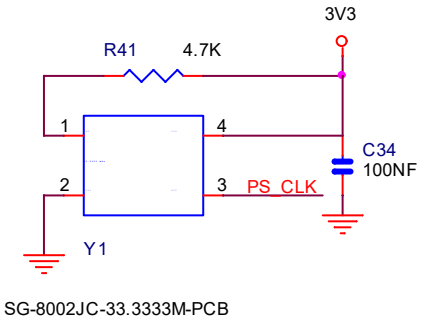
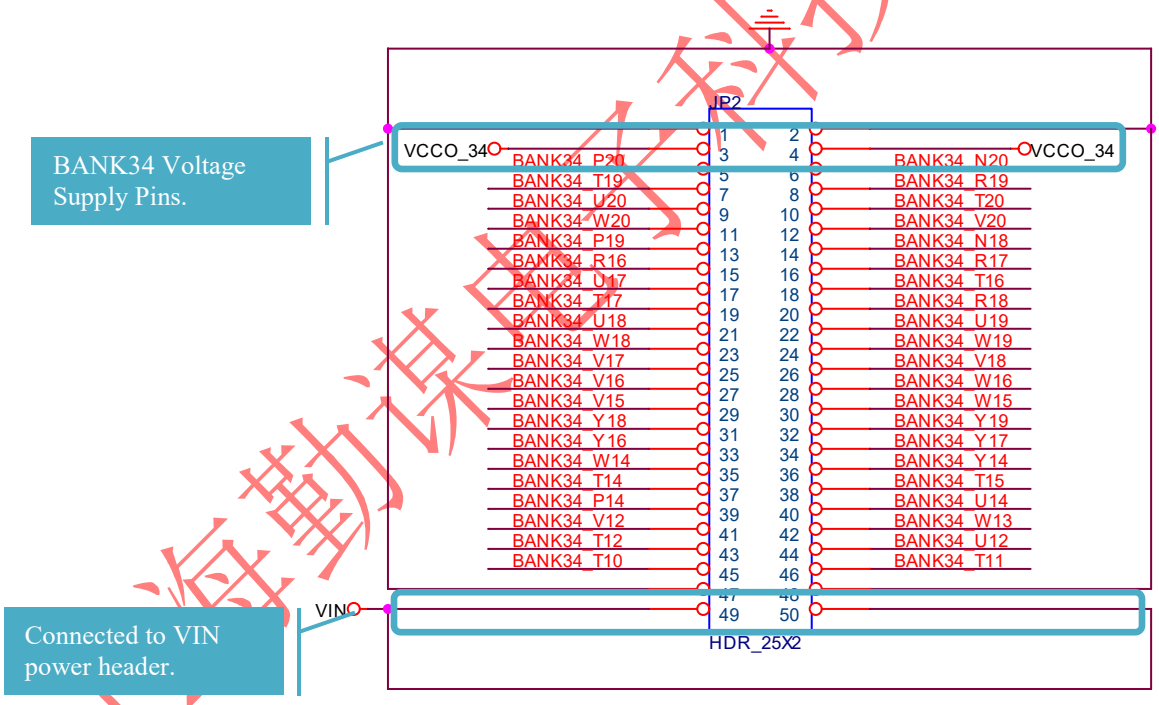


Figure 2-10. 50MHz System Clock

2.2.4 User Extension IOs

The Bajie Board has one 50P 2.54mm pitch header which could be used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc. All these IOs are extended from BANK34, PL IOs.



The Bajie Board also has three 12P 2.54mm pitch headers which extend some PS IOs and some PL IOs from BANK35. The 12P headers' IO definitions are compatible with Digilent's PMOD interface.

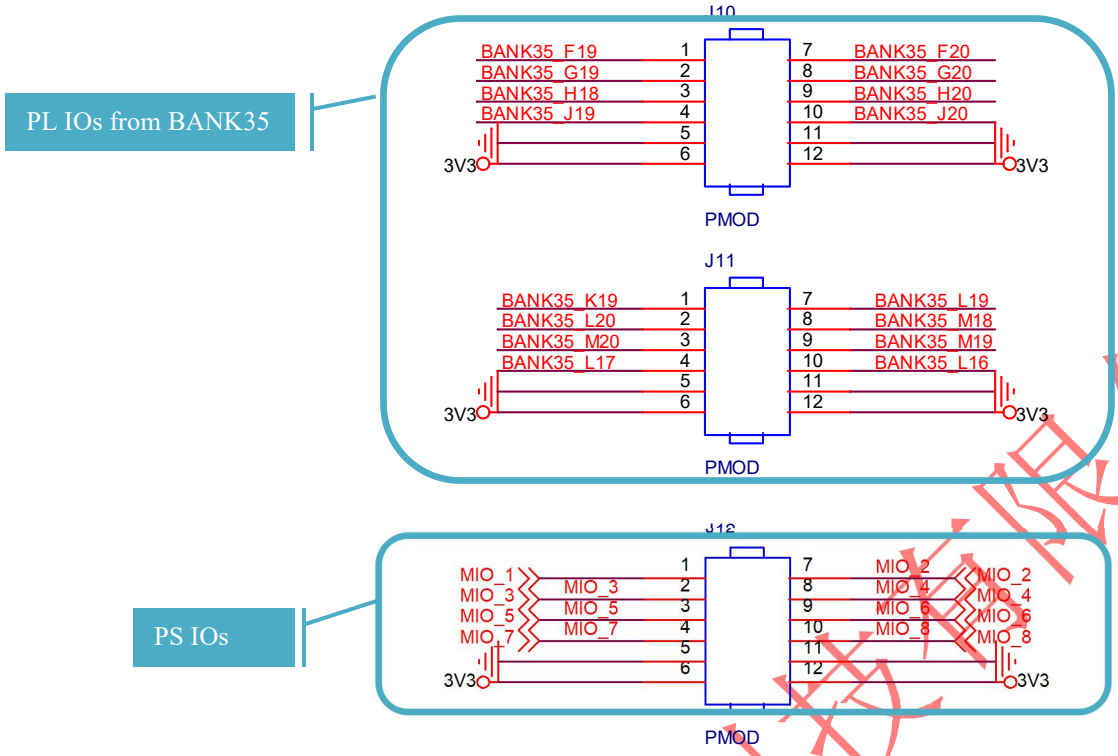


Figure 2-11. Extension IO

2.2.5 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

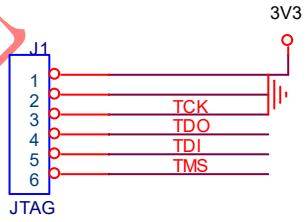


Figure 2-12. JTAG Port

2.2.6 User LEDs

Below image shows two user LEDs and 3.3V power supply indicator:

Figure 2-13. 3.3V Power Supply Status Indicator

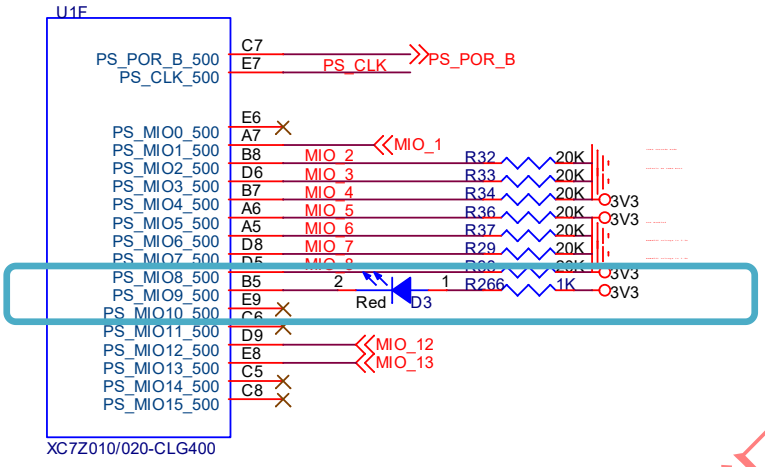


Figure 2-14. LED Connected to PS MIO[9]

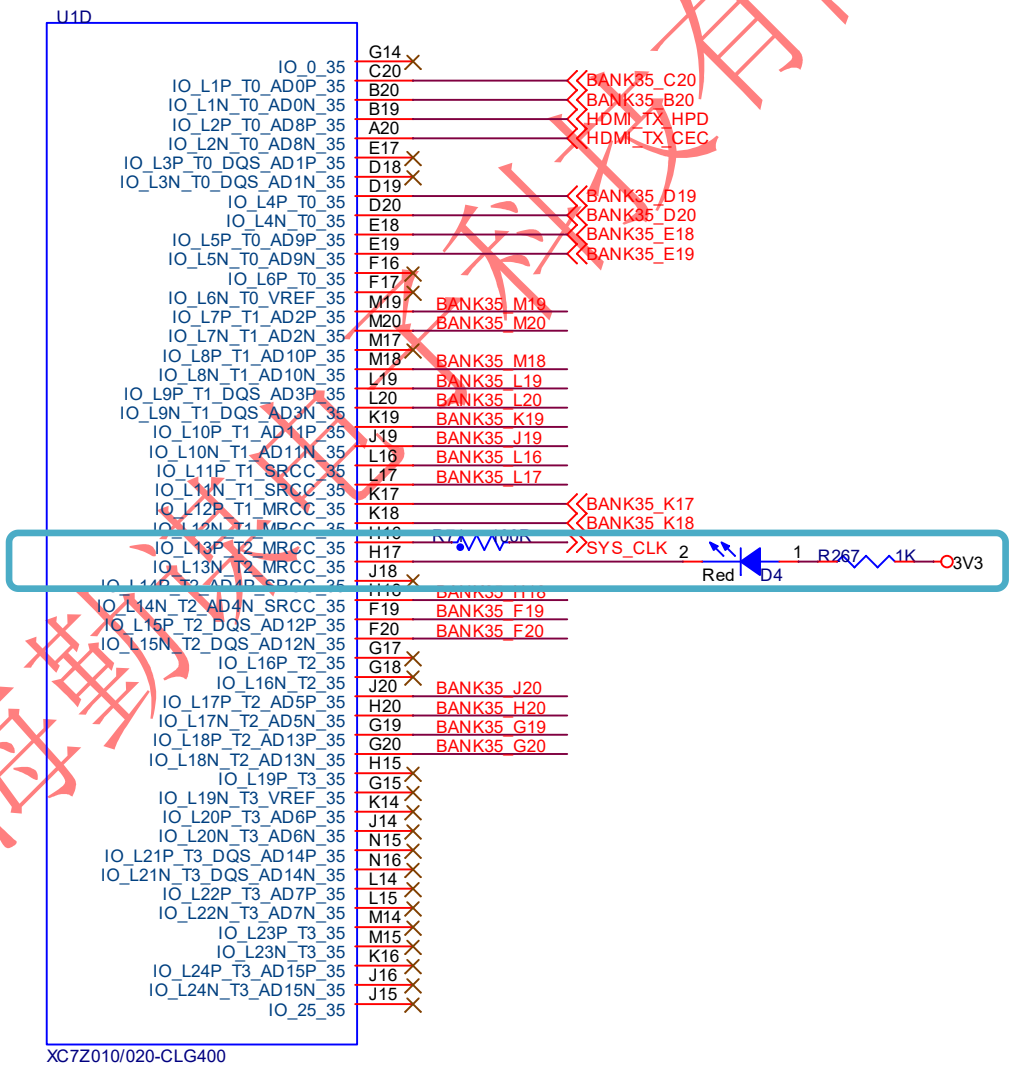


Figure 2-15. LED Connected to PL PIN H17

The LED D2 will be turned on after the PL successfully loading configuration file from SD card during power on stage. In this case, LED D2 could be used as PL loading status indicator.

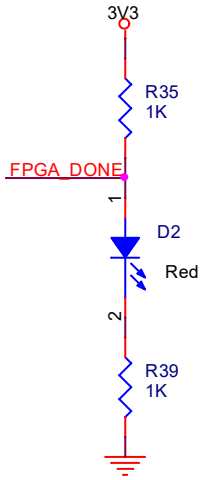


Figure 2-16. FPGA_DONE Status Indicator

2.2.7 User Keys

Below image shows the PS_RST reset key:

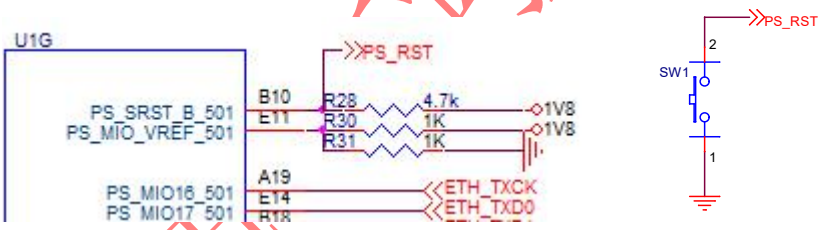


Figure 2-17. PS_SRST Key

Below image shows the user key connected to PL side:

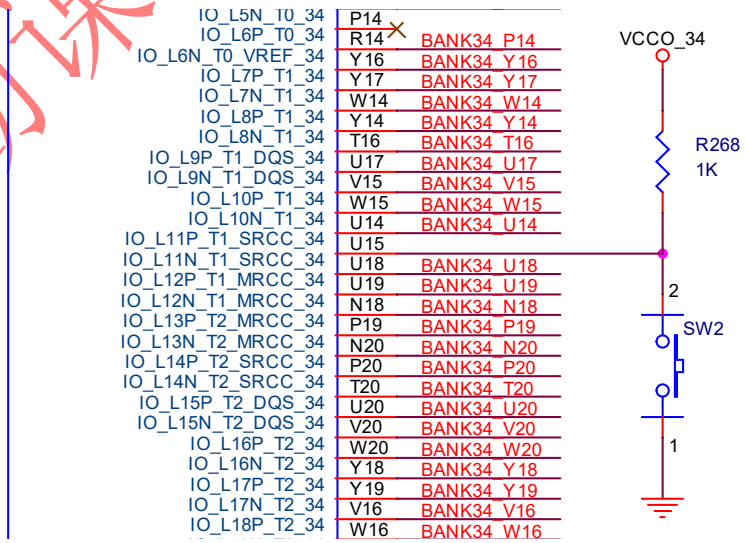


Figure 2-18. PL Side User Key

2.2.8 DDR3 Memory

The Bajie Board has on board 16bit width data bus, 512MB memory size DDR3 MT41K256M16TW-107:P provided by Micron. Below image shows the detailed hardware design:

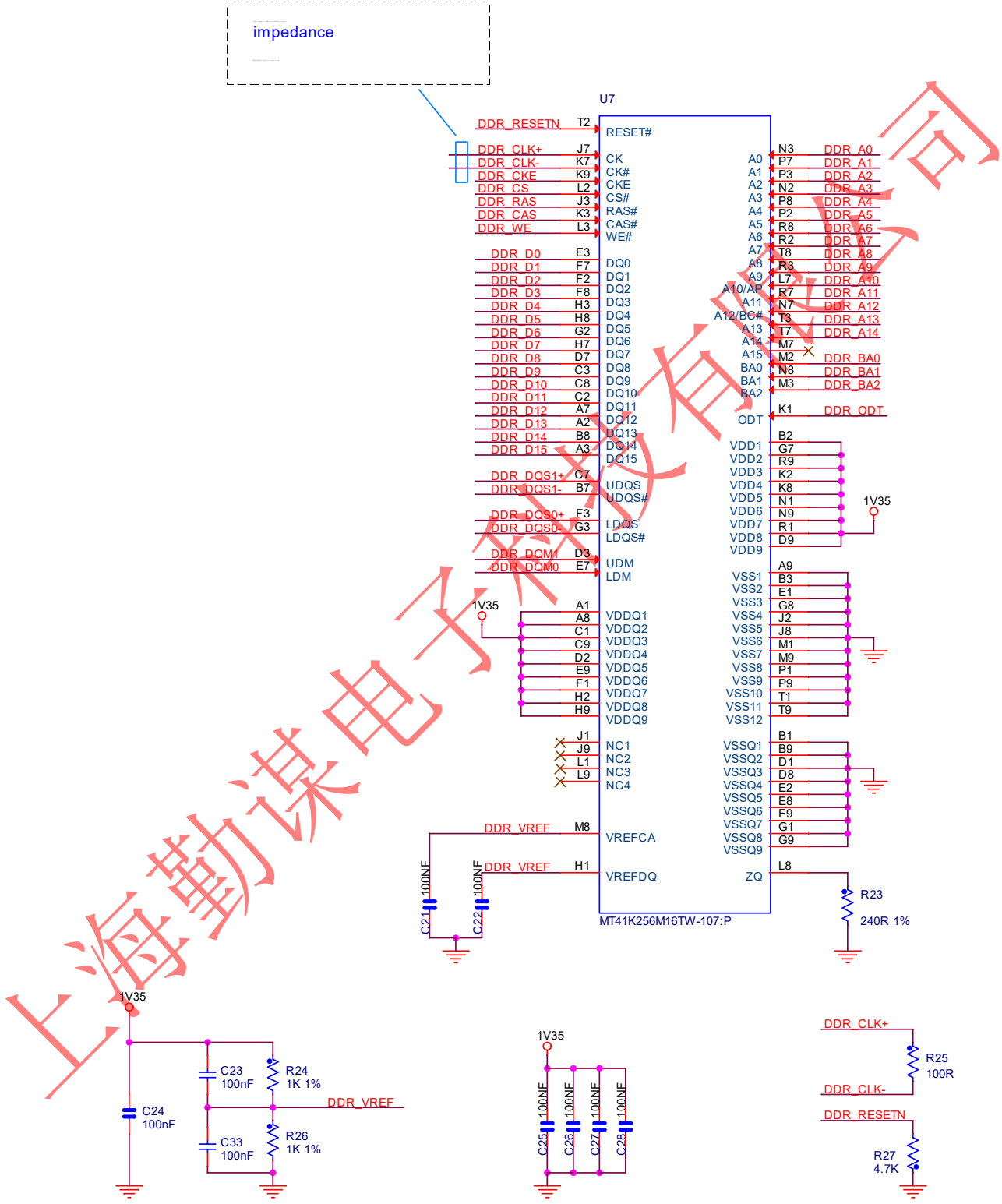


Figure 2-19. DDR3 Memory

2.2.9 RGMII Ethernet Interface

The Bajie Board provides RGMII ethernet interface by using RealTek's RTL8211E-VL. The RTL8211E-VL is connected to ZYNQ SoC's PS side. In default hardware design, it is working under 1000Mbps, RGMII mode. Detailed hardware design refers to below image.

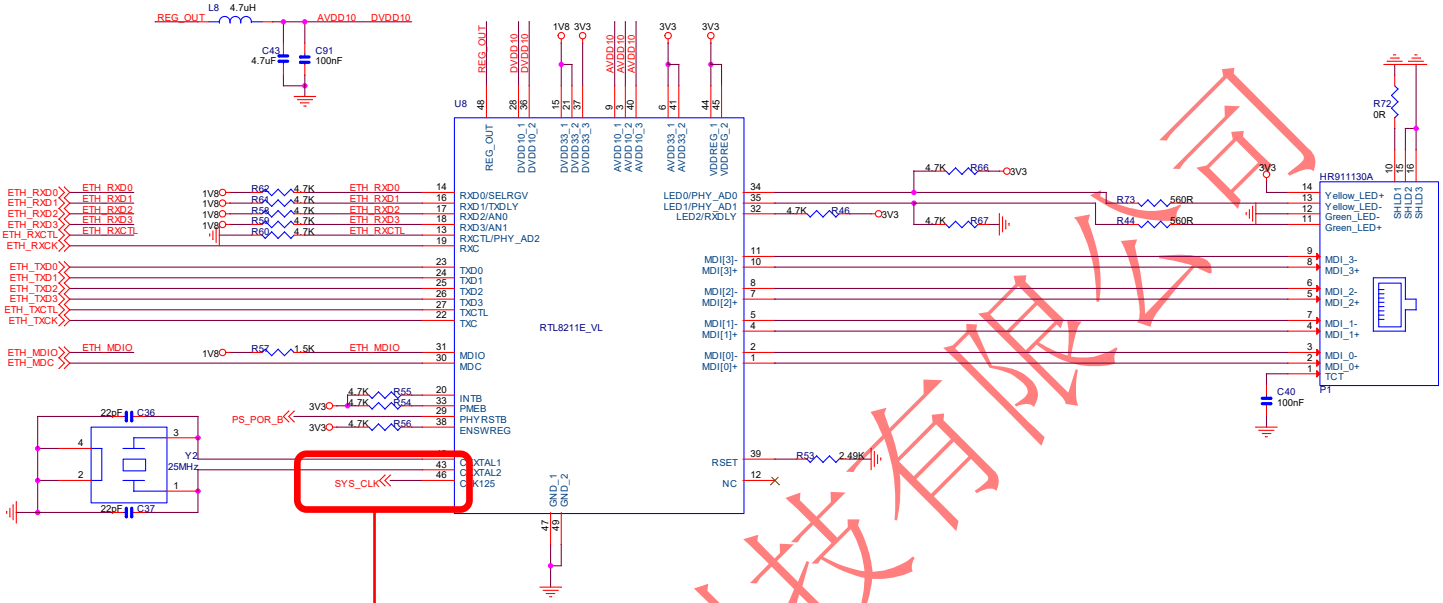
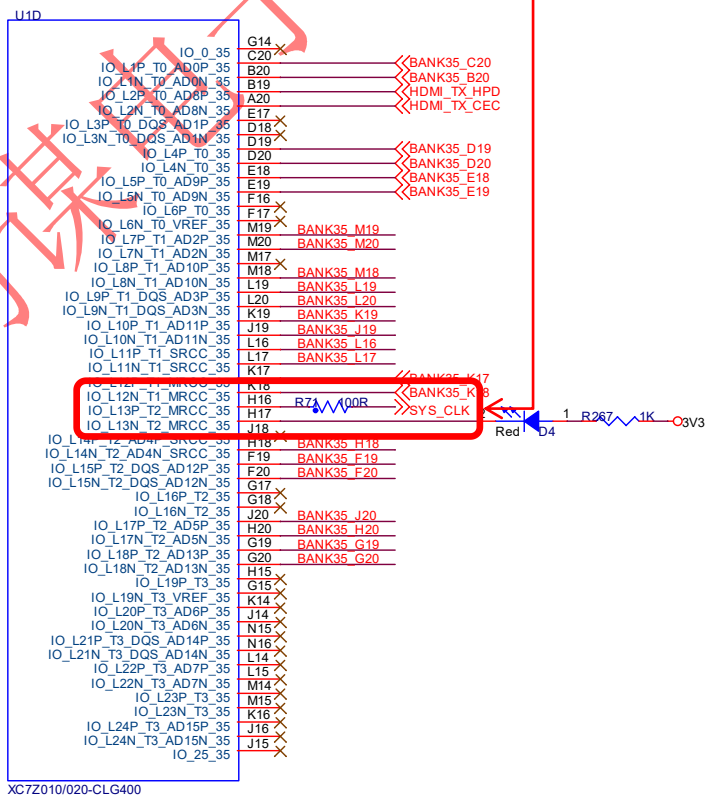


Figure 2-20. RGMII Ethernet

The RTL8211 generates 125MHz clock and then routed to the PL's MRCC pin. The SYS_CLK could be used as PL side's global clock.



2.2.10 HDMI Display Interface

The Bajie Board provides HDMI interface by using TI's TPD12S016 chip, which is a single-chip High Definition Multimedia Interface (HDMI) device with auto-direction sensing I2C voltage level shift buffers, a load switch, and integrated low capacitance high-speed electrostatic discharge (ESD) transient voltage suppression (TVS) protection diodes. Below image shows the hardware design.

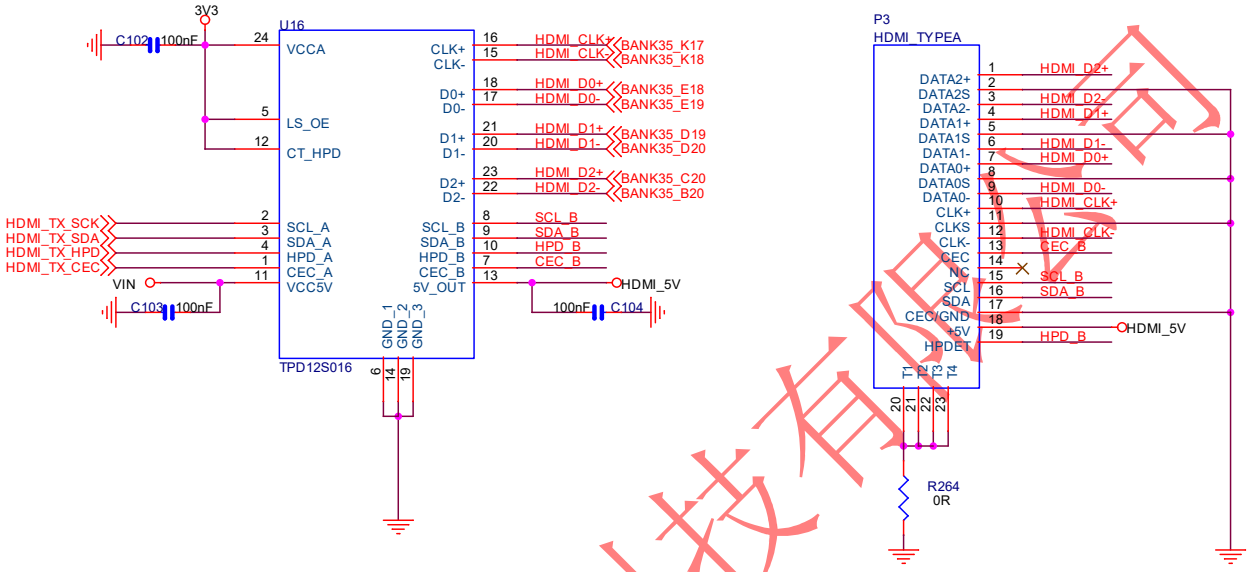


Figure 2-21. HDMI Interface

2.2.11 USB to UART Interface

The CP2102N is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102N includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102N on the Bajie board.

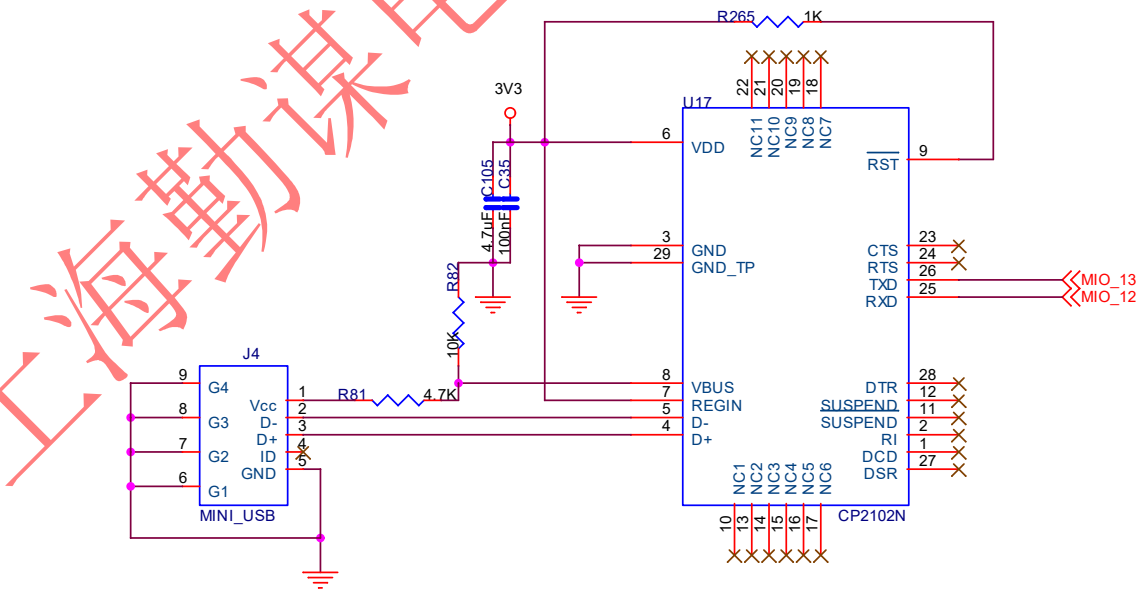


Figure 2-22. CP2102 Hardware Design

3. Reference

[1] ug585-Zynq-7000-TRM.pdf
[2] ds187-XC7Z010-XC7Z010-Data-Sheet.pdf
[3] ug865-Zynq-7000-Pkg-Pinout.pdf
[4] MT41K256M16TW-107:P.pdf
[5] tps563201.pdf
[6] RTL8211E.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	01/11/2020	Initial Version.
1.0	03/11/2020	V1.0 Formal Release.