

USBC1
USB3.1C16PFSMT

B1 GND A12

B4 VBUS CC2 B5 VBUS SBU1 A9 VBUS A8

B6 D+ DN1 A7 D- A6

B7 D- DP1 A5 D+ CC1 A4

B8 SBU2 CC1 A4

B9 VBUS VBUS

B12 GND A1

R6 5.1k

R5 5.1k

GND

The diagram illustrates a hardware modification for a serial port. A single VCCIO pin is connected to four resistors, each labeled RN1 10K. These resistors are connected in parallel to the TX, RX, CTS, and RTS pins of a serial port connector. This setup provides a constant voltage to these pins, which is necessary for the correct operation of the serial port in certain modes.

Pinout diagram for J1 HDR-M-2.54_1x5 connector:

- Pin 1: VCC
- Pin 2: VCCIO
- Pin 3: RX
- Pin 4: TX
- Pin 5: GND

A circuit diagram showing two capacitors, C2 and C3, connected in parallel. The top terminal of the parallel combination is connected to VCC, and the bottom terminal is connected to GND. Capacitor C2 has a value of 100nF, and capacitor C3 has a value of 4.7uF. The capacitors are represented by two parallel lines of different lengths.

[illegible]

Note:
Internal regulator has max current of 50mA @ 3.3V.
Remove R7 on circuit board if using external voltage regulator.
This will prevent the chip's regulator from competing with the external one.
The external regulator must output 1.8-3.3V to power the chip.

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