EE 3220 – System-on-Chip Design – 2021/22 Spring

Assignment 3 – Due date: April 15 (Friday) – 23:59pm

Submission method – Canvas online assignment collection box

Name: _____

Date: _____

Student ID: _____ **Mark: _____**

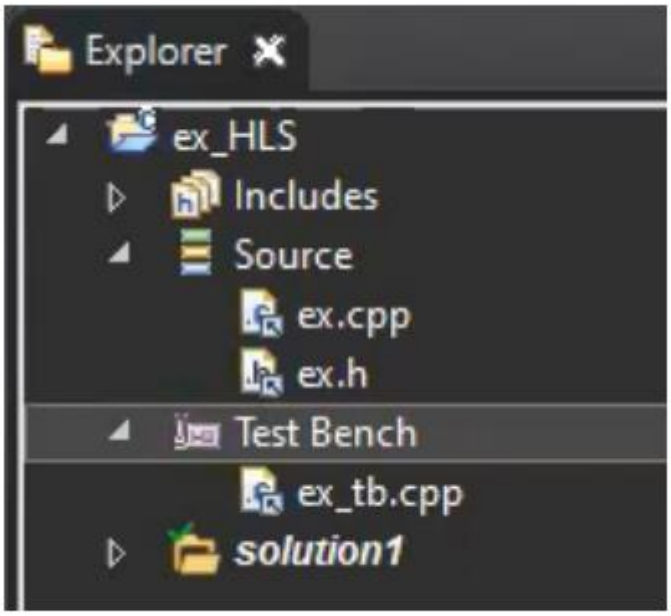
Submission guidelines:

- Please prepare your assignment in "PDF" format. (1%)
- Please rename your file to "EE3220 – assignment 3 – studentID.pdf". (1%)
- For late submission, 10% deduction per day.

Question: Please review the tutorial 9 and use Vitis HLS to design a new IP of arithmetic logic unit based on C code. And submit a report to record relative steps.

a. For the requirements of the new IP are shown in following:

1. The new IP should be named as ALU.
2. Please make sure that you have created the files similar with Tutorial 9 as follows:

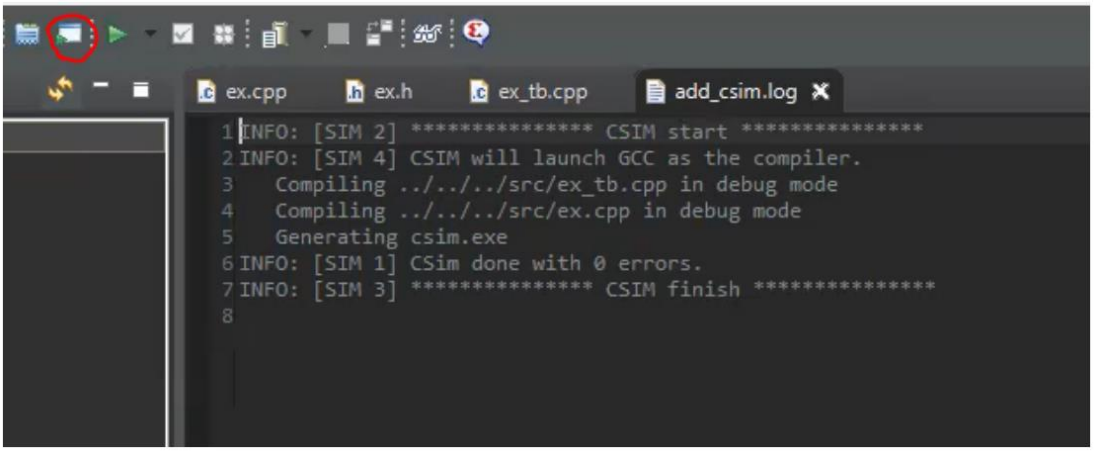


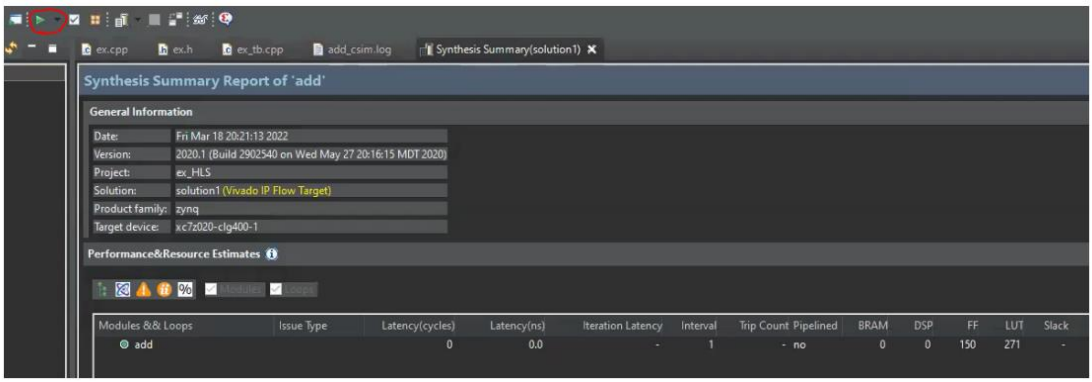
3. It should contain at least **2 functions of arithmetic add and subtract,** please revise your code in relative file.

4. Please follow the steps in tutorial 9 carefully and realize “Run C Simulation, C Synthesis, C/RTL Cosimulation”

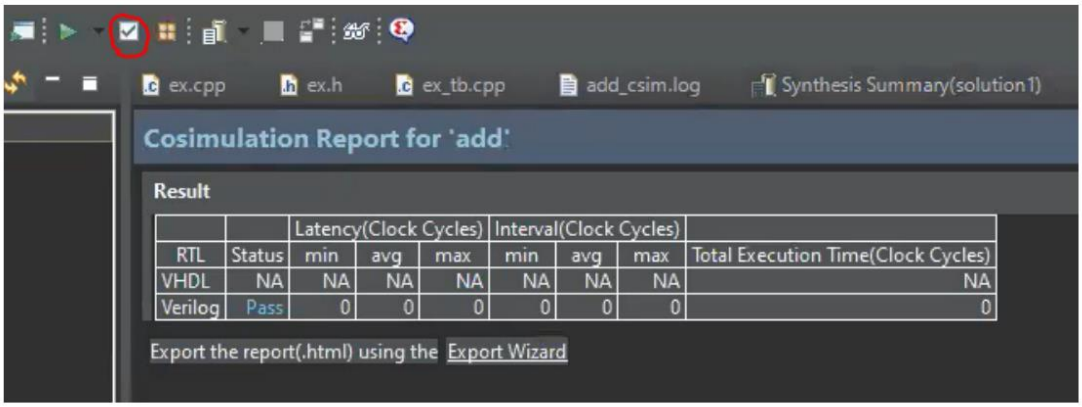
b. For the assignment you are going to submit, please include your results with codes, figures, and HLS solutions in your assignment and submit a report. In the report, you can refer to the following instructions:

1. Please show your codes in the report and put them in appendix at last of your assignment, to show that you have successfully **designed ALU and revised header file.**
2. Please show that you have finished relative steps, **including Run C Simulation, C Synthesis, C/RTL Cosimulation in figures as following:**





3. Please show that you have successfully finished the **Cosimulation report as the HLS solutions.** For example some results just like the following figure.



4. After finishing the previous steps, what do you learn from HLS? What are the advantages of HLS compared with VHDL in Vivado? Please make an explanation based on the experience from learning tutorials.

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