EE 2004
Week 2 Tutorial
Solution

1. State the three main parts of a digital computer.
   CPU, Memory, IO

2. List the three components inside a CPU.
   ALU, Registers, Control Unit

3. List the three bus types present in every CPU.

   Data Bus, Address Bus, Control Bus

4. Describe the sequence of signals that occurs on the address bus, the control bus, and the data bus when a microcomputer fetches an instruction.

   Fetching is just a read operation from program memory. For the sequences of read operation, i) CPU places address on address bus ii) CPU places control command to control bus (with read & memory request) iii) memory place data to data bus.

5. Instruction processing consists of two steps: fetching and execution. Answer the following two questions:

   (a) List the three steps that are performed during execution.

   Please see p.33 of Chapter 1.
   1. The control unit decodes the instruction and move data to ALU.
   2. ALU executes the instruction.
   3. *ALU stores the result in memory.*

   (b) Suppose that the program and data memories are separated as in Harvard architecture. For the fetching stage, which memory does the CPU need access? How about the execution stage?

   Fetching needs access of the program memory. Execution needs access of the data memory.

6. Answer the following questions:
   (a) How many nibbles are 16 bits? 16/4 = 4
   (b) How many bytes are 32 bits? 32/8 = 4
   (c) If a word is defined as 16 bits, how many words is a 64-bit data item? 64/16 = 4
   (d) What is the exact value (in decimal) of 1 meg (M)? 2^{20}
   (e) How many K is 1 meg (M)? $2^{20}/2^{10} = 2^{10}$K
   (f) What is the value (in decimal) of 1 giga (G)? 2^{30}
   (g) How many K is 1 giga (G)? $2^{30}/2^{10} = 2^{20}$K

(h) How many meg is 1 giga (G)? $2^{30}/2^{20} = 2^{10}$M

(i) If a given computer has a total of 8 megabytes of memory, how many bytes (in decimal) is this? How many kilobytes is this?
$8x2^{20}$ bytes = $8x2^{10}x2^{10}$bytes = $8x2^{10}$KB.

7. A given mass storage device such as a hard disk can store 2 gigabytes of information. Assuming that each page of text has 25 rows and each row has 80 columns of ASCII characters (each character = 1 byte), approximately how many pages of information can this disk store?

1 million pages

8. Assume each memory location stores a byte. In a computer, memory locations 10000H to 9FFFFH are available for user. The first location is 10000H and the last location is 9FFFFH. Calculate the following:
(a) The total number of bytes available (in decimal)
(b) The total number of kilobytes (in decimal)

(a) 589824 bytes
(b) 576 kbytes

9. A given computer has a 32-bit data bus. What is the largest unsigned number that can be carried into the CPU at a time?

2^{32} - 1 or 4294967295

10. The data bus widths of several computers are listed below. For each computer, list the maximum unsigned value that can be brought into the CPU at a time (in hex and in decimal).

(a) Apple 2 with an 8-bit data bus
(b) IBM PC with a 16-bit data bus
(c) IBM PC with a 32-bit data bus
(d) Cray computer with a 64-bit data bus

(a) FFh, 2^8 – 1= 255
(b) FFFFh, 2^{16} - 1 = 65535
(c) FFFF FFFFh, 2^{32} - 1 = 4294967295
(d) FFFF FFFF FFFF FFFFh, 2^{64} – 1 = 18 446 744 073 709 551 615

11. Assuming that each memory location stores a byte, find the total amount of memory, in the units requested, for each of the following CPUs, given the size of the address buses.

(a) 16-bit address bus (in K)
(b) 24-bit address bus (in megabytes)
(c) 32-bit address bus (in megabytes and gigabytes)
(d) 48-bit address bus (in gigabytes, and terabytes)

(a) 64K $2^{10} = 1k$; $2^{16} = 2^6 \times 2^{10} = 64k$
(b) 16M $2^{20}=1M$; $2^{24} = 1M \times 2^4 = 16M$

(c) 4096 M, 4G $2^{32} = 2^{20} \times 2^{12} = 1M \times 4096 = 2^{30} \times 2^{2} = 1G \times 4$

(d) 262144 G, 256 T $2^{48} = 2^{30} \times 2^{18} = 1G \times 262144 = 2^{40} \times 256 = 1T \times 256$

12. Consider data bus and address bus, which is unidirectional and which is bidirectional?

Data bus is bidirectional. Address bus is unidirectional.

13. Which register of the CPU holds the address of the instruction to be fetched?

PC (Program Counter)

14. Which section of the CPU is responsible for performing addition?

ALU

15. Is microprocessor or microcontroller more suitable to the von Neumann architecture? Why?

Microprocessor is more suitable to the von Neumann architecture. Program and data memories are implemented external to the CPU. Address and data bus wires need to be longer. Separate buses for data and code as required in Harvard architecture would make the microprocessor system large and expensive.

16. Is microprocessor or microcontroller more suitable to the Harvard architecture? Why?

Microcontroller is more suitable to the Harvard architecture. Program and data memories in microcontrollers are implemented in an IC chip. Distance between ROM and RAM is on the micron scale. Thus, it is not expensive to implement separate data and program buses in a microcontroller. In addition, data and program memory can be accessed simultaneously to allow pipelining.