BAUD rate CONtrol register

Auto-BauD OVerFlow [7] ABDOVF (R/W 0)	ReCeive IDLe [6] RCIDL (R/W 0)	RX DaTa Polarity [5] RXDPT (R/W 0)	TX ClocK Polarity [4] TXCKP (R/W 0)	Baud Rate Generator 16-bit [3] BRG16 (R/W 0)	---- [2] (R 0)	Wake-Up Enable [1] WUE (R/W 0)	Auto Baud-Rate ENable [0] ABDEN (R/W 0)

File h'FB8' **BAUDCON**

SPBRGH File h'FB0' X_H

SPBRG File h'FAF' X_L

Fosc/[64(X+1)]

Serial Port Baud Rate Generator

Fosc

f/4   f/4   0   0

Clock

Transmit shift register

TranSmit data REGister

File h'FAD' **TXREG**

Data out   RC6/TX

Receive Data pipeline

Receive shift register

ReCeive data REGister

File h'FAE' **RCREG**

Data in   RC7/RX

Serial Data
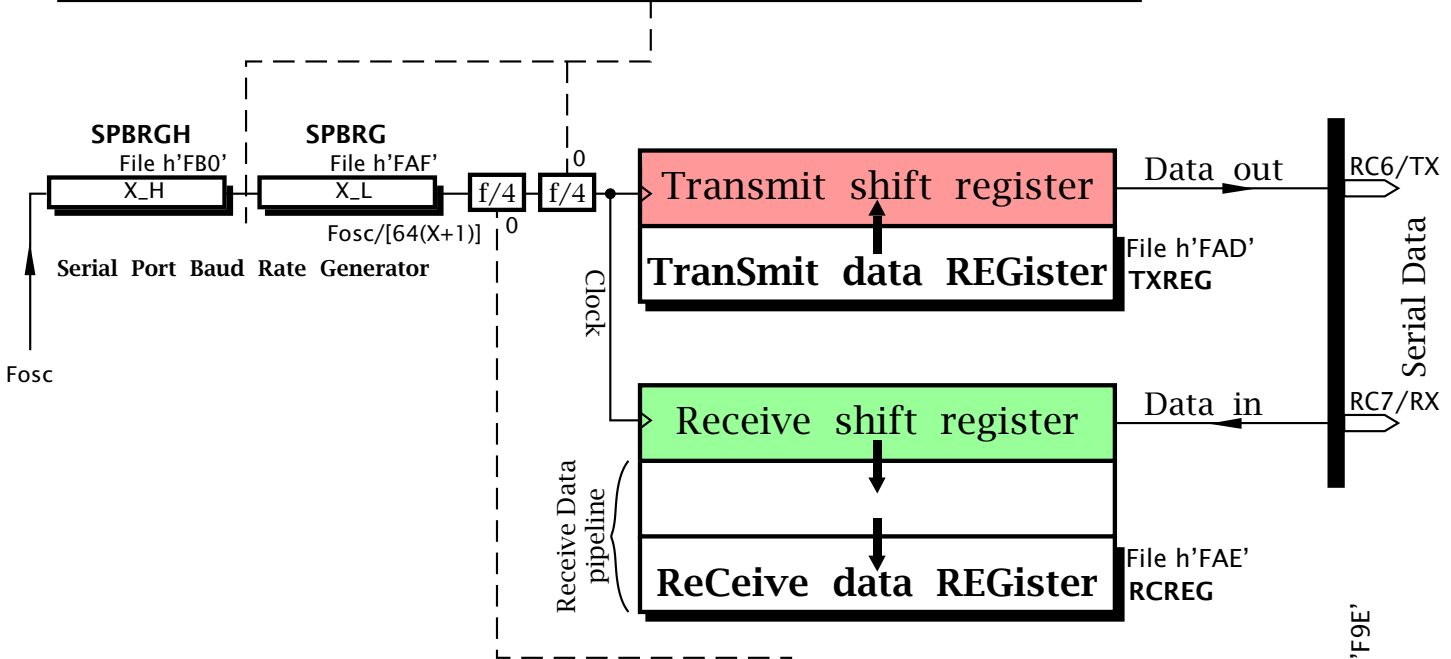
TranSmit STAtus and control register

X [7] (R/W 0)	Transmit data length 9-bit [6] TX9 (R/W 0)	Transmit ENable [5] TXEN (R/W 0)	0 [4] SYNC (R/W 0)	SEND Break [3] SENDB (R/W 0)	Baud Rate Generator High speed [2] BRGH (R/W 0)	TRansMiT shift reg empty [1] TRMT (R 1)	TX Data bit 9 [0] TX9D (R/W 0)

File h'FAC' **TXSTA**

ReCeive STAtus and control register

Serial Port ENable [7] SPEN (R/W 0)	Receive data length 9-bit [6] RX9 (R/W 0)	X [5] (R/W 0)	Continuous Receive ENable [4] CREN (R/W 0)	ADdress Detect ENable [3] ADDEN (R/W 0)	Framing ERRor [2] FERR (R 0)	Overflow ERRor [1] OERR (R 0)	RX Data bit 9 [0] RX9D (R X)

File h'FAB' **RCSTA**

File h'F9E' **PIR1**

TX buffer empty [4] TXIF (R/W 0)	RX register full [5] RCIF (R/W 0)