EE 2004
Week 12 Homework
Solution

1. Suppose that there is a 12-bit ADC with $V_{ref+} = 4V$ and $V_{ref-} = 1V$. Find the corresponding voltage values for the A/D conversion results of 80, 180, 480, 640, 960, 1600, 2048, 3200 and 4000.

   Use this equation: $V_k = V_{REF-} + k\left(\frac{V_{REF+} - V_{REF-}}{2^n - 1}\right)$

2. Suppose we have an ADC that expresses the digital result in 4 bits. $V_{ref+} = 5V$ and $V_{ref-} = 0V$. Demonstrate the steps required by the successive approximation algorithm to convert 2.3V to its digital representation. In your answer, you should do the following in each iteration of the algorithm:
   a. Convert the digital representation you guessed to an analog voltage using this equation: $V_k = V_{REF-} + k\left(\frac{V_{REF+} - V_{REF-}}{2^n - 1}\right)$
   b. Explain how you arrive at your digital result after the completion of each iteration.

   The A/D conversion result (denoted as SAR hereafter) is initialized as 0000.The successive approximation algorithm runs for 4 iterations, because the ADC result is represented in 4 bits.

   1st Iteration:
   Guess MSB of the result as 1 → SAR = 1000 → $V_k = 0 + 8\left(\frac{5-0}{2^4-1}\right) = 2.67V$ *→ Is 2.3V >2.67V? No → Our guess of MSB was wrong → SAR = 0000.*

   2nd iteration:
   Guess 2nd MSB of the result as 1 → SAR = 0100 → $V_k = 0 + 4\left(\frac{5-0}{2^4-1}\right) = 1.33V$ *→ Is 2.3V>1.33V? Yes → Our guess of 2nd MSB was correct → SAR = 0100.*

   3rd iteration:
   Guess 3rd MSB of the result as 1 → SAR = 0110 → $V_k = 0 + 6\left(\frac{5-0}{2^4-1}\right) = 2V$ *→ Is 2.3V>2V? Yes → Our guess of 3rd MSB was correct → SAR = 0110.*

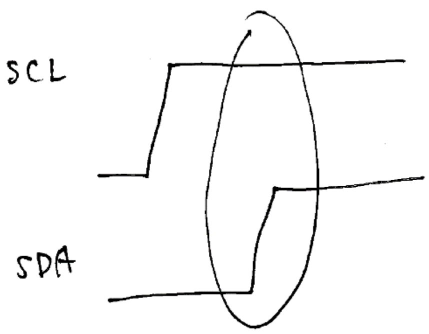
   4th iteration:
   Guess 4th MSB (i.e., LSB) of the result as 1 → SAR = 0111 → $V_k = 0 + 7\left(\frac{5-0}{2^4-1}\right) = 2.33V$ *→ Is 2.3V>2.33V? No → Our guess of LSB was wrong → SAR = 0110.*

   Final result: SAR = 0110

3. In I²C, the start condition can only be asserted if both the SDA and SCL lines float high. These two lines are usually brought high by an assertion of the stop condition.
   a. Give an example in which a start condition must be asserted without first asserting a stop condition. Explain why the stop condition cannot be asserted first.

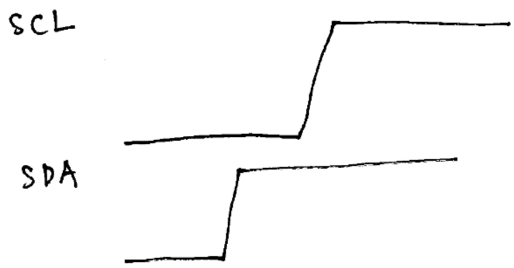
      In the situation in which the master wants to communicate with another slave or change the data transfer direction, the master needs to send out a new control byte (which consists of a 7-bit slave address followed by a bit determining the data transfer direction). The control byte must be preceded by a start condition. A stop condition cannot be asserted because the master wants to send more data after the change without releasing the bus. If a stop condition is asserted first, other master device can grab the control of the bus.

   b. Without asserting a stop condition, it is still possible to bring the SDA and SCL high. Draw a timing diagram demonstrating this possibility.



(a) STOP Condition

A stop condition occurs when the SDA line is brought high when the SCL line floats high.



(b) Bring SDA = SCL = 1 without asserting the stop condition

If the SDA line is brought high before the SCL line is brought high, ~~no stop condition is asserted~~ both lines can be brought high without asserting the stop condition.

This technique is used in the Repeated Start condition to bring the SDA and SCL lines to high before asserting a start condition.