EE3220 System-on-Chip Design

Tutorial Note 3

ARM-based 32-bit MCUs Debug & UART



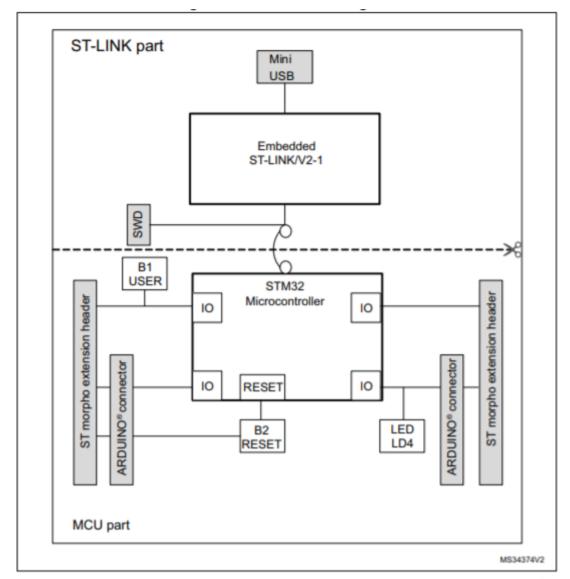
Objective

- In this tutorial, you will be able to learn:
 - The basic feature and design tools of ARM Cortex-M architecture.
 - Debug system architecture and experiment with Keil Studio.
 - Serial communication bus— UART and USART.



Overview of NUCLEO F401-RE

- Common features
- STM32 microcontroller in LQFP64 package
- I user LED shared with ARDUINO®
- I user and I reset push-buttons
- 32.768 kHz crystal oscillator
- Board connectors:
- ARDUINO® Uno V3 expansion connector
- ST morpho extension pin headers for full access to all STM32 I/Os
- Flexible power-supply options: ST-LINK, USB VBUS, or external sources
- On-board ST-LINK debugger/programmer with USB re-enumeration
- capability: mass storage, Virtual COM port and debug port
- Comprehensive free software libraries and examples available with the
- STM32Cube MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs)
- including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE
- Board-specific features
- External SMPS to generate Vcore logic supply
- 24 MHz HSE
- Board connectors:
- External SMPS experimentation dedicated connector
- Micro-AB or Mini-AB USB connector for the ST-LINK
- MIPI® debug connector
- Arm® Mbed Enabled™ compliant





Development tools

- The board is supported by many tools and IDEs many vendors
 - ARM Development Studio (licensed)
 - ARM® Mbed online
 - ARM Keil Studio Cloud
 - STM32CubeIDE (free)
 - IAR Systems IAR Embedded Workbench® (licensed)
 - Keil®: MDK-ARM(a) (licensed)
 - GCC-based IDEs
 - CrossWorks
 - SEGGER Embedded Studio (commercial with free-trial)
 - SW4STM32 (free)
 - TrueSTUDIO (free)
 - MATLAB® and Simulink® (licensed)



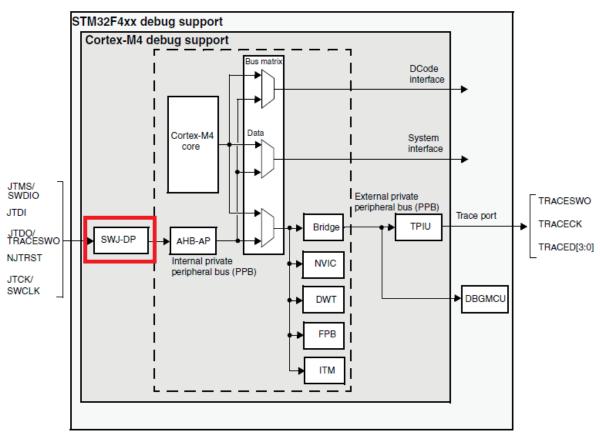
Debug system overview

- The STM32F401RE is built around a Cortex®-M4 with FPU core which contains hardware extensions for advanced debugging features:
 - The debug extensions allow the core to be stopped either on a given instruction fetch (breakpoint)
 or data access (watchpoint).
 - When stopped, the core's internal state and the system's external state may be examined.
 - Once examination is complete, the core and the system may be restored and program execution resumed.
- Two interfaces for debug are available:
 - Serial wire
 - JTAG debug port



STM32 MCU and Cortex®-M4 debug block

- The Arm® Cortex®-M4 with FPU core provides integrated on-chip debug support. It is
 - comprised of:
 - SWJ-DP: Serial wire / JTAG debug port
 - AHP-AP: AHB access port
 - ITM: Instrumentation trace microcell
 - FPB: Flash patch breakpoint
 - DWT: Data watchpoint trigger
 - TPUI:Trace port unit interface
 - ETM: Embedded Trace Macrocell





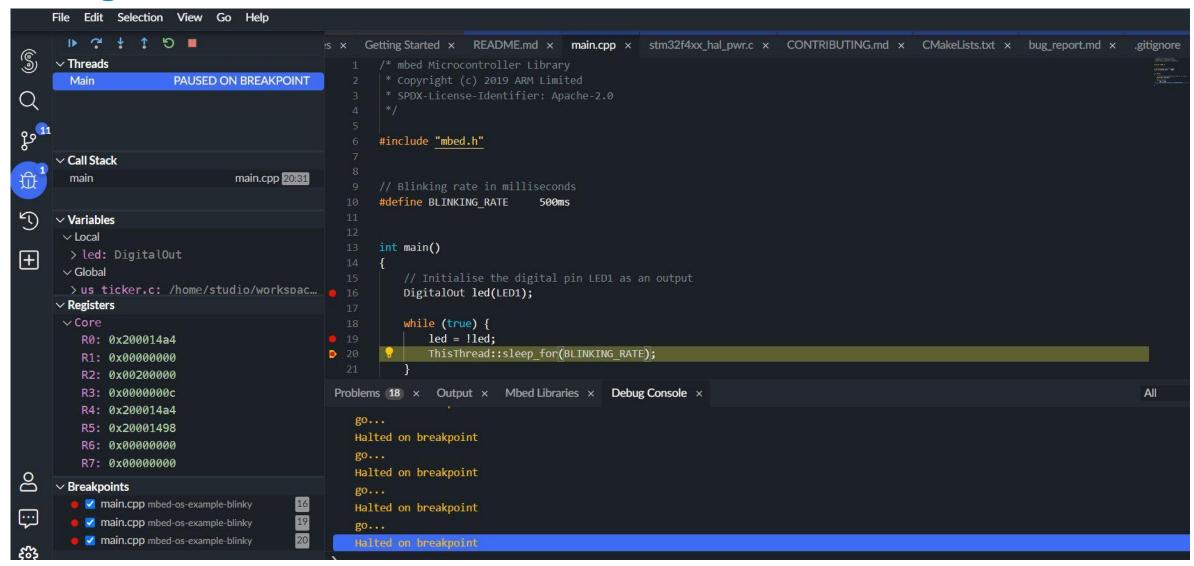
SWJ debug port

- The core of the STM32F401RE integrates the Serial Wire / JTAG Debug Port (SWJ-DP). It is an Arm® standard CoreSight debug port that combines a JTAGDP (5-pin) interface and a SW-DP (2-pin) interface.
 - The JTAG Debug Port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
 - The Serial Wire Debug Port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.
- TRACESWO (asynchronous trace) SWJ-DP TDO TDI TDI nTRST **NJTRST** nTRS7 JTAG-DP TCK **nPOTRST** SWD/JTAG power-on nPOTRS1 **DBGRESETn SWDITMS** DBGDI JTMS/SWDIO **←** ► **SWDO** DBGDO SW-DP **SWDOEN** DBGDOEN **SWCLKTCK** JTCK/SWCLK DBGCLK

• In STM32F401RE, debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.



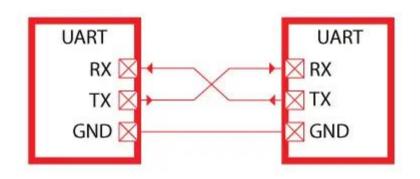
Debug in Keil Studio

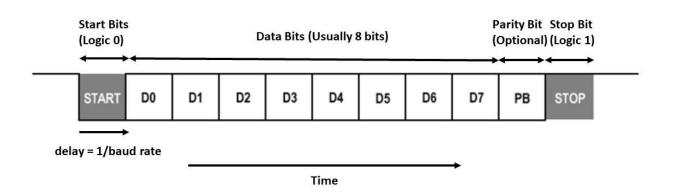




UART

- Universal Asynchronous Receiver Transmitter (UART) is one of the simplest and the most common protocols for serial communication between hardware devices.
- A UART device requires only two wires, one for transmitting and the other for receiving, to support full duplex communication.
- The UART module converts data into a stream of serial bits and transmits in a packet form shown in the following figure. The data stream is transferred at a fixed baud rate in both direction.

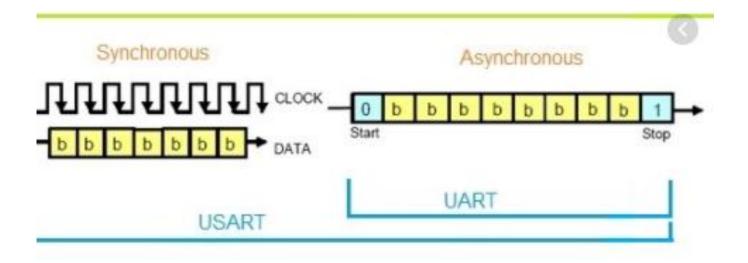






USART

- USART a Universal Synchronous/Asynchronous Receiver/Transmitter
 - In synchronous mode, have a reference clock signal to receiver
 - Receiver could not know the baud rate





USART Configure

Baud rate register (USART_BRR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIV_Mantissa[11:0]												DIV_Fra	ction[3:0]	
гw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw



USART Configure (cont'd)

Control register 3 (USART_CR3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Rese	unund		ONEBIT	CTSIE	CTSE	RTSE	DMAT	DMAR	SCEN	NACK	HDSEL	IRLP	IREN	EIE
	ivese	i veu		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Set as 0x0000 if no flow control



USART Configure (cont'd)

Control register 2 (USART_CR2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	LINEN	STO	P[1:0]	CLKEN	CPOL	CPHA	LBCL	Res.	LBDIE	LBDL	Res.		ADD	[3:0]	
ixes.	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

STOP[1:0]: STOP bits

• 00: I Stop bit



USART Configure (cont'd)

Control register I (USART_CRI)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OVER8	Reserved	UE	М	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	RWU	SBK
rw	Res.	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- Bit 2 RE: Receiver enable
 - 0: Receiver is disabled
 - I: Receiver is enabled and begins searching for a start bit ← enable RX
- Bit 3 TE: Transmitter enable
 - 0:Transmitter is disabled
 - I:Transmitter is enabled ← enable TX
- Bit I2 M:Word length.
 - 0: I Start bit, 8 Data bits, n Stop bit
 - 1: 1 Start bit, 9 Data bits, n Stop bit
- Bit 13 UE: USART enable
 - 0: USART prescaler and outputs disabled
 - I: USART enabled

- Bit 7TXEIE:TXE interrupt enable
 - 0: Interrupt is inhibited
 - I:An USART interrupt is generated whenever TXE=1 in the USART_SR register ← After NVIC setting done



For more details

- Go to board website read more reference document.
 - https://www.st.com/en/microcontrollers-microprocessors/stm32f40lre.html#documentation
- Reference document.
 - RM0368 Reference manual

 $\underline{https://www.st.com/resource/en/reference_manual/dm00096844-stm32f40\,I\,xb-c-and-stm32f40\,I\,xd-e-advanced-arm-based-32-bit-mcus-stmicroelectronics.pdf}$

Cont	ents		
1	Doc	umentation conventions	
	1.1	List of abbreviations for registers	
	1.2	Glossary	
	1.3	Peripheral availability	
2	Men	nory and bus architecture	
	2.1	System architecture	
		2.1.1 I-bus	
		2.1.2 D-bus	
		2.1.3 S-bus	
		2.1.4 DMA memory bus	
		2.1.5 DMA peripheral bus	
		2.1.6 BusMatrix	
		2.1.7 AHB/APB bridges (APB)	
	2.2	Memory organization	
	2.3	Memory map	
		2.3.1 Embedded SRAM	
		2.3.2 Flash memory overview	
		2.3.3 Bit banding	
	2.4	Boot configuration	
3	Emb	pedded Flash memory interface	
	3.1	Introduction	
	3.2	Main features	
	3.3	Embedded Flash memory in STM32F401xB/C and STM32F401xD/E	
	3.4	Read interface 46	
	0.4	3.4.1 Relation between CPU clock frequency and Flash memory read time . 46	
		3.4.2 Adaptive real-time memory accelerator (ART Accelerator™)	
	3.5	Erase and program operations	
	5.5	3.5.1 Unlocking the Flash control register	
		3.5.2 Program/erase parallelism	
		3.5.3 Erase	
2/847		RM0308 Rev 5	

Contents				RM0368
		18.6.5	I ² C Data register (I2C_DR)	498
		18.6.6	I ² C Status register 1 (I2C_SR1)	498
		18.6.7	I ² C Status register 2 (I2C_SR2)	501
		18.6.8	I ² C Clock control register (I2C_CCR)	503
		18.6.9	I ² C TRISE register (I2C_TRISE)	504
		18.6.10	I ² C FLTR register (I2C_FLTR)	504
		18.6.11	I2C register map	505
19			nchronous asynchronous receiver JSART)	506
	19.1	USART	introduction	506
	19.2	USART	main features	506
	19.3	USART	functional description	507
		19.3.1	USART character description	510
		19.3.2	Transmitter	511
		19.3.3	Receiver	514
		19.3.4	Fractional baud rate generation	519
		19.3.5	USART receiver tolerance to clock deviation	529
		19.3.6	Multiprocessor communication	530
		19.3.7	Parity control	532
		19.3.8	LIN (local interconnection network) mode	533
		19.3.9	USART synchronous mode	535
		19.3.10	Single-wire half-duplex communication	537
		19.3.11	Smartcard	538
		19.3.12	IrDA SIR ENDEC block	540
		19.3.13	Continuous communication using DMA	542
		19.3.14	Hardware flow control	544
	19.4	USART	interrupts	547
	19.5	USART	mode configuration	548
	19.6	USART	registers	548
		19.6.1	Status register (USART_SR)	548
		19.6.2	Data register (USART_DR)	551
		19.6.3	Baud rate register (USART_BRR)	551
		19.6.4	Control register 1 (USART_CR1)	551
		19.6.5	Control register 2 (USART_CR2)	554
		19.6.6	Control register 3 (USART_CR3)	555
		19.6.7	Guard time and prescaler register (USART_GTPR)	557
16/847			RM0368 Rev 5	47/

RM0368				Conten
		22 16 2	OTG FS global registers	7
			Host-mode registers	
			Device-mode registers	
			OTG_FS power and clock gating control register (OTG_FS_PCGCCTL)	
		22.16.6	OTG_FS register map	7
	22.17		S programming model	
			Core initialization	
		22.17.2	Host initialization	7
		22.17.3	Device initialization	70
		22.17.4	Host programming model	7
		22.17.5	Device programming model	71
		22.17.6	Operational model	7
		22.17.7	Worst case response time	8
		22.17.8	OTG programming model	8
23	Debu	g supp	ort (DBG)	80
	23.1	Overvie	9W	80
	23.2	Referen	nce Arm® documentation	8
	23.3	SWJ de	ebug port (serial wire and JTAG)	80
		23.3.1	Mechanism to select the JTAG-DP or the SW-DP	8
	23.4	Pinout a	and debug port pins	8
		23.4.1	SWJ debug port pins	8
		23.4.2	Flexible SWJ-DP pin assignment	
		23.4.3	Internal pull-up and pull-down on JTAG pins	
		23.4.4	Using serial wire and releasing the unused debug pins as GPIC	
	23.5	STM32	F401xB/C and STM32F401xD/E JTAG TAP connection	8
	23.6	ID code	es and locking mechanism	8
		23.6.1	MCU device ID code	
		23.6.2	Boundary scan TAP	
		23.6.3	Cortex®-M4 with FPU TAP	
		23.6.4	Cortex®-M4 with FPU JEDEC-106 ID code	8
	23.7	JTAG d	ebug port	
	23.8	SW del	bug port	8
	20.0	23.8.1	SW protocol introduction	
		23.8.2	SW protocol sequence	
477			RM0368 Rev 5	21/8

