EE 2004
Week 12 Homework

1. Suppose that there is a 12-bit ADC with $V_{ref+} = 4V$ and $V_{ref-} = 1V$. Find the corresponding voltage values for the A/D conversion results of 80, 180, 480, 640, 960, 1600, 2048, 3200 and 4000.

2. Suppose we have an ADC that expresses the digital result in 4 bits. $V_{ref+} = 5V$ and $V_{ref-} = 0V$. Demonstrate the steps required by the successive approximation algorithm to convert 2.3V to its digital representation. In your answer, you should do the following in each iteration of the algorithm:
    a. Convert the digital representation you guessed to an analog voltage using this equation: $V_k = V_{REF-} + k\left(\frac{V_{REF+} - V_{REF-}}{2^n - 1}\right)$
    b. Explain how you arrive at your digital result after the completion of each iteration.

3. In I^2C, the start condition can only be asserted if both the SDA and SCL lines float high. These two lines are usually brought high by an assertion of the stop condition.
    a. Give an example in which a start condition must be asserted without first asserting a stop condition. Explain why the stop condition cannot be asserted first.
    b. Without asserting a stop condition, it is still possible to bring the SDA and SCL high. Draw a timing diagram demonstrating this possibility.