Experiment-2(A)

Aim:

To implement a CMOS inverter of level (1, 3 and 54) and analyse its dc characteristics.

Tool Used:

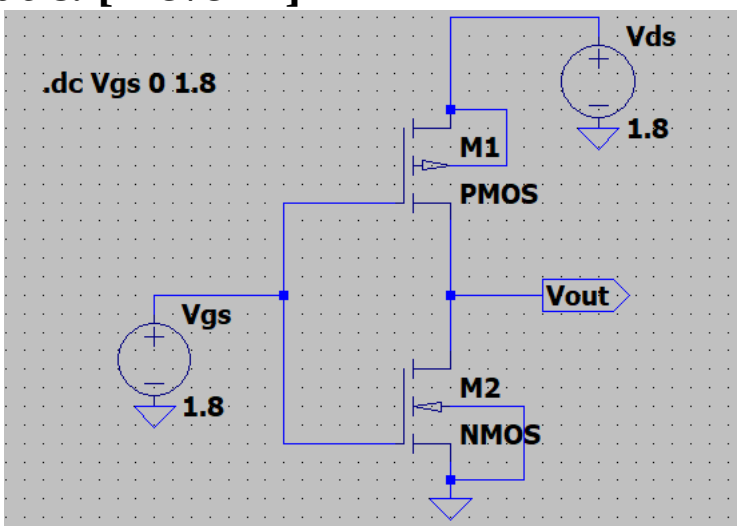
LTspice

Theory:

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

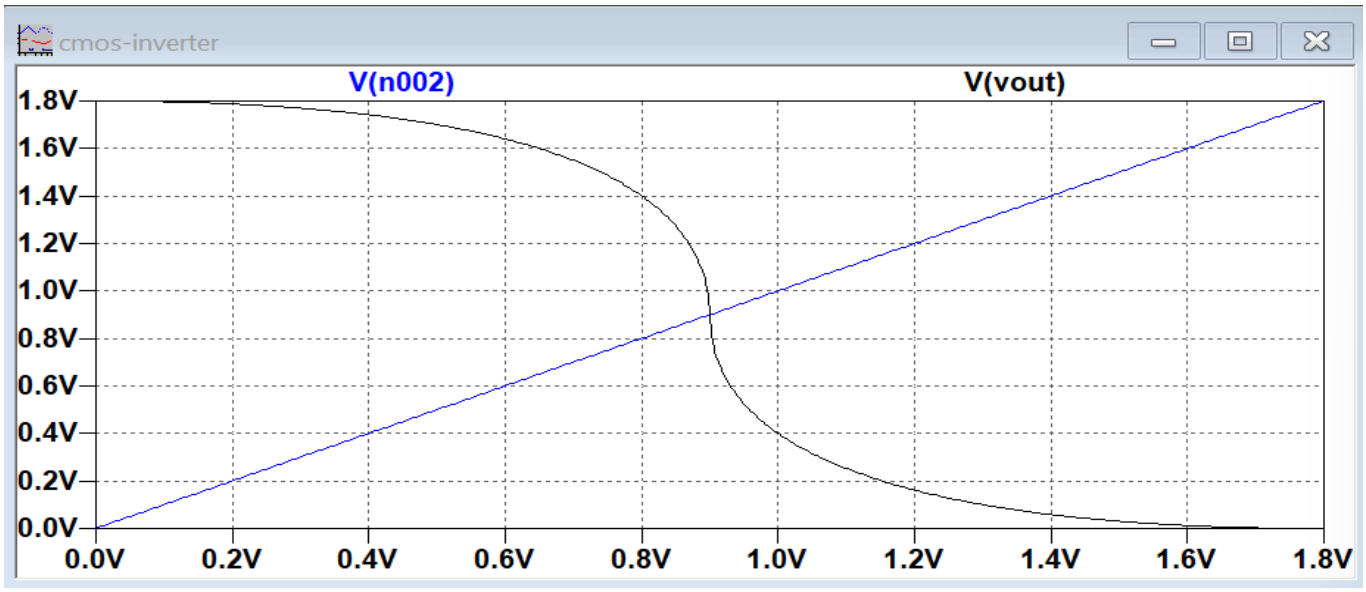
In CMOS inverter an n-type MOSFET acts as a pull-down transistor between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of Resistive Inverter, CMOS inverter has a p-type MOSFET in a pull-up transistor between the output and the higher-voltage rail (often named Vdd).

Circuit Schematic: [Level 1]

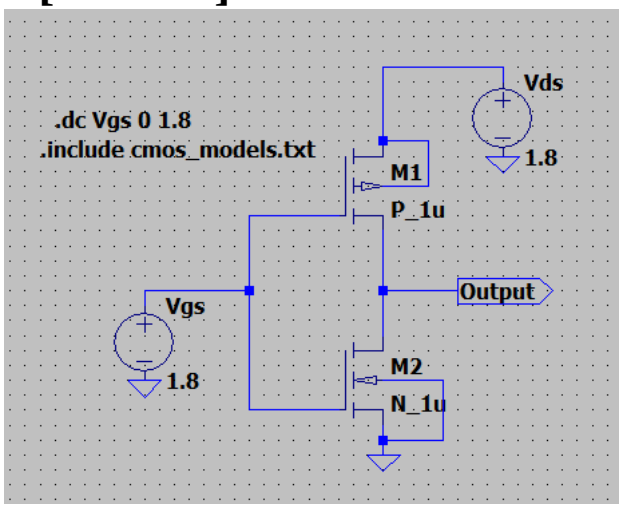


Output Waveforms:

Dc Transfer characteristics (Vgs vs. Vout)

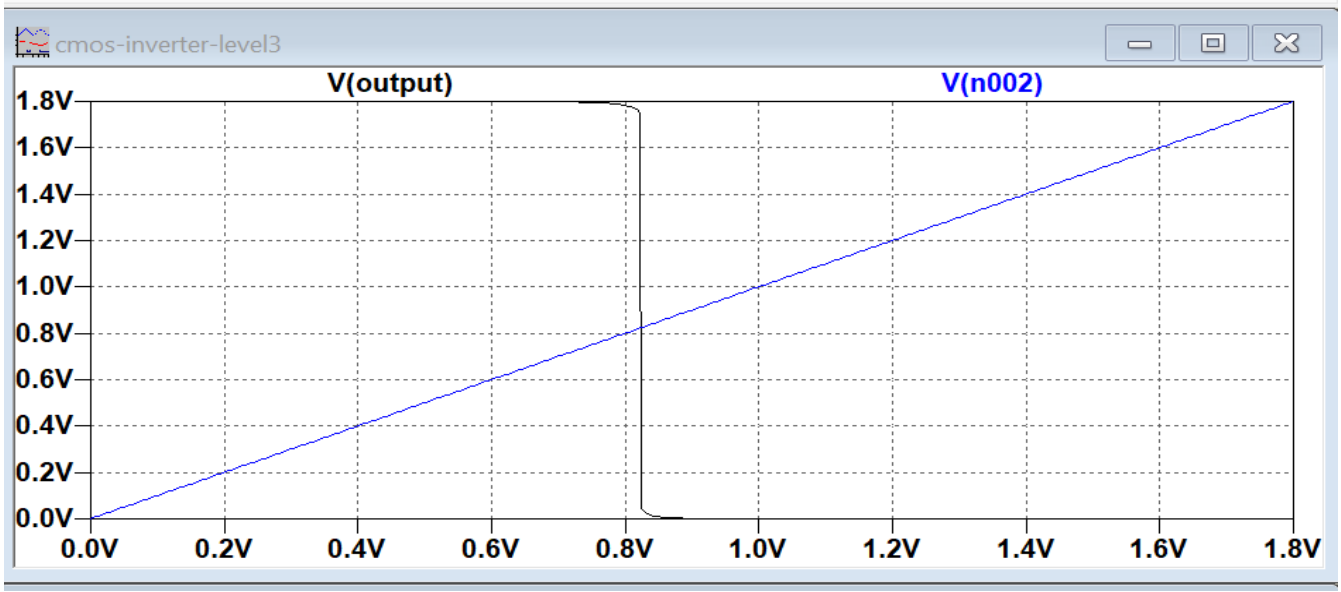


Circuit Schematic: [Level 3]

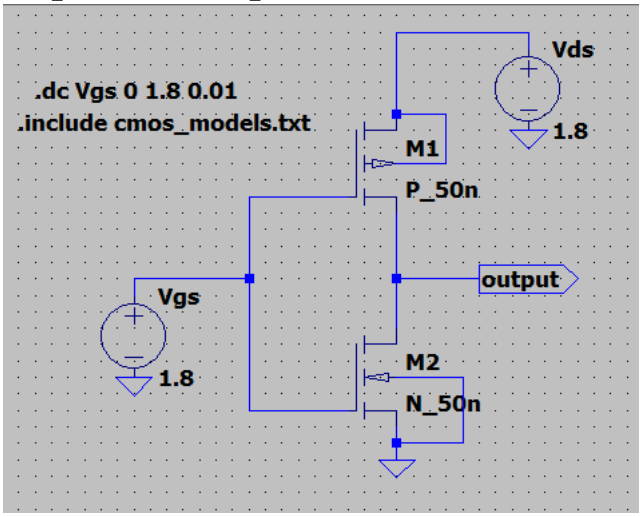


Output Waveforms:

Dc Transfer characteristics (Vgs vs. Vout) for (W/L)p / (W/L)n = 5

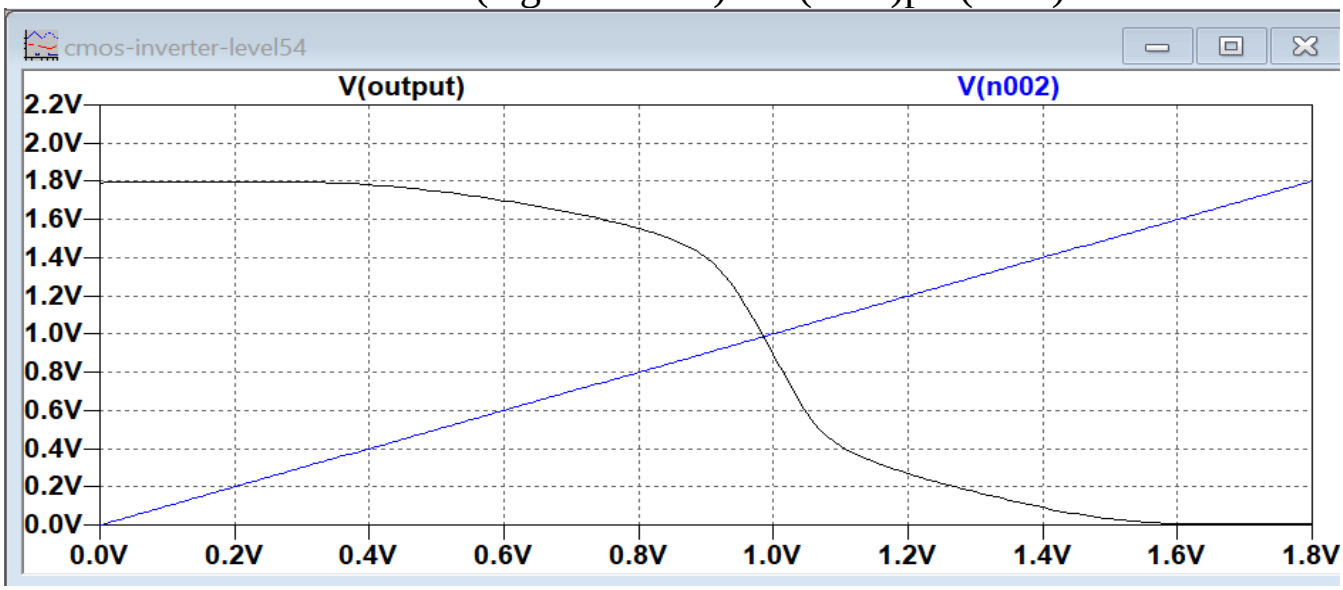


Circuit Schematic: [Level 54]



Output Waveforms:

Dc Transfer characteristics (Vgs vs. Vout) for (W/L)p / (W/L)n = 2.2



Result:

The circuit is stimulated for 3 levels of CMOS inverter and the dc characteristics are visualized.