Experiment-3

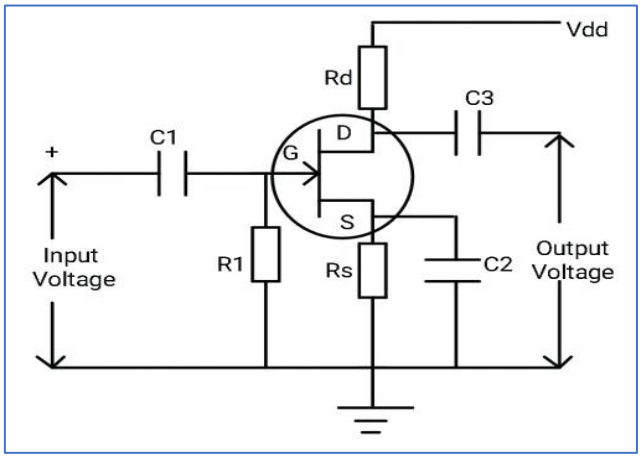
Aim:

Design a single stage common source amplifier with resistive load for a gain of 10 and analyse its transient and AC characteristics.

Tool Used: LTspice software

Theory:

When the input signal is applied at the gate terminal and source terminal, then the output voltage is amplified and obtained across the resistor at the load in the drain terminal. This is called a common source amplifier. The circuit diagram of the common source amplifier with N-channel MOSFET along with the coupling and biasing capability is shown.



This circuit will be similar to the common-emitter follower of Bipolar Junction transistor. If we use P-channel FET, the polarity of the input voltage will be reversed.

For a Level 3 NMOS let's assume

VDD = 1.8V

VT = 0.4V

VGS = 0.6V

Kn = 120µA/V^2,

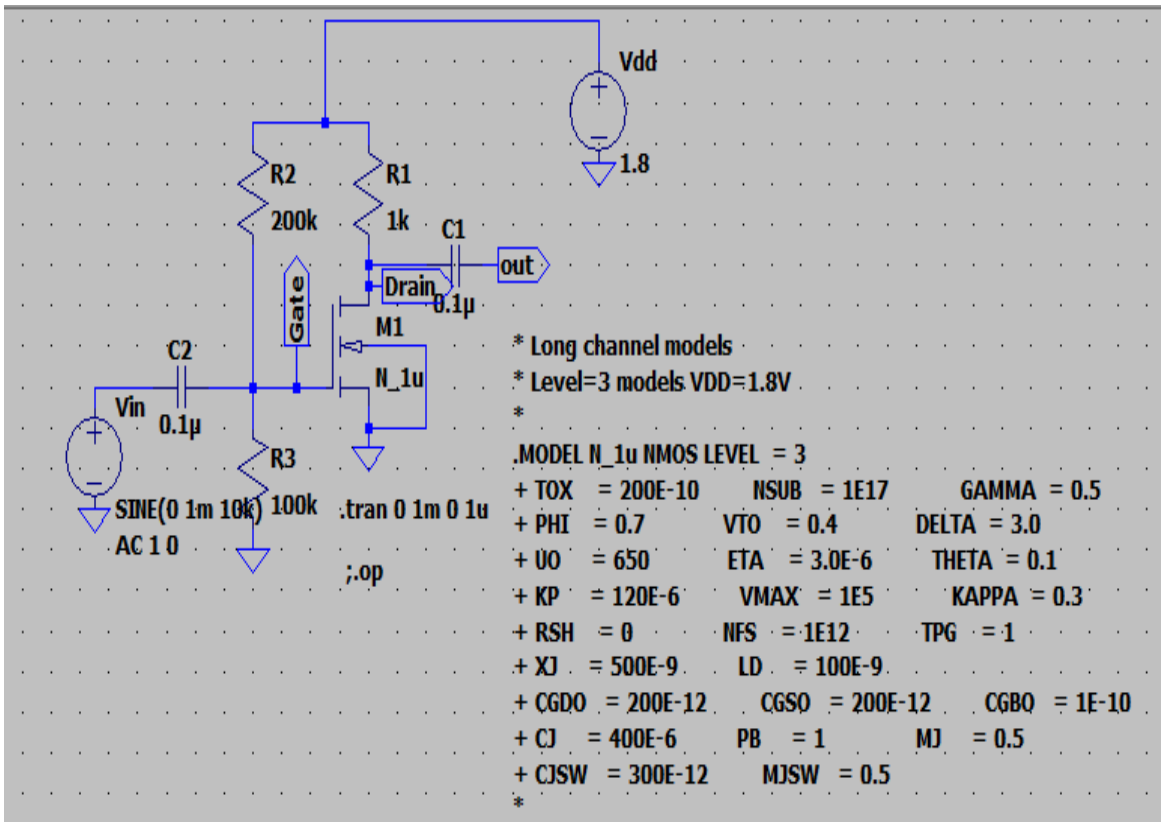
Which gives a value of (W/L) = 448 for 1mA ID.

Also, for these values' gm is attained as 10mΩ-1, therefore for gain 10, RD is taken as 1KΩ.

The value of VDS should be maintained above (VGS - VT = 0.6 - 0.4 = 0.2V) for the transistor to stay in saturation region.

As W/L is 416, the width is taken as 448µm and the length is taken as 1µm.

Circuit Schematic: [Level 3]



DC Operating Point

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        --- Operating Point ---

V(drain):       0.200254        voltage
V(gate):        0.6             voltage
V(n001):        1.8             voltage
V(out):         2.00254e-008    voltage
V(n002):        0               voltage
Id(M1):         0.00159975      device_current
Ig(M1):         0               device_current
Ib(M1):         -2.10249e-013   device_current
Is(M1):         -0.00159975     device_current
I(C2):          6e-020          device_current
I(C1):          -2.00254e-020   device_current
I(R3):          6e-006          device_current
I(R2):          6e-006          device_current
I(R1):          0.00159975      device_current
I(Vin):         6e-020          device_current
I(Vdd):         -0.00160575     device_current
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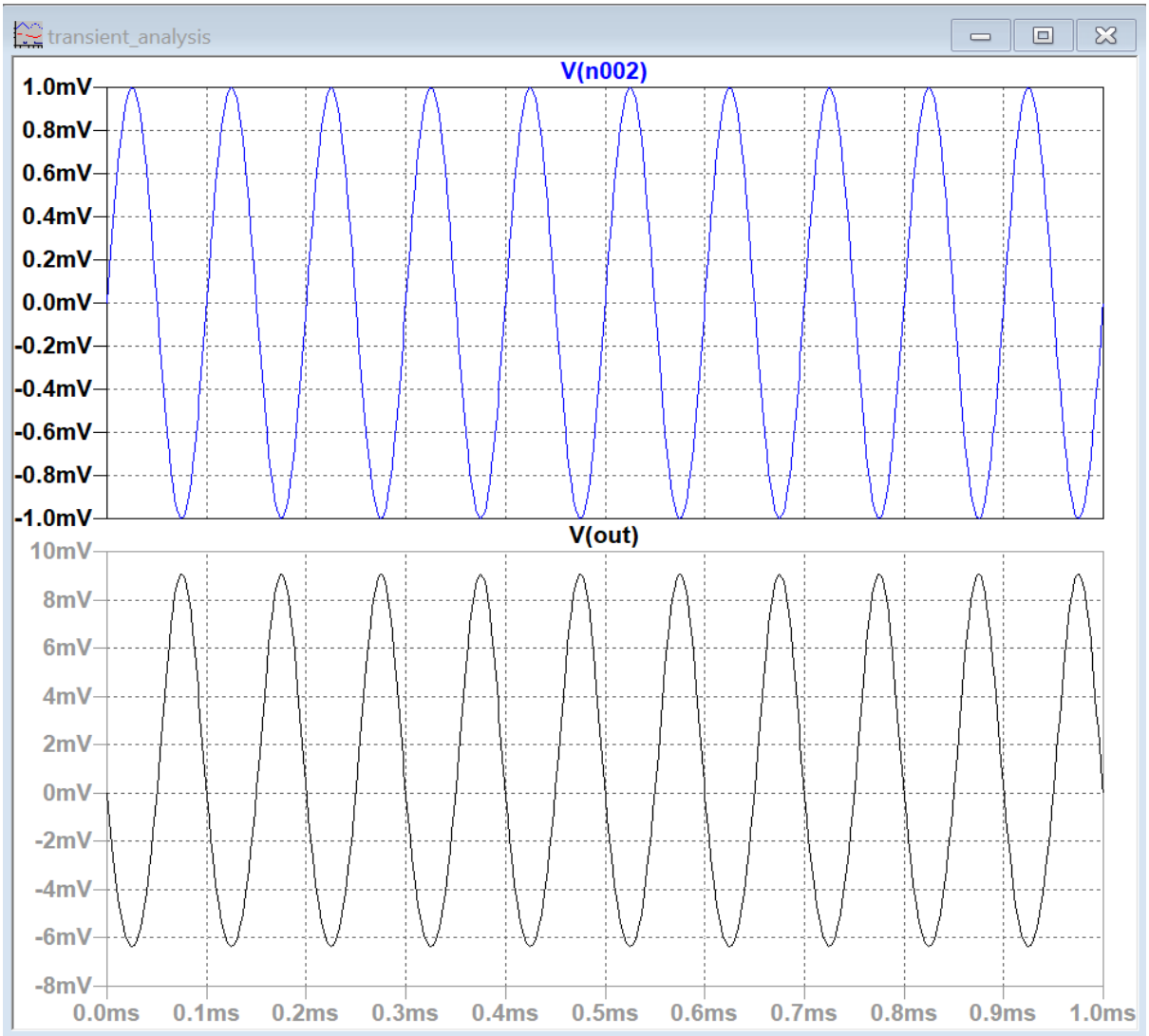
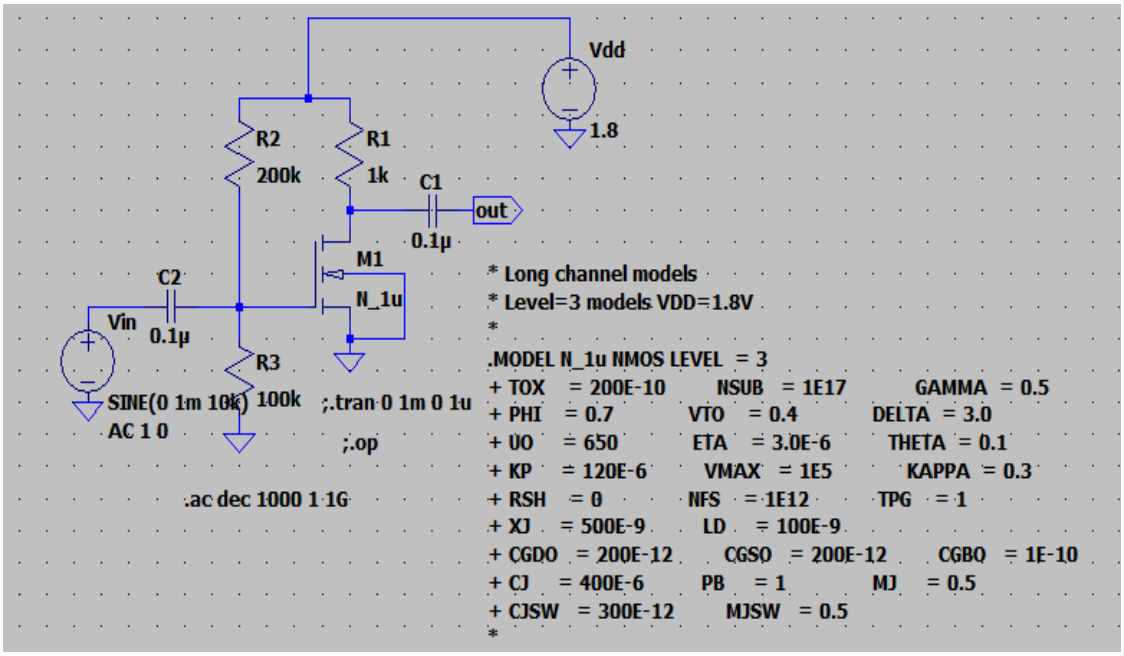
Output Waveforms:

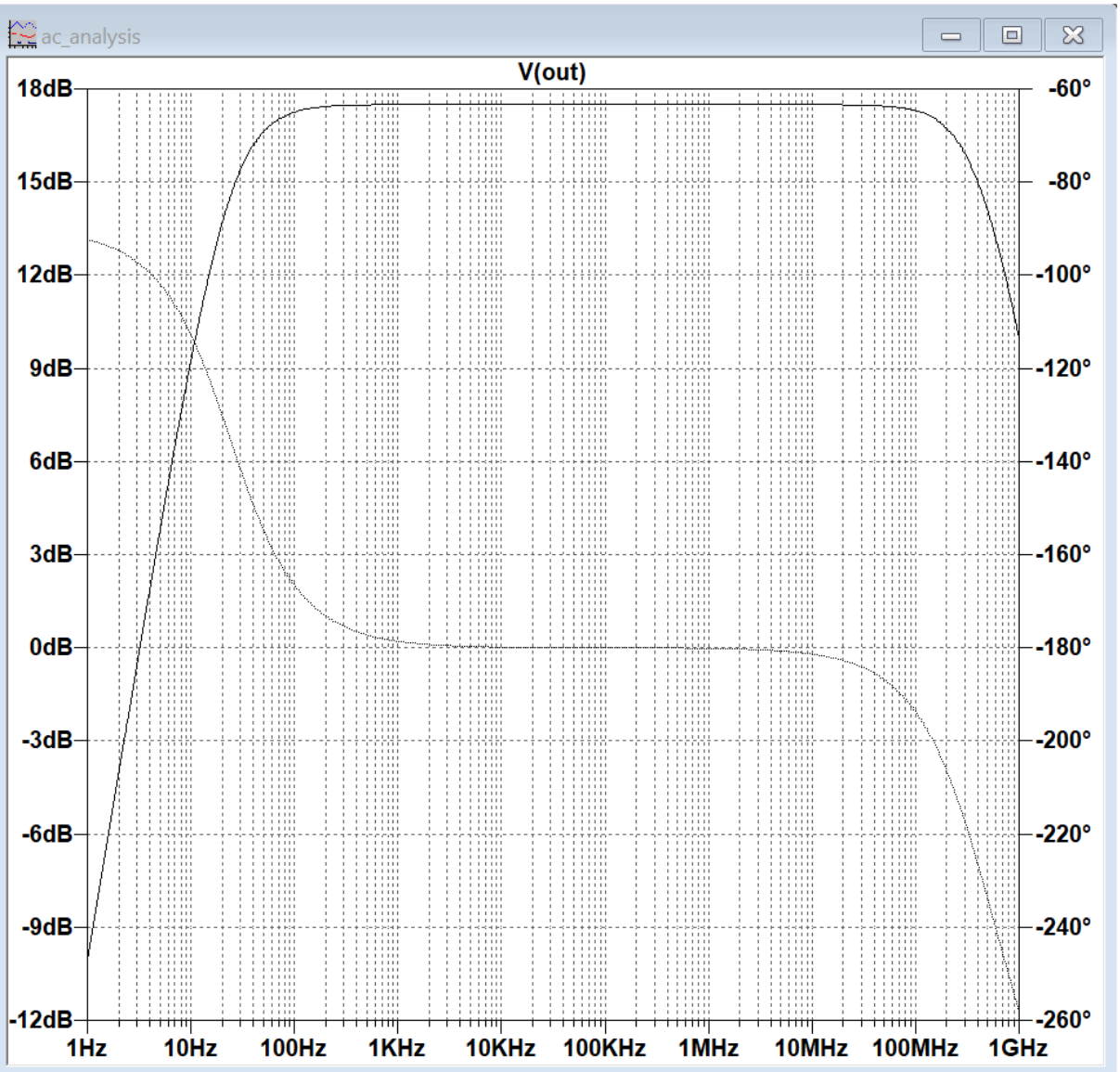
Transient Response:



AC Analysis:



Output Waveforms:



Result:

The common source amplifier for level3 of CMOS inverter circuit is designed for a gain of 10 and the transient and AC characteristics are verified to be correct.