Experiment-7

Aim:

To design a differential amplifier with active load for a gain 100 and analyse its transient characteristics.

Tool Used:

LTspice tool

Theory:

Differential amplifiers amplify the difference between two voltages making this type of operational amplifier circuit a Subtractor unlike a summing amplifier which adds or sums together the input voltages.

For a Level NMOS let's assume

$$VDD = 1.8V$$

$$VT = 0.4V$$

$$Kn = 120 \mu A/V2$$
,

For a Level PMOS let's assume

$$VDD = 1.8V$$

$$VT = -0.4V$$

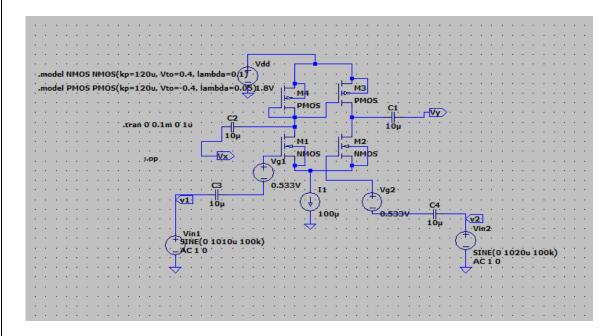
$$Kp = 120\mu A/V2$$
,

Which gives a value of (W/L) = (46.8) for 1mA ID.

The value of VDS should be maintained above (VGS - VT = 0.6 - 0.4 = 0.2V) for the transistor to stay in saturation region.

As for M2 and M1, the width is taken as 468 μm and the length is taken as 10 μm and for M3 and M4, the width is taken as 10 μm and the length is taken as 10 μm .

Circuit Schematic:



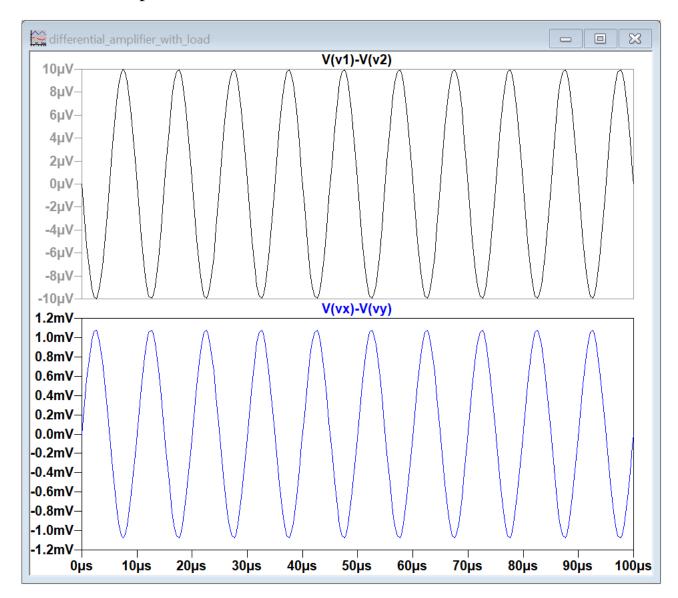
DC Operating Point

* C:\Users\singh\Documents\LTSpice\Analog IC Design Lab\Lab7\differ

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--- Operating Point ---
V(n003):
               0.515111
                              voltage
V(n007):
               0.533
                              voltage
V(n005):
               0.00285173
                              voltage
V(n002):
               0.515111
                              voltage
V(n006):
               0.533
                              voltage
V(n001):
               1.8
                              voltage
               5.15106e-006
V(vy):
                              voltage
V(v2):
                              voltage
V(v1):
               0
                              voltage
V(n009):
               0
                              voltage
V(n008):
                              voltage
               5.15106e-006
V(vx):
                              voltage
Id(M4):
               5e-005
                              device_current
               -0
Ig(M4):
                              device_current
Ib (M4):
               1.29489e-012
                              device current
Is(M4):
                -5e-005
                              device current
               5e-005
                              device_current
Id(M3):
Iq(M3):
               -0
                              device current
               1.29489e-012 device_current
Ib(M3):
Is(M3):
                -5e-005
                              device current
                5e-005
Id(M1):
                              device current
Ig(M1):
                              device_current
               -5.2226e-013
Ib (M1):
                              device current
Is(M1):
               -5e-005
                              device current
Id(M2):
               5e-005
                              device_current
Ig(M2):
                              device current
                -5.2226e-013
Ib (M2):
                              device_current
Is (M2):
                -5e-005
                              device_current
               0
I(C4):
                              device current
I(C3):
               0
                              device current
I(C2):
               5.15106e-018
                              device_current
I(C1):
                -5.15106e-018
                                             device_current
               0.0001
I(I1):
                              device_current
I(Vg1):
               0
                              device current
               0
I (Vg2):
                              device current
I (Vdd):
               -0.0001
                              device_current
I(Vin1):
               0
                              device_current
I(Vin2):
                              device_current
```

Output Waveforms:

Transient Response:



Result:

The circuit is designed for a gain of 100 and the output is verified to be correct.