Experiment-2(B)

Aim:

To implement a Resistive Load inverter and analyze its transient and dc characteristics.

## Tool Used:

LTspice

Theory:

The basic structure of a resistive load inverter is shown in the figure given below. Here, enhancement type nMOS acts as the driver transistor. The load consists of a simple linear resistor RL. The power supply of the circuit is VDD and the drain current ID is equal to the load current IR. When the input of the driver transistor is less than threshold voltage VTH (Vin < VTH), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the VDD. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and nMOS goes in saturation region.
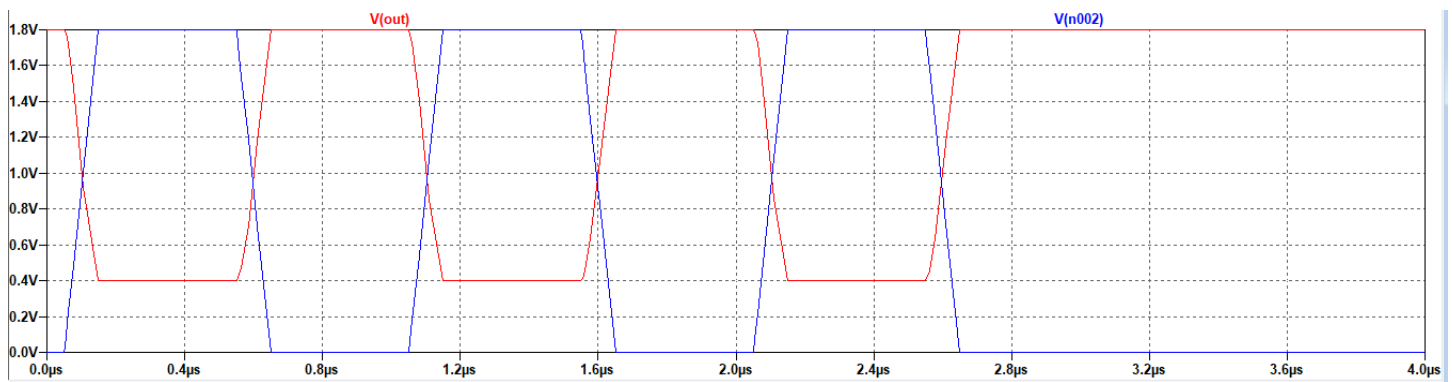
Circuit Schematic:
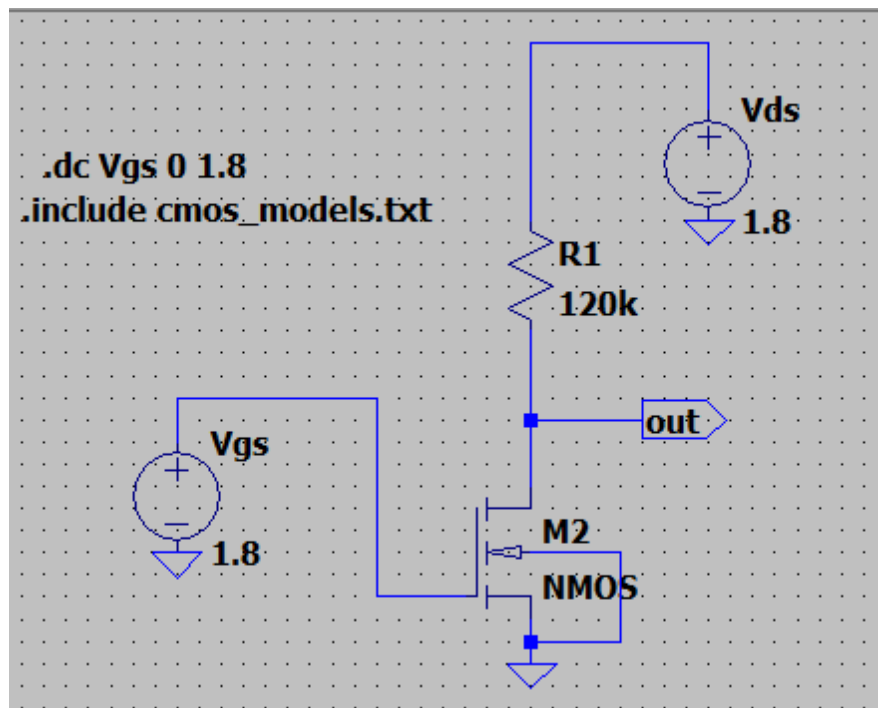
Output Waveforms:

Dc Transfer characteristics (Vgs vs. Vout)
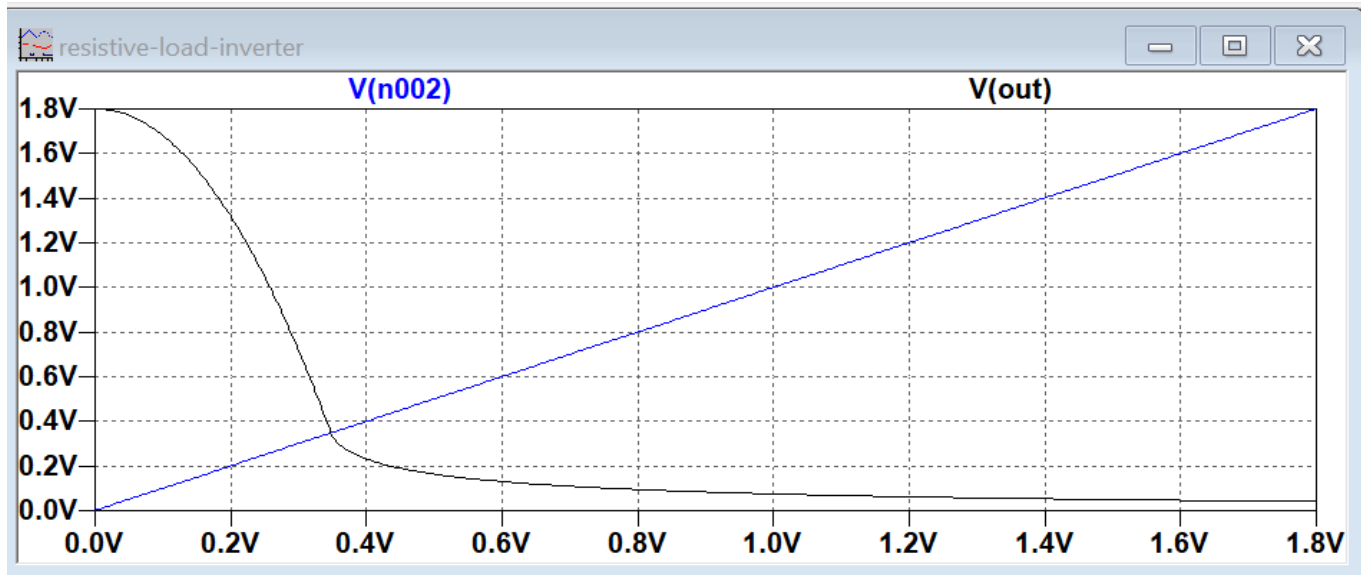
Transient characteristics

Result:

The circuit is stimulated with 120k resistor and the dc characteristics are visualized.