REFERÊNCIA

Vahid, F., Sistemas Digitais: Projeto, Otimização e HDLs, Cap. 8, Bookman, 2008.

SEÇÃO A - DIAGRAMAS DE BLOCOS

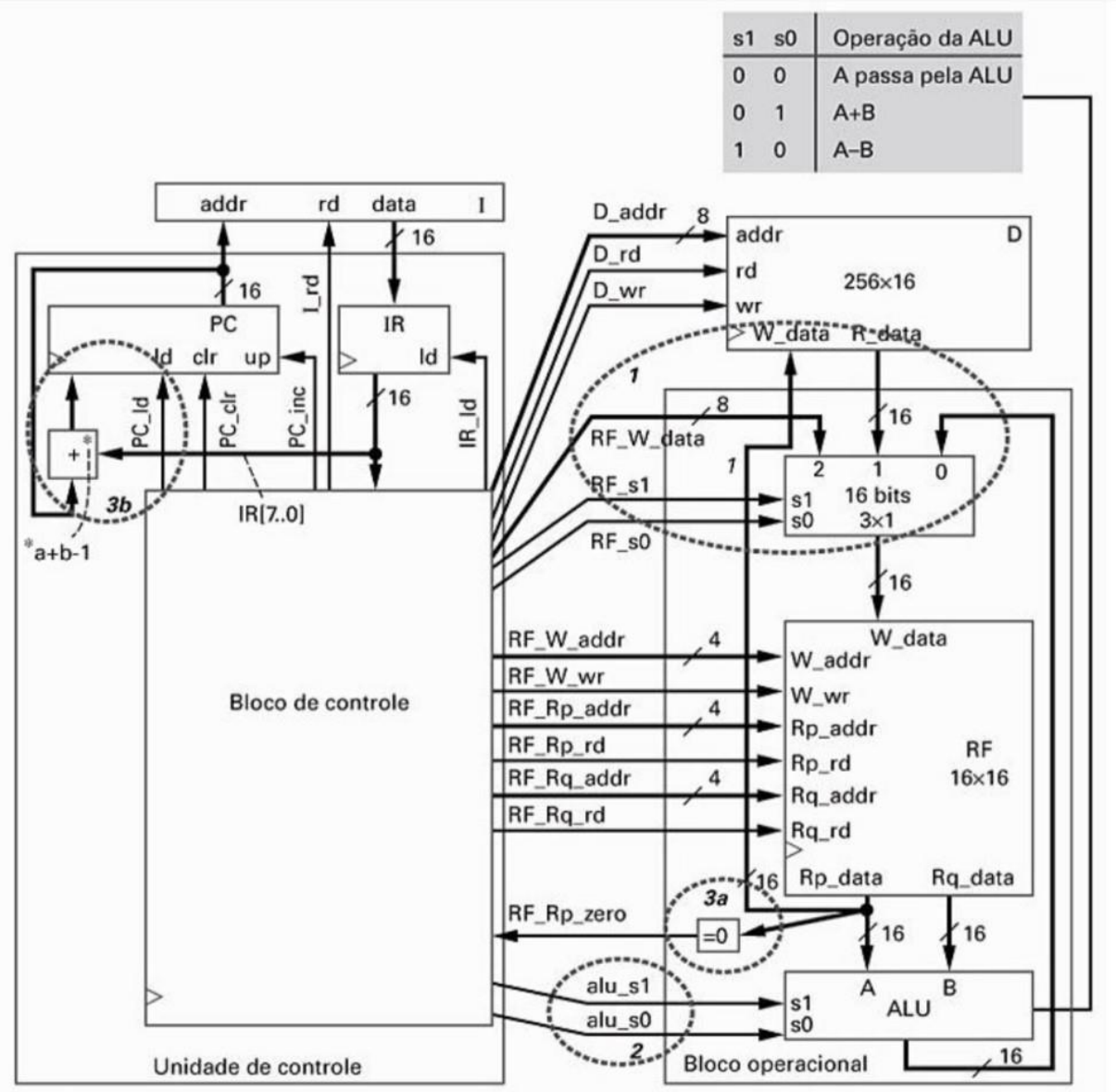

Figura 1: Diagrama de Blocos CPU de 6 Instruções (Vahid, 2008).

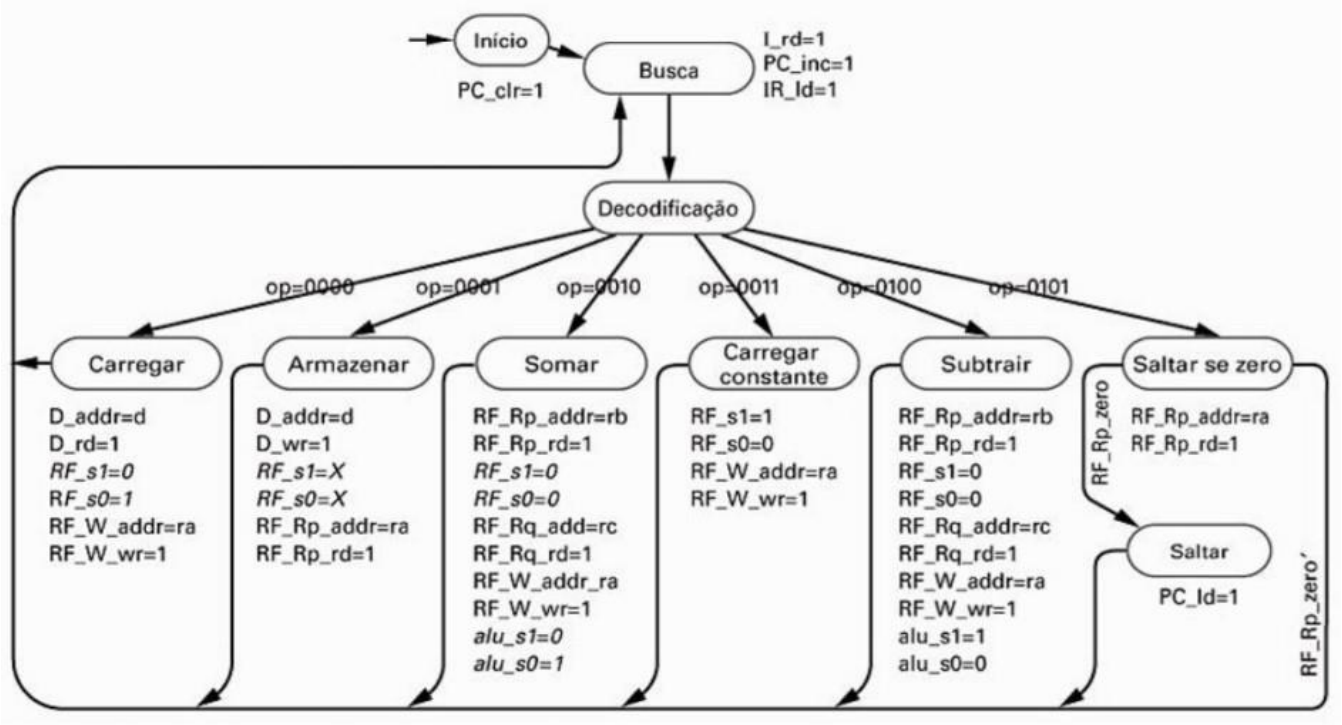

Figura 2: Diagrama de Estados Bloco de Controle (Vahid, 2008).

Instrução	Significado
MOV Ra, d	Rf[a]=D[d]
MOV d, Ra	D[d]=RF[a]
ADD Ra, Rb, Rc	RF[a]=RF[b]+RF[c]
MOV Ra, #C	RF[a]=C
SUB Ra, Rb, Rc	RF[a]=RF[b]-RF[c]
JMPZ Ra, offset	PC=PC+offset se RF[a]=0

Instrução	Código de operação
MOV Ra, d	0000
MOV d, Ra	0001
ADD Ra, Rb, Rc	0010
MOV Ra, #C	0011
SUB Ra, Rb, Rc	0100
JMPZ Ra, offset	0101

Figura 3: Conjunto de Instruções da CPU (Vahid, 2008).

SEÇÃO B - FORMAS DE ONDA DOS TESTBENCH

Figura 4: Forma de Onda ALU

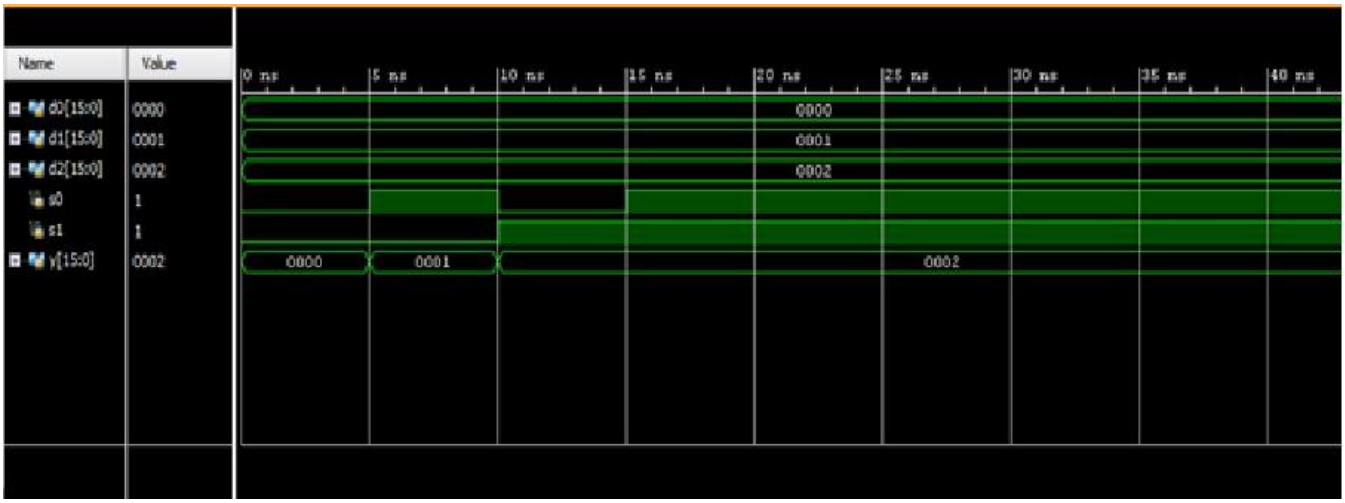

Figura 5: Forma de Onda MUX

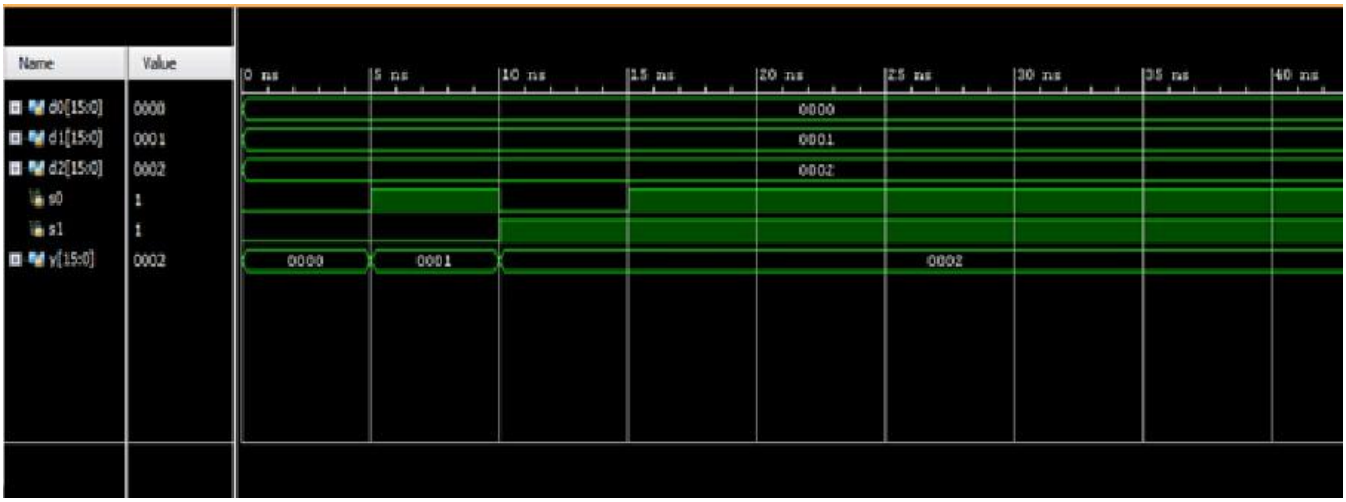

Figura 6: Forma de Onda RF

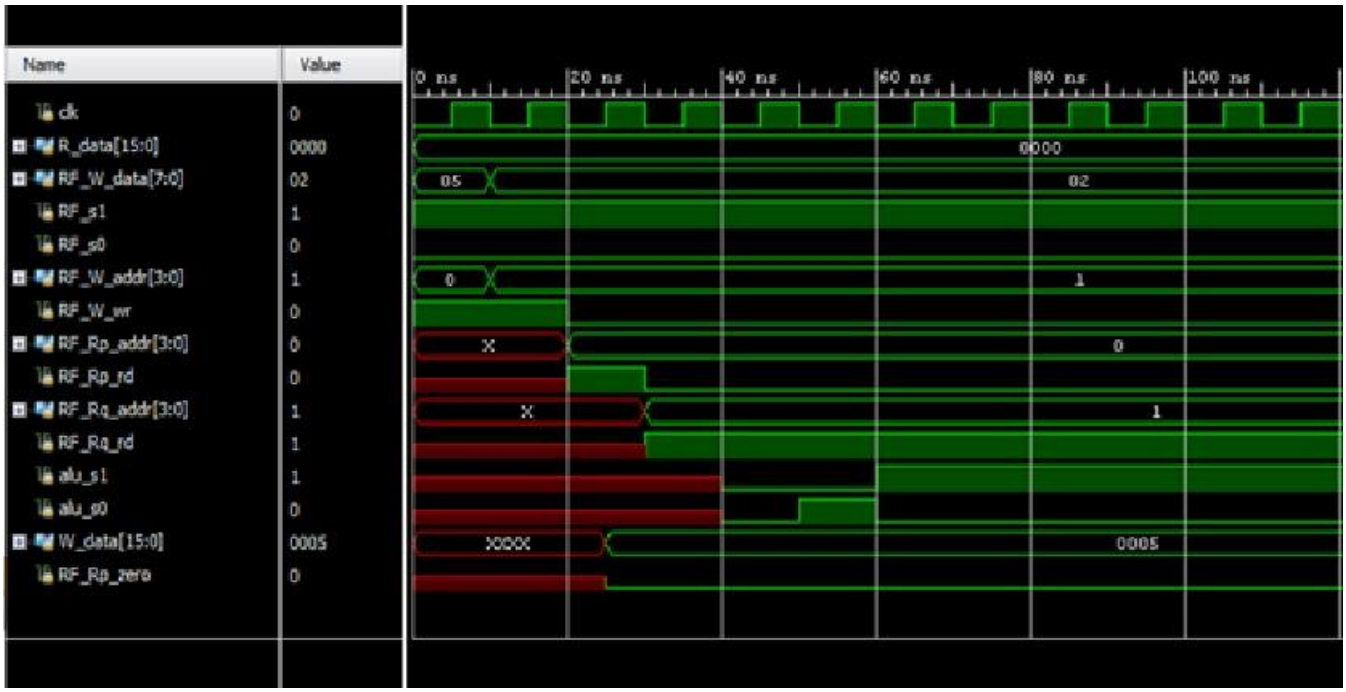

Figura 7: Forma de Onda Bloco Operacional

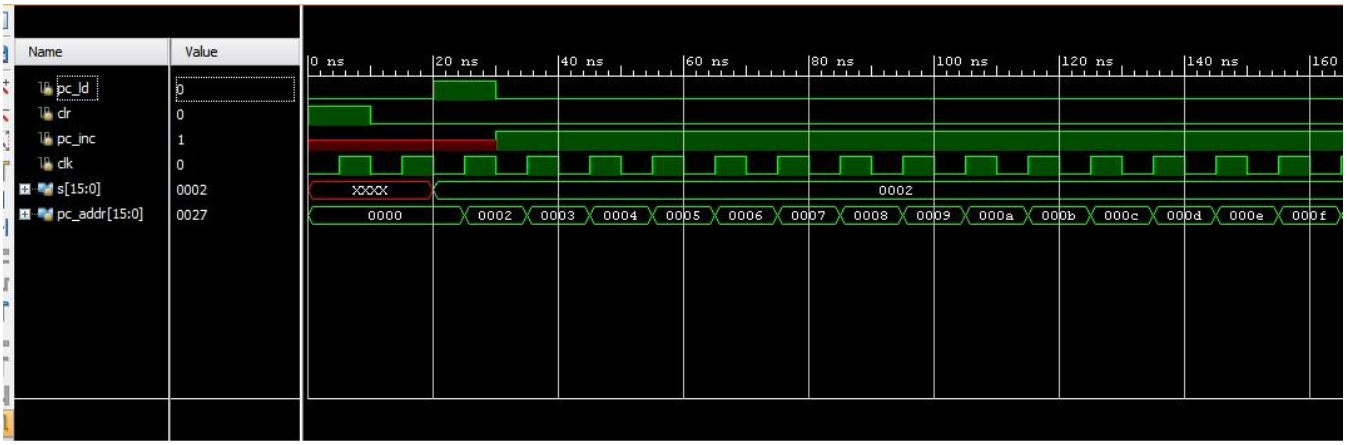

Figura 8: Forma de Onda do PC Counter

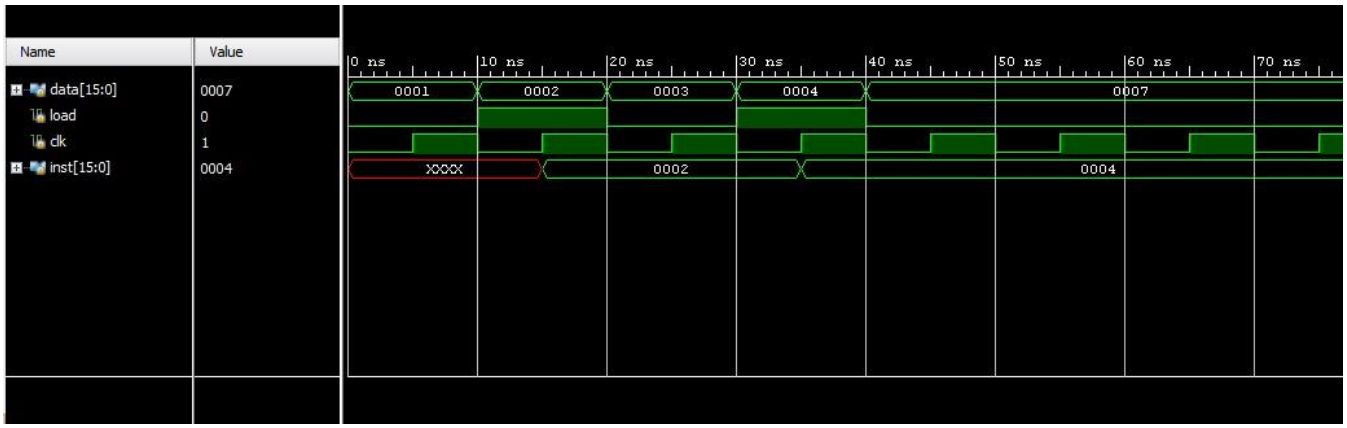

Figura 9: Forma de Onda do IR

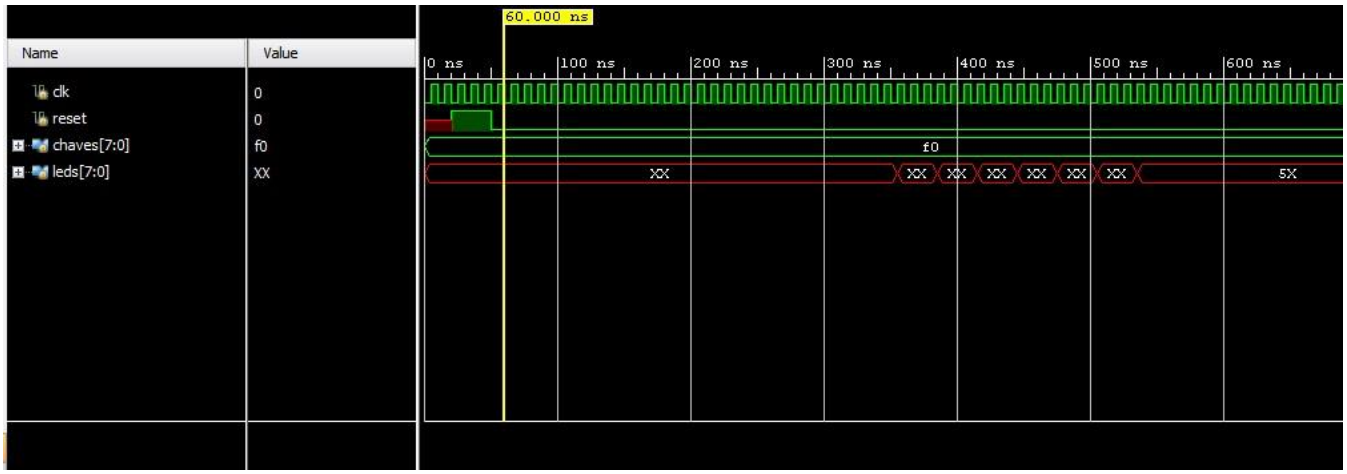

Figura 10: Forma de Onda do Top Level

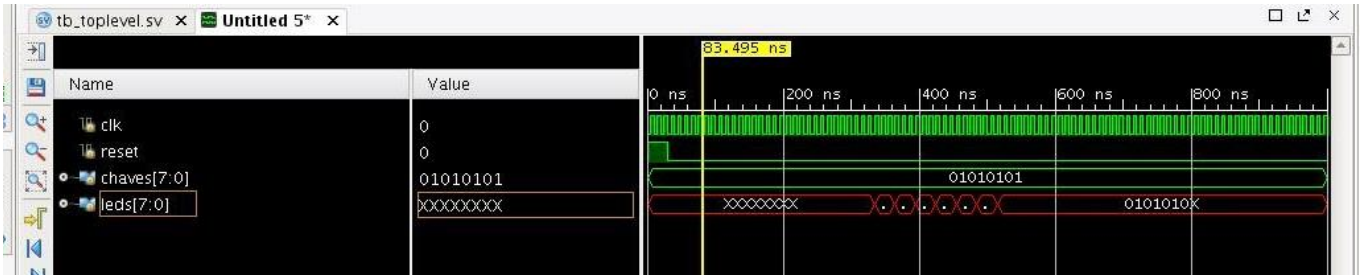

Figura 11: Forma de Onda do TOP Level

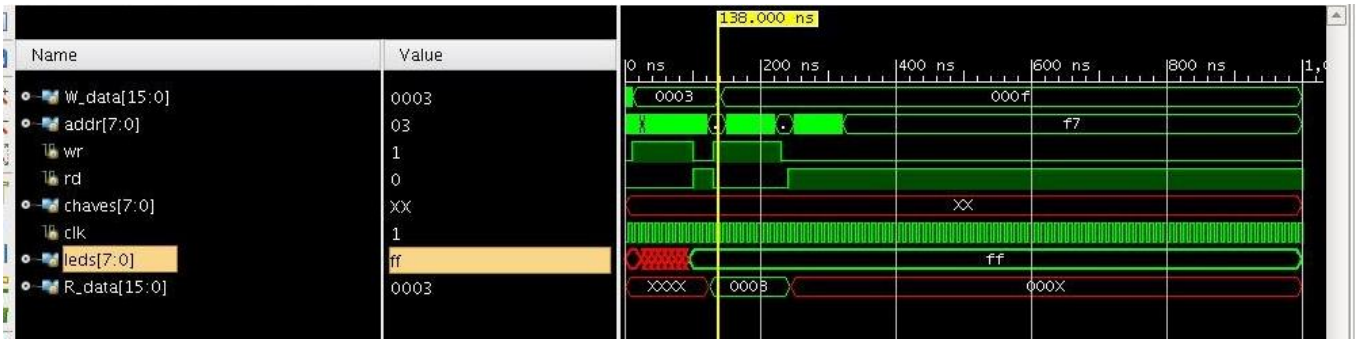

Figura 12: Forma de Onda do RAM