Introduction to VLSI

Lab 4

By:

Rebecca Curtis

Kancy Robinson
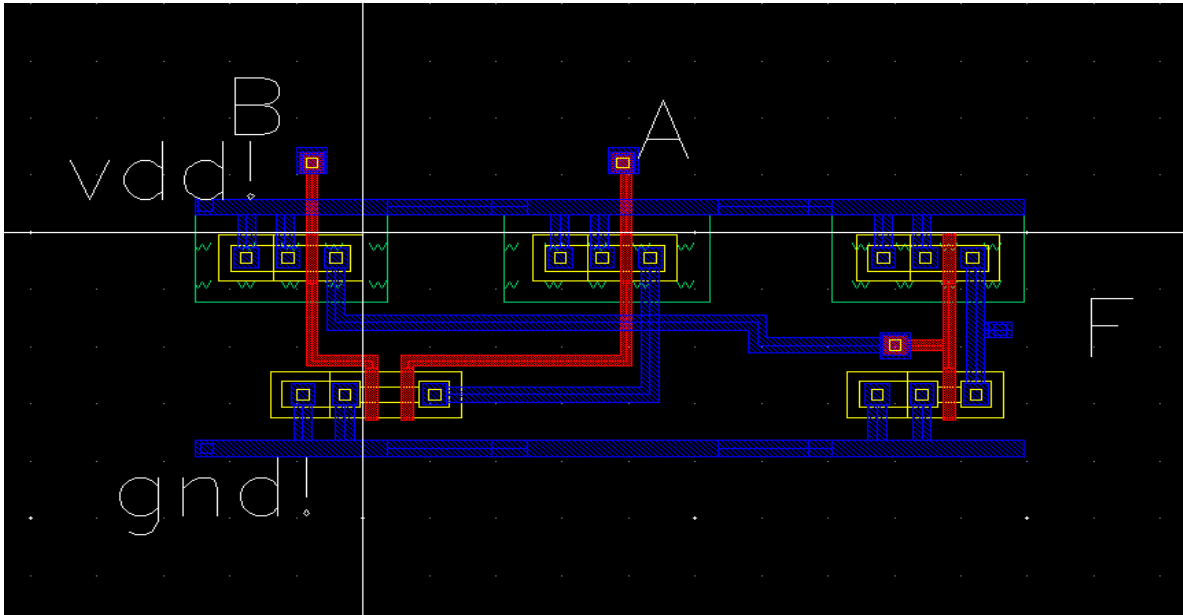
David Zemon

Table of Contents

AND

Layout

Specifications

Total Area: $A = 4.5\,\mu m \times 12.465\,\mu m = 56.093\,\mu m^2$

Power Consumption: $P = 40\,mA \cdot 2.2\,V + 31\,mA \cdot 2.2\,V = 75\,mW$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/and/LVS/layout/netlist
      count
      7             nets
      5             terminals
      3             pmos
      3             nmos

    Net-list summary for /tmp/davidzGit/project/and/LVS/schematic/netlist
      count
      7             nets
      5             terminals
      3             pmos
      3             nmos


    Terminal correspondence points
    N5        N3        A
    N4        N2        B
    N3        N5        F
    N2        N1        gnd!
    N6        N0        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
```

```
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.

                        layout  schematic
                        instances
      un-matched        0       0
      rewired                   0       0
      size errors       0       0
      pruned            0       0
      active            6       6
      total             6       6

                          nets
      un-matched        0       0
      merged            0       0
      pruned            0       0
      active            7       7
      total             7       7

                        terminals
      un-matched        0       0
      matched but
      different type            1       1
      total             5       5
```

NAND

Layout

Specifications

Total Area: $A = 4.86\,\mu m\ x\ 9.0\,\mu m = 43.74\,\mu m^2$

Power consumption: $P = 334.3\,\mu A \cdot 1.8\,V + 41.31\,\mu A \cdot 1.8\,V = 676.098\,mW$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/nand/LVS/layout/netlist
      count
      6             nets
      5             terminals
      2             pmos
      2             nmos

    Net-list summary for /tmp/davidzGit/project/nand/LVS/schematic/netlist
      count
      6             nets
      5             terminals
      2             pmos
      2             nmos


    Terminal correspondence points
    N4            N7            A
    N3            N2            B
    N2            N6            F
    N1            N1            gnd!
    N5            N0            vdd!

Devices in the netlist but not in the rules:
      pcapacitor
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.
                          layout   schematic
                          instances
      un-matched            0        0
      rewired                        0         0
      size errors           0        0
      pruned                0        0
      active                4        4
      total                 4        4

                            nets
      un-matched            0        0
      merged                0        0
      pruned                0        0
      active                6        6
      total                 6        6

                          terminals
      un-matched            0        0
      matched but
      different type                 0         0
      total                 5        5
```
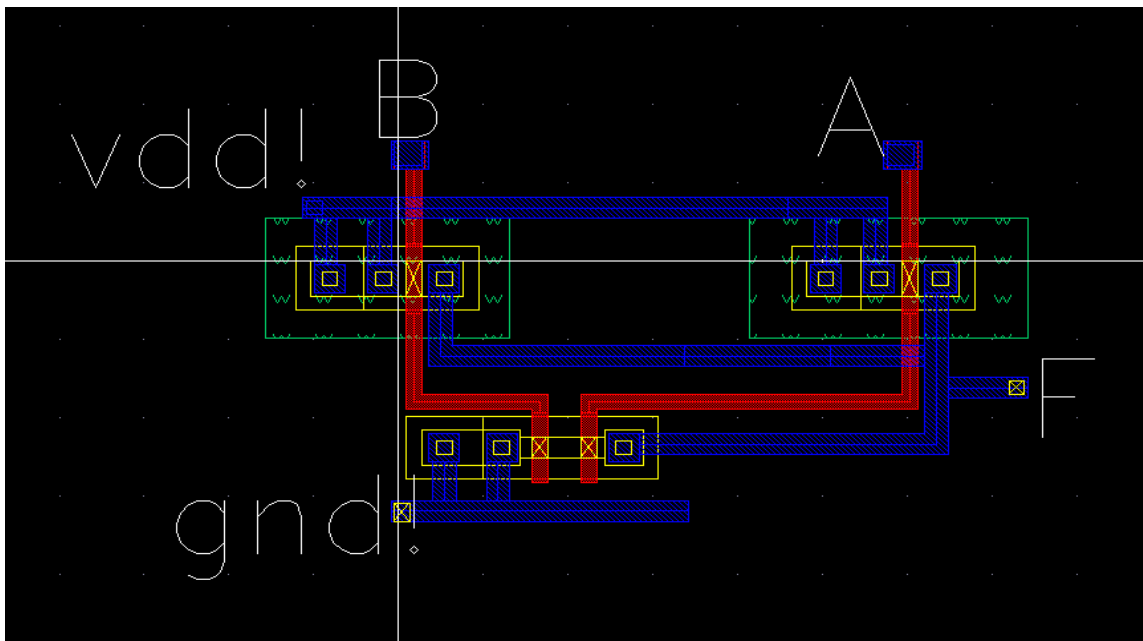
OR

Layout

Specifications

Total Area: $A = 4.545\,\mu m\ x\ 11.475\,\mu m = 52.154\,\mu m^2$

Power Consumption: $P = 89.97\,\mu A \cdot 1.8\,V + 560.97\,\mu A \cdot 1.8\,V = 1{,}171.692\,mW$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/or/LVS/layout/netlist
      count
      7              nets
      5              terminals
      3              pmos
      3              nmos

    Net-list summary for /tmp/davidzGit/project/or/LVS/schematic/netlist
      count
      7              nets
      5              terminals
      3              pmos
      3              nmos


    Terminal correspondence points
    N5        N2        A
    N4        N5        B
    N3        N3        F
    N2        N0        gnd!
    N6        N1        vdd!

Devices in the rules but not in the netlist:
```

```
      cap nfet pfet nmos4 pmos4
The net-lists match.

                      layout  schematic
                        instances
      un-matched          0      0
      rewired                    0      0
      size errors         0      0
      pruned              0      0
      active              6      6
      total               6      6

                        nets
      un-matched          0      0
      merged              0      0
      pruned              0      0
      active              7      7
      total               7      7

                      terminals
      un-matched          0      0
      matched but
      different type             0      0
      total               5      5
```
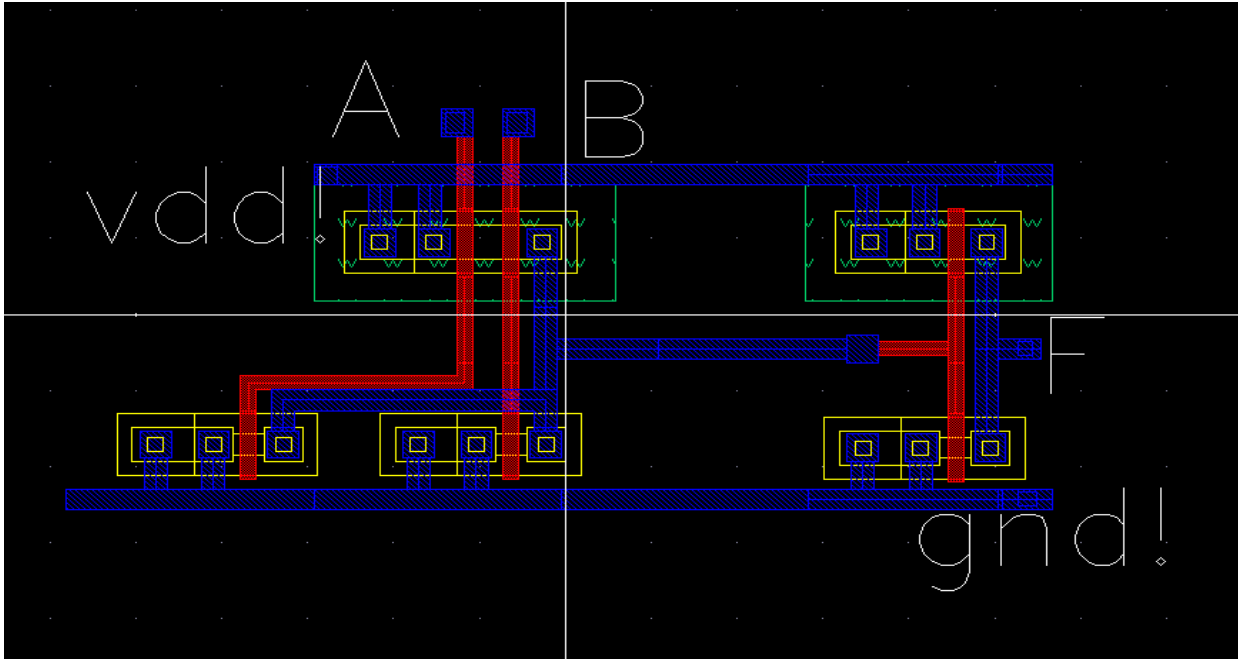
NOR

Layout:

Specifications

Total Area: $A = 5.265\ \mu m\ x\ 7.245\ \mu m = 38.145\ \mu m^2$

Power Consumption: $P = 532.08\ \mu A \cdot 1.8\ V + 87.703\ \mu A \cdot 1.8\ V = 1{,}115.609\ mW$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/nor/LVS/layout/netlist
      count
      6              nets
      5              terminals
      2              pmos
      2              nmos

    Net-list summary for /tmp/davidzGit/project/nor/LVS/schematic/netlist
      count
      6              nets
      5              terminals
      2              pmos
      2              nmos


    Terminal correspondence points
    N4          N7          A
    N3          N5          B
    N2          N2          F
    N1          N1          gnd!
    N5          N0          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout   schematic
                            instances
        un-matched          0        0
        rewired                      0        0
        size errors         0        0
        pruned              0        0
        active              4        4
        total               4        4

                             nets
        un-matched          0        0
        merged              0        0
        pruned              0        0
        active              6        6
        total               6        6

                            terminals
        un-matched          0        0
        matched but
        different type               0        0
        total               5        5
```
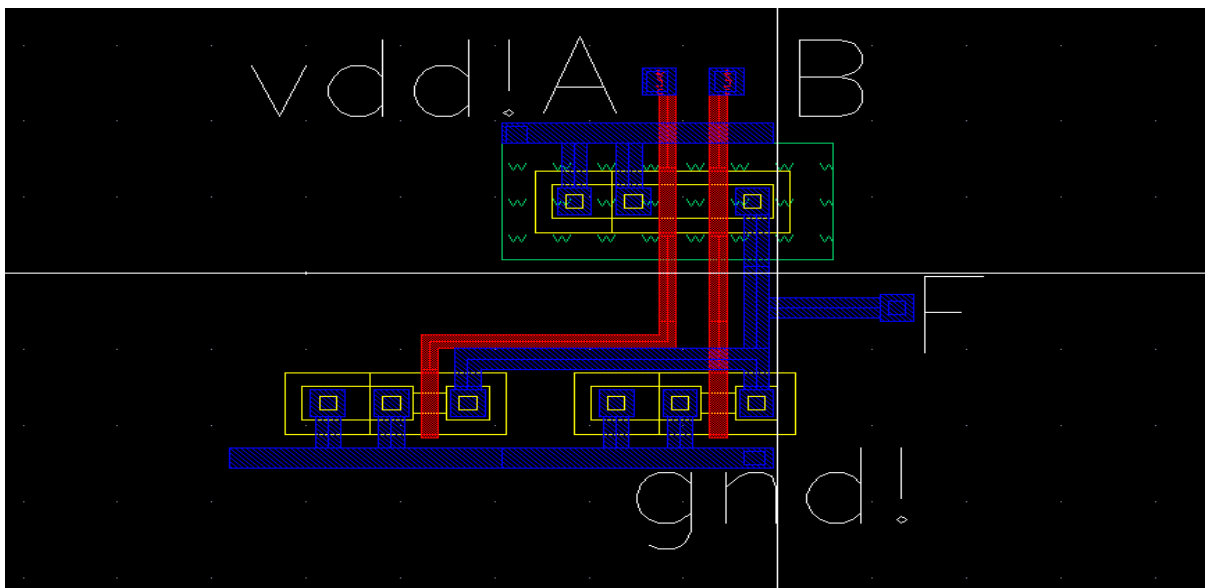
XNOR

Layout

Specifications

Total Area: $A = 12.825 \, \mu m \, x \, 33.795 \, \mu m = 433.421 \, \mu m^2$

Power Consumption: $P = 665.82 \, \mu A \cdot 1.8 \, V = 1,198.476 \, mW$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/xnor/LVS/layout/netlist
        count
        16              nets
        5               terminals
        12              pmos
        12              nmos

    Net-list summary for /tmp/davidzGit/project/xnor/LVS/schematic/netlist
        count
        16              nets
        5               terminals
        12              pmos
        12              nmos


    Terminal correspondence points
    N14         N3          A
    N13         N5          B
    N12         N4          F
    N11         N0          gnd!
    N15         N1          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4
```

```
The net-lists match.

                        layout   schematic
                          instances
        un-matched      0        0
        rewired                  0        0
        size errors     0        0
        pruned          0        0
        active          24       24
        total           24       24

                          nets
        un-matched      0        0
        merged          0        0
        pruned          0        0
        active          16       16
        total           16       16

                          terminals
        un-matched      0        0
        matched but
        different type           0        0
        total           5        5
```
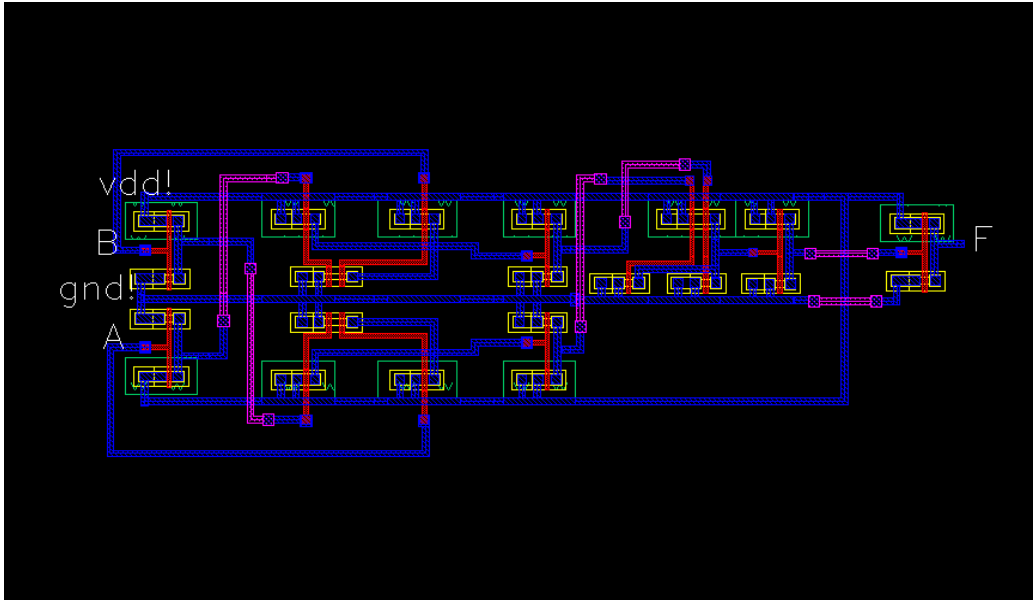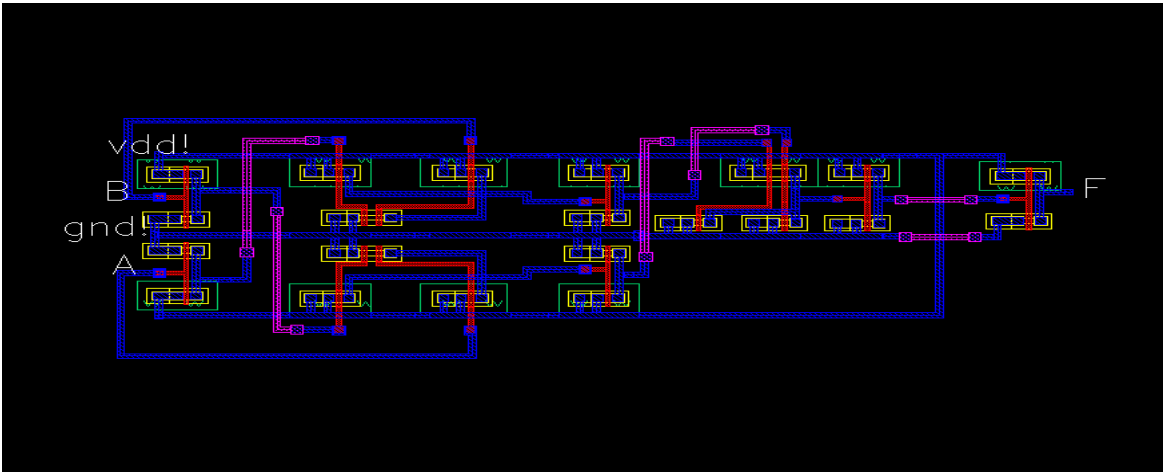
XOR

Layout

Specifications

Total Area: $34.11\,\mu m \times 12.375\,\mu m = 422.111\,\mu m^2$

Power Consumption: $P = 666.48\,\mu A \cdot 1.8\,V = 1,199.664\,\mu W$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/xor/LVS/layout/netlist
      count
      15          nets
      5           terminals
      11          pmos
      11          nmos
```

```
    Net-list summary for /tmp/davidzGit/project/xor/LVS/schematic/netlist
      count
    15          nets
    5           terminals
    11          pmos
    11          nmos


    Terminal correspondence points
    N13       N6          A
    N12       N7          B
    N11       N3          F
    N10       N1          gnd!
    N14       N0          vdd!
Devices in the netlist but not in the rules:
      pcapacitor
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.

                        layout  schematic
                        instances
    un-matched          0       0
    rewired                     0       0
    size errors         0       0
    pruned              0       0
    active              22      22
    total               22      22

                         nets
    un-matched          0       0
    merged              0       0
    pruned              0       0
    active              15      15
    total               15      15

                        terminals
    un-matched          0       0
    matched but
    different type              0       0
    total               5       5
```
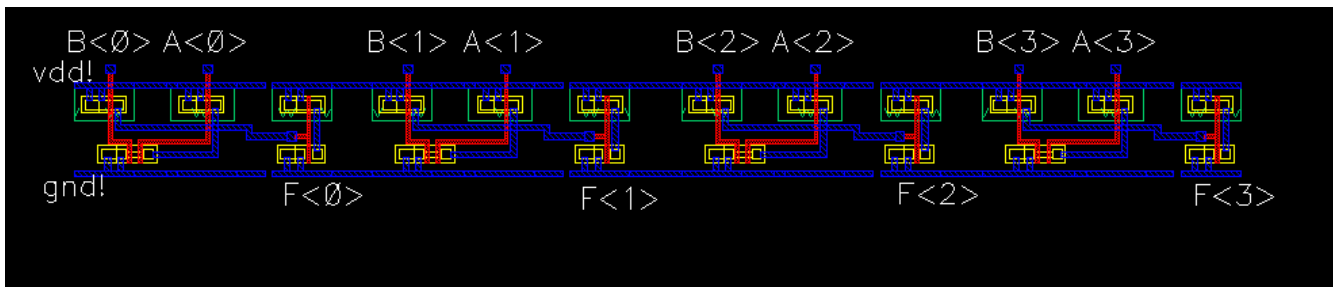
4-Input AND

Layout

Specifications

Total Area: $A = 5.49\,\mu m \times 56.385\,\mu m = 309.554\,\mu m^2$

Power Consumption: $P = 343.76\,\mu A \cdot 1.8\,V + 359.4\,\mu A \cdot 1.8\,V + 349.56\,\mu A \cdot 1.8\,V = 1{,}959.3432\,\mu W$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/4bit_and/LVS/layout/netlist
      count
      22          nets
      14          terminals
      12          pmos
      12          nmos

    Net-list summary for /tmp/davidzGit/project/4bit_and/LVS/schematic/netlist
      count
      22          nets
      14          terminals
      12          pmos
      12          nmos


    Terminal correspondence points
    N15        N10        A<0>
    N13        N12        A<1>
    N11        N13        A<2>
    N8         N11        A<3>
    N20        N6         B<0>
    N18        N8         B<1>
    N17        N9         B<2>
    N16        N7         B<3>
    N12        N3         F<0>
    N9         N2         F<1>
    N21        N4         F<2>
    N19        N5         F<3>
    N10        N1         gnd!
    N14        N0         vdd!

Devices in the netlist but not in the rules:
       pcapacitor
Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4

The net-lists match.

                        layout   schematic
                        instances
       un-matched       0        0
       rewired                   0        0
       size errors      0        0
       pruned           0        0
       active           24       24
       total            24       24


                          nets
       un-matched       0        0
       merged           0        0
       pruned           0        0
       active           22       22
       total            22       22


                        terminals
       un-matched       0        0
       matched but
       different type            0        0
       total            14       14
```
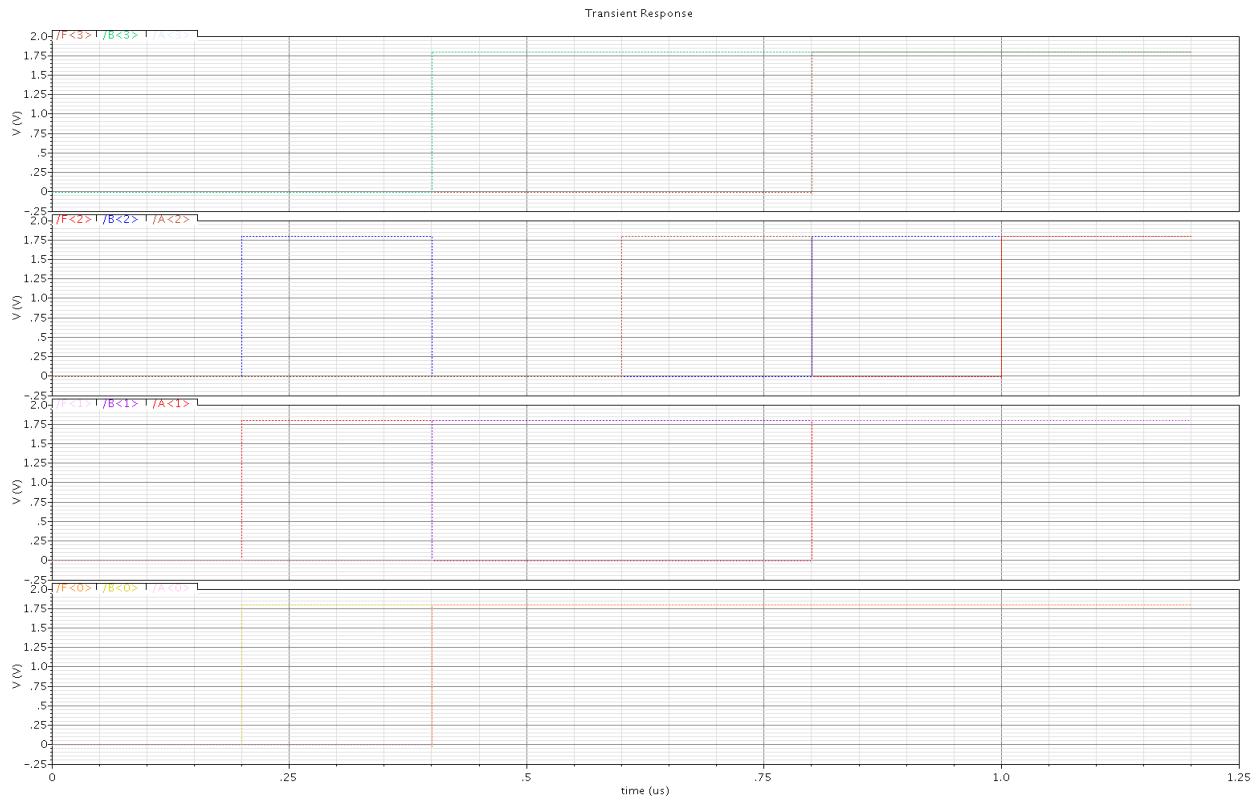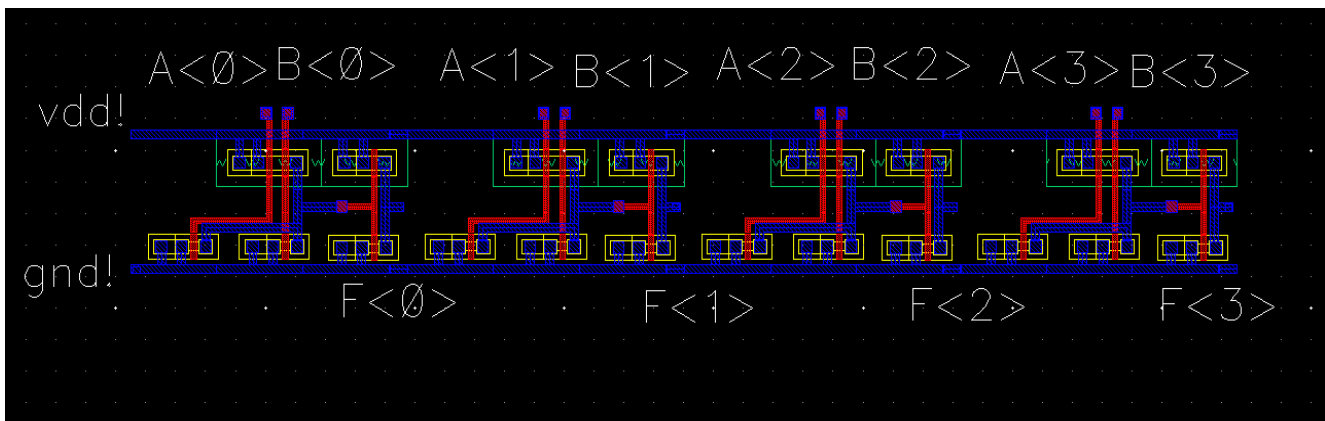
Post Layout Simulation

4-Input OR

Layout

Specifications

Total Area: $A = 4.54\,\mu m \times 37.035\,\mu m = 168.139\,\mu m^2$

Power Consumption: $P = -7.835\,\mu A \cdot 1.8\,V + 778.04\,uA \cdot 1.8\,V + 776.5\,\mu A \cdot 1.8\,V = 2{,}785.572\,\mu W$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/4bit_or/LVS/layout/netlist
      count
      22          nets
      14          terminals
      12          pmos
      12          nmos

    Net-list summary for /tmp/davidzGit/project/4bit_or/LVS/schematic/netlist
      count
      22          nets
      14          terminals
      12          pmos
      12          nmos


    Terminal correspondence points
    N15       N8        A<0>
    N13       N9        A<1>
    N11       N10       A<2>
    N8        N3        A<3>
    N20       N11       B<0>
    N18       N4        B<1>
    N17       N5        B<2>
    N16       N12       B<3>
    N12       N7        F<0>
    N9        N13       F<1>
    N21       N2        F<2>
    N19       N6        F<3>
    N10       N0        gnd!
    N14       N1        vdd!

Devices in the netlist but not in the rules:
      pcapacitor
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.

                      layout   schematic
                      instances
      un-matched      0        0
      rewired                  0        0
      size errors     0        0
      pruned          0        0
      active          24       24
      total           24       24

                        nets
      un-matched      0        0
      merged          0        0
      pruned          0        0
      active          22       22
      total           22       22

                      terminals
      un-matched      0        0
      matched but
      different type           0        0
      total           14       14
```
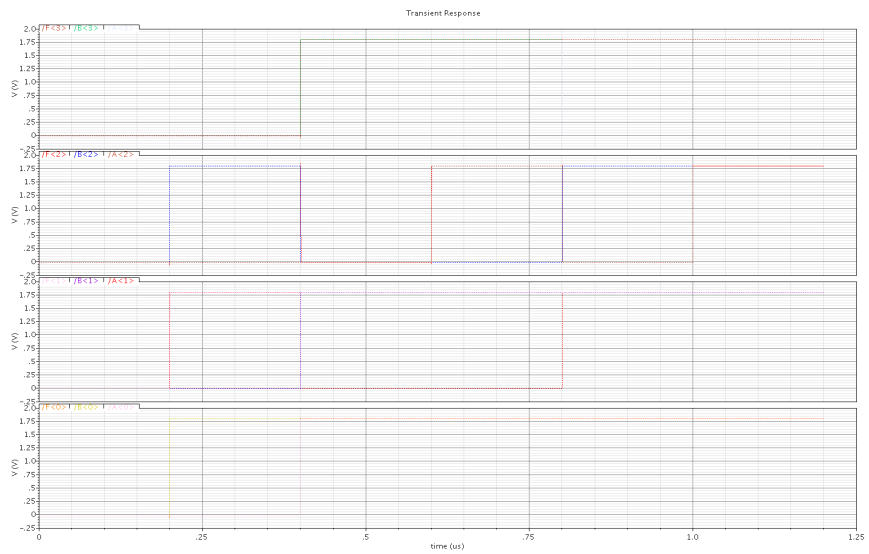
Post Layout Simulation

4-Input XNOR

Layout

Specifications

Total Area: $A = 38.07 \, \mu m \, x \, 64.53 \, \mu m = 2{,}456.657 \, \mu m^2$

Power Consumption:
$$P = 712.66 \, \mu A \cdot 1.8 \, V + 626.39 \, \mu A \cdot 1.8 \, V + 604.03 \, \mu A \cdot 1.8 \, V + 665.62 \, \mu A \cdot 1.8 \, V = 4{,}695.66 \, \mu W$$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/4b_xnor/LVS/layout/netlist
      count
      58            nets
      14            terminals
      48            pmos
      48            nmos

    Net-list summary for /tmp/davidzGit/project/4b_xnor/LVS/schematic/netlist
      count
      58            nets
      14            terminals
      48            pmos
      48            nmos


    Terminal correspondence points
    N50        N2          A<0>
    N49        N3          A<1>
    N47        N4          A<2>
    N44        N5          A<3>
    N56        N6          B<0>
    N54        N7          B<1>
    N53        N8          B<2>
    N52        N9          B<3>
    N48        N10         F<0>
    N45        N11         F<1>
    N57        N12         F<2>
    N55        N13         F<3>
    N46        N0          gnd!
    N51        N1          vdd!

Devices in the netlist but not in the rules:
      pcapacitor
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.

                        layout   schematic
                        instances
      un-matched        0        0
      rewired                    0        0
      size errors       0        0
      pruned            0        0
      active            96       96
      total             96       96


                        nets
      un-matched        0        0
      merged            0        0
      pruned            0        0
      active            58       58
      total             58       58


                        terminals
      un-matched        0        0
      matched but
      different type             0        0
      total             14       14
```
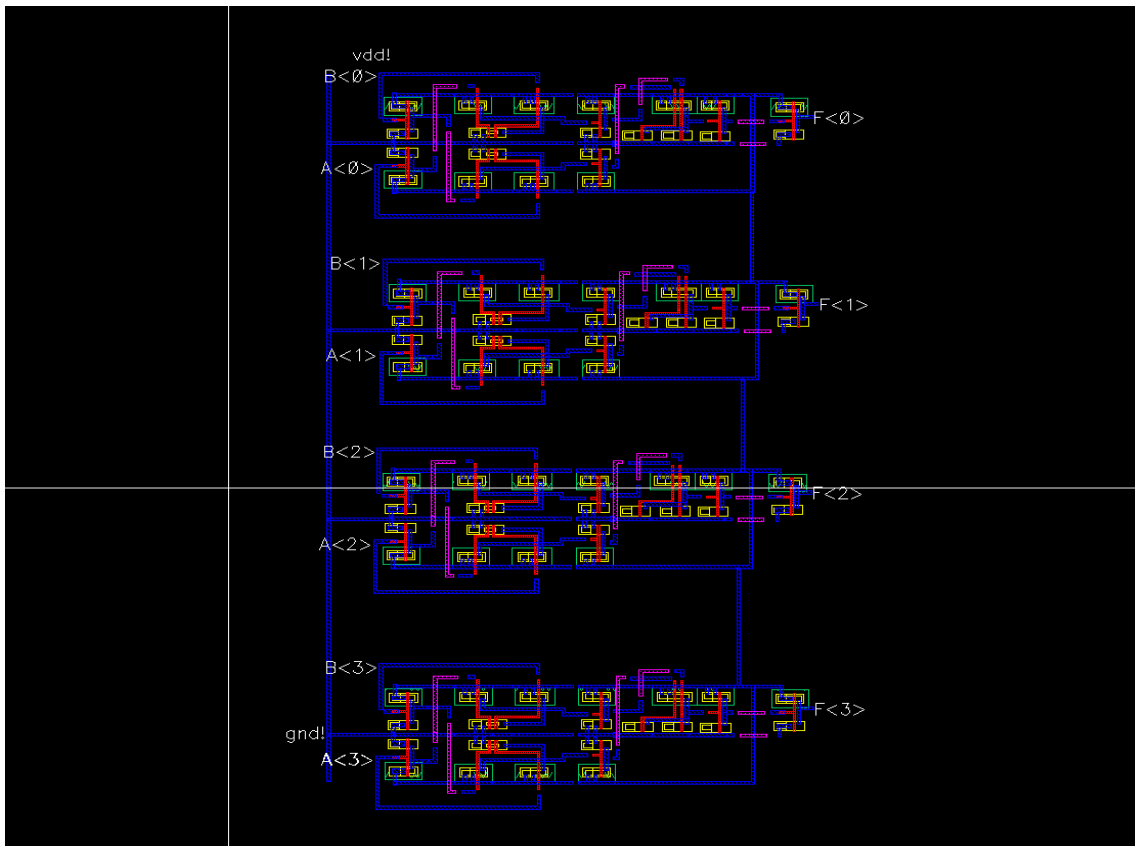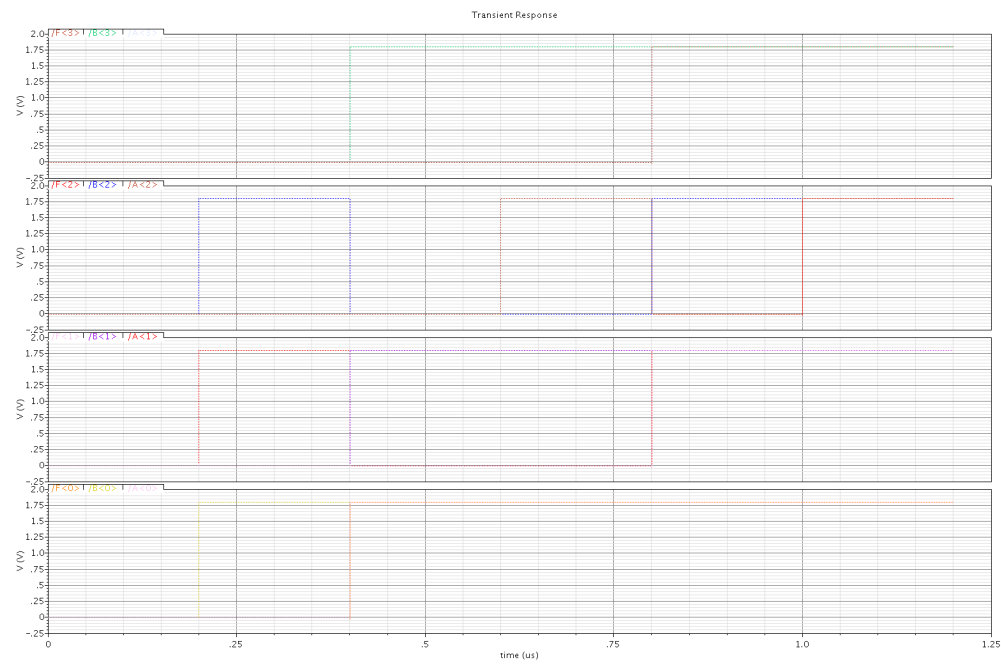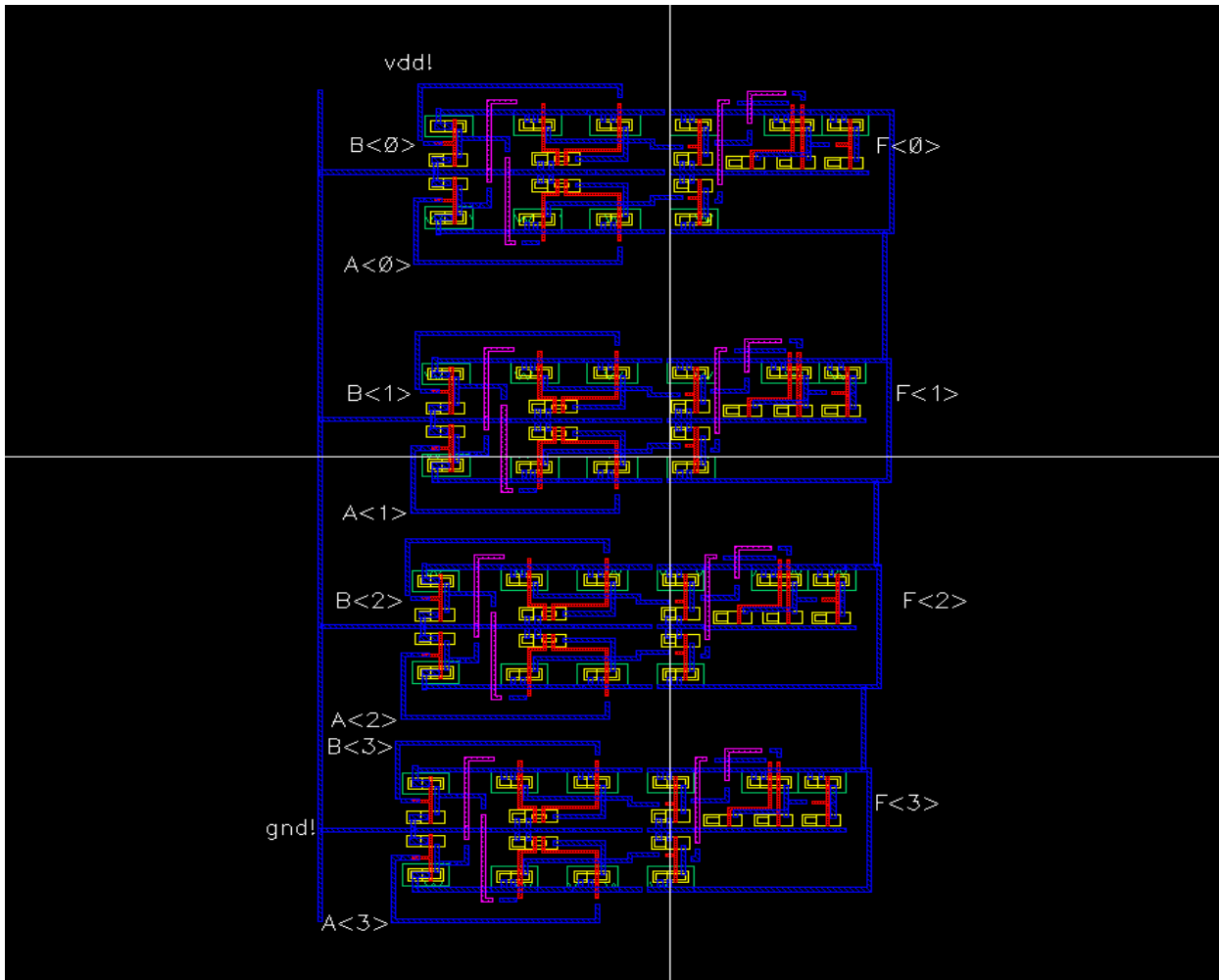
Post Layout Simulation

Transient Response

4-Input XOR

Layout

Specifications

Total Area: $A = 33.975 \, \mu m \, x \, 59.04 \, \mu m = 2{,}005.884 \, \mu m^2$

Power Consumption: $P = 602.94 \, \mu A \cdot 1.8 \, V = 1{,}085.292 \, \mu W$

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/4bit_xor/LVS/layout/netlist
      count
      54          nets
      14          terminals
      44          pmos
      44          nmos

    Net-list summary for /tmp/davidzGit/project/4bit_xor/LVS/schematic/netlist
      count
```

```
     54            nets
     14            terminals
     44            pmos
     44            nmos


   Terminal correspondence points
   N46       N3         A<0>
   N45       N4         A<1>
   N43       N2         A<2>
   N40       N13        A<3>
   N52       N8         B<0>
   N50       N7         B<1>
   N49       N6         B<2>
   N48       N5         B<3>
   N44       N9         F<0>
   N41       N10        F<1>
   N53       N11        F<2>
   N51       N12        F<3>
   N42       N1         gnd!
   N47       N0         vdd!

Devices in the netlist but not in the rules:
       pcapacitor
Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4

The net-lists match.

                      layout  schematic
                      instances
        un-matched       0       0
        rewired                  0        0
        size errors      0       0
        pruned           0       0
        active          88      88
        total           88      88


                        nets
        un-matched       0       0
        merged           0       0
        pruned           0       0
        active          54      54
        total           54      54


                      terminals
        un-matched       0       0
        matched but
        different type           0        0
        total           14      14
```
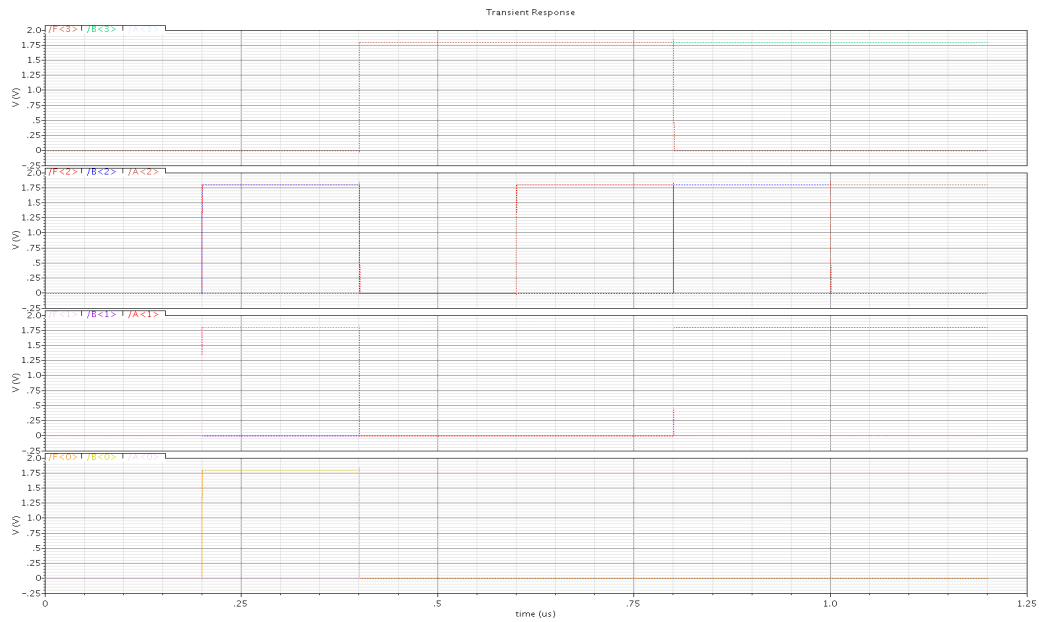
Post Layout Simulation

1-bit Full Adder

Layout

Specifications

Total Area: $A = 54.855\,\mu m \times 31.95\,\mu m = 1752.617\,\mu m^2$

Power Consumption:

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/1b_fullAdder/LVS/layout/netlist
      count
      36          nets
      5           terminals
      31          pmos
      31          nmos

    Net-list summary for /tmp/davidzGit/project/1b_fullAdder/LVS/schematic/netlist
      count
      36          nets
      7           terminals
      31          pmos
      31          nmos


    Terminal correspondence points
    N35         N2          A
    N34         N9          B
    N33         N4          Ci
    N32         N6          Co
    N31         N8          S

Devices in the netlist but not in the rules:
      pcapacitor
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.

                          layout  schematic
                          instances
      un-matched          0       0
      rewired                     0        0
      size errors         0       0
      pruned              0       0
      active              62      62
      total               62      62

                           nets
      un-matched          0       0
      merged              0       0
      pruned              0       0
      active              36      36
      total               36      36

                          terminals
      un-matched          0       0
      matched but
      different type              0       0
      total               5       7
```
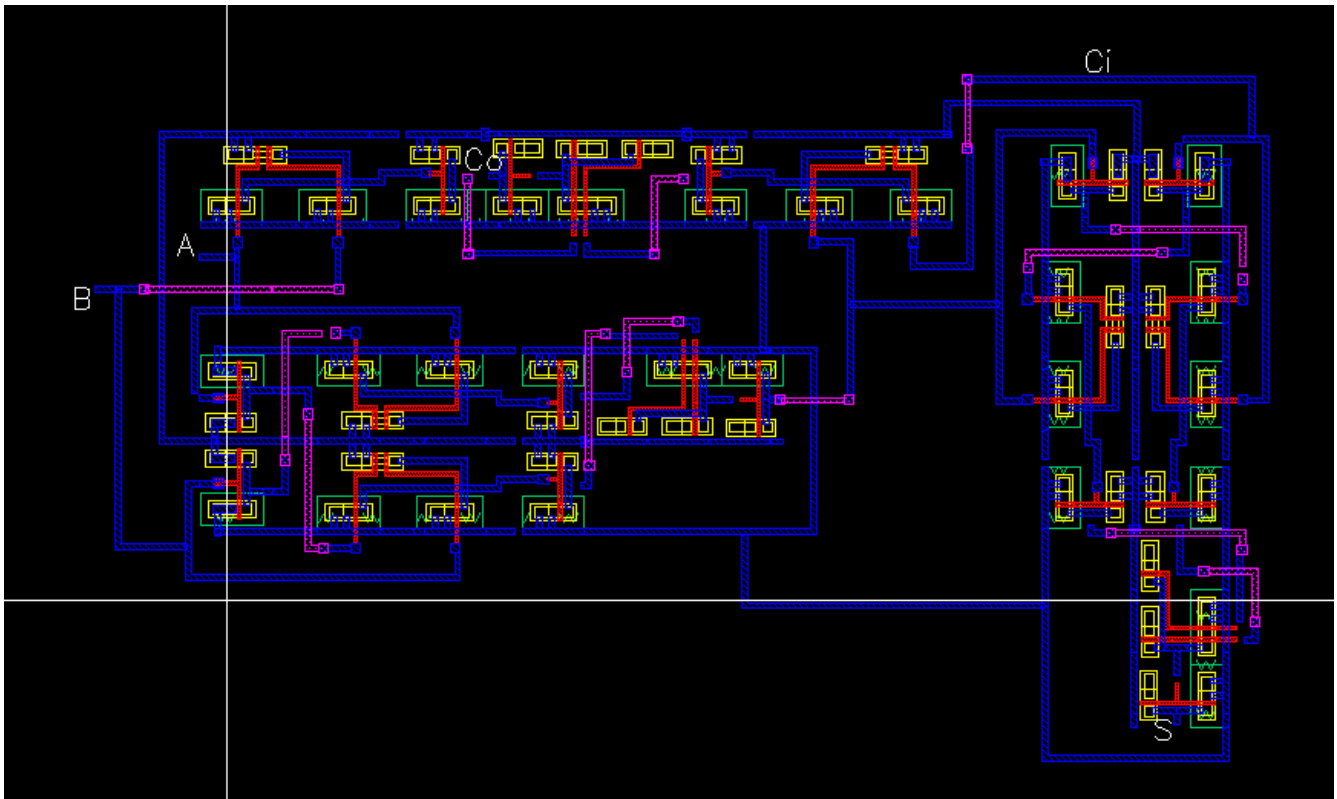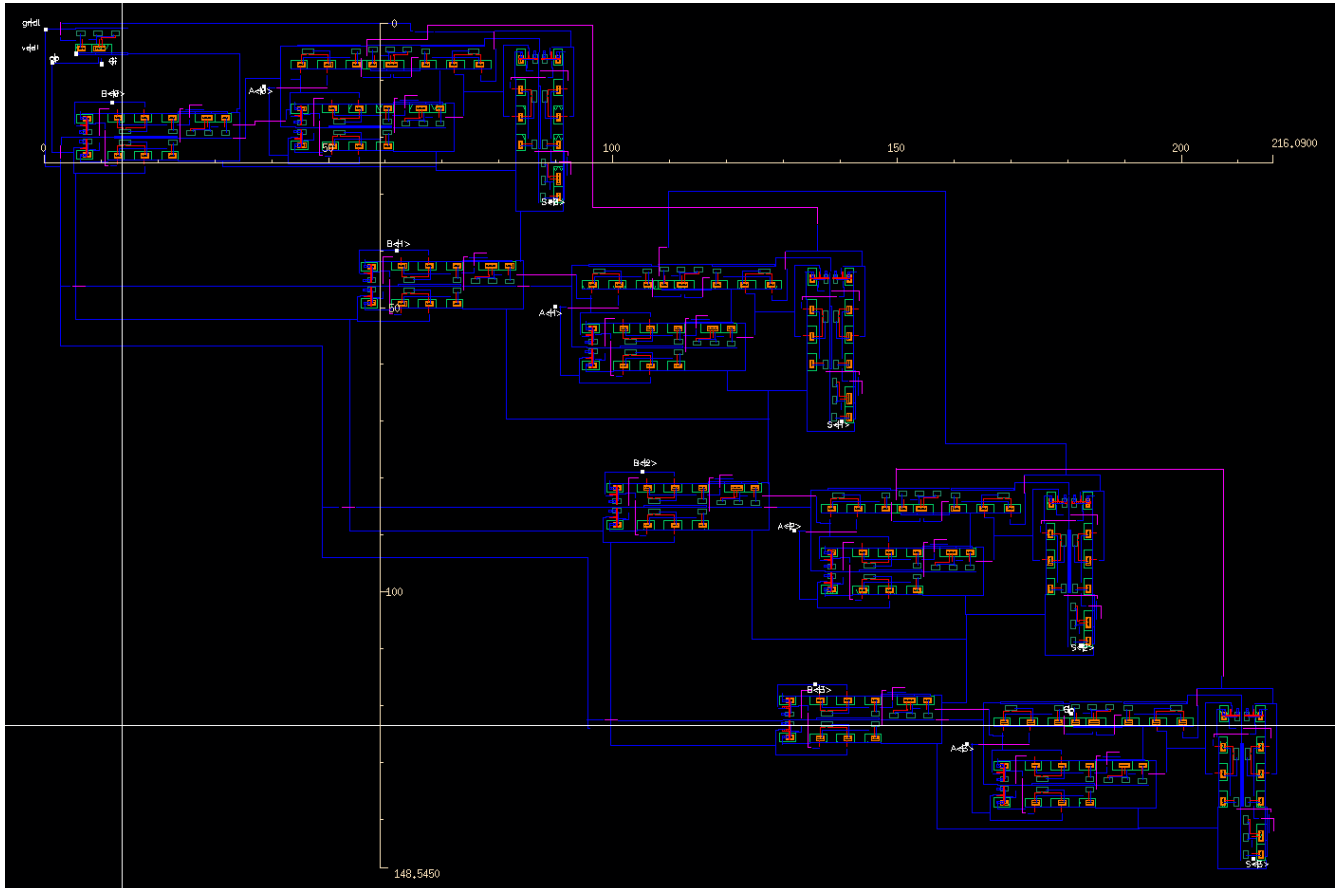
Post Layout Simulation

4-bit Adder/Subtracter

Layout

Specifications

Total Area: $A = 217.395\,\mu m\;x\;149.31\,\mu m = 32{,}459.247\,\mu m^2$

Power Consumption:

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /tmp/davidzGit/project/4b_adder_subtractor/LVS/layout/netlist
        count
        183          nets
        17           terminals
        171          pmos
        171          nmos

    Net-list summary for /tmp/davidzGit/project/4b_adder_subtractor/LVS/schematic/netlist
```

```
    count
    183           nets
    17            terminals
    171           pmos
    171           nmos


    Terminal correspondence points
    N177      N5        A<0>
    N173      N4        A<1>
    N169      N6        A<2>
    N166      N7        A<3>
    N182      N8        B<0>
    N181      N9        B<1>
    N180      N10       B<2>
    N179      N11       B<3>
    N175      N3        Ci
    N172      N21       Co
    N178      N12       S<0>
    N174      N13       S<1>
    N171      N14       S<2>
    N168      N15       S<3>
    N167      N1        gnd!
    N170      N24       op
    N176      N0        vdd!

Devices in the netlist but not in the rules:
      pcapacitor
Devices in the rules but not in the netlist:
      cap nfet pfet nmos4 pmos4

The net-lists match.

                        layout   schematic
                        instances
    un-matched          0        0
    rewired                      0        0
    size errors         0        0
    pruned              0        0
    active              342      342
    total               342      342

                          nets
    un-matched          0        0
    merged              0        0
    pruned              0        0
    active              183      183
    total               183      183

                        terminals
    un-matched          0        0
    matched but
    different type               0        0
    total               17       17
```

Post Layout Simulation