Introduction to VLSI
Final Report

11 December 2013

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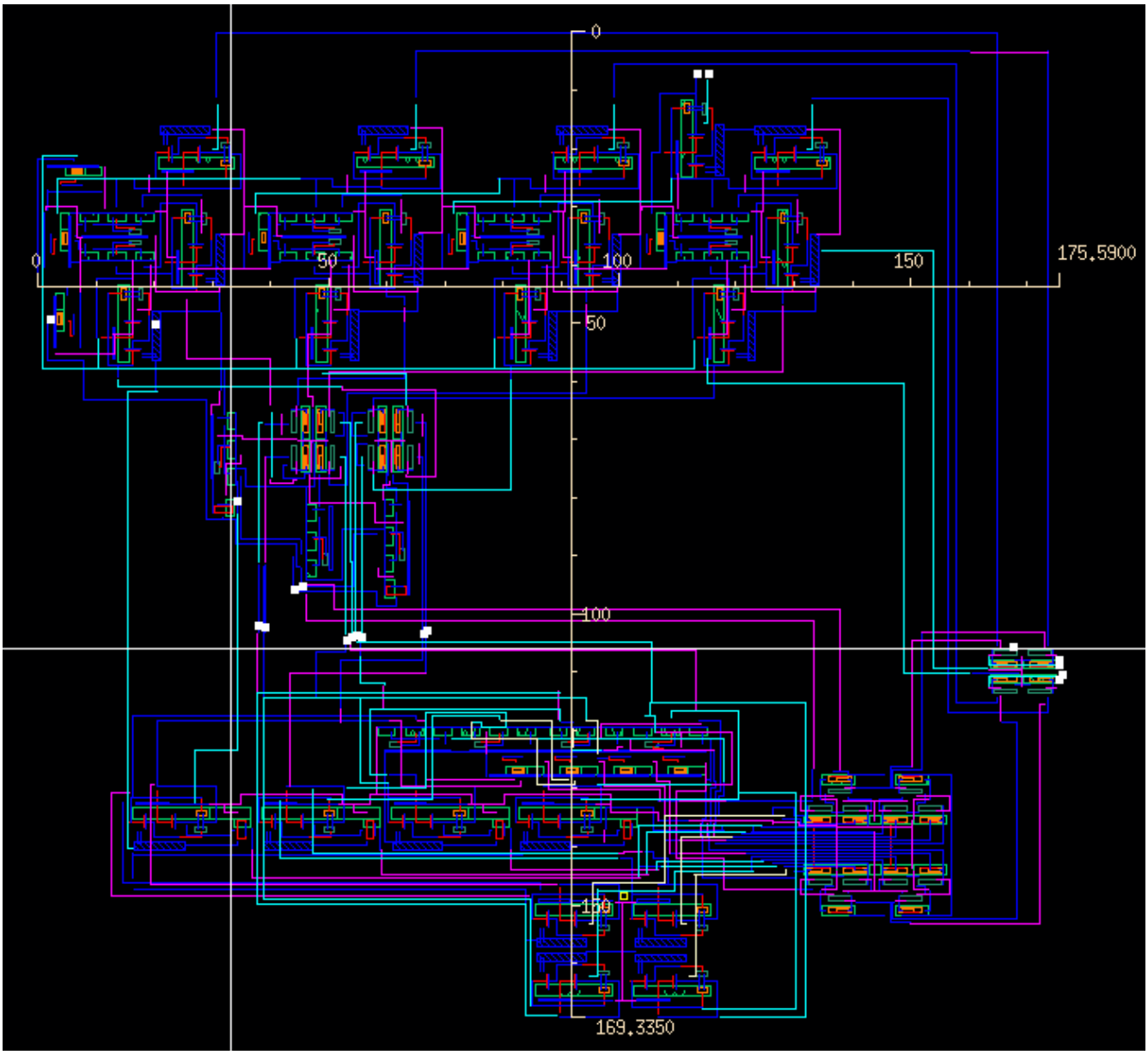
Layout Design



Total Area

$$Area = 175.59\,\mu m \cdot 169.335\,\mu m = 29{,}733\,\mu m^2$$

Total Power Consumption

$$P = 1.8 \cdot \left(V_{dd} + \sum_{i=0}^{3} A_i + \sum_{i=0}^{3} B_i + \sum_{i=0}^{2} Op_i + C_i \right) = 12.6135\,mW$$

Worst Case Propagation Delay

For worst case propagation delay, we chose to use the following input conditions:

$$A = 1111$$
$$B = 1111$$
$$C_i = 1$$
$$Op = 100(Add)$$
$$T = 10\,ns$$
$$t_{rise} = 10\,ps$$

This yielded a worst case delay of $t_p = 795\,ps$.