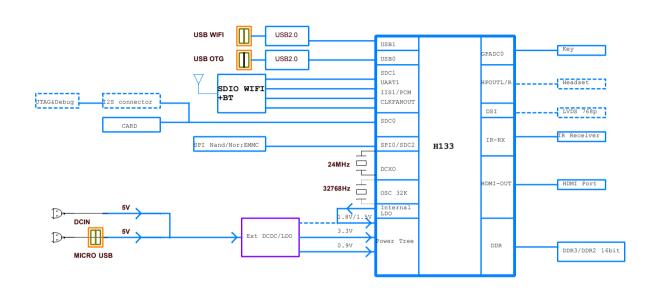
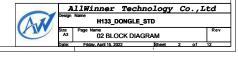
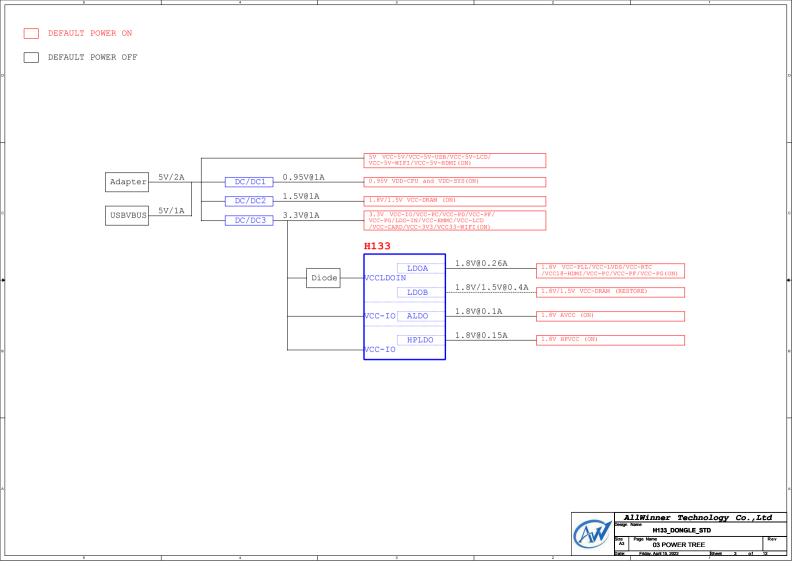
### Revision Description Date Drawn Checked Approved Index: Ver 0.1 2020-12-31 Releas version Ver 1.0 AddAW859 2021-04-07 YJY JIAYONG YINWET P01 VERSION HISTORY Add UART2 /5 and SPI test point P02 BLOCK DIAGRAM P03 POWER TREE Ver 1.1 ADD FALE FEL KEY 2021-11-21 WJH YJY YINWEI ADD DDR2 P04 GPIO ASSIGNMENT ADD USB WIFT ADD DCDC4 for dram P05 POWER P06 SOC1 Ver 1.2 Merge VDD-CPU and vdd-SYS 2022-01-05 WJH YJY YINWEI P07 SOC2 PO8 DDR3 VCC-DRAM change to ext DCDC P09 FLASH Change the DCDC-EN for power -sequency in Merge Ver 1.3 2022-02-25 WJH YJY YINWEI P10 AUDIO VDD-CPU AND VDD-SYS. P11 USB CARD HDMI DELETE SPDIF IN Fuction P12 WIFI BT Ver 1.4 2022-04-12 WJH YJY YINWEI Delete SGM809 OPTIONAL P13 DDR2 P14 USB WIFI AllWinner Technology Co., Ltd H133 DONGLE STD 01 VERSION HISTORY

**VERSION HISTORY** 

# BLOCK





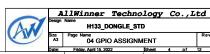


# **GPIO ASSIGNMENT**

Ball Number	Ball Name	GPIO Multiplex Function	Ball Numbe	
15	PB0	PWM3/IR_TX/TWI2_SCK/SPI1_WP/DBI_TE/UART0_TX/UART2_TX/SPDIF_OUT/PB_EINT0	B8	PG0
014	PB1	PWM4/I2S2_DOUT3/TWI2_SDA/I2S2_DIN3/UART0_RX/UART2_RX/IR_RX/PB_EINT1	C9	PG1
013	PB8	DMIC_DATA3/PWM5/TW12_SCK/SP11_HOLD/DBI_DCX/DBI_WRX/ UART0_TX/UART1_TX/PB_EINT8	A8	PG2
214	PB9	DMIC DATA2/PWM6/TWI2 SDA/SPI1 MISO/DBI SDI/DBI TE/DBI DCX/	В7	PG3
	-	UARTO_RX/UART1_RX/PB_EINT9	A6	PG4
213	PB10	DMIC DATA1/PWM7/TWI0_SCK/SPI1_MOSI/DBI_SDO/CLK_FANOUT0/ UARTT RTS/PB EINT10	C7	PG5
315	PB11	DMIC DATAO/PWM2/TWIO_SDA/SPI1_CLK/DBI_SCLK/CLK_FANOUT1/ UARTI_CTS/PB_EINT11	B4 A3	PG6 PG7
B14	PB12	DMIC CLK/PWMO/SPDIF IN/SPI1 CS/DBI CSX/CLK FANOUT2/IR RX/PB EINT12	В3	PG8
			A2	PG9
Ball Number	Ball Name	GPIO Multiplex Function	C4	PG10
F3	PC2	SPIO CLK/SDC2 CLK/PC EINT2	В6	PG11
F2	PC3	SPIO CSO/SDC2 CMD/PC EINT3	C6	PG12
71	PC4	SPIO_MOSI/SDC2_D2/BOOT_SELO/PC_EINT4	B5	PG13
33	PC5	SPIO_MISO/SDC2_D1/BOOT_SEL1/PC_EINT5	C5	PG14
G2	PC6	SPIO_WP/SDC2_DO/UART3_TX/TWI3_SCK/DBG_CLK/PC_EINT6	A4	PG15
13	PC7	SPIO_HOLD/SDC2_D3/UART3_RX/TWI3_SDA/TCON_TRIG/PC_EINT7	B2	PG16
			C10	PG17
Ball Number	Ball Name	GPIO Multiplex Function	В9	PG18
N15	PD0	LCD0_D2/LVDS0_V0P/DSI_D0P/TWI0_SCK/PD_EINT0		
N14	PD1	LCD0_D3/LVDS0_V0N/DSI_D0N/UART2_TX/PD_EINT1	Ball Numbe	rBall N
M15	PD2	LCD0_D4/LVDS0_V1P/DSI_D1P/UART2_RX/PD_EINT2	B1	PF0
M14	PD3	LCD0_D5/LVDS0_V1n/DSI_D1n/UART2_RTS/PD_EINT3	C3	PF1
L15	PD4	LCD0_D6/LVDS0_V2P/DSI_CKP/UART2_CTS/PD_EINT4	C2	PF2
L14	PD5	LCD0_D7/LVDS0_V2N/DSI_CKN/UART5_TX/PD_EINT5	D3	PF3
K15	PD6	LCD0_D10/LVDS0_CKP/DSI_D2P/UART5_RX/PD_EINT6	D2	PF4
K14	PD7	LCD0_D11/LVDS0_CKN/DSI_D2N/UART4_TX/PD_EINT7	D1	PF5
J15	PD8	LCD0_D12/LVDS0_V3P/DSI_D3P/UART4_RX/PD_EINT8	E2	PF6
J14	PD9	LCDO D13/LVDSO V3N/DSI D3N/PWM6/PD EINT9		

.l Number	Ball Name	GPIO Multiplex Function					
В8	PG0	SDC1_CLK/UART3_TX/RGMII_RXCTRL/RMII_CRS_DV/PWM7/PG_EINT0					
C9	PG1	SDC1_CMD/UART3_RX/RGMII_RXD0/RMII_RXD0/PWM6/PG_EINT1					
A8	PG2	SDC1_D0/UART3_RTS/RGMII_RXD1/RMII_RXD1/UART4_TX/PG_EINT2					
в7	PG3	SDC1_D1/UART3_CTS/RGMII_TXCK/RMII_TXCK/UART4_RX/PG_EINT3					
A6	PG4	SDC1_D2/UART5_TX/RGMII_TXD0/RMII_TXD0/PWM5/PG_EINT4					
C7	PG5	SDC1_D3/UART5_RX/RGMII_TXD1/RMII_TXD1/PWM4/PG_EINT5					
В4	PG6	UART1_TX/TWI2_SCK/RGMII_TXD2/PWM1/PG_EINT6					
A3	PG7	UART1_RX/TWI2_SDA/RGMII_TXD3/SPDIF_IN/PG_EINT7					
В3	PG8	UART1_RTS/TWI1_SCK/RGMII_RXD2/UART3_TX/PG_EINT8					
A2	PG9	UART1_CTS/TWI1_SDA/RGMII_RXD3/UART3_RX/PG_EINT9					
C4	PG10	PWM3/TWI3_SCK/RGMII_RXCK/CLK_FANOUT0/IR_RX/PG_EINT10					
В6	PG11	I2S1_MCLK/TWI3_SDA/EPHY_25M/CLK_FANOUT1/TCON_TRIG/PG_EINT11					
C6	PG12	I2S1_LRCK/TWIO_SCK/RGMII_TXCTRL/RMII_TXEN/CLK_FANOUT2/PWM0/UART1_TX/PG_EINT12					
В5	PG13	I2S1_BCLK/TWI0_SDA/RGMII_CLKIN/RMII_RXER/PWM2/LEDC_DO/UART1_RX/PG_EINT13					
C5	PG14	I2S1_DINO/TWI2_SCK/MDC/I2S1_DOUT1/SPI0_WP/UART1_RTS/PG_EINT14					
A4	PG15	I2S1_DOUT0/TWI2_SDA/MDIO/I2S1_DIN1/SPI0_HOLD/UART1_CTS/PG_EINT15					
В2	PG16	IR_RX/TCON_TRIG/PWM5/CLK_FANOUT2/SPDIF_IN/LEDC_DO/PG_EINT16					
C10	PG17	UART2_TX/TWI3_SCK/PWM7/CLK_FANOUT0/IR_TX/UART0_TX/PG_EINT17					
В9	PG18	UART2_RX/TWI3_SDA/PWM6/CLK_FANOUT1/SPDIF_OUT/UART0_RX/PG_EINT18					
l Number	Ball Name	GPIO Multiplex Function					
B1	PF0	SDCO_D1/JTAG_MS/R_JTAG_MS/I2S2_DOUT1/I2S2_DINO/PF_EINTO					
C3	PF1	SDCO_DO/JTAG_DI/R_JTAG_DI/I2S2_DOUTO/I2S2_DIN1/PF_EINT1					
C2	PF2	SDCO_CLK/UARTO_TX/TWIO_SCK/LEDC_DO/SPDIF_IN/PF_EINT2					
D3	PF3	SDCO_CMD/JTAG_DO/R_JTAG_DO/I2S2_BCLK/PF_EINT3					
D2	PF4	SDCO_D3/UARTO_RX/TWIO_SDA/PWM6/IR_TX/PF_EINT4					
D1	PF5	SDC0 D2/JTAG CK/R JTAG CK/I2S2 LRCK/PF EINT5					

SPDIF\_OUT/IR\_RX/I2S2\_MCLK/PWM5/PF\_EINT6



#### **POWER 5V DCIN TO PS** OVP RP1 NC/0R R0805 USBVBUS DCIN-5V VCC-5V-USB OP1 VCC EV HDMI CP1 10uF-16V WPM2026 -3/TR SOT-23 CP3 10uF-16V CP4 10K RP2 100nF C0402 6K8-1% XBS104S14 OP2 C0402 C0603 R0402 R0402 SQD155\_270H MMRT3906LT1G NC. SOD155 270H118 10K R0402 RP6 66K5-1% R0402 GND PS DCDC1 VDD-CPU 2.2uH-2A VCC-3V3 LP200 250H100 CP8 CP9 100nF 10uF C0402 C0603 调立调调调调调调 RPZ 100K CP10 4.7uF-10V RP9 NC/0R NOTE:CPU R1=15K;Mount R3/R4/R5/C14; RP10 100K SOT23-5 RY3408/SY8088AAC R0402 COTEDNED SON SON VDD-CPUFB →>> VDD-CPUFB RP12 QR R0402 GND R5) CPU-P-PWM >> CPU-P-PWM dynamic voltage regulator For POWER-ON SEQUENCE Do not change GND PS DCDC2 Vout=0.6\*(1+R1/R2)+R1\*(0.6-Vpwm)/(R3+R4+R5) VDD-CPU VDD-SYS 100K 2.2uH-2A 1A R0402 VCC-3V3 / RP18 NC/100K CP15 4.7uF-10V DCDC2 CP16 RP37 0R R0603 C0603 SOT23-5 RY3408/SY8088AAQ RP2 SOT5P95B160 300H13020K-19 R1=30K,Default Voltage 1.5V for VCC-DRAM (Merge VDD-CPU and SYS) GND If DCDC2 use for VCC-DRAM . NC the CP18 RP18 RP22 (Green Block) Mount RP42 (Blue Block) If DCDC2 use for VDD-SYS, NC the RP42 (Blue Block) Mount the CP18 RP18 RP22 (Green Block) R1=12K,Default Voltage 0.96V for VDD-SYS (separate VDD-CPU and SYS)

2.2uH-2A 2A

RP3 20K 1 R0402 CP21 CP22 C0603 (1+81/827) R2 C0402 C0603

GND GND

Default 3.3V

LP200\_250H100 CP19\_20pFL

DCDC3

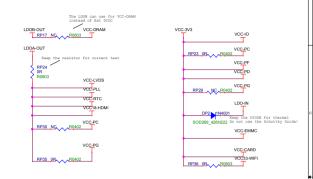
GND

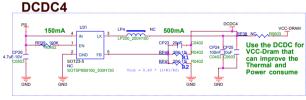
2 GND FB 5 SOT23-5 RY3420/SY8089AAAC SOT5P95B160\_300H130

700mA

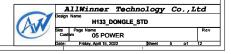
CP20 4.7uF-10V C0603

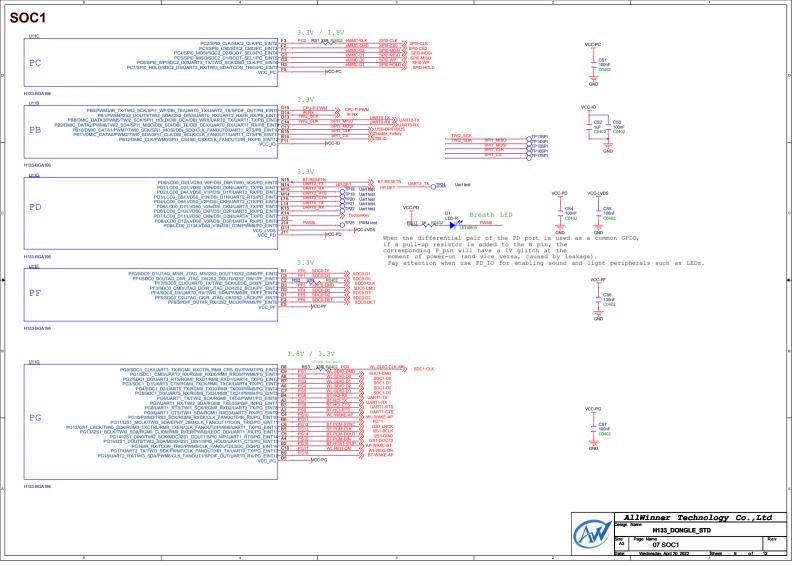
GND

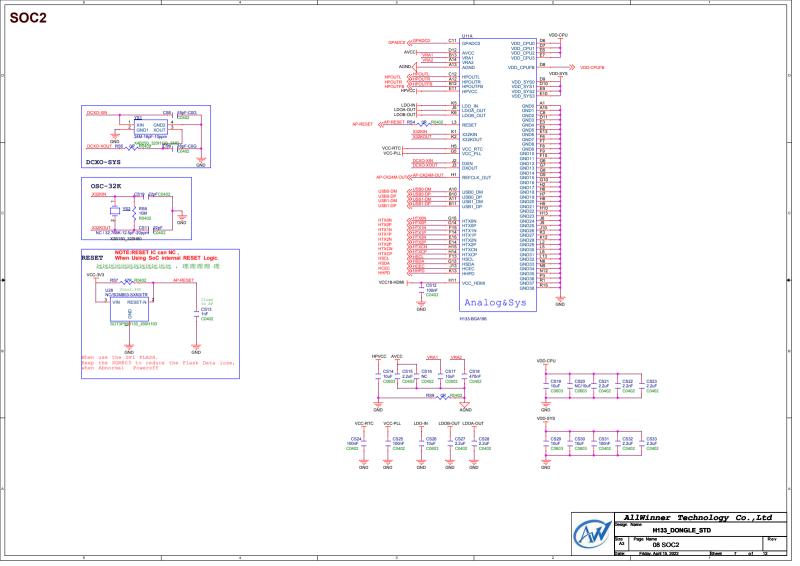


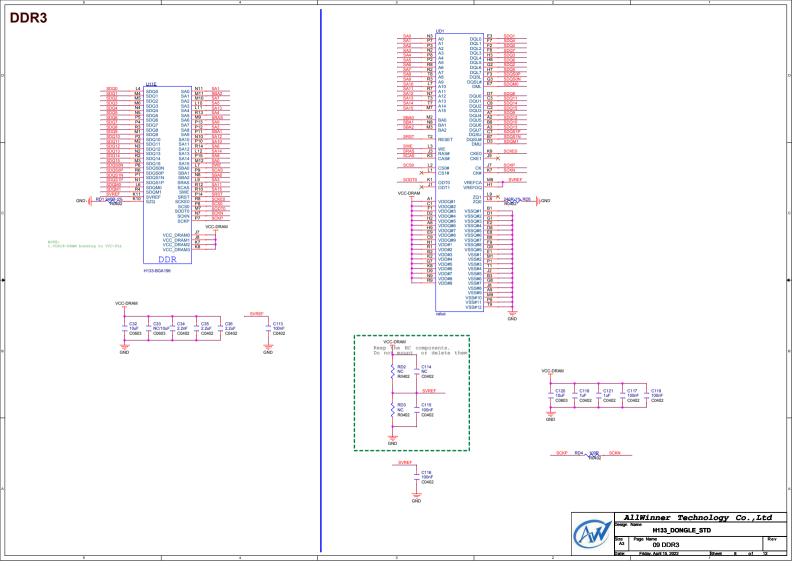


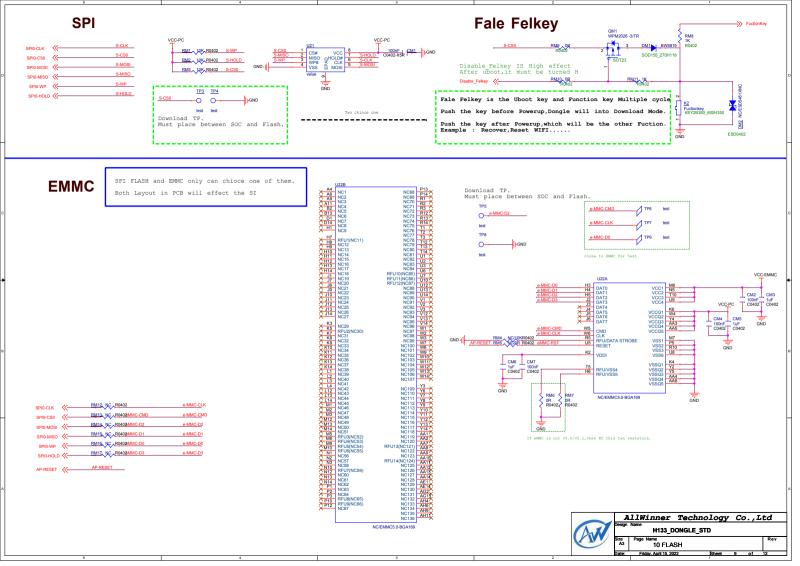
	DCDC1 (EXT)	DCDC2 (EXT)	DCDC3 (EXT)	DCDC4 (EXT)	LDOB (IN)	LDOA (IN)	REMARK
		VCC-DRAM 1.5/1.8V		NC		VCC-PLL VCC-RTC VCC-1V8	Merge VDD-CPU and VDD-SYS ,that Cpu-freqency below 900Mhz.The Power comsume is below2.5W@4K30,And the thermal will be very low.
Performance PLAN		0.9V		VCC-DRAM 1.5/1.8V		VCC-PLL VCC-RTC VCC-1V8	Separate VDD-CPU and VDD-SYS ,The Cpu-frequency upon to 1.2Ghz .The Power comsume is below2.5W@4K30,And the thermal will be very low.
	VDD-CPU VDD-SYS (0.95V)		VCC-WIFI VCC-3V3 LDOIN		VCC-DRAM 1.5/1.8V		Merge VDD-CFU and VDD-SYS ,that Cpu-freqency below 900Mhz.VCC-Dram be supplied by internal LDOB,instead of Ext DCDC.

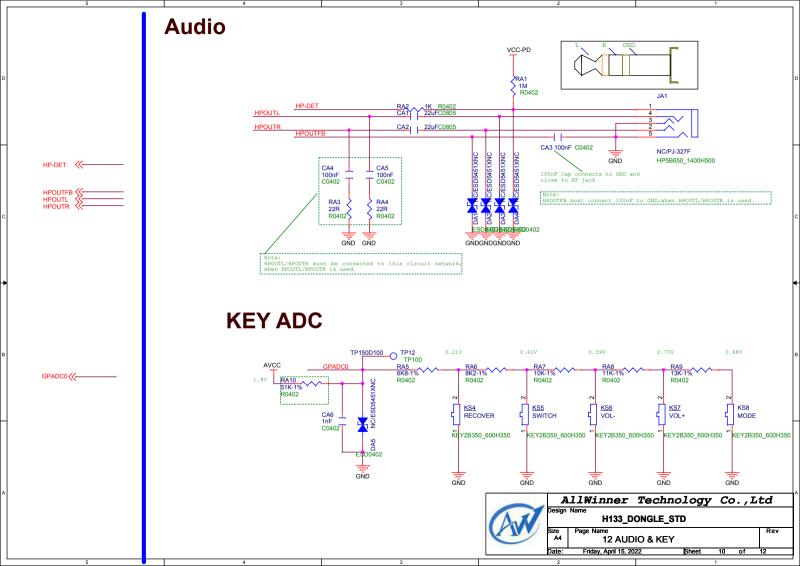


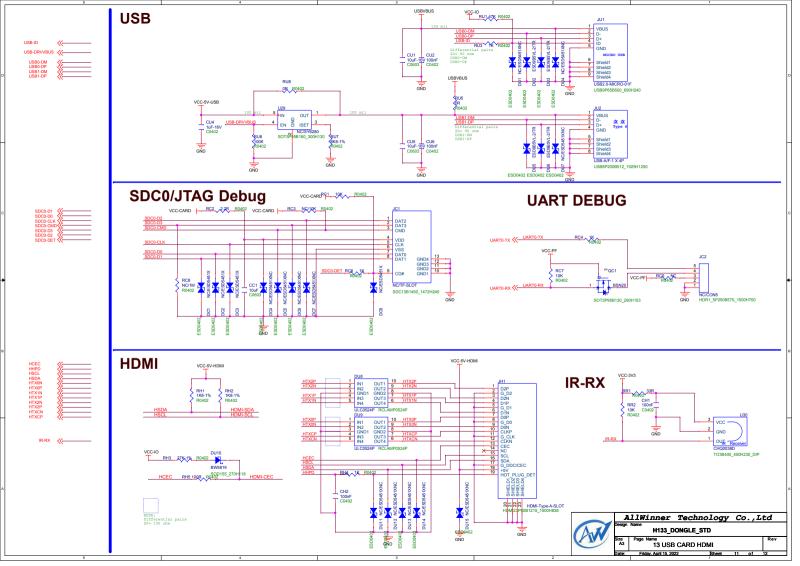


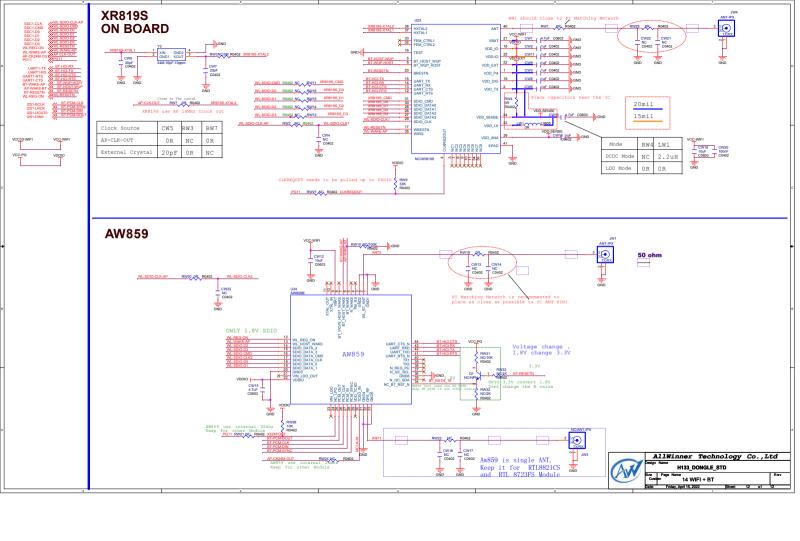












## DDR2 UD1 M8 A0 M7 A1 M7 A2 M8 A4 M3 A4 M5 A7 A5 A7 A6 A7 A7 A10 T A11 T A12 M8 A10 T A12 M8 A10 T A12 M8 A10 T A12 M8 A10 T A14 MC4 A15 MC6 A14 MC6 A15 DQ0 DQ1 DQ2 DQ3 DQ4 DQ6 DQ6 DQ7 LDQS LDQS# LDM SA0 N11 SA1 M10 SA2 L10 SA3 L11 SA4 R13 SA5 M9 SA6 P13 SA7 P12 SA8 P11 SA9 N10 SA10 P10 SA11 R14 SA12 R14 M4 SDQ0 M5 SDQ1 M6 SDQ2 N4 SDQ3 N5 SDQ4 N5 SDQ4 SDQ6 P4 SDQ6 R3 SDQ7 R3 SDQ8 R3 SDQ8 M1 SDQ8 P2 SDQ9 M2 SDQ10 N3 SDQ11 N3 SDQ112 SDQ12 SDQ13 R2 SDQ13 R2 SDQ14 M3 SDQ14 R6 SDQ50 P1 SDQ50P DQ8 DQ9 DQ10 DQ11 DQ12 DQ14 DQ15 UDQS UDQS# UDQS# K3 K7 L7 RAS# CAS# N1 SDQS1N L6 SDQS1P L6 SDQS1P SDQM0 K11 SDQM1 K10 SVREF SZQ L8 CS0# CKE0 GND | RD1 240R-1% VCC-DRAM A1 VDD1 J9 VDD2 M9 VDD3 R1 VDD4 VDD5 C1 VDDQ1 C3 VDDQ2 C7 VDDQ3 ODTO VREF VCC\_DRAM0 VCC\_DRAM1 VCC\_DRAM2 VCC\_DRAM3 VCC\_DRAM3 VSS1 NOTE: 1.VDD18-DRAM bonding to VCC-PLL VSS2 VSS3 VSS4 VSS5 VSSQ1 VSSQ2 VDDQ4 VDDQ5 VDDQ6 VDDQ7 DDR H133-RGA196 VDDQ8 VDDQ9 VDDQ10 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10 VSSL VDDL X E2 NC1 NC2 VCC-DRAM C32 10uF C33 NC/10uF C0603 C35 2.2uF C0402 C34 2.2uF C0402 C113 100nF VCC-DRAM Keep the NC components. Do not mount or delete them T C0402 C0603 C0402 GND C114 NC T C0402 VCC-DRAM RD2 NC/2K R0402 RD3 NC/2K R0402 GND SCKP RD4 100R SCKN \_\_\_ C116 100nF T C0402 AllWinner Technology Co., Ltd H133\_DONGLE\_STD 13 DDR2

