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Remark on the master's dissertation and the oral presentation

This master's dissertation is part of an exam. Any comments formulated by the assessment committee during the oral presentation of the master's dissertation are not included in this text.

Abstract

Lorem ipsum dolor sit amet, consectetur adipiscing elit, sed do eiusmod tempor incididunt ut labore et dolore magnam aliquam quaerat voluptatem. Ut enim aeque doleamus animo, cum corpore dolemus, fieri.

Table of contents

GLOSSARY

2X2 TUNABLE COUPLER	*A tunable coupler with two inputs and two outputs* 5
API	*Application Programming Interface* 11, 14, 15, 16, 17, 18, 19, 20, 23, 33
ASIC	*Application Specific Integrated Circuit* 16
CPLD	*Complex Programmable Logic Device* 3
CPU	*Central Processing Unit* 27
DRY	*Don't Repeat Yourself* 18, 47
DSL	*Domain Specific Language* 8, 11, 22, 23
DSP	*Digital Signal Processor* .....
ECS	*Entity-Component-System* .....
EDA	*Electronic Design Automation* 46, 49
FIR	*Finite Impulse Response* 5, 6
FPGA	*Field Programmable Gate Array* 1, 3, 8, 16, 23, 26, 27, 45, 48
FPPGA	*Field Programmable Photonic Gate Array* 3
FSR	*Free Spectral Range* 44
GPL-3.0	*GNU General Public License version 3.0* 21
GPU	*Graphics Processing Unit – also commonly used for highly parallel computing and machine learning* 27
HAL	*Hardware Abstraction Layer* 35, 36, 42, 46, 47, 49
HDL	*Hardware Description Language* 8, 10, 11, 12, 16, 17, 23, 24, 26, 27, 28
HLS	*High Level Synthesis* 22, 23, 27, 28
HPC	*High Performance Computing* 10
HTTP	*Hypertext Transfer Protocol – the protocol used for web navigation* 16
I/O	*Input/Output* .....
IC	*Integrated Circuit* 26
IDE	*Integrated Development Environment* 15
IIR	*Infinite Impulse Response* 5, 6
IP	*Intellectual Property* 17
JTAG	*Joint Test Action Group – A standard for testing integrated circuits* 13
LLVM	*Low Level Virtual Machine* 27
LSP	*Language Server Protocol* 15
LUT	*Look Up Table* 26, 47
MEMS	*Microelectromechanical Systems* 5
MZI	*Mach-Zehnder Interferometer* 36, 37, 48
PHÔS	*Photonic Hardware Description Language* 19, 21, 50
PIC	*Photonic Integrated Circuit* ..... IX, 1, 2, 3, 4, 17

PPA	*Power, Performance, Area*	27
PRG	*Photonics Research Group*	45
RF	*Radio Frequency*	1, 37, 39
RTL	*Register Transfer Level*	8, 26, 27, 28, 32
SPICE	*Simulation Program with Integrated Circuit Emphasis*	1, 2, 8, 16, 23, 45
SQL	*Structured Query Language*	8
TDD	*Test Driven Development*	16
VHDL	*VHSIC (*Very High Speed Integrated Circuit*) Hardware Description Language*	XI, 10, 21, 22, 28, 29
VHSIC	*Very High Speed Integrated Circuit*	VIII, XI, 10
VERILOG-A	*A continuous-time subset of Verilog-AMS (*Verilog for Analog and Mixed Signal*)*	2
VERILOG-AMS	*Verilog for Analog and Mixed Signal*	VIII, 2, 8, 10, 21, 22, 23, 33

List of figures

List of tables

List of listings

Accessibility in this document

Short overview of accessibility and readability features of this document.

Accessibility

This document was designed with accessibility to color blind and visually impaired people in mind. The colors used are generally chosen to have good contrast for color blind individuals, as can be seen here. Most colored elements are accompanied by an icon, generally from the unicode standard to make it screen reader friendly. Additionally, all images have alternate text descriptions.

Navigation

All elements and references are clickable for ease of navigation in the document. Additionally, all figures, table, glossary entries, and references are clickable and will take you to the appropriate section. External links, those being links that lead to a website, are highlighted in blue and underlined.

Info boxes

For improved readability and breaking up of the monotony of the text, this document uses info boxes. These boxes are used to highlight important information, such as definitions, remarks, conclusion and important hypotheses. Below you will find a full list of the different types of info boxes used in this document.

Definition: This is a **definition**, the word or phrase in bold is the term being defined. They are generally adapter from the literature and are used for important elements that are not common knowledge for photonic engineers.

Definition usually have a source in the footer

This is an info box, it contains information that is tangential or useful for the understanding of the document, but not essential.

This is a question box, it contains an important research question or hypothesis that is being investigated in the document.

The footer contains a link to where the question is answered.

This is a conclusion or summary box, it contains a summary with key information that are needed for subsequent sections. Additionally, this is where answers to questions and hypothesis are given.

1.
Introduction

TODO

1.1 Motivation

This section serves as the motivation for the research and development of appropriate abstractions and tools for the design of photonic circuits, especially as it pertains to the programming of so-called Photonic FPGAs (*Field Programmable Gate Array*) [3] or Photonic Processors. As with all other types of circuit designs, such as digital electronic circuits, analog electronic circuits and RF circuits, appropriate abstractions can allow the designer and/or engineer to focus on the functionality of their design rather than the implementation [4]. One may draw parallels between the abstraction levels used when designing circuits and the abstractions used when designing software. Most notably the distinction made in the software-engineering world between imperative and declarative programming. The former is concerned with the "how" of the program while the latter is focused on the "what" of the program [5].

At a sufficiently high level of abstraction, the designer is no longer focusing on the implementation details (imperative) of their design, but rather on the functionality and behavioural expectations of their design (declarative) [5]. In turn, this allows the designer to focus on what truly matters to them: the functionality of their design.

Currently, a lot of the work being done, on photonic circuits, is done at a very low level of abstraction, close to the component-level [6]. This leads to several issues for broader access to the fields of photonic circuit design. Firstly, it requires expertise and understanding of the photonic component, their physics and the, sometimes complex, relationship between all of their design parameters. Secondly, it requires a large amount of time and effort to design and simulate a photonic circuit. Physical simulation of photonic circuit is generally slow [6, 7], which has led to efforts to simulate photonic circuit using SPICE (*Simulation Program with Integrated Circuit Emphasis*) [8]. Finally, the design and implementation of photonic circuit is generally expensive, requiring taping-out of the design and working with a froundry for fabrication. This increases the cost, but also increases the time to market for the product [9].

This therefore means, that there is a large interest in constructing new abstractions, method of simulation and design tools for photonic circuit design. Especially for rapid prototyping and iteration of photonic circuits. This is the reason that research in the field of programmable photonics, and especially recirculating programmable photonics has had growing interest in the past few years. This master's thesis has for purpose to find new ways in which the user can easily design their photonic circuit and program them onto those programmable PICs (*Photonic Integrated Circuit*) [9].

Additionally, photonic circuits are often not the only component in a system. They are often used in conjunction with other technologies, such as analog electronics, used in driving the photonic components, digital electronic, to provide control and feedback loops and RF (*Radio Frequency*) to benefit from the high bandwidth, high speed capabilities of photonics [10]. Therefore, it is of interest to the user to co-simulate [6, 11] their photonic circuits with the other components of their systems. This is a problem that is partly addressed using SPICE simulation [8]. However, especially with regards to digital co-

simulation, SPICE tools are often lacking, making the process difficult [12], relying instead on alternatives such as Verilog-A (*A continuous-time subset of Verilog-AMS (*Verilog for Analog and Mixed Signal*)*).

In this work, the beginning of a solution to these problems will be offered by introducing a new way of designing photonic circuit using code, a novel way of simulating these circuits and a complete workflow for the design and programming of circuit will be presented. Finally, an extension of the simulation paradigm will be introduced, allowing for the co-simulation of the designs with digital electronics, which could, in time, be extended to analog electronics as well.

1.1.a Research questions

The main goal of this work is to design a system to program photonic circuits, this entails the following:

1. How to express the user's intent?
    - What programming languages and paradigms are best suited?
    - What workflows are best suited?
    - How does the user test and verify their design?
2. How to translate that intent into a programmable PIC configuration?
    - What does a compiler need to do?
    - How to support future hardware platforms?
    - What are the unit operations that the hardware platform must support?

The remainder of this work will be structured following these questions until the formulation of thorough answers to them; followed by a series of mockups to demonstrate the potential use of the workflow. Finally, demonstrations based on the prototype of the aforementioned workflow will be presented showing the potential and the capabilities of the simulation system.

2.
Programmable photonics

As previously mentioned in Section 1.1, the primary goal of this thesis is to find which paradigms and languages are best suited for the programming of photonic FPGAs. However, before discussing these topics in detail, it is necessary to start discussing the basic of photonic processors. This chapter will therefore start by discussing what photonic processors are, what niche they fill and how they work. From this, the chapter will then move on to discuss the different types of photonic processors and how they differ from each other. Finally, this chapter will conclude with the first and most important assumption made in all subsequent design decisions.

In this document, the names Photonic FPGA and Photonic Processor are used interchangeably. They are both used to refer to the same thing, that being a programmable photonic device. The difference is that the former predates the latter in its use. Sometimes, they are also called FPPGA (*Field Programmable Photonic Gate Array*) [13].

2.1 Photonic processors

In essence, a photonic FPGA or photonic processor is the optical analogue to the traditional digital FPGA. It is composed of a certain number of gates connected using waveguides, which can be programmed to perform some function [14]. However, whereas traditional FPGAs use electrical current to carry information, photonic processors use light contained within waveguide to perform analog processing tasks.

However, it is interesting to note that, just like traditional FPGAs, there are devices that are more general forms of programmable PIC (*Photonic Integrated Circuit*)[3] than others, just like CPLDs (*Complex Programmable Logic Device*) are less general forms of FPGAs. As any PIC that has configurable elements could be considered a programmable PIC, it is reasonable to construct a hierarchy of programmability, where the most general device is the photonic processor, which is of interest for this document, going down to the simplest tunable structures.

Therefore, looking at Figure 1, one can see that four large categories of PIC can be built based on their programmability. The first ones (a) are not programmable at all, they require no tunable elements and are therefore the simplest. The second category (b) contains circuits that have tunable elements but fixed function, the tunable element could be a tunable coupler, modulator, phase shifter, etc. and allows the designer to tweak the properties of their circuit during use, for purposes such as calibration, temperature compensation, signal modulation or more generally, altering the usage of the circuit. The third kind of PIC is the feedforward architecture (c), which means that the light is expected to travel in a specific direction, it is composed of gates, generally containing tunable couplers and phase shifters. Additionally, external devices such as high speed modulators, amplifiers and other elements can be added. Finally, the most generic kind of programmable PIC is the recirculating mesh (d), which, while also composed of tunable couplers and phase shifters, allows the light to travel in either direction, allowing for more general circuits to be built as explored in Section 2.1.g.

(a) (b) (c) (d)

FIGURE 1 A hierachy of programmable PICs (*Photonic Integrated Circuit*), starting at the non-programmable single function PIC (a), moving then to the tunable PIC (b), the feedfoward architecture (c) and finally to the photonic processor (d).

In this work, the focus will be on the fourth kind of tunability, the most generic. However, the work can also apply to photonic circuit design in general and is not limited to photonic processors. As will be discussed in Section 2.1.g, the recirculating mesh is the most general kind of programmable PIC, but also the most difficult to represent with a logic flow of operation due to the fact that the light can travel in either direction. Therefore, the following question may be asked:

> ? At a sufficiently high level of abstraction, can a photonic processor be considered to be equivalent to a feedforward architecture?
>
> This will be answered in Section 2.2.c.

This question, which will be the driving factor behind this first section, will be answered in Section 2.2.c. However, before answering this question, it is necessary to first discuss the different types of photonic processors and how they differ from each other. Additionally, the answer to that question will show that the solution suggested in this thesis is also applicable for feedfoward systems.

2.1.a COMPONENTS

As previously mentioned, a photonic gate consists of several components. This section will therefore discuss the different components that can be found in a photonic processor and how they work, as well as some of the more advanced components that can also be included as part of a photonic processor.

WAVEGUIDES

The most basic photonic component that is used in PICs is the waveguide. It is a structure that confines light within a certain area, allowing it to travel, following a pre-determined path from one place on the chip to another. Waveguides are, ideally, low loss, meaning that as small of a fraction of the light as possible is lost as it travels through the waveguide. They can also be made low dispersion allowing for the light to travel at the same speed regardless of its wavelength. This last point allows modulated signals to be transmitted without distortion, which is important for high speed communication.

TUNABLE 2X2 COUPLERS

A 2x2 tunable coupler is a structure that allows two waveguides to interact in a pre-determined way. It is composed of two waveguides whose coupling, that being the amount of light "going" from one waveguide to the other, can be controlled. There are numerous ways of implementing couplers. In Figure 2 an overview of the different modes of operation of a 2x2 coupler is given. It shows that, depending on user input, an optical coupler can be in one of three modes, the first one (b) is the bar mode, where there is little to no coupling between the waveguides, the second one (c) is the cross mode, where the light is mostly coupled from one waveguide to the other and the third one (d) is the partial mode, where the light is partially coupled from one waveguide to the other based on proportions given by the user.

The first mode (b), allows light to travel without interacting, allowing for tight routing of light in a photonic mesh. The second mode is also useful for routing, by allowing signals to cross with little to no interference. The final state allows the user to interfere two optical signals together based on predefined proportions. This is useful for applications such as filtering for ring resonators or splitting.

(a) (b) (c) (d)

Figure 2 Different states of a 2x2 optical coupler, (a) a simplified coupler, (b) in "bar" mode, (c) in "cross" mode, (d) in "partial" mode.

There are many construction techniques for building 2x2 couplers, each with their own advantages and disadvantages. The most common ones are the Mach-Zehnder interferometers with two phase shifters. However, other techniques involve the user of MEMS (*Microelectromechanical Systems*) or liquid crystals [3, 14, 15].

Detectors

todo

2.1.b Meshes

todo

2.1.c Fast modulators

2.1.d Fast detectors

2.1.e Amplifiers

2.1.f Filters

2.1.g Feedforward and recirculating mesh

Both architecture rely on the same components [3], those being 2x2 tunable couplers (*A tunable coupler with two inputs and two outputs*), optical phase shifters and optical waveguides. These elements are combined in all-optical gates which can be tuned to achieve the user's intent. Additionally, to provide more functionality, the meshed gates can also be connected to other devices, such as high speed modulators, amplifiers, etc. [3, 14, 15]

The primary difference between a feedfoward architecture and a recirculating architecture, is the ability for the designer to make light travel both ways in one waveguide. As is known [16], in a waveguide light can travel in two direction with little to no interactions. This means that, without any additional waveguides or hardware complexity, a photonic circuit can be made to support two guiding modes, one in each direction. This property can be used for more efficient routing cite along with the creation of more structures.

As it has been shown[15], recirculating meshes offer the ability to create more advanced structures such as IIR (*Infinite Impulse Response*) elements, whereas feedforward architectures are limited to FIR (*Finite Impulse Response*) systems. This is due to inherent infinite impulse response of the ring resonator cell, while in a feedforward architecture, the Mach-Zehnder

interferometers have a finite impulse response. But, not only does the recirculating mesh allow the creation of IIR cells, it still allows the designer to create FIR cells when needed.

2.1.h Potential use cases of photonic processors

2.1.i Embedding of photonic processor in a larger system

2.2 Circuit representation

2.2.a Netlist and nets

2.2.b Bi-directional systems

2.2.c Feedforward approximation

As mentioned in Section 2.1, a type of photonic processor is the feedfoward processor, which, assumes that light "flows" from an input port to an output port in a single direction. However, we are interested in the more complex, more capable processor that uses recirculating meshes. Therefore, one may wonder if the assumption that one can design a generic circuit using a feedforward approximation is valid. In this section, we will show that, given a sufficient level of abstraction, any bi-directional photonic circuit can be represented by an equivalent, higher-level, feedforward circuit.

Theory has shown that one may view a waveguide as a four port devices, with each end of the waveguide being composed of two ports: an incoming and an outgoing port. This is due to the fact that, in a waveguide, light can travel in both directions with little to no interactions. This means that, in a waveguide, one can have two guiding modes, one in each direction [17]. Therefore, one can already see that each physical port, as well as each waveguide in the device can be split into two ports, one for each direction. This is a common approximation done in many simulation tools that assume that each signal is an *analytical signal* at a fixed wavelength in a single mode [6].

This therefore gives the first approximation: each physical port is split into two ports, one for each direction. This means that, from the perspective of a user, they can easily split the light incoming from a port and process it in the desired way. And they can easily output light that has been processed into a port with little to no interactions with the rest of the circuit. This is the first step in the feedforward approximation.

The second step in this approximation is to show that, given a sufficient level of abstraction, any circuit can be represented as an element that has zero or more input ports and zero or more output ports. But, as previously mentioned, some circuits, such as ring resonators, have an IIR (*Infinite Impulse Response*) that requires a recirculating mesh to be built. This is where the abstraction comes into play. One can view a ring resonator as a black box that has input and output ports and that has a certain scattering matrix that links each pair of input and output port as can be seen in Figure 3.

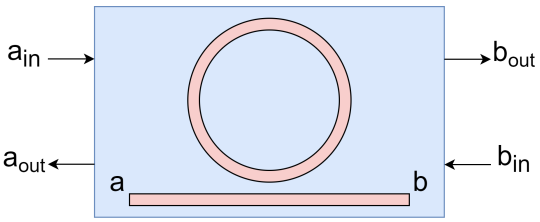


FIGURE 3 A black box representation of a ring resonator. The input and output ports are labeled as $a_{\text{in}}, b_{\text{in}}$ and $a_{\text{out}}, b_{\text{out}}$ respectively.",

It has been shown that, given a sufficient level of abstraction, any bi-directional photonic circuit can be represented by an equivalent, higher-level, feedforward circuit. This result is crucial for the formulation of the requirements for the programming interface of such a photonic processor. And is the basis on which the rest of this document is built.

2.3 Difficulties

2.3.a Wavelength as a continuum

2.3.b Amplitude as a continuum

2.3.c Temperature dependence

2.3.d Manufacturing tolerances

2.3.e Non-linearities

2.4 Initial design requirements

2.4.a Interfacing

2.4.b Programming

2.4.c Reconfigurability

2.4.d Tunability

3.

Programming of photonic processors

The primary objective of this chapter is to explore the different aspects of programming photonic processors. This chapter will start by looking at different traditional programming ecosystems and how different languages approach common problems when programming. Then an analysis of the existing software solutions and their limitations will be done. Finally, an analysis of relevant programming paradigms will be done. The secondary objective of this chapter is to make the reader familiar with concepts and terminology that will be used in the rest of the thesis. This chapter will also introduce the reader to different programming paradigms that are relevant for the research at hand, as well as programming language concept and components. As this chapter also serves as an introduction to programming language concepts, it is written in a more general way, exploring components of programming ecosystems – in Section 3.4 – before looking at specificities that are relevant for the programming of photonic processors.

3.1 Programming languages as a tool

Definition: **Imperativeness** refers to whether the program specifies the expected results of the computation (declarative) or the steps needed to perform this computation (imperative). These differences may be understood as the difference between *what* and *how*, or what the program should do and how it should do it.

Adapted from [5]

Programming languages, in the most traditional sense, are tools used to express *what* and, depending on its imperativeness and paradigm, *how* a device should perform a task. A device in this context, means any device that is capable of performing sequential operations, such as a processor, a microcontroller or another device. However, programming languages are not limited to programming computers, but are increasingly used for other tasks. So-called DSLs (*Domain Specific Language*) are languages designed for specific purposes that may intersect with traditional computing or describe traditional computing tasks, but can also extend beyond traditional computing. DSLs can be used to program digital devices such as FPGAs, but also to program and simulate analog systems such as Verilog-AMS or SPICE.

Additionally, programming languages can be used as a tool to build strong abstractions over traditional computing tasks. For example, SQL (*Structured Query Language*) is a language designed to describe database queries, by describing the *what* and not the *how*, making it easier to reason about the queries being executed. Other examples include *Typst*, the language used to create this document.

Furthermore, some languages are designed to describe digital hardware, so-called RTL (*Register Transfer Level*) HDLs (*Hardware Description Language*). These languages are used to describe the hardware in a way that is closer to the actual hardware, and therefore, they are not used to describe the *what* but the *how*. These languages are not the focus of this thesis, but they are important to understand the context of the research at hand, and they will be further examined in Section 3.4.l where they applicability to the research at hand will be discussed.

As such, programming languages can be seen, in a more generic way, as tools that can be used to build abstractions over complex systems, whether software systems or hardware systems, and therefore, the ecosystem surrounding a language can be seen as a toolbox providing many amenities to the user of the language. Is it therefore important to understand these components and reason about their importance, relevance and how they can best be used for a photonic processor.

3.2 Typing in programming languages

Definition: A **type system** is a system made of rules that assigns a property called a type to values in a program. It dictates how to create them, what kind of operations can be done on those values, and how they can be combined.

Adapted from [18]

Definition: **Static or dynamic typing** refers to whether the type of arguments, variables and fields is known at compile time or at runtime. In statically typed languages, the type of values must be known at compile time, while in dynamically typed language the type of values is computed at runtime.

Adapted from [18]

All languages have a type system, it provides the basis for the language to reason about values. It can be of two types: static or dynamic. Static typing allows the compiler to know ahead of executing the code what each value is and means. This allows the compiler to provide features such as type verification – that a value has the correct type for an operation – but also to optimize the code to improve performance. On the contrary, dynamic typing does not determine the type of values ahead of time, instead forcing the burden of type verification to the user. This practice makes development easier at the cost of increase overhead during execution and the loss of some optimizations [19]. Additionally, dynamic typing is a common source of runtime errors for programs written in a dynamically typed language, something that is caught during the compilation process in statically typed languages.

Therefore, static typing is generally preferred for applications where speed is a concern, as is the case in *C* and *Rust*. However, dynamic typing is preferred for applications where iteration speed is more important, such as in *Python*. However, some languages exist at the intersection of these two paradigms, such as *Rust* which can infer parts of the type system at compile time, allowing the user to write their code with fewer type annotations, while still providing the benefits of static typing. This is achieved through a process called type inference, where the compiler generally uses the de facto standard algorithm called *Hindley-Milner* algorithm [20, 21], which will be discussed further in Section 5.

3.3 Explicitness in programming languages

In language design, one of the most important aspect to consider is the explicitness of the language, that is, how much details must the user manually specify and how much can be inferred. This is a trade-off between the expressiveness of the language and the complexity of the language. A language that is too explicit is both difficult to write and to read, while a language that is too implicit is difficult to understand and reason about, while also generally being more complex to implement. Therefore, it is important to find a balance between these two extremes. Another factor to take into account is that too much "magic", that is operations being done implicitly, can lead to difficult to understand code, unexpected results and bugs that are difficult to track down.

Therefore, it is in the interest of the language designer and users to find a balance where the language is sufficiently expressive while also being sufficiently explicit. This is, generally, a difficult balance to find and can take several iterations to achieve. This balance is not the same for every programming languages either, the target audience of the language tends to govern, at least to some extent, which priorities are put in place. For example, performance focused systems, such as HPC (*High Performance Computing*) solutions, tend to be very explicit, with find grained control to eke out the most performance, while on the contrary, systems designed for beginners might want to be more implicit, sacrificing complexity and fine grained control for ease of use..

3.4 Components of a programming ecosystem

An important part of programming any kind of programmable device is the ecosystem that surrounds that device. The most basic ecosystem components that are necessary for the use of the device are the following:

- a language reference or specification: the syntax and semantics of the language;
- a compiler or interpreter: to translate the code into a form that can be executed by the device;
- a hardware programmer or runtime: to physically program and execute the code on the device.

These components are the core elements of any programming ecosystem since they allow the user to translate their code into a form the device can execute. And then to use the device, therefore, without these components, the device is useless. However, these components are not sufficient to create a user-friendly ecosystem. Indeed, the following component list can also be desirable:

- a debugger: to aid in the development and debugging of the code;
- a code editor: to write the code in, it can be an existing editor with support for the language;
- a formatter: to format the code in a consistent way;
- a linter: a tool used to check the code for common mistakes and to enforce a coding style;
- a testing framework: to test and verify the code;
- a simulator: to simulate the execution of the code;
- a package manager: to manage dependencies between different parts of the code;
- a documentation generator: to generate documentation for the code;
- a build system: to easily build the code into a form that can be executed by the device.

With the number of components desired one can conclude that any endeavour to create such an ecosystem is a large undertaking. Such a large undertaking needs to be carefully planned and executed. And to do so, it is important to look at existing ecosystems and analyse them. This section will analyse the ecosystems of the following languages, when relevant:

- *C*: a low-level language that is mostly used for embedded systems and operating systems;
- *Rust*: a modern systems language mostly used for embedded systems and high performance applications;
- *Python*: a high-level language that is mostly used for scripting and data science;
- *VHDL (*VHSIC Hardware Description Language*)*: an HDL (*Hardware Description Language*) that is used to describe digital hardware;
- *Verilog-AMS*: an analog simulation language that has been used to describe photonic circuits [22];

Each of these ecosystems comes with a certain set of tools in addition to the aforementioned core components. Some of these languages come with tooling directly built by the maintainers of the languages, while others leave the development

of these tools to the community. However, it should be noted that, in general, tools maintained by the language maintainers directly tend to have a higher quality and broader usage than community-maintained tools.

Additionally, the analysis done in this section will give pointers towards the language choice used in the development of the language that will be presented in Section 5, which will be a custom DSL language for photonic processors. As this language will not be self-hosted – its compiler will not be written in itself – it will need to use an existing language to create its ecosystem.

3.4.a Language specification & reference

Definition: A **programming language specification** is a document that formally defines a programming language, such that there is an understanding of what programs in that language means. This document can be used to ensure that all implementations of the language are compatible with one another.

Adapted from [23]

Definition: A **programming language reference** is a document that outlines the syntax, features and usage of a programming language. It serves as a simplified version of the specification and is usually written during development of the language.

Adapted from [23]

A programming specification is useful for languages that are expected to have more than one implementation, as it outlines what a program in that languages is expected to do. Indeed, code that is written following this specification should therefore be able to be executed by any implementation of the language and produce the same output. However, this is not always the case, several languages with proprietary implementations, such as *VHDL* and *SystemC* – two languages used for hardware description of digital electronics – have issues with vendored versions of the language [24].

This previous point is particularly interesting for the application at hand: assuming that the goal is to reuse an existing specification for the creation of a new photonic HDL, then it is important to select a language that has a specification. However, if the design calls for an API (*Application Programming Interface*) implemented in a given language instead, then it does not matter. Indeed, in the latter case, the specification is the implementation itself.

Additionally, when reusing an existing specification for a different purpose than the intended one, it is important to check that the specification is not too restrictive. Indeed, as has been previously shown in Section 2.1, the programming of photonic processors is different from the programming of electronic processors. Therefore, special care has to be taken that the specification allows for the expression of the necessary concepts. This is particularly important for languages that are not designed for hardware description, such as *C* and *Python*. Given that photonics has a different target application and different semantics, most notably the fact that photonic processors are continuous analog systems – rather than digital processes – these languages may lack the needed constructs to express the necessary concepts, they may not be suitable for the development of a photonic HDL. Given the effort required to modify the specification of an existing language, it may be better to create a new language from dedicated for photonic programming.

Furthermore, the language specification is only an important part of the ecosystem being designed when reusing an existing language. However, if creating a new language or an API, then the specification is irrelevant. It is however desirable to create a specification when creating a new language, as it can be used a thread guiding development. With the special

consideration that a specification is only useful when the language is mature, immature languages change often and may break their own specification. And maintaining a changing specification as the language evolve may lower the speed at which work is done. For example, *Rust* is widely used despite lacking a formal specification [25].

3.4.b Compiler

Definition: A **compiler** is a program that translates code written in a higher level programming language into a lower level programming language or format, so that it can be executed by a computer or programmed onto a device.

Adapter from [26]

The compiler has an important task, they translate the user's code from a higher level language, which can still remain quite low-level, as in the case of *C*, into a low-level representation that can be executed. The type of language used determines the complexity of the compiler, in general, the higher the level of abstraction, the more work the compiler must perform to create executable artefacts.

An alternative to compilers are interpreters which perform this translation on the fly, such is the case for *Python*. However, HDLs tend to produce programming artefacts for the device, a compiler is more appropriate for the task at hand. This therefore means that *Python* is not a suitable language for the development of a photonic HDL. Or at least, it would require the development of a dedicated compiler for the language.

One of the key aspects of the compiler, excluding the translation itself, is the quality of errors it produces. The easier the errors are to understand and reason about, the easier the user can fix them. Therefore, when designing a compiler, extreme care must be taken to ensure that the errors are as clear as possible. Language like *C++* are notorious for having frustrating errors [27], while languages like *Rust* are praised for the quality of their errors. This is an important aspect to consider when designing a language, as it can make or break the user experience. Following guidelines such as the ones in [27] can help in the design of a compiler and greatly improve user experience.

Components

Compilers vary widely in their implementation, however, they all perform the same basic actions that may be separated into three distinct components:

- the frontend: which parses the code and performs semantic analysis;
- the middle-end: which performs optimisations on the code;
- the backend: which generates the executable artefacts.

The frontend checks whether the program is correct in terms of its usage of the syntax and semantics. It produces errors that should be helpful for the user [27]. Additionally, in statically typed languages, it performs type checking to ensure that types are correct and operations are valid. In general, it is the frontend that produces a simplified, more descriptive, version of the code to be used in further stages [21]. The middle-end performs multiple functions, but generally, it performs optimisations on the code. These optimisations can be of various types, and are generally used to improve the performance of the final executable. As will se discussed in Section 5, while performance is important, it is not the main focus of the proposed language. Therefore, the middle-end can be simplified. Finally, the backend, has the task of producing the final executable. This is a complex topic in and off itself, as it requires the generation of code for the target architecture. In the case of *C* using *Clang* – a common compiler for *C*– this is done by the LLVM compiler framework [28]. However, as with the

middle-end, the final solution suggested in this work will not require the generation of traditional executable artefacts. Instead, some of the tasks that one may group under the backend, such as place-and-route, will still be required and are complex enough to warrant their own research.

3.4.c Hardware-programmer & runtime

Definition: The **hardware-programmer** is a tool that allows the user to write their compilation artefacts to the device. It is generally a piece of software that communicates with the device through a dedicated interface, such as a USB port. Most often, it is provided by the manufacturer of the device.

Adapted from [29]

The hardware-programmer is an important part of the ecosystem, as it is required to program the physical hardware. Usually it is also involved in debugging the device, such as with interfaces like JTAG (*Joint Test Action Group – A standard for testing integrated circuits*). However, as this may be considered part of the hardware itself, it will not be further discussed in this section. However, it must be considered as the software must be able to communicate with the device.

Definition: The **runtime** is a program that runs on the device to provide the base functions of the device, such as initialization, memory management, and other low-level functions [26]. It is generally provided by the manufacturer of the device.

Adapted from [29]

In the case of a photonic processor, it is as of yet unclear what tasks and functions it will perform for the rest of the ecosystem, and warrants its own research and work. The runtime is a device-specific component, and as such, it is not possible to design it as a generic, reusable, component. Therefore, it is mentioned as a necessary component, and will be discussed in further details in Section 5 but will not be further considered in this section.

In general, the hardware-programmer and the runtime work hand-in-hand to provide the full programmability of the device. As the hardware-programmer is the interface between the user and the device, and the runtime is the interface between the device and the user's code compiled artefacts. Therefore, these two components are what allows the user's code to not only be executed on the device, but also to have access to the device's resources.

3.4.d Debugger

Definition: A **debugger** is a program that allows the user to inspect the state of the program as it is being executed. In the case of a hardware debugger, it generally works in conjunction with the hardware-programmer to allow the user to inspect the state of the device, pause execution and step through the code.

Adapted from [26]

The typical features of debuggers include the ability to place break-points – point in the code where the execution is automatically paused upon reaching it – step through the code, inspect the state of the program, then resume the execution of the program. Another common feature is the ability to pause on exception, essentially, when an error occurs, the debugger will pause the execution of the program and let the user inspect what caused this error and observe the list of function calls that lead to the error.

Some of the functions of a debugging interface are hard to apply to analog circuitry such as in the case of photonic processors. And it is evident that traditional step-by-step debugging is not possible due to the realtime, continuous nature of analog circuitry. However, it may be possible to provide mechanisms for inspecting the state of the processor by sampling the analog signals present within the device.

Due to the aforementioned limitations of existing digital debuggers, no existing tool can work for photonic processors. Instead, traditional analog electronic debugging techniques, such as the use of an oscilloscope are preferable. However, traditional tools only allow the user to inspect the state at the edge of the device, therefore, inspecting issues inside of the device require routing signals to the outside of the chip, which may not always be possible. However, it is interesting to note that this is an active area of research [30, 31, 32], for analog electronics at least, and it would be interesting to see what future research yields and how much introspection will be possible with "analog debuggers".

3.4.e Code formatter

Definition: A **code formatter** is a program that takes code as input and outputs the same code, but formatted according to a set of rules. It is generally used to enforce a consistent style across a codebase such as in the case of the *BSD project* [33] and *GNU style* [34].

Adapted from [35]

Most languages have code formatters such as *rustfmt* for *Rust* and *ClangFormat* for the *C* family of languages. These tools are used to enforce rules on styling of code, they play an important role in keeping code bases readable and consistent. Although not being strictly necessary, they can enhance the programmer's experience. Additionally, some of these tools have the ability to fix certain issues they detect, such as *rustfmt*.

Most commonly, these tools rely on *Wadler-style* formatting [36]. Due to the prominence of this formatting architecture, it is likely that, when developing a language, a library for formatting code will be available. This makes the development of a formatting code much easier as it is only necessary to implement the rules of the language.

3.4.f Linting

Definition: A **linter** is a program that looks for common errors, good practices, and stylistic issues in code. It is used in conjunction with a formatter to enforce a consistent style across a codebase. They also help mitigate the risk of common errors and bugs that might occur in code.

Adapted from [35]

As with formatting, most languages have linters made available either through officially maintained tools or with community maintained initiatives. As these tools provide means to mitigate common errors and bugs, they are an important part of the ecosystem. They can be built as part of the compiler directly, or as a separate tool that can be run on the codebase. Additionally, linters often lack support for finding common errors in the usage of external libraries. Therefore, when developing an API, linters are limited in their ability check for proper usage of the API itself and care must be done to ensure that the API is used correctly, such as making the library less error-prone through strong typing.

Nonetheless, linters are limited in their ability to detect only common errors and stylistic issues, as they can only check errors and issues for which they have pre-made rules. They cannot check for more complex issues such as logic errors.

However, the value of catching common errors and issues cannot be understated. Therefore, whether selecting a language to build an API or creating a custom language, it is important to consider the availability and quality of linters.

As for implementation of linters, they generally rely on a similar architecture than formatters, using existing components of the compiler to read code. However, they differ by matching a set of rules on the code to find common errors. Creating a good linter is therefore more challenging than creating a good formatter as the number of rules required to catch common errors may be quite high. As en example *Clippy*, *Rust*'s linter, has 627 rules [37].

Interestingly, as in the case of *Clippy*, some rules can also be used to suggest better, more readable ways of writing code, colloquially called good practices. For example, *Clippy* has a rule that suggests lowering cognitive load using the rule `clippy::cognitive_complexity` [37]. This rules suggests that functions that are too complex as defined in the literature [38] should be either reworked or split into smaller, more readable code units.

3.4.g Code editor

Definition: A **code editor** is a program that allows the editing of text files. It generally provides features that are aimed at software development such as syntax highlighting, code completion, and code navigation.

Adapted from [39]

As previously mentioned, most code editors also provide features aimed at software development. Features such as syntax highlighting: which provides the user with visual cues about the structure of the code, code completion: which suggest possible completions for the code the user is currently writing, and code navigation: allows the user to jump to the definition or user of a function, variable, or type. These features help the user be more productive and navigate codebases more easily.

In general, it is not the responsibility of the programming language to make a code editor available. Fully featured programming editors are generally called IDEs (*Integrated Development Environment*). Indeed, most users have a preferred choice of editor with the most popular being *Visual Studio Code*, *Visual Studio* – both from *Microsoft* – and *IntelliJ* – a *Java*-centric IDE from *JetBrains* [40]. Additionally, most editors have support for more than one language, either officially or through community maintained plugins – additional software that extends the functionality of the editor.

When creating a new language, effort should therefore not go towards creating a new editor as much as supporting existing editors. This is usually done by creating plugins for common editors, however this approach leads to repetition has editors use different language for plugin development. Over the past few years, a new standard, LSP (*Language Server Protocol*), has established itself as a de-facto standard for editor support [41]. Allowing language creators to provide an LSP implementation and small wrapper plugins for multiple editors greatly reducing the effort required to support multiple editors. LSP was originally introduced by *Microsoft* for *Visual Studio Code*, but has since been adopted by most editors [41].

3.4.h Testing & simulation

Definition: **Testing** is the process of checking that a program produces the correct output for a given input. It is generally done by writing a separate programs that runs parts – or the entirety – of the tested program and checks that it produces an output, and that the produced output is correct.

Adapted from [42, 43]

Testing can generally be seen as a way of checking that a program works as intended. Checking for logical errors rather than syntactic errors, as the compiler would. Tests can be written ahead of the writing of the program, this is then called TDD (*Test Driven Development*) [44]. Additionally, external software can provide metrics such as *code coverage* that inform the user of how much of their code is being tested [45].

Testing also comes in several forms, one may write *unit tests* that test a single function, *integration tests* that test the interaction between functions or module, *regression tests* that test that a bug was fixed and does not reappear in newer versions, *performance tests* – also called *benchmarks* – which test the performance of the programs or parts of the program, and *end-to-end tests* which test the program as a whole.

Additionally, there also exists an entirely different kind of tests called *constrained random* which produces random, but correct, input to a program and checks that, in no conditions, does the program crash. This is generally utilized to find edge cases that are not properly handled as well as testing the robustness of the program – especially areas concerning security and memory management.

Most modern programming language such as *Rust* provide a testing framework as part of the language ecosystem. However, these testing framework may need to be expanded to provide library-specific features to test more advanced usage. As an example, one may look at libraries like *Mockito* which provides features for HTTP (*Hypertext Transfer Protocol – the protocol used for web navigation*) testing in *Rust* [46].

Therefore, when developing an API, it is important to consider how the API itself will be tested, but also how the user is expected to test their usage of the API. Additionally, when creating a language, it is important to consider how the language will be tested, and what facilities will be provided to the user for testing of their code.

Definition: **Simulation** is the process of running a program that simulates the behavior of a physical device. It is used to test that HDLs produce the correct state for a given input and starting state, while also checking that the program does so in the correct timing, power consumption limits, etc.

Adapted from [42, 43]

Simulation is more specific to HDLs and embedded development than traditional computer development, where the user might want to programmatically test their code on the target platform without needing the physical device to be attached to a computer. For this reason, the hardware providers make simulators available to their users. These simulators are used to run the user's code as if it was running on real hardware, providing the user with tools for introspection of the device and checking that the program behaves as expected. As an example, *Xilinx* provides a simulator for their FPGAs called *Vivado Simulator*. This simulator allows the user to run their code on a simulated FPGA and check that the output is correct. This is an important tools for the users of HDLs as it allows them to test their code without needed access to the physical devices. Furthermore, it allows programmers working on ASICs (*Application Specific Integrated Circuit*) to simulate their code, and therefore their design before manufacturing of a prototype.

There exists a plethora of simulation tools, as previously mentioned, *Vivado Simulator* allows users to test their FPGA code, other tools such as *QEMU* allow users to test embedded platforms. Additionally, a lot of analog simulations tools exist, most notably the SPICE family of tools, which allow the simulation of analog electronics. There is also work being done to simulate photonic circuits using SPICE [8].

Finally, there also exist tools for physical simulation, such as *Ansys Lumerical* which are physical simulation tools that simulate the physical interactions of light with matter. These tools are used during the creation of photonic components used when creating PICs. However, they are generally slow and require large amounts of computation power [6, 7]. Therefore, when creating an API or a language for photonic processor development, it is desirable to consider how simulation will be performed and the level of details that this simulator will provide. The higher the amount of details, the higher the computational needs.

Verification As previously mentioned, when writing HDL code, it is desirable to simulate the code to check that it behaves correctly. Therefore, it may even be desirable to automatically simulate code in a similar way that unit tests are performed. This action of automatically testing through simulation is called *verification*. As verification is an important part of the HDL workflow and ecosystem. It is critical that any photonic programming solution provides a way to perform verification. This would be done by providing both a simulator and a tester and then providing a way of interface both together to perform verification.

3.4.i Package manager

Definition: A **package manager** or **dependency manager** is a tool that allows users to install and manage dependencies of their projects. These dependencies are generally libraries, but they can also be tools such as testing frameworks, etc.

Adapted from [47]

Package management is an integral part of modern language ecosystems. It allows users to easily install dependencies from the community as well as share dependencies with the community. This is done through the use of a global repository of packages. Additionally, some package managers provide a way to create private repositories for protection of intellectual property.

This last point is of particular interest for hardware description. It is common in the hardware industry to license the use of components – generally called IPs (*Intellectual Property*). Therefore, any package manager designed to be used with an HDL must provide a way of protecting the intellectual property of package providers and users alike.

Additionally, package manager often offer version management, allowing the user to specify which version of a package they wish to use. As well as allowing package providers to update their packages as they get refined and improved. The same can be applied for hardware description as additional features may be added to a component, or hardware bugs may be fixed.

Finally, package managers usually handle nested dependencies, that is, they are able to resolve the dependencies of the dependencies, making the experience of a user wishing to use a specific package easier. This lets creators of dependencies themselves build on top of existing community solutions, providing for a more cohesive ecosystem. It is also important to point out that nested dependencies can cause conflicts, and therefore, package managers must provide a way to resolve these conflicts. This is usually done using *semantic versioning* which is a way of specifying version number that allow, to some degree, automatic conflict resolution [48].

3.4.j Documentation generator

Definition: A **documentation generator** is a tool that allows users to generate documentation for their code using their code. This is usually done by using special comments in the code that are then extracted and interpreted as documentation.

Adapted from [49]

The most common document generators are *Doxygen* used by the *C* and *C++* community and *Javadoc* used by the *Java* community. Generally, documentation generators produce documentation in the form of a website, where all the documentation and components are linked together automatically. This makes navigating the documentation easier for the user.Additionally, some documentation generators such as *Rustdoc* for the *Rust* ecosystem, provide a way to include and test examples directly in the documentation. This makes it easier for users to understand and use new libraries they might be unfamiliar with. For this reason, when developing an API, having a documentation generator built into the language is highly desirable. As the documentation can serve as a way for users to learn the API but also for maintainers to understand the implementation of the API itself. Additionally, when creating a new language, care might be given to documentation generators, as they can provide a way for users to document their code and for maintainers to document the language and it standard library. Finally, as technical documentation is the primary source of information for developers [40], it is essential to take this need from users into account.

3.4.k Build system

Definition: A **build system** is a tool that allows users to build their projects.

Adapted from [26]

Build systems play an essential role in building complex software. As modern software is generally composed of many files that are compiled together, along with having dependencies, configuration and many other resources, it is difficult to compile modern software projects by hand. For these reasons, build systems are available. They provide a way to specify how a project should be built, this can be done in an explicit way: where the user specifies the steps that should be taken, the dependencies and how to build them. This approach would be similar to the popular *CMake* build system for the *C* family of languages. Other build systems like *Cargo* for *Rust* provide a mostly implicit way of building projects, where the user only specifies the dependencies and, by using a standardized file structure, the build system is able to infer how to build the project. This approach is easier to use and leads to more uniform project structure. This means that, in combination with other tools such as formatters and linters, projects built using tools like *Cargo* all *look* alike, making them easy to navigate for beginners and experienced users alike. Additionally, not having to create *CMake* files for every new project follows the DRY (*Don't Repeat Yourself*) principle, which is a common mantra in programming.

Additionally, build systems can provide advanced features that are of particular interest of hardware description languages. Features such as *feature flags* are particularly useful. A feature flag is a property that can be enabled during building that is additive, it adds additional features to the program. As a simple example, consider the program in Listing 1: it will print `"Hello, world!"` when it is called. A feature flag called `custom_hello` may be used to add the function in Listing 2 which allows the user to specify a name to greet. It is purely additive: adding functionality to the previous library and uses the `custom_hello` feature flag to conditionally enable the additional feature. This example is trivial, but this idea can be

expanded. Another example might be a feature flag that enables an additional type of modulator in a library of reusable photonic components. Some libraries even take a step further, where almost all of their features are gated, which allows them to be very lean and fast to compile, however this is not a common occurrence.

```rust
/// Prints `Hello, world!` in the console.
fn print_hello_world() {
    println!("Hello, world!");
}
```

Listing 1 | Simple function that prints `"Hello, world!"`, in *Rust*.

```rust
/// Prints `Hello, {name}!` in the console.
#[cfg(feature = "custom_hello")]
fn print_hello_world(name: String) {
    println!("Hello, {name}!");
}
```

Listing 2 | Function that prints `"Hello, {name}!"` with a custom name, in *Rust*.

Whether providing the user with an API or creating a new language, it is important to consider how the user's program must be built. As this task can quickly become quite complex. Enforcing a fixed folder structure and providing a ready-made build system that handles all common building tasks can greatly improve the user experience. And especially the experience of newcomers as it might avoid them having to do obscure tasks such as writing their own *CMake* files.

3.4.l Summary

As has been shown, in order to build a complete, user friendly ecosystem, a lot of components are necessary or desirable. Official support for these components might be preferred as they lead to lower fracturing of their respective ecosystems. In Table 1, an overview of components that are required, desirable or not needed, along with a short description and their applicability for different scenarios are mentioned. Some components are more important than others and are required to build the ecosystem. Most notably the compiler, hardware-programmer, and testing and simulation tools. Without these components, the ecosystem is not usable for hardware development. However, while the other components are not strictly needed, a lot of them are desirable: having proper debugging facilities makes the ecosystem easier to use. Similarly, having a build system can help the users get started with their projects faster.

In Table 1, there is a distinction made on the type of design that is pursued, as will be discussed in Section 5, this thesis will create a new hardware description language, but the possibility of creating an API was also discussed. And while an API is not the retained solution, one can use this information for the choice of the language in which this new language, called PHÔS (*Photonic Hardware Description Language*), will be implemented. Indeed, the same components that make API designing easy, also make language implementation easier. As will be discussed in Section 3.11, PHÔS will be implemented in *Rust*. The language meets all of the requirement by having first party support for all of the required and desired components for an API design. Additionally, its high performance and safety features make it a good candidate for a reliable implementation of the PHÔS ecosystem.

Component	Description	Importance	
		API design	language design
Language specification	Defines the syntax and semantics of the language.	~	~
Compiler	Converts code written in a high-level language to a low-level language.	✓	~ (interpreted[1])
Hardware-programmer & runtime	Allows the execution of code on the hardware.	✓	✓
Debugger	Allows the user to inspect the state of the program at runtime.	~	~
Code formatter	Allows the user to format their code in a consistent way.	~	~
Linter	Allows the user to check their code for common mistakes.	✗	~
Code editor	Allows the user to write code in a user-friendly way.	✗ (provided by the ecosystem[2])	✗
Testing & simulation	Allows the user to test their code.	✓	✓
Package management	Allows the user to install and manage dependencies.	~	~
Documentation generator	Allows the user to generate documentation for their code.	✓	~
Build system	Allows the user to more easily build their codebase.	~	~

Table 1 This table shows the different components that are needed (✓), desired (~) or not needed (✗) for an ecosystem. It compares their importance for different scenarios, namely whether developing an API that is used to program photonic processors or whether creating a new language for photonic processor development.

1. Interpreted languages are languages that are not compiled to machine code, but rather interpreted at runtime. This means that they do not require a compiler per se, but rather an interpreter.
2. A code editor is provided as an external tool, however, support for the language must be provided by the ecosystem. That being said, it is not a requirement and is desired rather than required.

Finally, Table 2 compares the ecosystem of existing programming and hardware description languages and their components. It shows that some ecosystems, like *Python*'s, have a lot of components, but that not all of them are first party nor is there always an agreement within the community on the best tool. However *Rust* is a particularly strong candidate in this regard, as it has first party support for all of the required components with the exception of hardware-programming and debugging tools. But as also noted in Table 2, most other languages do not come with first party support fot these tools either. However, as will be discussed in Section 3.5, it is difficult to learn, has not seen use in hardware synthesis and is

therefore not a good fit for regular users. But its strong ecosystem makes it a good candidate for a language implementation, something for which it has a thriving ecosystem of many libraries, colloquially called *crates*, fit for this purpose.

One can also see from Table 2, that simulation and hardware description ecosystems tend to be highly proprietary and incomplete. This is a problem that can be solved by providing a common baseline for all task relating to photonic hardware description, where only the lowest level of the technology stack: the platform support is vendored. Forcing platforms, through an open source license such as GPL-3.0 (*GNU General Public License version 3.0*), to provide a common interface for their hardware, will allow for a common ecosystem to be built on top of it. This is the approach that will hopefully be taken by PHÔS, which will be discussed in Section 5.11.

Components	Traditional languages			Hardware description & simulation languages	
	C	Rust	Python	Verilog-AMS	VHDL
Language specification	✓ [50]	✗ [25]	✗ [51]	✓ [52]	✓ [53]
Compiler	~ [1] (*Clang* & *GCC*)	✓ (*rustc*)	~ (*PyPy* & *Numba*)	✗ (simulated)	~ (synthesized)
Hardware-programmer & runtime	~ [2] (vendored)	~ [2] (vendored)	~ [2] (vendored)	~ [3] (vendored)	~ (vendored)
Debugger	~ [4] (*GDB* & *LLDB*)	~ [4] (*GDB* & *LLDB*)	✓ (*PDB*)	~ (vendored)	~ (vendored)
Code formatter	~ (*clang-format* & *uncrustify*)	✓ (*rustfmt*)	~ (*Black*)	✗ [5]	✗ [5]
Linter	~ (*clang-tidy* & *uncrustify*)	✓ (*Clippy*)	~ (*Black*)	✗ [5]	✗ [5]
Code editor support	~ (*clangd* & *ccls*)	✓ (*rust-analyzer*)	~ (*Pyright*)	✗ [5]	✗ [5]
Testing	~ (*CUnit*)	✓ (*rustc*)	~ (*Pytest*)	~ (*SVUnit*)	~ (*VUnit*)
Simulation	~ [2] (vendored)	~ [2] (vendored)	~ [2] (vendored)	~ (vendored)	~ (vendored)
Package management	✗	✓ (*Cargo*)	✓ (*PyPI*)	✗ [6]	✗ [6]
Documentation generator	~ (*Doxygen*)	~ (*Rustdoc*)	~ (*Sphinx*)	✗ [5]	✗ [5]

Build system	~ (*CMake*)	✓ (*Cargo*)	~ [7] (*Poetry*)	~ (vendored)	~ (vendored)

Table 2 This table compares the ecosystems of different programming and hardware description languages. It shows whether the components are first party (✓), third party but well supported (~) or third party but not well supported or non existent (×). For each component, is also lists the name of the tool that is most commonly used for that purpose.

Notes:

1. *C* has multiple, very popular, compilers, such as *GCC* and *Clang*. However, these are third party, and for embedded and HLS (*High Level Synthesis*) development, there is no de facto standard.
2. Traditional programming languages usually rely on programmers and runtime provided by the hardware vendor of the targetted embedded hardware.
3. *Verilog-AMS (*Verilog for Analog and Mixed Signal*)* is a language used for simulation, not hardware description.
4. *C* and *Rust* generally share debuggers due to being native languages.
5. There does seem to exist some formatters, linters, code editor support and documentation generators for *Verilog-AMS* and *VHDL*, but they are not widely used and are sparsely maintained.
6. Due to the difficulty in handling intellectual property in hardware, there is no ubiquitous package manager for hardware description languages.
7. Python being interpreted, it does not need a build system, but some dependency and environment automation tools such as *Poetry* exist and are widely used.

With the previous sections, it can be seen that creating a user-friendly ecosystem revolves around the creation of tools to aid in development. The compiler and language cannot be created in isolation, and the ecosystem as a whole has to be considered to achieve the broadest possible adoption.

Depending on the choice of implementation, the components of the ecosystem will change. However, whether the language already exists or whether it is created for the purpose of programming photonic processors, special care needs to be taken to ensure high usability and productivity through the availability or creation of tools to aid in development.

As will be discussed in Section 5, the chosen solution will be the creation of a custom DSL for photonic processors. This will be done due to the unique needs of photonic processors, and the lack of existing languages that can be used for development targetting such devices. And this ecosystem will need to be created from scratch. However, the analysis done in this section will be used to guide the development of this ecosystem.

3.5 Overview of Syntaxes

Following the analysis of programming ecosystem components, this section will analyse the different syntaxes employed by various, common, programming languages. The goal of this section is to build an intuition on what these syntaxes look

like, what they mean and how they can be applied in Section 6.1. As that section will compare simple examples and how one might implement simple photonic circuits in each of these languages. Additionally, this section will also analyse the syntaxes of existing HDLs and other DSLs that are used to program digital electronics – most notably FPGAs – and analog electronics. This analysis will also provide insight into whether these languages are suitable for programmable photonics. As programmable photonics works using different paradigms than digital and analog electronics, it is important to understand these differences and why they makes these existing solutions unsuitable.

The first analysis, which looks at traditional programming languages, will be done by looking at the syntaxes of the following languages: *C*, *Rust*, and *Python*. These languages have been chosen as they are some of the most popular languages in the world, but also because they each bring different strength and weaknesses with regards to the following aspects:

- *C* is a low-level language that is used as the building block for other non-traditional computation types such as FPGAs by being used for HLS [54], but is also being used for novel use cases such as quantum programming [55].
- *Rust* is another low-level language, it has not seen wide use in HLS or other non-traditional computation types, but it has modern features that make it a good candidate for API development. However, *Rust* has a very steep learning curve which makes it unsuitable for non-programmers [56].
- *Python* is a common language that is used by a wide proportion of researchers and engineers [40, 57], which makes it a great candidate as the starting point of any language development. It is also used for some HDL development [58] and has been used for the development of the existing photonic processor APIs, as well as for other non-traditional computation types such as quantum computing. However, it is a high-level, generally slow language with a syntax that is generally not suitable for hardware description, as will be further discussed later.

The second analysis, will focus on different forms of HDLs (*Hardware Description Language*) and simulation languages. Most notably, the following languages will be analyzed:

- *SytemC* is a language that has seen increased use in HLS for FPGAs.
- *MyHDL* is a library for *Python* that gives it hardware description capabilities.
- *VHDL*: a common HDL used for FPGA development and other digital electronics [59].
- *Verilog-AMS*: a superset of *Verilog* that allows for the description of analog electronics. It has seen use in the development of photonic simulation, most notably in *Ansys Lumerical* [22].
- *SPICE*: a language that is used for the simulation of analog electronics. *SPICE* as seen use in the development of photonic simulation [8].

The goal of the second analysis will be to see whether any of these languages can be reused or easily adapter for photonic simulation. In the end, none of these languages really fit the needs of photonic development, most notably with regards to ease of use. Nonetheless, the analysis provides insight that can be useful when designing a new language. It is also important to note that there are two distinct families of languages in the aforementioned list: there are digital HDLs and analog simulation-centric languages. Therefore this comparison will be done in two parts, one for each family of languages.

3.5.a Traditional programming languages

To compare traditional programming language, a simple, yet classical example will be used: *FizzBuzz*, which is a simple program that prints the number from 1 to 100, printing *Fizz* when the number is divisible by 3, *Buzz* when the number is divisible by 5 and *FizzBuzz* when the number is divisible by both 3 and 5. The *C* implementation of *FizzBuzz* is shown in Listing 3. The *Rust* implementation of *FizzBuzz* is shown in Listing 4. The *Python* implementation of *FizzBuzz* is shown in

Listing 5. For each of those languages, many different implementations are possible, however, a simple and representative version was used. As performance are not the focus of this comparison, choosing the most optimized implementation is not necessary.

Programming languages often take inspiration from one another, as such, most modern languages are inspired by *C*, which is itself inspired by *B*, *ALGOL 68* and *FORTRAN* [60]. *C* has had a large influence on languages such as *Python* [61] and *Rust* [25] – through *C++* and *Cyclone* – but also on HDLs such as *Verilog* (and therefore *Verilog-AMS*). As such, this section will start with an outlook of the syntax of *C* and discuss some of its shortcomings with regards to more modern languages. Additionally, the more difficult aspects of the language will be discussed, most notably manual memory management and pointer semantics, as these two aspects are error prone and even considered to be the root cause for most security vulnerabilities [62].

A simple *C* implementation of *FizzBuzz* can be found in Listing 3, it shows several important aspects of *C*:

- blocks of code are surrounded by curly braces (`{` and `}`);
- statements are terminated by a semicolon (`;`), however curly braces can be omitted for single line statement;
- variables are declared with a type and a name, and optionally initialized with a value;
- functions are declared with a return type, a name, a list of arguments and a body;
- ternary operators are available, for shorter, but less readable conditional statements;
- *C* lacks a lot of high level constructs such as string, relying instead on arrays of characters;
- *C* has a lot of low-level constructs such as pointers, which are used to pass arguments by reference;
- *C* is not whitespace or line-space sensitive and statement can span multiple lines;
- *C* uses a preprocessor to perform text substitution, such as importing other files;
- *C* needs a `main` function to be defined, which is the entry point of the program.

```c
#include <stdio.h>
#include <string.h>

void main() {
    char buffer[88];
    for(int i = 0; i <= 100; i++) {
        int len = sprintf(
            buffer,
            "%s%s",
            i % 3 ? "" : "Fizz",
            i % 5 ? "" : "Buzz");
        if (len == 0)
            sprintf(buffer, "%d", i);
        printf("%s\n", buffer);
    }
}
```

Listing 3 | *FizzBuzz* implemented in *C*, based on the *Rosetta Code* project [1].

The *Rust* implementation of *FizzBuzz* can be found in Listing 4, it shows several important aspects of *Rust*:

- blocks of code are surrounded by curly braces (`{` and `}`);
- statements are terminated by a semicolon (`;`);
- loops use the range syntax (`..`) instead of manual iteration;
- printing is done using the `print` and `println` macros, which are similar to *C*'s `printf`;
- variables do not need to be declared with a type, as the compiler can infer it;
- *Rust* is not whitespace or line-space sensitive and statement can span multiple lines;
- *Rust* needs a `main` function to be defined, which is the entry point of the program.

Rust

```rust
use std::fmt::Write;

fn main() {
    for i in 1..=100 {
        let out = format!(
            "{}{}",
            if i % 3 == 0 { "Fizz" } else { "" },
            if i % 5 == 0 { "Buzz" } else { "" }
        );


        if out.len() == 0 {
            println!("{i}");
        } else {
            println!("{out}");
        }
    }
}
```

Listing 4 | *FizzBuzz* implemented in *Rust*, based on the *Rosetta Code* project [1]

The *Python* implementation of *FizzBuzz* can be found in Listing 5, it shows several important aspects of *Python*:

- blocks of code are delimited by indentation;
- statements are terminated by a newline;
- loops use the `range` function instead of manual iteration;
- printing is done using the `print` function;
- variables do not need to be declared with a type, as the language is dynamically typed;
- *Python* is whitespace and line-space sensitive;
- *Python* does not need a `main` function to be defined, as the file itself is the entry point of the program.

Python

```python
for n in range(1,101):
    response = ''
    if not (n % 3):
```

```
4         response += 'Fizz'
5     if not (n % 5):
6         response += 'Buzz'
7     print(response or n)
```

Listing 5 | *FizzBuzz* implemented in *Python*, based on the *Rosetta Code* project [1].

These simple example show us some fundamental design decisions for *C*, *Rust*, and *Python*, most notably that *Python* is whitespace and line-space sensitive, while *C* and *Rust* are not. This is a design feature of *Python* that aids in making the code more readable and consistently formatted regardless of whether the user uses a formatter or not. Then, focusing on typing, *Python* is dynamically typed which makes the work of any compiler more difficult. Dynamic typing is a feature that generally makes languages easier to use at the cost of runtime performance, as type checking has to be done as the code is running. Per contra, *Rust* takes an intermediate approach between *Python*'s dynamic typing and *C*'s manual type annotation: *Rust* uses type inference to infer the type of variables, that means that users still need to annotate some types, but overall most variables do not need type annotations. This makes *Rust* easier to use than *C*, but also more difficult to use than *Python* from a typing point of view.

Additional features that the languages offer:

- *Python* and *Rust* both offer iterators, which are a high level abstraction over loops;
- *C* and *Rust* both offer more control over data movement through references and pointer;
- *Python* and *Rust* both have an official package manager, while *C* does not;
- *Python* and *Rust* are both memory safe, meaning that memory management is automatic and not prone to errors;
- *Rust* is a thread-safe language, meaning that multithreaded programs are easier to write and less prone to errors;
- *C* and *Rust* are both well suited for embedded development, while *Python* has seen use in embedded development, it is not as well suited as the other two languages, due to performance constraints;
- *Rust* does not have truthiness: only `true` and `false` are considered boolean values, while *Python* and *C* have truthiness, meaning that several types of values can be used as a boolean value.

3.5.b Digital hardware description languages

Unlike traditional programming languages, digital HDLs try and represent digital circuitry using code. This means that the code is not executed, but rather synthesized into hardware that can be built. This hardware is generally in one of two forms: logic gates that can be built discretely, or LUTs (*Look Up Table*) programmed on an FPGA. Both processes involve "running" the code through a synthesizer that produces a netlist and a list of operations that are needed to implement the circuit. As was previously discussed, in Section 3.1, languages can serve as the foundation to build abstractions over complex systems, however, most HDLs tend to only have an abstraction over the RTL (*Register Transfer Level*) level, which is the level that describes the movement, and processing of data between registers. Registers are memory cells commonly used in digital logic that store the result of operations between clock cycles. This means that the abstraction level of most HDLs is very low.

This low level of abstraction can be better understood by understanding three factors regarding digital logic programming, the first is the economic aspect, custom ICs (*Integrated Circuit*) are very expensive to design and produce, as such, the larger the design, the larger the dies needed, which increases cost; and FPGAs are very expensive devices, the larger the design, the

more space it physically occupies inside of the FPGA, increasing the size needed and therefore the cost. The second factor is the design complexity: the more complex the design, the more difficult it is to verify and the slower it is to simulate which decreases productivity. The third factor is with regard to performance, performance of a design is characterized by three criteria, one criterion is the speed of the algorithm being implemented, another one is the power consumed for a given operation, and the area that the circuit occupies. These performance definitions are often referred to be the acronym PPA (*Power, Performance, Area*). As such, the design is generally done at a lower level of abstraction to try and meet performance targets.

High-level synthesis

Definition: **High-level Synthesis (HLS)** is the process of translating high-level abstractions in a programming language into RTL (*Register Transfer Level*) level descriptions. This process is generally done by a compiler that takes as an input the high-level language and translates the code into a lower-level form.

Adapter from [54, 63]

There has been a push in recent years towards higher level of abstraction for digital HDLs. It takes the form of so-called HLS (*High Level Synthesis*) languages. These languages allow the user to build their design at a higher level of abstraction, which is generally simpler and more productive [64]. Allowing the user to focus on the feature they are trying to build and not the low level implementation of those designs. As was discussed in Section 3.1, this can be seen as a move towards declarative programming, or at least, a less imperative programming model. Coupled with the rise of hardware accelerator in the data center and cloud markets, which are generally either GPUs (*Graphics Processing Unit – also commonly used for highly parallel computing and machine learning*) or FPGAs, there has been an increased need for software developer to be able to use these FPGA based accelerators. Because these software developers are generally not electrical engineers, and due to the high complexity of FPGAs, developing for such devices is not an easy skill to acquire. This has provided an industry drive towards economically viable HLS languages and tools that can be used by software developers to program FPGA based accelerators.

Another advantage of HLS is the ability to test the hardware using traditional testing frameworks, as discussed in Section 3.4. l, testing systems for HDLs tend to be vendored and therefore difficult to port. Additionally, they are based on simulation of the behaviour which is generally slower than running the equivalent CPU (*Central Processing Unit*) instructions. Therefore, the ability to test the hardware using traditional testing frameworks is a major advantage of HLS languages. In the same way that it allows the use of regular testing frameworks, it also enables the reuse of well tested algorithms that may already be implemented in a given ecosystem which can drastically lower the development time of a given design, as well as reduce the risk of errors. In addition to being able to use existing testing framework, the code can be verified using provers and formal verification tools, which can prove the correctness of an implementation, something that does not exist for traditional RTL level development.

Given that HLS development is generally easier, more productive and allows for reuse of existing well-tested resources, it is a sensible alternative to traditional RTL level development. However, it does come at the cost of generally higher resource usage, and lower performance. This is due to the fact that the HLS abstractions are still not mature enough to meet the performance of hand-written HDL code. However, there has been a push towards greater level of optimization, such as using the breadth of optimization available in the LLVM (*Low Level Virtual Machine*) compiler. This has allowed HLS to reach a

level of performance that is acceptable for large swath of applications, especially when designed by non-specialists [65]. Other techniques such as machine learning based optimization techniques have been used to increase performance even further [66].

Modern RTL languages

In parallel to HLS development, a lot of higher level RTL languages and libraries have been created, such as *MyHDL*, *Chisel*, and *SpinalHDL*. These alternative are positioned as an alternative to traditional HDLs such as *SystemVerilog*, they are often libraries for existing languages such as *Python*, and therefore inherit their broad ecosystems. As discussed in Section 3.4.I, HDLs, tend to be lackluster – or highly vendor-locked – with regards to development tools. And just as in the case for HLS, this can be an argument in favour of using alternatives, such as these HDL implemented inside of existing languages.

These HDLs are generally implemented as translators, where, instead of doing synthesis down to the netlist level, they translate the user's code into a traditional HDL. As such, they are not a replacement for traditional HDLs, but offer a higher level of abstraction and better tooling through the use of more generic languages. This places these tools in an interesting place, where users can use them for their nicer ecosystems and easier development, but still have the low-level control that traditional HDLs offer. This is in contrast to HLS, where this control is often lost due to the higher level of abstraction over the circuit's behaviour. Additionally, these tools often integrate well with existing package-managers which are available for the language of choice, allowing for easy reuse and sharing of existing libraries.

3.5.c Comparison

For the comparison, three HDLs of varying reach and abstraction levels will be used: *VHDL*, *MyHDL*, and *SystemC*. They each represent one of the aforementioned categories, being traditional HDLs, modern RTL-level languages, and HLS languages. For this comparison, a simple example of an n-bit adder will be used, where n is a parameter of the design. This will allow the demonstration of procedural generation of hardware, as well as the use of modules and submodules to structure code.

Most HDL languages come with pre-built implementations of adders. Usually, the best implementation of the adder is chosen by the compiler or synthesis tool based on constraints defined by the user. These constraints can relate to the area, power consumption or timing requirements. In this case, the adders implemented are simple combinatory ripple-carry adders, which are generally not the best implementation.

In the first example, in Listing 6, it can be seen that the VHDL implementation is verbose, giving details for all parameters and having to import all of the basic packages (line 2). In VHDL, the ports, as well as other properties are defined in the `entity` and the implementation of the logic is done in an `architecture` block. This leads to functionality being spread over multiple locations, generally reducing readability.

```vhdl
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity Adder is
5  Generic(n:integer:=8);
6      Port ( Cin : in  STD_LOGIC;
7             A : in  STD_LOGIC_VECTOR (n-1 downto 0);
```

```
8             B : in  STD_LOGIC_VECTOR (n-1 downto 0);
9             Result : out  STD_LOGIC_VECTOR (n downto 0));
10 end Adder;
11
12 architecture Behavioral of Adder is
13     -- Full Adder component
14     COMPONENT FullAdder
15     PORT(
16         A : IN std_logic;
17         B : IN std_logic;
18         Cin : IN std_logic;
19         S : OUT std_logic;
20         Cout : OUT std_logic
21         );
22     END COMPONENT;
23     signal carry : std_logic_vector(n downto 0);
24 begin
25 -- external carry input
26 carry(0) <= Cin;
27 -- Array of full adders
28 FA_array: For i in 0 to n-1 generate
29     Inst_FullAdder: FullAdder PORT MAP(
30         A => A(i),
31         B => B(i),
32         Cin => carry(i),
33         S => Result(i),
34         Cout => carry(i+1) -- connect the output carry to the input carry of the
   next FA
35     );
36 end generate FA_array;
37 -- output carry
38 Result(n) <= carry(n);
39 end Behavioral;
```

Listing 6 | Example of a n-bit adder in VHDL, based on [2].

```
1  from myhdl import *                                          Python
2
3  @block
4  def bit_adder(A, B, Cin, S, Cout):
5      """ 1-bit adder with carry in and carry out """
```

```
    @always_comb
    def logic():
        S.next = A ^ B ^ Cin
        Cout.next = (A & B) | (A & Cin) | (B & Cin)

    return logic

@block
def nbit_adder(A, B, Cin, S, Cout):
    """ n-bit adder with carry in and carry out """
    @always_comb
    def logic():
        Carries = [Signal(bool(0)) for i in range(len(A))]
        Carries[0].next = Cin
        for i in range(len(A)):
            if i == len(A) - 1:
                bit_adder(A[i], B[i], Carries[i], S[i], Cout)
            else:
                bit_adder(A[i], B[i], Carries[i], S[i], Carries[i + 1])
    return logic
```

LISTING 7 | Example of a n-bit adder in *MyHDL*, based on [2].

```c
#include "systemc.h"

#ifndef N
    #define N 8
#endif

SC_MODULE (BIT_ADDER) {
    sc_in<sc_logic> a, b, cin;
    sc_out<sc_logic> sum,cout;

    SC_CTOR (BIT_ADDER)
{
        SC_METHOD (process);
        sensitive << a << b << cin;
    }

    void process() {
        sc_logic aANDb, aXORb, cinANDaXORb;
```

```
19
20          aANDb = a.read() & b.read();
21          aXORb = a.read() ^ b.read();
22          cinANDaXORb = cin.read() & aXORb;
23
24          sum = aXORb ^ cin.read();
25          cout = aANDb | cinANDaXORb;
26      }
27  };
28
29  SC_MODULE (NBIT_ADDER) {
30      sc_in<sc_lv<N> > a, b;
31      sc_in<sc_logic> cin;
32      sc_out<sc_lv<N> > sum;
33      sc_out<sc_logic> cout;
34
35      sc_signal<sc_logic> ss[N], cc[N];
36
37      BIT_ADDER* add[N];
38
39      SC_CTOR (NBIT_ADDER)
40  {
41          SC_METHOD (process);
42      }
43
44      void process() {
45          int i = 0;
46          for(i = 0; i < N; i++) {
47              char name[25];
48              sprintf(name, "add_%d", i);
49              add[i] = new BIT_ADDER(name);
50
51              if (i == 0) {
52                  add[i] << a[i] << b[i] << cin << sum[i] << cc[i + 1];
53              } else if (i == N - 1) {
54                  add[i] << a[i] << b[i] << cc[i] << sum[i] << cout;
55              } else {
56                  add[i] << a[i] << b[i] << cc[i] << sum[i] << cc[i + 1];
57              }
58          }
```

```
59         }
60     };
61
```

Listing 8 | Example of a n-bit adder in *SystemC*, based on [2].

3.5.d Analog simulation languages

3.6 Analysis of programming paradigms

3.6.a Imperative programming

3.6.b Object-oriented programming

3.6.c Functional programming

3.6.d Logic programming

3.6.e Dataflow programming

3.7 Existing framework

3.8 Long term compatibility and cross-vendor support

3.9 A primer on calculability and complexity

3.10 Hardware-software co-design

3.11 Summary

From the aforementioned criteria, one may give a score for each of the discussed languages based on its suitability for a given application. This is done in Table 3. The score is given on a scale of 1 to 5, with 1 being the lowest and 5 being the highest. The score is given based on the following criteria: the maturity of the ecosystem and the suitability for different scenarios that were previously explored, notably: API design, root language – i.e as the basis for reusing the existing ecosystem and syntax – and the implementation of a new language – i.e using the language to build the ecosystem components of a new language. RTL languages implemented on top of *Python* are not included in the table. Neither is SPICE due to its restrictive scope.

From Table 3, one can see that for the creation of a new language, the best languages to implement it in are *Rust* and *C*. And the best languages to inspire the syntax and semantics are *Python* and *Verilog-AMS*, additionally, *C* is also a good inspiration due its widespread use and the familiarity of its syntax. Finally, for the implementation of an API, the best choice is *Python* due to its maturity, simplicity and popularity in academic and engineering circles.

Language	Applications			
	Ecosystem	API design	Root language	New language
C	●●●○○	●●○○○	●●○○○	●●●●○
	C is a fully featured low-level language, it is performant and has a simple syntax. However, it lacks some of the more modern ecosystem components, and is error prone. Because of this, it is unsuitable for API design, since it would require the user to be familiar with memory management. It lacks a lot of the semantics of hardware description which makes it unsuitable as a root language. However, its large array of language-implementation libraries makes it a good candidate for the implementation of a new language.			
Rust	●●●●●	●●○○○	●●○○○	●●●●●
	Rust is a modern low-level language, it is very performant, has excellent first-party tooling, quickly growing in popularity, and has is memory safe. However, it has difficult syntax and semantics that is unwelcoming for non-developers, which makes it unsuitable for either API design or as a root language. However, its large array of language-implementation libraries coupled with its memory and thread safety makes it an excellent candidate for the implementation of a new language.			
Python	●●●●○	●●●●●	●●●●○	●●○○○
	Python is a mature high-level language that sees wide use within the academic community, it has great third-party tooling, and is easy to learn. These factors make it an excellent candidate for API design and as a root language. However, its slowness and error-prone dynamic typing make it an unsuitable candidate for the implementation of a new language.			
Verilog-AMS	●○○○○	○○○○○	●●●○○	○○○○○
	Verilog-AMS is a mixed signal simulation software, its ecosystem is lackluster with many proprietary tools which incurs expensive licenses. It not a generic language and is therefore not design for an API to be implemented in the language, nor is it suitable for the implementation of a new language. However, it is a mature language with a familiar syntax to electrical engineers which may make it suitable as the root language.			
VHDL	●○○○○	○○○○○	●○○○○	○○○○○
	VHDL is a mature language with a large ecosystem, but suffers from the same issues than Verilog-AMS, most notably that most tools are proprietary and licensed. Similarly, its nature as a hardware description language makes it unsuitable for API design or the creation of a new language. Its verbose syntax and semantics are difficult to learn and make the language difficult to read, which makes it unsuitable as a root language.			

Table 3 | Comparison of the different languages based on the criteria discussed in Section 3.11.

4.

Translation of intent & requirements

In Section 3, the different programming ecosystem components, paradigms and tradeoffs were discussed. In this section, the translation of the user's intent – i.e the design they wish to implement – will be discussed in further detail. The translation of intent is the way in which the user will write down their design, and how the program translate that design into an actionable, programmable, design. This section will also outline some of the features that are needed for easier translation of intent. This will be done by discussing important features such as *tunability*, *reconfigurability*, and *programmability*. These features revolve around the ability for the user to tune the operation of their programmed photonic processor as it is running. For this purpose, this section will introduce some novel concepts, such as *constraints* and its *solver* and *reconfigurability through branching*. These two important concepts will be discussed in details and synergize to create an easy to use, yet powerful, programming ecosystem for photonic processors.

Additionally to the aforementioned points, several key features were discussed in Section 2.4, the features relate to realtime control, which works in pair with *reconfigurability* and *tunability*, simulation, which will use *constraints* and its solver. Platform independence, which will be achieved through the design of a unified vendor-agnostic ecosystem and, the visualization of the design, which has lead to the design of the *marshalling layers* which will be discussed in Section 5.8.

Definition: **Synthesis** is the process of transforming the description of a desired circuit into a physical circuit.

Adapted from insert reference

Synthesis is the process of transforming the user's code into a physical circuit on the chip. It is done in a multitude of stages, that will be discussed in Section 5. These stages are all required to go from the user's code, which represents their intent, and turn it into an actionable design that can be executed on the photonic processor. The synthesis process is complex, involving many different components that all need to cooperate. Additionally, some of the tasks that synthesis must do, such as place-and-route, are incredibly computationally intensive and are often regarded as being NP-hard.

4.1 Functional requirements

Definition: A **functional requirement** is a requirement that specifies a function that a system or component of a system must be able to perform.

Adapted from insert reference

Before a user can design their circuit, they must list their functional requirement, these requirements are the functionality that they wish for their circuit to achieve. As previously discussed, in Section 3.1, one can see these requirement as the most declarative form of the user's intent. Therefore, one can see this step as the user's intent.

However, there are elements that are generally going to be common to all of those functional requirements. And can be seen as the functional requirements for intent translation. These requirements are can be seen in Table 4 and are discussed in the following sections.

	Requirement	Description	Discussion
	Ideal behaviour	As discussed in Section 2.3, devices vary from device to device and over time and temperature. The user should be able to program the device without having to worry about these variations.	Section 4.9
Realtime feedback	Reconfigurability	Reconfigurability allows the user to change the topology of their device at runtime, this is useful for several reasons, the primary reason is the ability to change behaviour based on configurations or inputs.	Section 4.5
	Tunability	Tunability on the other hand does not change the topology in itself, but rather changes the behaviour of the mesh through the tuning of elements already present in the mesh. This may be used to vary gains, phase shifters, switches, or couplers to affect the behaviour of the mesh. This can also allow the user to build feedback loops that they control.	Section 4.5
	Programmability	In order to be able to make use of tunability and reconfigurability, the user must be able to programmatically communicate with their programmed device. This is done through the user of a HAL (*Hardware Abstraction Layer*), that handles communication with the device.	Section 4.2
	Simulation	Simulation allows the user to test their code, verify whether it works and debug it before running it on the device. This is an important feature as it also allows the user to experiment without having access to the device.	Section 4.6
	Platform independence	Platform independence allows the user to focus on their design rather than the specific device it is expected to run on. While some degree of platform dependence is to be expected, most of the code should be platform independent and allowed to run on any device.	Section 4.7
	Visualization	Visualization allows the user to see the result of a simulation, what a finalized design looks like, block diagrams of functionality. All of these features can help the user in their design process, but also help the user when sharing information with others. Therefore, providing visualization is desireable.	Section 4.8

Table 4 | Functional requirements for intent translation

4.2 Programmability

Definition: A **HAL (*Hardware Abstraction Layer*)** is a library whose purpose is to abstract the hardware with a higher-level of abstraction, allowing for easier use and programming of the hardware.

Adapted from [67].

Programmability refers to the ability for the user to programmatically interact with their circuit while it is running. This is done using a HAL, which allows for interoperation between their software and their hardware, completing the hardware-software co-design loop. The HAL is made of two parts: the core HAL which is provided by the device manufacturer and the user HAL which is generated by the compiler based on the user's code.

Core HAL As previously mentioned, the core HAL is provided by the device manufacturer and consists mostly of communication routines, it handles the communication between the user's software and the device. This HAL is therefore platform specific and is not generated by the compiler. However, the core HAL must be able to communicate with the user HAL, which is generated by the compiler. This is done by enforcing that all HALs implement a common API that allows the user to interact with both the core HAL and the user HAL in a consistent way, making the code as portable as possible.

User HAL The user HAL is a higher level part of the HAL built from the user's design, it encapsulates the tunable values, reconfiguration states and detectors that are defined within the design, and allows the user to change these values, reconfigure the device and readout detectors. All the while, using the names the user defined for these different values. This allows the user to interact with the device in a way that is consistent with their design, and therefore easier to understand and use. This should improve productivity and reduce the risk of error in the hardware-software co-design interface.

User HAL template The user HAL needs to be generated from the user's design, however, there may be elements of this HAL that are platform specific and therefore must be generated instead by the device support package. This is expected to be done by allowing the device support package to generate part of the user HAL through template or custom code. This allows the device support package to provide platform-specific features to the user HAL or to optimize common implementations for the platform, further improving the quality and usability of the generated interface.

4.3 Intrinsic operations

From the physical properties and features of a photonic processor, as discussed in Section 2, one can derive a set of intrinsic operations that must be supported by the processor. These operation in themselves are not required to be on the chip, but the support packages of the chip must be able to understand them and produce errors when they are not implemented. A full list with a description can be found in Table 5. In this section, the intrinsic operators will be discussed in more detail.

Filter One of the core operations that almost all photonic circuit perform is filtering, they filter input signals to produce output signals of known spectral content. Due to the prevalence of filters in photonic circuits, coupled with their special constraint – see below – they have to be a unit operation for a photonic processor. During compilation and before place-and-route, the filter will be synthesized based on its arguments in order to produce a filter of the desired frequency response. There are many different types of filters, the most common ones, that can easily be implemented on a mesh – are MZIs (*Mach-Zehnder Interferometer*), ring resonators, and lattice filters. Additionally, compound filters combining multiple types of filters and more than one filter can be created. Therefore, it is the task of the compiler to chose the base filter based on the specification and performance criteria that the user has set. For example, the user might prioritize optimizing for mesh usage rather than finesse, or might optimize for flatness of the phase response rather than the mesh usage, etc.

Gain and loss All waveguides within a device will cause power loss in the optical signals, however, this loss may not be sufficient if the user is working with high power signal, therefore some devices might include special loss elements whose loss is tunable or at least known. Besides, following the same principle, some users may want to compensate for this loss by using gain sections, or even amplify incoming signals. Optical gain is difficult to obtain on silicon platforms, just like sources, but it is possible to obtain gain through the use of rare-earth doped waveguides, or other techniques such as micro-transfer printing. Therefore, the compiler must be able to synthesize gain and loss sections based on the user's specification. However, if the device does not support gain or loss, the compiler should produce an appropriate error to the user.

Modulator and detectors Two of the key applications of photonic processor is in telecommunication and processing of RF signals. Therefore, it stands to reason that modulators and detectors are key components that are expected to be present in most photonic processors. Additionally, based on the device, there may be an optimal type of modulator for either type – phase modulation or amplitude modulation – and the compiler may chose an appropriate implementation of the modulator. Additionally, the same is true for detectors although they would generally only be used for amplitude demodulation, with phase coherent demodulation being the responsibility of the user.

Splitters Signals are often split, and they may be split in specific ratios. For this reason, a splitter intrinsic operation that splits a signal into n new-signals with weight provided by the user is desirable. Internally, the compiler will likely have to implement these splitters as 1-to-2 splitters with specific splitting ratios, but the user should not have to worry about this. Additionally, the compiler can optimize the placement of these splitters to minimize the mesh usage, or to minimize non-linear effects in high power signals, or to maintain phase coherence between signals.

Combiners and interferometers A combiner is the inverse of a splitter, it combines n signals together, it can operate in one of two modes, it can either try and reach a target power level – which can be the maximum power – or it can interfere the signals with their differential phase to create interference. The user is responsible for choosing which implementation to use, however in cases where the phase is well known, the compiler may be able to optimize the design by using a phase coherent combiner, thus not requiring a feedback loop and a phase shifter.

Switches Some devices may have hardware optical switches, while other may need to rely on feedback loops. Generally, all platforms should be able to support switching, whether they rely on purpose-built hardware or on feedback loops does not matter. Switching can be useful in many applications, including telecommunication, signal processing, etc. It may be used to route test signals, route signal conditionally, or to implement simple reconfigurability without the added cost of having more than one mesh.

Sources A lot of applications will need generation of laser light, while this is difficult to achieve on silicon, it may be available on some devices. As laser sources are such an important part of photonics, it is important to at least plan for sources to be available in the future. Additionally, in some cases, the compiler may be able to synthesize a source from a gain source, reflectors and splitters. However, this is not always possible, and the compiler should be able to produce an error if the user requests a source and none is available.

Phase shifter Phase shifters are a necessary building block for a lot of more complex structures such as tunable MZIs, tunable filters, coherent communication, power combiners, etc. Therefore, as an integral part of the functioning of photonic processing, they must be present as an intrinsic operation. Additionally, they may be used in two different modes: the first mode is as a phase shifter, shifting the phase of a single signal, the second mode is as a differential phase shifter, imposing a phase shift with respect to another signal. This case is especially interesting as it can be used to implement complex quadrature modulation schemes. In Section 6, examples regarding coherent communication will be presented that make use of this intrinsic operation to implement complex modulation schemes, as well as to implement a beam forming network.

Delay lines Each waveguide being used on the chip adds latency to the signal. While this latency may be low at the scale of a modulated signal, it can still be relatively significant overall. For this reason, the device must provide ways for the user to align signals in time, either by using a delay line, or by using multiple wires of different lengths in order of matching the total optical length. It works nicely with the ability to express differential constraint which will be discussed in Section 4.4.

Intrinsic operation	Description	Arguments
Filter	Filters a given signal at a given wavelength or set of wavelengths. The architecture and parameters are derived automatically from its arguments and the constraints on its input signal.	• ✓ Input signal • ✓ Through signal • ~ Drop signal • ✓ Wavelength response
Gain/loss	Gain/loss sections allow the user to increase or decrease the power of a signal. The platform may not support gain or loss, in which case the operation will fail.	• ✓ Input signal • ✓ Output signal • ✓ Gain/loss
Modulator	A phase or amplitude modulator, that uses an external electrical signal as the modulation source. The implementation is chosen by the support package based on the type of modulator.	• ✓ Input signal • ✓ Output signal • ✓ Modulation source • ✓ Modulation type
Detector	A detector that converts an optical signal to an electrical signal.	• ✓ Input signal • ✓ Output signal
Splitter	A splitter that splits an optical signal into multiple optical signals.	• ✓ Input signal • ✓ Output signals • ✓ Splitting ratios
Combiner	A combiner that combines multiple optical signals into a single optical signal. While maximizing the total output power.	• ✓ Input signals • ✓ Output signal
Interferometers	A combiner that combines multiple optical signals into a single optical signal. Does not perform any power optimization.	• ✓ Input signals • ✓ Output signal
Switch	A switch that switches between two optical signals.	• ✓ Input signal • ✓ Output signal • ✓ Switch state
Source	A laser source that generates an optical signal.	• ✓ Output signal • ✓ Wavelength
Phase shifter	A phase shifter that shifts the phase of an optical signal. Optionally, performs the phase shift in reference to another signal.	• ✓ Input signal • ~ Reference signal • ✓ Output signal • ✓ Phase shift
Delay	A delay that delays an optical signal.	• ✓ Input signal • ✓ Output signal • ✓ Delay

Table 5 Intrinsic operations in photonic processors, with their name, description and arguments. For each arguments, an icon indicates whether the argument is required (✓) or optional (~). Additionally, the type of the value is also indicated by an icon, it can be optical (☼), electrical (ϟ), or a value (⁓).

4.4 Constraints

Constraints are a technique for expressing constraints on values and signals. They are associated with each signal or value to give additional information regarding its contents. In Section 9, the concept of using constraints with *refinement types* will also be discussed as a potential future expansion of constraints. The core idea of constraints is that the user can use them to specify additional information about their signals at a given point in the code. Additionally, they can be used to check the validity of the code, and to infer additional constraints. This is done by the *constraint solver*. This section will discuss the multiple aspects of constraints, and their use.

Constraints in themselves are not a new concept, however, the way in which they are applied to include more complex constraints, to simulate circuits, and inferring them, does *appear* to be novel.

Constraints for validation The primary use of constraints is for the validation of the code. This is done by the *constraint solver* discussed later. The constraint solver will use the constraints to check whether they are compatible with one another. This is done by annotating some functions with constraints, and then checking whether the input signals are compatible with those constraints. If the constraints are not compatible, a warning, or an error can be presented to the user.

Constraints can be of many types, the likely most common ones are going to be constraints on power, gain, wavelength, delay, and phase. The reasoning behind why delay and phase are different constraints is because they most often will have different semantics, where phase refers to the phase of the light within the waveguide and the delay will mostly impact the delay of the modulated information on the signal. Since light operates at frequencies much higher than the RF range, one can consider the phase of the light to be mostly decoupled from the phase of the signal. These constraints can be used to verify the validity of the code, and to inform the compiler how to optimize and generate the design. Indeed, in some cases, the user might have a high power signal coming onto the chip that gets split. The place-and-route system can either place the splitter close to the input or closer to the components using this light. One can use the input power constraint to make a decision, since at high power, there will be increased non-linearities and losses within the waveguide. Therefore, the place-and-route can use this information to make a decision on where to place the splitter. This is just one example of how constraints inform the compilation system and can be used to optimize the design.

Constraints for simulation Additionally to the aforementioned constraints, one can also express constraints that are useful for simulation such as noise sources, modulation inputs, etc. These constraints do not make sense for the compilation process as they are not actionable at compile time; however, they are actionable for creating more realistic, closer to physical simulations. These special constraints can be used for a variety of things and are in essence non-synthesizable, whereas the other constraints are synthesizable.

These non-synthesizable constraints, can be couple with synthesizable constraints to create a more realistic, yet very inexpensive simulation. As will be discussed in Section 4.6, simulating circuits using constraints is extremely fast. And due to the integration of constraints within the language, as will be discussed in Section 5.3.a, it makes them an inherent part of the user's design. Meaning that accurate, yet fast, simulations are available to the user at all times.

Constraints for optimization As previously mentioned, constraints can be used as indicators for stages within the synthesis process. Therefore, it stands to reason that constraints can be used to optimize the design. The compiler can use constraints to remove unnecessary components, or to optimize the placement of said components. A simple example, a signal going through a filter might have a constraint on the wavelength, and the filter might have a constraint on the wavelength. If the compiler can prove that the filter is not needed, it can remove the filter altogether. Alternatively, if it detects that after the filter there would be so signal left, it can remove the filter and all dependent components, simplifying the design. This is just one example of how constraints can be used to optimize the design.

Constraints as realtime feedback As discussed in Section 2.1.a.c, there are power detectors on the chip that can be used for monitoring purposes. These detectors are expected to be implicitly and automatically used most of the time through the use of intrinsic components and their platform-specific implementation. However, it can be interesting to give access to these monitors to the user. This can be done by using constraints on the power and gain. Where these constraints can be used to check, while the device is running whether constraints on power and gain are respected, notifying the user if they are not. This gives the user the ability to add detection of erroneous events, such as the loss of an input or failing to meet gain requirements. This can be used to notify the user's control software of the error so that they may react appropriately to the error. Indeed, through the use of detectors, and especially implicit detectors, the user may gain insight into the state of the device.

Categories of constraints Using the aforementioned sections, one can categorize constraints into three distinct categories: synthesizable constraints, which are used for realtime feedback, simulation constraints, which are used for simulation, and meta constraints which are only used by the compiler. These three categories are not mutually exclusive: most constraints can be used by the compiler and for simulation, but some of them are only used for these purposes, therefore, one can see all constraints as being a hierarchy that can be seen in Figure 4. It shows that all constraints are simulation constraints, some of which are meta constraints and some of those are also synthesizable constraints. In Table 6, the different types of constraints are listed along with their category and a short explanation.

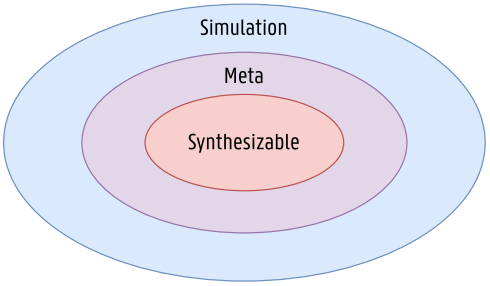


Figure 4 Hierarchy of constraints, showing that all constraints are simulation constraints, within that are meta constraints within which are synthesizable constraints.

	Constraint	Description
Synthesizable	Power	Power constraints are used to specify the power of a signal. At runtime, it can check whether signals are present and within certain power budgets by using detectors.
	Gain	Gain constraints are used to specify the gain created by a component. It can use detectors around a gain section to check whether a gain section is able to meet its parameters and to allow feedback control.
Meta	Wavelength	Wavelength constraints are used to specify the wavelength content of a signal. This is used for optimization of filters and other wavelength dependent components.
	Delay	Delay constraints are used to specify the actual, minimum, or maximum delay of a signal. This can be used to meet delay requirements after place-and-route.
	Phase	Phase constraints are used to specify differential phase of a signal. This can be used to ensure that phase sensitive circuits are able to work as intended.
Simulation	Noise	Noise constraints are used to add noise onto a signal. This can be used to simulate noise sources and to simulate the impact of noise on a device.
	Modulation	Modulation constraints are used to specify the modulation of a signal.

Table 6 | Different constraints on signals along with their category and a short explanation.

Constraints on values Expanding upon the concept on constraints further, it is possible to add constraints on values other than signals. It can allow the user to set specific constraints, typically on numerical values that can be used for two purposes. The first purpose is to allow validation of value automatically without needing to write manual tests for values, this is often called a *precondition*. The second purpose, which is further explained in Section 4.5, is the ability to discord reconfigurable states that cannot be reached based on the constraints. This is an optimization that can be done relatively easily by the compiler.

Constraint inference Constraints propagate through operations done in succession. Each intrinsic operation done on a signal adds its own constraints to the existing constraints. This allows the compiler to infer constraints on intermediary and output signals based on existing constraints and the constraints of the intrinsic operations. This is done by the compiler to allow the user to specify as few constraints as possible, while still being able to infer the constraints on the signals. This feature is critical for the usability of the ecosystem, as it reduces the burden placed on the user of manually annotating their functions and signals with constraints. The constraints of entire functions can be computed and then summarized – i.e simplified and grouped together – which simplifies the role of the simulator as it is simply using these simplified constraints and applying them to input spectrums and signals. This leads to a more efficient simulation which is much faster than traditional physical simulations. This is examined further in Section 8.

Constraint solver The solver is the tool that the compiler uses to summarize and check constraints. It is used by the compiler for these two operations, where it will summarize the constraints on each signal such that it can be easily simulated, and it will verify that constraints are compatible. Additionally, in cases where the constraints depend on tunable values – i.e values that can be changed at runtime – the solver can use a prover and the constraints on the tunable value to determine whether the constraints are compatible. This is done by using a prover such as *Z3*. However, this is a very computationally expensive process and must therefore only be performed when necessary. This is why the compiler will only use the prover when the constraints depend on tunable values.

Therefore, one can see the constraint solver as a tool composed of two subsystems, the first one computing and verifying constraints based on known data, it is simpler and faster, and the second one computing and verifying constraints based on tunable values, it is more complex, relying instead on a prover, which is solver.

Limitations of constraints There are however limitations of the constraint system, most notably that, using the aforementioned solver, constraints are limited to exclusively feedforward system. And as discussed in Section 2.2.c, one can represent any recirculating circuit as a feedforward system. But there is one necessary condition for this to hold: it *must* be at a higher level of abstraction. When building the abstraction, this axiom cannot be assumed true. Therefore, the constraint system is limited in such cases. Therefore, the system must provide an "escape-hatch", which allows the user to manually specify constraints at the edge of abstractions, such that the compiler can use them outside of the abstraction while pausing computation inside. When pausing this computer, the user can now express recirculating circuits easily by using the escape-hatch to specify constraints on signals that are not feedforward.

Constraints can be used to validate signals, eliminate branches, and simulate the design. They are implemented using the constraint-solver which can either combine constraints or using a prover like *Z3* to verify constraints. However, they are limited to feedforward systems, and therefore an escape-hatch is needed to specify constraints on recirculating circuits.

4.5 Tunability & Reconfigurability

Definition: **Tunability** is the ability to change the value of a value at runtime to impact the behavior of the programmed device.

Tunable values are values that can be interacted with, by the user, at runtime. They can be any non-signal value in the user's program, typically numerical values, that the user defines as being tunable values. These values can be seen as tuning-knobs that the user can access at runtime to change the behaviour of their circuit, and to implement their own custom feedback loops. Tunable values can impact several parts of the design at once, for example, a single value may determine the center frequency of operation of a bank of filters, all of them being changed when one tunable value has been changed. This makes tunable values especially powerful as their impact can be propagated through the entire design.

The core idea behind tunable values is that the user can now represent parts of the parameters of their design as runtime values that can be interacted with, while keeping all of the derived values within the circuit code itself. The purpose of this design is to make hardware-software co-design easier and more productive. Where instead of having the complex relationships between parameters expressed within the "software" part of hardware-software co-design, they can instead be directly expressed on what they impact: the "hardware" part. This makes the design process more intuitive, and also removes the potential for discrepancies between the hardware and the software.

Additionally, the user should be able to name their tunable values and to be able to access them by name within their own code. This further improves the usability of the system, as it removes the need to maintain complex, error-prone table of registers and their corresponding values. Instead, the user can address their tunable value in a natural way through its name, and HAL can take care of the rest: translating these names and values into an appropriate set of registers and values.

This means that the physical parameters of each element, can be represented as natural parameters – i.e numerical values – while the underlying hardware uses lower-level likely binary values and flags. This improves the development experience of the device provider as well, as they can now integrate within their platform support package, the code required to do data conversion, further simplifying the development of new support packages.

Furthermore, the use of constraints on values, such as explained in Section 4.4, can be used by the compiler to further detect the need for reconfigurability automatically, without additional user input. It can also be used to validate that when a tunable value is changed in the user's software, that it meets its requirements, ensuring that the user cannot change the value to an invalid one, where the device might then operate in an undefined state.

Definition: **Reconfigurability** is the ability to change the structure of the device at runtime to change the topology of the device and therefore its behaviour.

Additionally, one of the most important functional requirements, is the reconfigurability. Its goal is to allow the user to reconfigure the mesh – or only parts of it – while the device is running. This can be achieved in a number of way, but the most natural way is to use branches within the code to determine the boundaries between reconfigurability regions. Then, through the use of tunable values, these regions can be automatically selected based on its value.

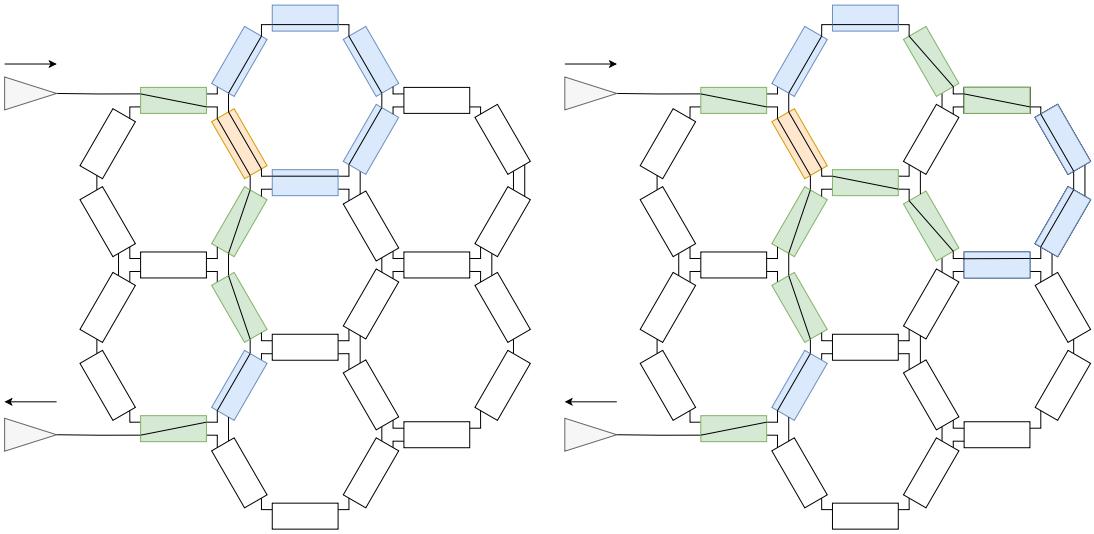
However, this brings a set of difficult problems to solve, the first of which is the ability to determine whether a state is even reachable. However, this can be done using constraints, through the constraint solver for tunable constraints, one can verify which states are reachable or not, and discard those that are unreachable. This is a powerful optimization, as it greatly decreases the amount of states that need to be place-and-route, and therefore the amount of time needed to compile the mesh.

Indeed, consider the following example, the user instantiates a mesh containing 64 input signals and 64 output signals, based on branching, each input signal can go into one of two filters. This therefore means that there are 2^{64} possible states. It can easily be understood that this is an intractable problem, as it would be almost impossible to synthesize the project. However, if the system is able to determine that for each signal, only two states are reachable, this comes down to 128 states, which is much more tractable. Therefore, one can see that there is an interest in finding ways of reducing the amount of states that need to be synthesized. One such way is by using the constraint solver to eliminate unreachable states. The second way is by finding subsets of the overall circuits that are independent from one another, and therefore can be mostly synthesized in isolation.

Neither of those two tasks are trivial, and therefore, it is desirable to let the user specify some of the state reduction manually, letting the user take care of parts of the more complex cases. One can draw a parallel between this and the use of the escape-hatch for constraints, as it is a similar concept, where the user can specify constraints manually at the edge of abstraction, while here the user can specify how to reduce the amount of states manually. Additionally, this idea of figuring out which parts of the mesh are independent from one another, is similar to the halting problem, which is undecidable. However, by limiting the maximum number of iterations, the recursion depth, or both, one can make it decidable. But despite being decidable, it still incurs a heavy computational cost.

In Figure 5, one may see what reconfigurability might look like on a fictitious device, where based on an input variable, a simple boolean in this case, the device will use either of two meshes. Each state (a) and (b) represents a different mesh that

implements a different filter. In this example the user would have created a tunable boolean that they can set at runtime, and based on its value, the appropriate mesh will be selected.



(a) (b)

FIGURE 5 Example of reconfigurability on a fictitious device. Each state (a) and (b) represent a different filter. The second (b) filter has a longer ring and therefore a higher FSR (*Free Spectral Range*) than the first one (a). Squares of different color represent photonic gates in different states: blue represents through gates, green represent cross gates, and yellow represents partial gates. The gray triangles represent optical ports.

Reconfigurability allows the user to create modular designs, where, at runtime, the user can select a different state to fit their needs. Reconfigurability is achieved through branching of the code. The user can specify tunable values that are used to select the appropriate branch. The number of states is exponential but can be decreased using the constraint solver to remove unnecessary branches, by finding independent subsets of the mesh, and by letting the user specify some of the state reduction manually.

4.6 Simulation

As previously discussed, the user must also be able to simulate their circuit. The traditional approach of physical simulation is slow, and therefore, it may be desirable to find solutions to make simulations faster. As was discussed in Section 1.1, there is ongoing research in using SPICE to simulate photonic circuits, additionally, some of this work is being conducted at the PRG (*Photonics Research Group*). One of the main advantages of this solutions, as opposed to the one that will be presented below, is that it allows for recirculating meshes. However, it is not as fast as the solution presented in this document, and therefore, it is not as well suited for the use case of this project. Additionally, the SPICE based simulations may be able to incorporate more effects, such as the effects of the non-linearity of components, which may lead to more accurate simulations. Despite this, the user may not want a physically correct simulation, instead they may want a simulation that is fast, and representative of their circuit without all of the limitations of the physical hardware. In essence, this is similar to simulations for FPGA development, where the simulations are not physical yet are still representative.

The simulation scheme that is suggested in this research, is to use constraints to simulate the circuit. The idea is that the constraint solver can be used to summarize the constraints on each net. It can then be used to calculate analytically the value of each net, and therefore, the value of each signal. The main difference with other approaches, is that due to the relative simplicity of constraints, this can be done very quickly, with relatively simple code. This simplicity both improves the performance of the simulation, as will be discussed in Section 8, but also decreases the work required to maintain and update this simulator as time goes on.

In practice, simulations would be separated into two categories: time domain simulation, which take one or more signals modulated onto carrier optical signals and simulated their processing, and a frequency domain simulation which looks at the frequency and phase response of the device. The reasoning behind this separation is as follows: due to the extremely high frequency of light, accurately representing light in the time domain is extremely difficult, as it requires very small time steps. Instead, if using the frequency domain, one can decouple the modulated signals, by using the spectral envelope of the modulated signal as the input to the simulation. This therefore allows for easy analysis of the spectral performance without the computation cost of small timesteps. Then, in the time domain, the user specifies sets of wavelengths which are then modulated with the signal of interest which can be passed through the device. This allows time domain simulation to use much bigger time steps, on the order of the modulate signal's period, rather than timesteps on the order of the light's period.

However, this does introduce a limitation, due to this dichotomy, the user needs to simulate both effect separately and analyze the results themselves. While this makes the process of simulation more limited, it also makes it more flexible, as if the user only needs one of the simulation kinds, they can avoid needing to simulate the other, decreasing computation time further.

Simulation ecosystem There exist many tools for simulation of photonic circuits. Additionally, there also exist a lot of tools for the kind of resolution that is being done. It is therefore of interest to reuse as much as the existing tools out there as possible. As long as these tools are free, they do not incur a cost on the user's end. Additionally, by reusing existing tools, the user can benefit the ecosystem that surrounds these solutions and the community that uses them. Furthermore, it also makes the development of the simulation ecosystem simpler, as it no longer required writing the entire simulation ecosystem from scratch. Instead reusing existing tools and making use of the best-in-class tools for each tasks.

4.7 Platform independence

As the development of photonic processor continues, it must be expected that new devices will bring new features, different hardware programming interfaces, and characteristics. Ideally, all of the code would be backward and forward compatible, being able to be programmed on an older or a newer device with little to no adjustments. Therefore, one must plan for platform support right at the core of the design of a photonic processor ecosystem. In this document several approaches will be suggested for tackling this issue. These approaches are meant to be used in conjunction with each other.

Standard library All platforms must share a common standard library that contains base building blocks and some more advanced synthesis tools – i.e filter synthesis – that is common across all devices. This library must be able to be used by all devices, therefore, it must be able to be compiled into the intrinsic operations mentioned in Section 4.3. Additionally, by providing common building blocks and abstraction, it makes the development of circuits targetting photonic processors easier. This is similar to the standard library that exists for regular software development, where the language provides a set of functionalities out-of-the-box that can be used by the user.

Platform support packages Each platform must come with a platform support packages that implements several tools: a hardware programmer for programming the circuit onto the device; compatibility layer for the standard library such that the standard library is compatible with the hardware; some device-specific libraries for additional features if needed; a place-and-route implementation, it may be shared across many devices, but the support package must at least list compatible place-and-route implementations. With these components, the user's circuit should be able to be compiled, while using the standard library, then programmed onto the device for a working circuit.

Hardware abstraction layer Each platform must come with a HAL which allows the user to interact with the device programmatically at runtime. This HAL must provide features for communicating, setting tunable components and reading the state of the device. The HAL can be reused across devices, as long as the devices have similar hardware interfaces. In Section 5.10, this will be further discussed, including how parts of the HAL can be generated based on the user's design for improved usability and easier hardware-software co-design.

Constraint packages It must also come with information regarding delays and phase response of its different components, as well as the capabilities of some of its components like amplifiers, modulators, etc. This information can be used by constraint-solver and the simulation ecosystem to more accurately represent the capabilities of the circuit and allow the user to make informed decisions. Additionally, a platform may come with additional simulation-specific constraints for more accurate simulations, in addition to the additional information provided by the constraint packages.

4.8 Visualization

There are several types of simulations that may be useful for the user: the user might want to visualize the generated circuit mesh superimposed onto a schematic representation of the device, to verify that no critical components were removed through constraints, to see the usage at a glance, or to visualize whether the place-and-route performed adequately. This visualization is already presented in the existing library and exists in EDA (*Electronic Design Automation*) tools for photonics. Therefore, such visualization facilities must be offered to the user. Especially due to the fairly early stage of research, the ability to communicate results visually is critical to the user's understanding of the results. Another kind of visualization the user will want is the results of the simulation results. Therefore, the ecosystem must provide easy visualization of results.

Applying DRY As is the case of the simulation ecosystem, one can reuse existing tools and libraries for visualization that are already on the market. This is an application of the DRY (*Don't Repeat Yourself*) principles, where one can reuse existing tools and libraries rather than rewriting them from scratch. This also allows the user to benefit from the large ecosystem of visualization tools that already exist, and to use the tools they are most familiar with, or that gives the best results for their application. Examples of such visualizations can be seen in Figure 5 that shows the mesh and the state of each gate, and a simulation result in Figure 6 which shows the results of a time-domain simulation using the aforementioned constraint-solver.

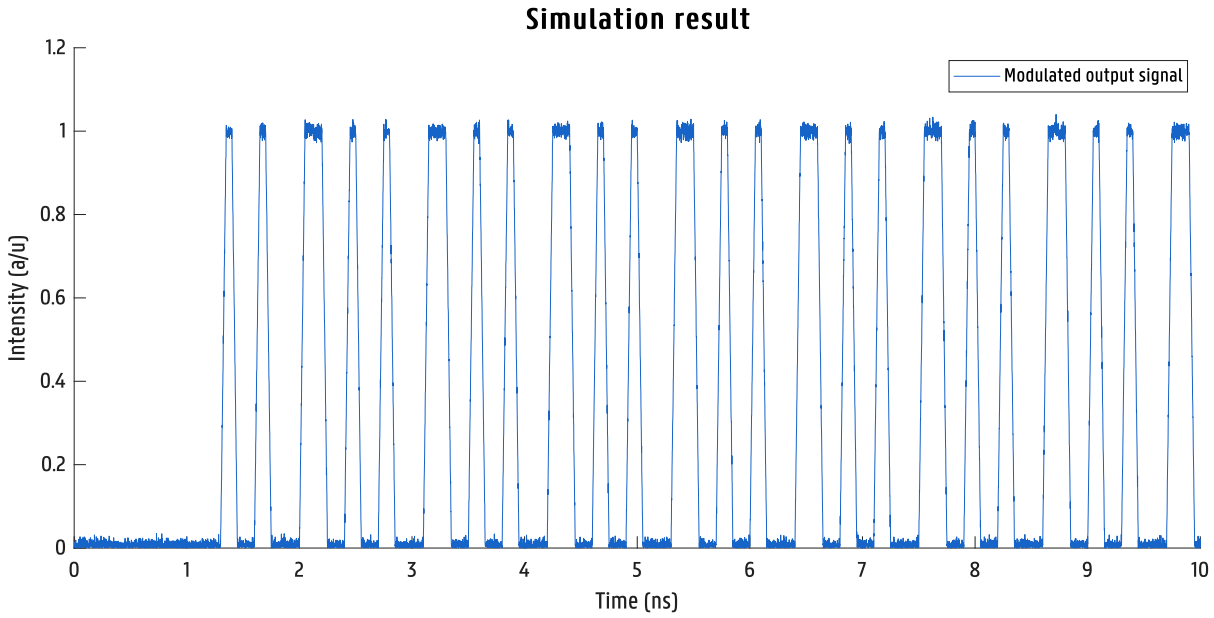


Figure 6 Example visualization of a time-domain simulation result, showing a $10\ \mathrm{Gb/s}$ modulated PRBS 15 sequence on top of a $1550\ \mathrm{nm}$ carrier. The simulation was performed using the constraint-solver. Shown is a $10\ \mathrm{ns}$ window of the simulation. The simulation was ran for a total of $1\ \mu\mathrm{s}$ with an average execution time of $9\ \mathrm{ms}$. The simulation simulates a laser source with noise and the rise and fall time of the modulated signal, the rise and fall time being $50\ \mathrm{ps}$.

4.9 Calibration and variation mitigations

Photonic circuits can be very sensitive to manufacturing variations and temperature variations. Therefore, each device must come with mitigation techniques that can aid in making the device behave as ideally as possible. This is expected to generally be done through the use of calibration curves or calibration LUTs. And by using feedback loops to ensure that a component behaves as expected. For example, a power combiner might maximize power output using a feedback loop on a phase shifter to create constructive interference.

Feedback loops Feedback loops are an essential part of being able to overcome variations, especially those caused by temperature variations. A feedback loop can be used to read a power monitor present on the chip and adjust the tunable value of another element. Feedback loops can be built-in, as in added automatically by the compiler for specific tasks, based on the device support package and the intrinsics being used. Or they can be created manually by the user, in which case they must write code that, using the HAL, reads the sensors and then writes to whichever tunable value they need.

Wavelength dependence Additionally to manufacturing variability and temperature dependence, the device's response are also wavelength dependent. This is due to the physical properties of the materials from which the device is made of, hence there are no easy ways of mitigating these effects. However, by using constraints, the compiler can know which wavelengths are expected in which component, and similarly to using calibration curves for device-to-device variability, it can use similar response curves to adjust the circuit to the expected wavelength. This is expected to be done automatically by the compiler, but it requires that the user specifies wavelength constraints.

4.10 Resource management

Another aspect of design circuits for programmable devices, whether they be traditional processors, FPGAs or photonic processor is resource management. Built into the hardware a limited number of elements, and the user must be able to use these elements as efficiently as possible. This may be especially true for photonic processors where, currently, the number of gates are relatively small. Below is Table 7 that lists potential resources that may be present on the device. These resources are obtained from the description of intrinsic values in Section 4.3 and the components of a photonic processor detailed in Section 2.1.

Resource	Description
Photonic gate	The photonic gate is the core element of the photonic processor, it can be arranged in a grid, whether square, triangular or hexagonal. It generally contains a 2-by-2 tunable coupler and power detectors for monitoring. It is used to process the light and to route the light around the chip.
High-speed detector	High-speed detectors are used to demodulate the light, they can operate either in an amplitude demodulation scheme or be used with interference to perform phase demodulation.
High-speed modulator	High-speed modulators are used to modulate the light, they can operate either in an phase modulation scheme or be used with a MZI to perform amplitude modulation.
Laser source	Laser sources are used to generate light at a given wavelength directly inside of the device. Currently, due to the devices being made in silicon, there are none on prototypes, however, in the future they may be added using epitaxial growth or micro-transfer printing.
Gain section	Gain sections are used to amplify the light, they are generally made of a semiconductor optical amplifier or an erbium-doped waveguide section. As with laser sources, there are currently no gain sections on prototypes.
Optical port	These are the ports at the edge of the device that can be used to couple light in and out of the device.
Switch	Switches can be either implemented using the mesh and couplers, using a power splitter with its coupling coefficient being controlled by a tunable value, or built into the device itself as dedicated hardware. Currently, there are no dedicated hardware switches, but they may be added in future devices.

Table 7 | List of device resources and their description.

4.11 Responsibilities and duties

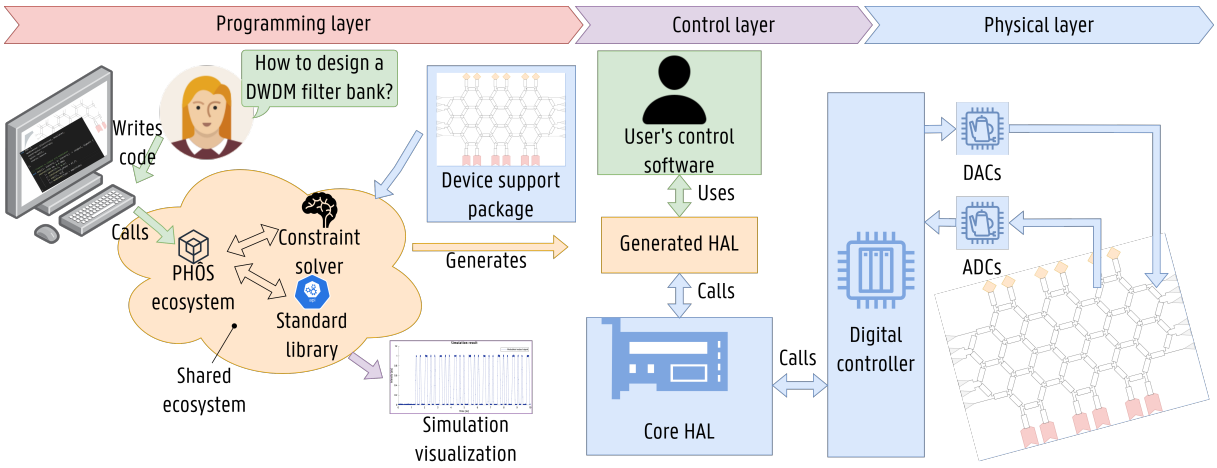


Figure 7 Responsibilities of each actor in the ecosystem, elements in orange are the responsibility of the ecosystem developer, it includes the compiler, constraint solver and standard library, it also contains parts of the HAL generator. Elements in blue are the responsibility of the chip designer, it includes the device itself, the core HAL, and the device support package. In green are the responsibility of the user, this includes the user's design and the user's control software. It also shows the different components of the ecosystem that have been discussed so far and their overall interaction with one another.

As with most ecosystems, the responsibilities for the development of different parts and the duties of maintaining these parts are split between different actors. In this case, one can see the ecosystem being designed in this thesis has having four actors: the user who is responsible for the design of their circuit and their own control software and they are also responsible for the maintenance of their own code and the compatibility of this code with the ecosystem. The second actor is the developer of the ecosystem itself, their responsibility is spread among several tasks, from the programming ecosystem components discussed in Section 3, the standard library, and the constraint solver. Due to the critical importance of these tools, the duties of maintaining some degree of backward and forward compatibility along with making sure that the tools are as bug-free as possible falls on the ecosystem developer. The third actor is the chip provider, they design the actual physical layer: the photonic processor. Because of this, they must also produce the device support package and the core HAL. Their responsibilities are to ensure that their device is compatible with the common parts of the ecosystem, that their devices can work in expected use scenarios, and to provide the HAL generator. The fourth and final actor are all of the external tool provider, those can be libraries developers, EDA tool developers, etc. Most of the time, their projects' licenses will remove any and all responsibilities from their user. Therefore, special care must be taken when integrating external tools and libraries that they are maintained by trustworthy actors. A summary of these responsibilities and their interactions with one another can be seen in Figure 7.

5.
The PHÔS programming language

From all of the information that has been presented so far regarding translation of intent and requirements (Section 4), programming paradigms (Section 3.6), and with the inadequacies of existing languages (Section 3.11), it is now apparent that it may be interesting to create a new language which would benefit from dedicated semantics, syntax, and integrates elements from fitting programming paradigms. This language should be designed in such a way that it is able to easily and clearly express the intent of the circuit designer, while also being able to translate this code into a programmable format for the hardware. Additionally, this language should be similar enough to languages that are common within the scientific community such that it is easy to learn for engineers. Finally, this language should be created in such a way that it provides both the level of control needed for circuit design, and the level of abstraction needed to clearly express complex ideas. Indeed, the language that is presented in this thesis, PHÔS, is designed to fulfill these lofty goals.

In the following sections, the initial specification, the syntax, constraint system, and other various elements of the language will be discussed. Then, in Section 6, examples will be shown how the language can be used to express various circuits. However, before discussing the language in itself, it is important to discuss the design of the languages, the existing languages it draws inspiration from, and the lessons it incorporates from them.

5.1 Design

The name of the language, PHÔS, is a reference to the ancient Greek word for light or daylight, φῶς (phôs).

5.2 PHÔS: an initial specification

5.3 Syntax

5.3.a Constraints

5.4 Standard library

5.5 Compiler architecture

5.5.a Lexing

5.5.b Parsing

5.5.c The abstract syntax tree

5.5.d Desugaring

5.5.e AST to high-level intermediary representation

5.5.f HIR to medium-level intermediary representation

5.5.g MIR to bytecode

5.6 Virtual machine

5.7 Execution artefacts

5.8 Marshalling library

5.8.a Moving data around

5.8.b Modularity

5.9 Place-and-route

5.10 Hardware abstraction library

5.11 Adopting PHÔS

5.12 State of the project

Due to the complexity of implementing a software ecosystem, PHÔS is still in its infancy. While some components were created and tested, such as the *parser*, the *abstract syntax tree*, and a *syntax highlighter*, the language is not currently usable. Therefore, the language is a work in progress and the syntax is subject to changes. Additionally, examples serve as a way to illustrate the language and are not necessarily valid.

5.13 Putting it all together

6.

Examples of photonic circuit programming

6.1 Using traditional programming languages

7.
Extending PHÔS

8.
Simulation in PHÔS

9.
Future work

9.1.a Implementation

9.1.b Dependent types & refinement types

9.1.c Advanced constraint solving

9.1.d Improve simulation using an ECS

9.1.e Co-simulation with digital electronic

9.1.f Towards co-simulation with analog electronic

9.1.g Place-and-route

9.1.h Programming of generic photonic circuits

10.
Conclusion

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