Amber Open Source Project

Amber 2 Core Specification

April 2013

Table of Contents

1 Introduction

The Amber processor core is an ARM-compatible 32-bit RISC processor. The Amber core is fully compatible with the ARM® v2a instruction set architecture (ISA) and is therefore supported by the GNU toolset. This older version of the ARM instruction set is supported because it is not covered by patents so can be implemented without a license from ARM. The Amber project provides a complete embedded system incorporating the Amber core and a number of peripherals, including UARTs, timers and an Ethernet MAC.

There are two versions of the core provided in the Amber project. The Amber 23 has a 3-stage pipeline, a unified instruction & data cache, a Wishbone interface, and is capable of 0.8 DMIPS per MHz. The Amber 25 has a 5-stage pipeline, seperate data and instruction caches, a Wishbone interface, and is capable of 1.0 DMIPS per Mhz. Both cores implement exactly the same ISA and are 100% software compatible.

The Amber 23 core is a very small 32-bit core that provides good performance. Register based instructions execute in a single cycle, except for instructions involving multiplication. Load and store instructions require three cycles. The core's pipeline is stalled either when a cache miss occurs, or when the core performs a wishbone access.

The Amber 25 core is a little larger and provides 15% to 20% better performance that the 23 core. Register based instructions execute in a single cycle, except for instructions involving multiplication. Load and store instructions also execute in a single cycle unless there is a register conflict with a following instruction. The core's pipeline is stalled when a cache miss occurs in either cache, when an instruction conflict is detected, or when the core performs a wishbone access.

Both cores has been verified by booting a 2.4 Linux kernel. Versions of the Linux kernel from the 2.4 branch and earlier contain configurations for the supported ISA. The 2.6 version of Linux does not explicitly support the ARM v2a ISA so requires more modifications to run. Also note that the cores do not contain a memory management unit (MMU) so they can only run the non-virtual memory variant of Linux.

The cores were developed in Verilog 2001, and are optimized for FPGA synthesis. For example there is no reset logic, all registers are reset as part of FPGA initialization. The complete system has been tested extensively on the Xilinx SP605 Spartan-6 FPGA board. The full Amber system with the A23 core uses 32% of the Spartan-6 XC6SLX45T-3 FPGA Look Up Tables (LUTs), with the core itself occupying less than 20% of the device using the default configuration, and running at 40MHz. It has also been synthesized to a Virtex-6 device at 80MHz, but not yet tested on a real Virtex-6 device. The maximum frequency is limited by the execution stage of the pipline which includes a 32-bit barrel shifter, 32-bit ALU and address incrementing logic.

For a description of the ISA, see "Archimedes Operating System - A Dabhand Guide, Copyright Dabs Press 1991", or "Acorn RISC Machine Family Data Manual, VLSI

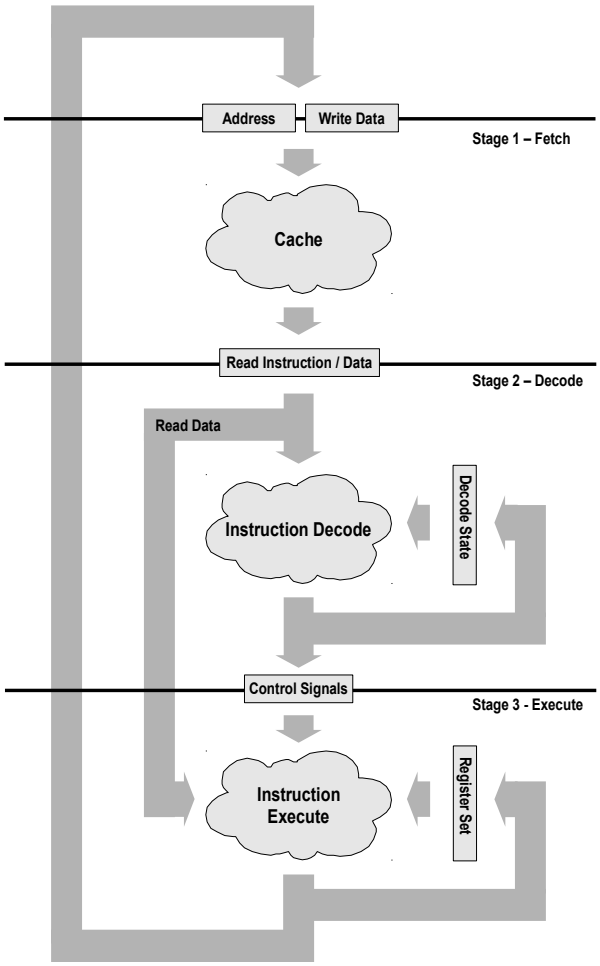
Technology Inc., 1990".

1.1 Amber 23 Features

- 3-stage pipeline.
- 32-bit Wishbone system bus.
- Unified instruction and data cache, with write through and a read-miss replacement policy. The cache can have 2, 3, 4 or 8 ways and each way is 4kB.
- Multiply and multiply-accumulate operations with 32-bit inputs and 32-bit output in 34 clock cycles using the Booth algorithm. This is a small and slow multiplier implementation.
- Little endian only, i.e. Byte 0 is stored in bits 7:0 and byte 3 in bits 31:24.

The following diagram shows the data flow through the 3-stage core.

Figure 1 - *Amber 23 Core pipeline stages*



1.2 Amber 25 Features

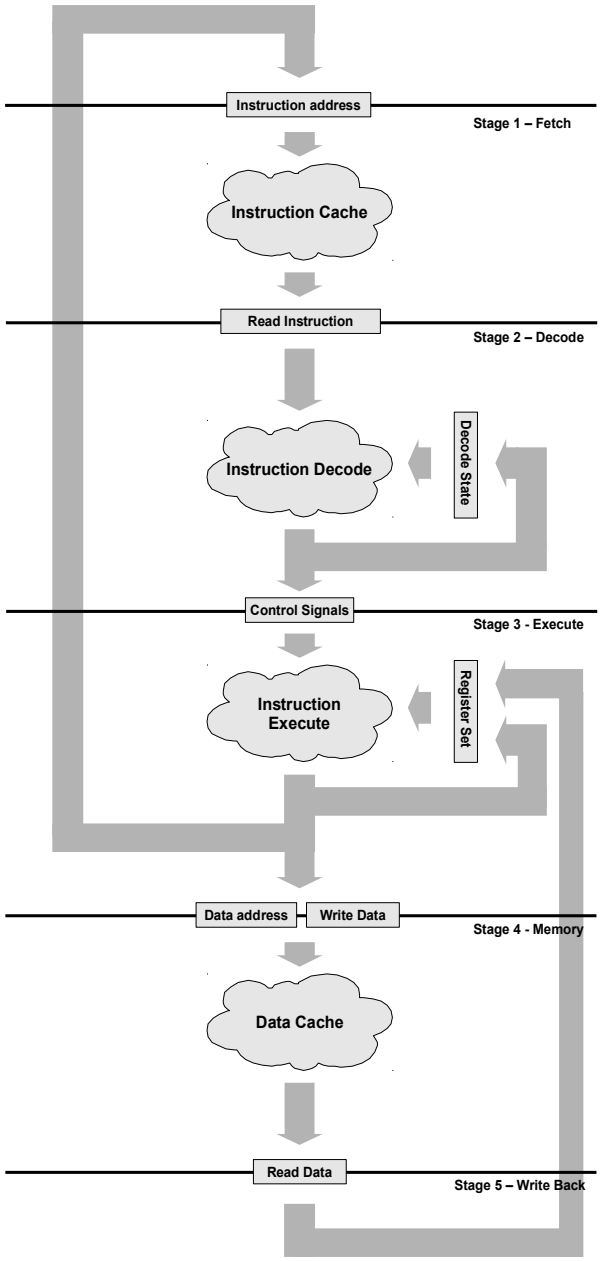
- 5-stage pipeline.
- 32-bit Wishbone system bus.
- Seperate instruction and data caches. Each cache can be either 2,3,4 or 8 ways and each way is 4kB. Both caches use a read replacement policy and the data

cache operates as write through. The instruction cache is read only.

- Multiply and multiply-accumulate operations with 32-bit inputs and 32-bit output in 34 clock cycles using the Booth algorithm. This is a small and slow multiplier implementation.
- Little endian only, i.e. Byte 0 is stored in bits 7:0 and byte 3 in bits 31:24.

The following diagram shows the data flow through the 5-stage core.

Figure 2 - *Amber 25 Core pipeline stages*



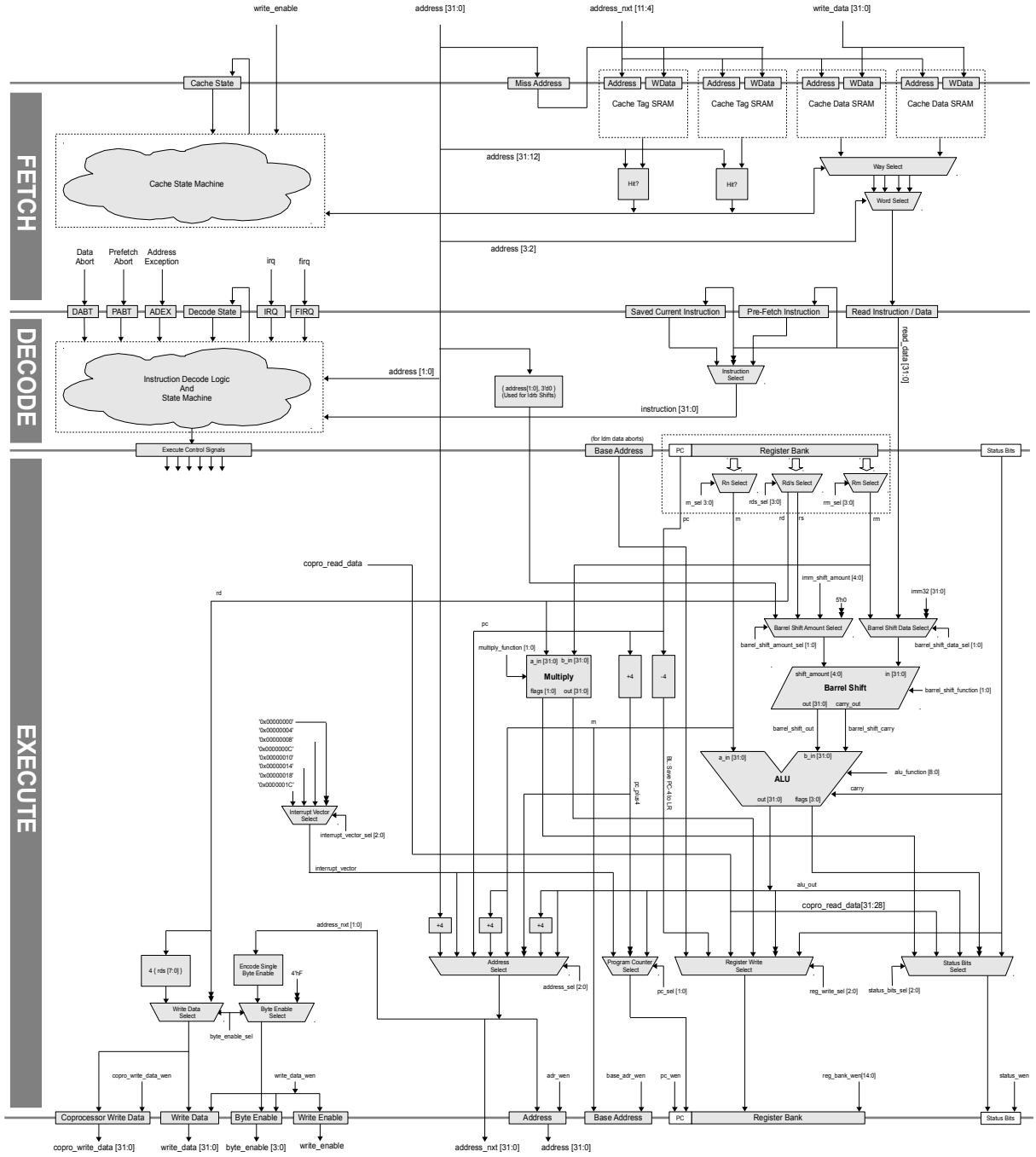
2 Amber 23 Pipeline Architecture

The Amber 2 core has a 3-stage pipeline architecture. The best way to think of the pipeline structure is of a circle. There is no start or end point. The output from each stage is registered and fed into the next stage. The three stages are;

- **Fetch** – The cache tag and data RAMs receive an unregistered version of the address output by the execution stage. The registered version of the address is compared to the tag RAM outputs one cycle later to decide if the cache hits or misses. If the cache misses, then the pipeline is stalled while the instruction is fetched from either boot memory or main memory via the Wishbone bus. The cache always does 4-word reads so a complete cache line gets filled. In the case of a cache hit, the output from the cache data RAM goes to the decode stage. This can either be an instruction or data word.
- **Decode** - The instruction is received from the fetch stage and registered. One cycle later it is decoded and the datapath control signals prepared for the next cycle. This stage contains a state machine that handles multi-cycle instructions and interrupts.
- **Execute –** The control signals from the decode stage are registered and passed into the execute stage, along with any read data from the fetch stage. The operands are read from the register bank, shifted, combined in the ALU and the result written back. The next address for the fetch stage is generated.

The following diagram shows the datapath through the three stages in detail. This diagram closely corresponds to the Verilog implementation. Some details, like the wishbone interface and coprocessor #15 have been left out so as not to overload the diagram completely.

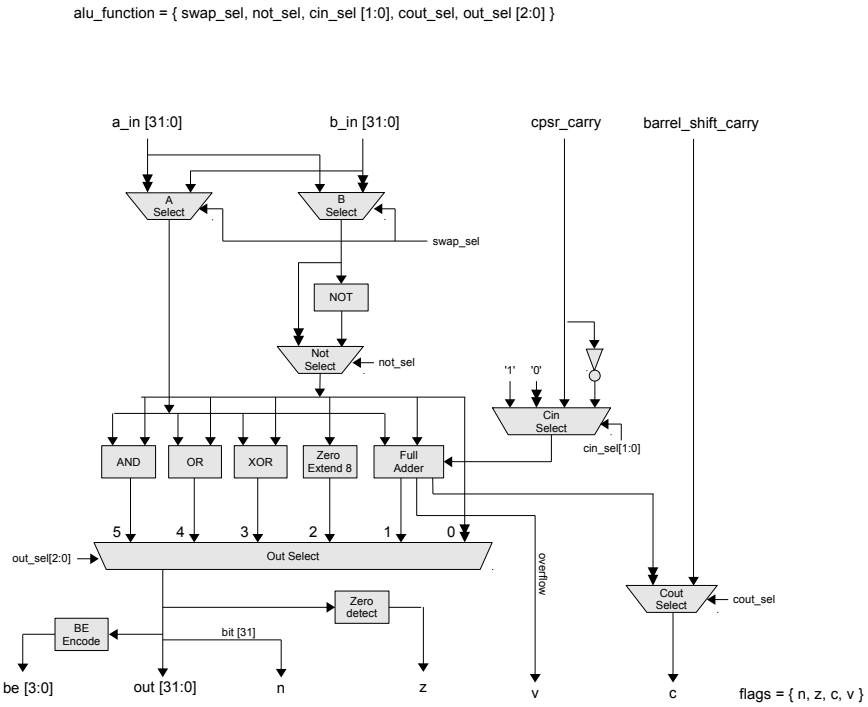
Figure 3 - *Detailed 3-Stage Pipeline Structure*



2.1 ALU

The diagram below shows the structure of the Arithmetic Logic Unit (ALU). It consists of a set of different logical functions, a 32-bit adder and a mux to select the function.

Figure 4 - *ALU Structure*



The alu_function[6:0] bus in the core is a concatenation of the individual control signals in the ALU. The following table describes these control signals.

Table 1 ALU Function Encoding

Field	Function
swap_sel	Swaps the a and b inputs
not_sel	Selects the NOT version of b
cin_sel[1:0]	Selects the carry in to the full added from { c_in, !c_in, 1, 0 }. Note that bs_c_in is the carry_in from the barrel shifter.
cout_sel	Selects the carry out from { full_adder_cout, barrel_shifter_cout }
out_sel[2:0]	Selects the ALU output from { 0, b_zero_extend_8, b, and_out, or_out, xor_out, full_adder_out }

2.2 Pipeline Operation

2.2.1 Load Example

The load instruction causes the pipeline to stall for two cycles. This section explains why this is necessary. The following is a simple fragment of assembly code with a single load instructon with register instructions before and after it.

```
0  mov r0, #0x100
4  add r1, r0, #8
8  ldr r4, [r1]
c  add r4, r4, r0
```

The table below shows which instruction is active in each stage of the processor core for each clock tick. When the core comes out of reset the execute stage starts generating fetch addresses. It starts at 0 and increments by 4 each tick. In tick 1 the first instruction, at address 0, is fetched, This simple example assumes that all accesses are already present in the cache so fetches only take 1 cycle. Otherwise read accesses on the wishbone bus would add additional stalls and complicate this example.

At tick 2 the first instruction, 0, is decoded and at tick 3 it is executed. This means that the r0 register, which is the destination for instruction 0, does not output the new value until tick 4, where it is used as an input to the second instruction.

At tick 5 the load instruction, instruction 8, stalls the decode stage. In the execute stage it calculates the load address and this is used by the fetch stage in tick 6. Also in tick 5 the instruction c is saved to the pre_fetch_instruction register. This is used once the load instruction has finished and its use saves needing an additional stall cycle to reread instruction c.

At tick 6 the value at address 0x108 is fetched and at tick 7 it is written into r4. The new value of r4 is then available for instruction c in tick 8.

Table 2 Pipeline load example

Stage	Tick 0	Tick 1	Tick 2	Tick 3	Tick 4	Tick 5	Tick 6	Tick 7	Tick 8
Fetch									
address	-	0	4	8	c	10	108	10	14
access type		read	read	read	read	read, ignored	read	read	read
Decode									
instruction	-	-	0	4	8	8	8	c	10
pre_fetch_instruction	-	-	-	-	-	[c]	[c]		
Execute									
instruction	-	-	-	0	4	8	8	8	c
address_nxt	0	4	8	c	10	108	10	14	18

2.2.2 Store Example

The store instruction also causes the pipeline to stall for two cycles. This section explains why this is necessary. The following is a simple fragment of assembly code with a single store instructon with register instructions before and after it.

```
0  mov r0, #0x100
4  mov r1, #17
8  str r1, [r0]
c  add r1, r0, #20
```

The table below shows which instruction is active in each stage of the processor core for each clock tick. At tick 5 the store instruction, instruction 8, stalls the decode stage. In the execute stage it calculates the store address and this is used by the fetch stage in tick 6. Also in tick 5 the instruction c is saved to the pre_fetch_instruction register. This is used once the store instruction has finished and its use saves needing an additional stall cycle to reread instruction c. In tick 7 the instruction after the store instruction is decoded and in tick 8 it is executed.

Table 3 Pipeline store example

Stage	Tick 0	Tick 1	Tick 2	Tick 3	Tick 4	Tick 5	Tick 6	Tick 7	Tick 8
Fetch									
address	-	0	4	8	c	10	100	10	14
access type		read	read	read	read	read, ignored	write	read	read
Decode									
instruction	-	-	0	4	8	8	8	c	10
pre_fetch_instruction	-	-	-	-	-	[c]	[c]		
Execute									
instruction	-	-	-	0	4	8	8	8	c
address_nxt	0	4	8	c	10	100	10	14	18

3 Instruction Set

The following table describes the instructions supported by the Amber 2x core.

Table 4 Amber 2 core Instruction Set

Name	Type	Syntax	Description
adc	REGOP	`adc{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Add with carry** adds two values and the Carry flag.
add	REGOP	`add{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Add** adds two values.
and	REGOP	`and{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**And** performs a bitwise AND of two values.
b	BRANCH	`b{<cond>} <target_address>`	**Branch** causes a branch to a target address.
bic	REGOP	`bic{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Bit** *clear* performs a bitwise AND of one value with the complement of a second value.
bl	BRANCH	`bl{<cond>} <target_address>`	**Branch and link** cause a branch to a target address. The resulting instruction stores a return address in the link register (r14).
cdp	COREGOP	`cdp{<cond>} <coproc>, <opcode_1>, <CRd>, <CRn>, <CRm>, <opcode_2>`	**Coprocessor data processing** tells a coprocessor to perform an operation that is independent of Amber registers and memory. This instruction is not currently implemented by the Amber core because there is no coprocessor in the system that requires it.
cmn	REGOP	`cmn{<cond>}{p} <Rn>, <shifter_operand>`	**Compare negative** compares one value with the twos complement of a second value, simply by adding the two values together, and sets the status flags. If the p flag is set, the pc and status bits are updated directly by the ALU output.
cmp	REGOP	`cmp{<cond>}{p} <Rn>, <shifter_operand>`	**Compare** compares two values by subtracting <shifter operand> from <Rn>, setting the status flags. If the p flag is set, the pc and status bits are updated directly by the ALU output.
eor	REGOP	`eor{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Exclusive OR** performs a bitwise XOR of two values.
ldc	CODTRANS	`lcd{<cond>} <coproc>, <CRd>, <addressing_mode>`	**Load coprocessor** loads memory data from a sequence of consecutive memory addresses to a coprocessor. This instruction is not currently implemented by the Amber core because there is no coprocessor in the system that requires it.
ldm	MTRANS	`ldm{<cond>}<addressing_mode> <Rn>{!}, <registers>`	**Load multiple** loads a non-empty subset, or possibly all, of the general-purpose registers from sequential memory locations. It is useful for block loads, stack operations and procedure exit sequences.
		`ldm{<cond>}<addressing_mode> <Rn>, <registers_without_pc>^`	This version loads User mode registers when the processor is in a privileged mode. This is useful when performing process swaps.
		`ldm{<cond>}<addressing_mode> <Rn>{!}, <registers_and_pc>^`	This version loads a subset, or possibly all, of the general-purpose registers and the PC from sequential memory locations. The status bits are also loaded. This is useful for returning from an exception.
ldr	TRANS	`ldr{<cond>} <Rd>, <addressing_mode>`	**Load register** loads a word from a memory address. If the address is not word-aligned, then the word is rotated left so that the byte addresses appears in bits [7:0] of Rd.
ldrb	TRANS	`ldr{<cond>}b <Rd>, <addressing_mode>`	**Load register byte** loads a byte from memory and zero-extends the byte to a 32-bit word.
mcr	CORTRANS	`mcr{<cond>} <coproc>, <opcode_1>, <Rd>, <CRn>, <CRm>{, <opcode_2>}`	**Move to coprocessor from register** passes the value of register <Rd> to a coprocessor.
mla	MULT	`mla{<cond>}{s} <Rd>, <Rm>, <Rs>, <Rn>`	**Multiply accumulate** multiplies two signed or unsigned 32-bit values, and adds a third 32-bit value. The least significant 32 bits of the result are written to the destination register.
mov	REGOP	`mov{<cond>}{s} <Rd>, <shifter_operand>`	**Move** writes a value to the destination register. The value can be either an immediate value or a value from a register,

Name	Type	Syntax	Description
			and can be shifted before the write.
mrc	CORTRANS	`mrc{<cond>} <coproc>, <opcode_1>, <Rd>, <CRn>, <CRm>{, <opcode_2>}`	**Move to register from coprocessor** causes a coprocessor to transfer a value to an Amber register or to the condition flags.
mul	MULT	`mul{<cond>}{s} <Rd>, <Rm>, <Rs>`	**Multiply** multiplies two signed or unsigned 32-bit values. The least significant 32 bits of the result are written to the destination register.
mvn	REGOP	`mvn{<cond>}{s} <Rd>, <shifter_operand>`	**Move not** generates the logical ones complement of a value. The value can be either an immediate value or a value from a register, and can be shifted before the MVN operation.
orr	REGOP	`orr{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Logical OR** performs a bitwise OR of two values. The first value comes from a register. The second value can be either an immediate value or a value from a register, and can be shifted before the OR operation.
rsb	REGOP	`rsb{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Reverse subtract** subtracts a value from a second value.
rsc	REGOP	`rsc{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Reverse subtract with carry** subtracts one value from another, taking account of any borrow from a preceding less significant subtraction. The normal order of the operands is reversed, to allow subtraction from a shifted register value, or from an immediate value.
sbc	REGOP	`sbc{<cond>}{s} <Rd>, <Rn>, <shifter_operand>`	**Subtract with carry** subtracts the value of its second operand and the value of NOT(Carry flag) from the value of its first operand. The first operand comes from a register. The second operand can be either an immediate value or a value from a register, and can be shifted before the subtraction.
stc	CODTRANS	`stc{<cond>} <coproc>, <CRd>, <addressing_mode>`	**Store coprocessor** stores data from a coprocessor to a sequence of consecutive memory addresses. This instruction is not currently implemented by the Amber core because there is no coprocessor in the system that requires it.
stm	MTRANS	`stm{<cond>}<addressing_mode> <Rn>{!}, <registers>`	**Store multiple** stores a non-empty subset (or possibly all) of the general-purpose registers to sequential memory locations. The '!' causes Rn to be updated. The registers are stored in sequence, the lowest-numbered register to the lowest memory address (start_address), through to the highest-numbered register to the highest memory address (end_address).
		`STM{<cond>}<addressing_mode> <Rn>, <registers>^`	This version stores a subset (or possibly all) of the User mode general-purpose registers to sequential memory locations. The registers are stored in sequence, the lowest-numbered register to the lowest memory address (start_address), through to the highest-numbered register to the highest memory address (end_address).
str	TRANS	`str{<cond>} <Rd>, <addressing_mode>`	**Store register** stores a word from a register to memory.
strb	TRANS	`str{<cond>}b <Rd>, <addressing_mode>`	**Store register byte** stores a byte from the least significant byte of a register to memory.
sub	REGOP	`sub{<cond>}{s} <Rd>, <Rn>, <shifter_operand>` `i.e. Rd = Rn - shifter_operand`	**Subtract** subtracts one value from a second value.
swi	SWI	`swi{<cond>} <immed_24>`	**Software interrupt** causes a SWI exception. <immed_24> Is a 24-bit immediate value that is put into bits[23:0] of the instruction. This value is ignored by the Amber core, but can be used by an operating system SWI exception handler to determine what operating system service is being requested.
swp	SWAP	`swp{<cond>} <Rd>, <Rm>, [<Rn>]`	**Swap** loads a word from the memory address given by the value of register <Rn>. The value of register <Rm> is then stored to the memory address given by the value of <Rn>, and the original loaded value is written to register <Rd>. If the same register is specified for <Rd> and <Rm>, this instruction swaps the value of the register and the value at the memory address.
swpb	SWAP	`swp{<cond>}b <Rd>, <Rm>, [<Rn>]`	**Swap Byte** swaps a byte between registers and memory. It loads a byte from the memory address given by the value of register <Rn>. The value of the least significant byte of register <Rm> is stored to the memory address given by

Name	Type	Syntax	Description
			<Rn>, the original loaded value is zero-extended to a 32-bit word, and the word is written to register <Rd>. Can be used to implement semaphores.
teq	REGOP	`teq{<cond>}{p} <Rn>, <shifter_operand>`	**Test equivalence** compares a register value with another arithmetic value. The condition flags are updated, based on the result of logically XORing the two values, so that subsequent instructions can be conditionally executed. If the p flag is set, the pc and status bits are updated directly by the ALU output.
tst	REGOP	`tst{<cond>}{p} <Rn>, <shifter_operand>`	**Test** compares a register value with another arithmetic value. The condition flags are updated, based on the result of logically ANDing the two values, so that subsequent instructions can be conditionally executed. If the p flag is set, the pc and status bits are updated directly by the ALU output.

4 Instruction Set Encoding

Table 5 Overall instruction set encoding table.

	Type	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Processing	REGOP	Cond				0	0	**I**	Opcode				**S**	Rn				Rd				shifter_operand											
Multiply	MULT	Cond				0	0	0	0	0	0	**A**	**S**	Rd				Rn				Rs				1	0	0	1	Rm			
Single Data Swap	SWAP	Cond				0	0	0	1	0	**B**	0	0	Rn				Rd				0	0	0	0	1	0	0	1	Rm			
Single Data Transfer	TRANS	Cond				0	1	**I**	**P**	**U**	**B**	**W**	**L**	Rn				Rd				Offset											
Block Data Transfer	MTRANS	Cond				1	0	0	**P**	**U**	**S**	**W**	**L**	Rn				Register List															
Branch	BRANCH	Cond				1	0	1	**L**	Offset																							
Coprocessor Data Transfer	CODTRANS	Cond				1	1	0	**P**	**U**	**N**	**W**	**L**	Rn				CRd				CP#				Offset							
Coprocessor Data Operation	COREGOP	Cond				1	1	1	0	CP Opcode				CRn				CRd				CP#				CP			0	CRm			
Coprocessor Register Transfer	CORTRANS	Cond				1	1	1	0	CP Opcode			**L**	CRn				Rd				CP#				CP			1	CRm			
Software Interrupt	SWI	Cond				1	1	1	1	Ignored by processor																							
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Where

I_{25} = Immediate form of shifter_operand

L_{24} = Link; Save PC to LR

U_{23} = 1; address = Rn + offset_12

= 0; address = Rn - offset_12

B_{22} = Byte (0 = word)

A_{21} = Accumulate

L_{20} = Load (0 = store)

S_{20} = Update Condition flags

P_{24}, W_{21} : Select different modes of operation

4.1 Condition Encoding

All instructions include a 4-bit condition execution code. The instruction is only executed if the condition specified in the instruction agrees with the current value of the status flags.

Table 6 Cond: Condition Encoding

Condition	Mnemonic extension	Meaning	Condition flag state
4'h0	eq	Equal	Z set
4'h1	ne	Not equal	Z clear
4'h2	cs / hs	Carry set / unsigned higher or same	C set
4'h3	cc / lo	Carry clear / unsigned lower	C clear

Condition	Mnemonic extension	Meaning	Condition flag state
4'h4	mi	Minus / negative	N set
4'h5	pl	Plus / positive or zero	N clear
4'h6	vs	Overflow	V set
4'h7	vc	No overflow	V clear
4'h8	hi	Unsigned higher	C set and Z clear
4'h9	ls	Unsigned lower or same	C clear or Z set
4'h10	ge	Signed greater than or equal	N == V
4'h11	lt	Signed less than	N != V
4'h12	gt	Signed greater than	Z == 0,N == V
4'h13	le	Signed less than or equal	Z == 1 or N != V
4'h14	al	Always (unconditional)	-
4'h15	-	Invalid condition	-

4.2 Opcode Encoding

Table 7 REGOP: Opcode Encoding

Opcode	Mnemonic extension	Operation	Action
4'h0	**and**	Logical AND	Rd := Rn AND shifter_operand
4'h1	**eor**	Logical XOR	Rd := Rn XOR shifter_operand
4'h2	**sub**	Subtract	Rd := Rn - shifter_operand
4'h3	**rsb**	Reverse subtract	Rd := shifter_operand - Rn
4'h4	**add**	Add	Rd := Rn + shifter_operand
4'h5	**adc**	Add with carry	Rd := Rn + shifter_operand + Carry Flag
4'h6	**sbc**	Subtract with carry	Rd := Rn - shifter_operand - NOT(Carry Flag)
4'h7	**rsc**	Reverse subtract with carry	Rd := shifter_operand - Rn - NOT(Carry Flag)
4'h8	**tst**	Test	Update flags after Rn AND shifter_operand S bit always set
4'h9	**teq**	Test equivalence	Update flags after Rn EOR shifter_operand S bit always set
4'ha	**cmp**	Compare	Update flags after Rn – shifter_operand S bit always set
4'hb	**cmn**	Compare negated	Update flags after Rn + shifter_operand S bit always set
4'hc	**orr**	Logical (inclusive) OR	Rd := Rn OR shifter_operand
4'hd	**mov**	Move	Rd := shifter_operand (no first operand)
4'he	**bic**	Bit clear	Rd := Rn AND NOT(shifter_operand)
4'hf	**mvn**	Move NOT	Rd := NOT shifter_operand (no first operand)

4.3 Shifter Operand Encoding

This section describes the encoding of the shifter operand for register instructions.

Table 8 REGOP: Shifter Operand Encoding

Format	Syntax	25 'I'	11	10	9	8	7	6	5	4	3	2	1	0
32-bit immediate	#<immediate>	1	encode_imm				imm_8							
Immediate shifts	<Rm>	0	5'h0					2'h0		0	Rm			
	<Rm>, lsl #<shift_imm>	0	shift_imm					Shift		0	Rm			
	<Rm>, lsr #<shift_imm>													
	<Rm>, asr #<shift_imm>													
	<Rm>, ror #<shift_imm>													
	<Rm>, rrx	0	5'h0					2'b11		0	Rm			
Register Shifts	<Rm>, lsl <Rs>	0	Rs				0	Shift		1	Rm			
	<Rm>, lsr <Rs>													
	<Rm>, asr <Rs>													
	<Rm>, ror <Rs>													

4.3.1 Encode immediate value

Table 9 REGOP: Encode Immediate Value Encoding

Value	32-bit immediate value
4'h0	{ 24'h0, imm_8[7:0] }
4'h1	{ imm_8[1:0], 24'h0, imm_8[7:2] }
4'h2	{ imm_8[3:0], 24'h0, imm_8[7:4] }
4'h3	{ imm_8[5:0], 24'h0, imm_8[7:6] }
4'h4	{ imm_8[7:0], 24'h0 }
4'h5	{ 2'h0, imm_8[7:0], 22'h0 }
4'h6	{ 4'h0, imm_8[7:0], 20'h0 }
4'h7	{ 6'h0, imm_8[7:0], 18'h0 }
4'h8	{ 8'h0, imm_8[7:0], 16'h0 }
4'h9	{ 10'h0, imm_8[7:0], 14'h0 }
4'h10	{ 12'h0, imm_8[7:0], 12'h0 }
4'h11	{ 14'h0, imm_8[7:0], 10'h0 }
4'h12	{ 16'h0, imm_8[7:0], 8'h0 }
4'h13	{ 18'h0, imm_8[7:0], 6'h0 }
4'h14	{ 20'h0, imm_8[7:0], 4'h0 }
4'h15	{ 22'h0, imm_8[7:0], 2'h0 }

4.4 Register transfer offset encoding

Table 10 TRANS: Offset Encoding

Category	Type	Syntax	25 'I'	24 'P'	23 'U'	22 'B'	21 'W'	20 'L'	11	10	9	8	7	6	5	4	3	2	1	0
Immediate offset / index	Immediate offset	[<Rn>, #+/-<offset_12>]	0	1	-	-	0	-	offset_12											
	Immediate pre-indexed	[<Rn>, #+/-<offset_12>]!	0	1	-	-	1	-	offset_12											
	Immediate post-indexed	[<Rn>], #+/-<offset_12>	0	0	-	-	0	-	offset_12											
	Immediate post-indexed, unprivilaged memory access	[<Rn>], #+/-<offset_12>	0	0	-	-	1	-	offset_12											
Register offset /	Register offset	[<Rn>, +/-<Rm>]	1	1	-	-	0	-	8'h0								Rm			

Category	Type	Syntax	25 'I'	24 'P'	23 'U'	22 'B'	21 'W'	20 'L'	11	10	9	8	7	6	5	4	3	2	1	0
index	Register pre-indexed	[<Rn>, +/-<Rm>]!	1	1	-	-	1	-	8'h0								Rm			
	Register post-indexed	[<Rn>], +/-<Rm>	1	0	-	-	0	-	8'h0								Rm			
	Register post-indexed, unprivilaged memory access	[<Rn>], +/-<Rm>	1	0	-	-	1	-	8'h0								Rm			
Scaled register offset / index	Scaled register offset	[<Rn>, +/-<Rm>, <shift> #<shift_imm>]	1	1	-	-	0	-	shift_imm					Shift		0	Rm			
	Scaled register pre-indexed	[<Rn>, +/-<Rm>, <shift> #<shift_imm>]!	1	1	-	-	1	-	shift_imm					Shift		0	Rm			
	Scaled register post-indexed	[<Rn>], +/-<Rm>, <shift> #<shift_imm>	1	0	-	-	0	-	shift_imm					Shift		0	Rm			
	Scaled register post-indexed, unprivilaged memory access	[<Rn>], +/-<Rm>, <shift> #<shift_imm>	1	0	-	-	1	-	shift_imm					Shift		0	Rm			

Where;

Pre-indexed: Address adjusted before access

Post-indexed: Address adjusted after access

I_{25}, P_{24} and W_{21} encode the instruction as shown in the table above.

U_{23} = 1; address = Rn + offset_12

= 0; address = Rn – offset_12

B_{22} = 0; data type is 32-bit word

= 1; data type is byte

L_{20} = 1; load

= 0; store

4.5 Shift Encoding

This encoding is used in both register and single data transfer instructions.

Table 11 REGOP, TRANS: Shift Encoding

Condition	Type	Syntax
2'h0	Logical Shift Left	lsl
2'h1	Logical Shift Right	lsr
2'h2	Arithmetic Shift Right (sign extend)	asr
2'h3	Rotate Right with Extent (CO -> bit 31, bit 0 -> CO), if shift amount = 0, else Rotate Right	ror, rrx

4.6 Load & Store Multiple

Table 12 MTRANS: Index options with ldm and stm

Mode	Stack Load Equivalent	Stack Store Equivalent	Instructions	24 'P'	23 'U'	22 'S'	21 'W'	20 'L'
Increment After (ia)	Full Descending (fd)	Empty Ascending (ea)	ldmia, stmia, ldmfd, stmea	0	1	-	-	-
Increment Before (ib)	Empty Descending (ed)	Full Ascending (fa)	lmdib, stmib, ldmed, stmfa	1	1	-	-	-
Decrement After (da)	Full Ascending (fa)	Empty Descending (ed)	ldmda, stmda, ldmfa, stmed	0	0	-	-	-

Mode	Stack Load Equivalent	Stack Store Equivalent	Instructions	24 'P'	23 'U'	22 'S'	21 'W'	20 'L'
Decrement Before (db)	Empty Ascending (ea)	Full Descending (fd)	lmddb, stmdb, ldmea, stmfd	1	0	-	-	-

S_{22}

The S bit for ldm that loads the PC, the S bit indicates that the status bits loaded. For ldm instructions that do not load the PC and all stm instructions, the S bit indicates that when the processor is in a privileged mode, the User mode banked registers are transferred instead of the registers of the current mode. Ldm with the S bit set is unpredictable in User mode.

W_{21}

Indicates that the base register is updated after the transfer.

L_{20}

Distinguishes between Load (L==1) and Store (L==0) instructions.

4.7 Branch offset

Branch instructions contain an offset in the lower 24 bits of the instruction. This offset is combined with the current pc value to calculate the branch target, as follows:

1. Shift the 24-bit signed immediate value left two bits to form a 26-bit value.
2. Add this to the pc.

4.8 Booth's Multiplication Algorithm

Booth's algorithm involves repeatedly adding one of two predetermined values A and S to a product P, then performing a rightward arithmetic shift on P. Let m and r be the multiplicand and multiplier, respectively; and let x and y represent the number of bits in m and r.

1. Determine the values of A and S, and the initial value of P. All of these numbers should have a length equal to (x + y + 1).
    1. A: Fill the most significant (leftmost) bits with the value of m. Fill the remaining (y + 1) bits with zeros.
    2. S: Fill the most significant bits with the value of (−m) in two's complement notation. Fill the remaining (y + 1) bits with zeros.
    3. P: Fill the most significant x bits with zeros. To the right of this, append the value of r. Fill the least significant (rightmost) bit with a zero.
2. Examine the two least significant (rightmost) bits of P.
    1. If they are 01, find the value of P + A. Ignore any overflow.
    2. If they are 10, find the value of P + S. Ignore any overflow.

3. If they are 00, do nothing. Use P directly in the next step.

4. If they are 11, do nothing. Use P directly in the next step.

3. Arithmetically shift the value obtained in the 2nd step by a single place to the right. Let P now equal this new value.

4. Repeat steps 2 and 3 until they have been done y times.

5. Drop the least significant (rightmost) bit from P. This is the product of m and r.

Here is the algorithm in C-code form;

```
unsigned int mul ( unsigned int Rm, unsigned int Rs )
{
unsigned int multiply_result_hi, multiply_result_lo, n, booth_bits;

for (n=0;n<33;n++){
    if (n==0) {
        booth_bits          = ((Rs & 1)<<1);
        multiply_result_lo  = Rs;
        if      (booth_bits == 1) { multiply_result_hi = Rm;     }
        else if (booth_bits == 2) { multiply_result_hi = ~Rm + 1;}
        else                      { multiply_result_hi = 0;      }
        }
    else {
        booth_bits         =  multiply_result & 3;
        multiply_result_lo = (multiply_result_lo >>1) | (( multiply_result_hi & 1)<<31);
        multiply_result_hi = (multiply_result_hi >>1) | (multiply_result_hi & 0x80000000);
        if (booth_bits == 1) { multiply_result_hi = multiply_result_hi + Rm;        }
        if (booth_bits == 2) { multiply_result_hi = multiply_result_hi + (~Rm + 1); }
        }
    }

return multiply_result_lo;
}
```

5 Interrupts

Table 13 Interrupt Types

Interrupt Type	Processor Mode	Address
Reset	Supervisor (svc)	0x00000000
Undefined Instructions	Supervisor (svc)	0x00000004
Software Interrupt (SWI)	Supervisor (svc)	0x00000008
Prefetch Abort (instruction fetch memory abort)	Supervisor (svc)	0x0000000C
Data Abort (data access memory abort)	Supervisor (svc)	0x00000010
Address exception	Supervisor (svc)	0x00000014
IRQ (interrupt)	IRQ (irq)	0x00000018
FIRQ (fast interrupt)	FIRQ (firq)	0x0000001C
-	User (usr)	-

The modes other than User mode are known as privileged modes. They have full access to system resources and can change mode freely. When an exception occurs, the banked versions of r14, the link register, is used to save the pc value and status bits.

6 Registers

Table 14 Register Sets

User (USR)	Supervisor (SVC)	Interrupt (IRQ)	Fast Interrupt (FIRQ)
r0			
r1			
r2			
r3			
r4			
r5			
r6			
r6			
r7			
r8			r8_firq
r9			r9_firq
r10			r10_firq
r11 (fp)			r11_firq
r12 (ip)			r12_firq
r13 (sp)	r13_svc	r13_irq	r13_firq
r14 (lp)	r14_svc	r14_irq	r14_firq
r15 (pc)			

Table 15 Status Bits – Part of the PC

Field	Position	Type	Description
flags	[31:28]	User Writable	{ Negative, Zero, Carry, oVerflow }
I	27	Privileged	IRQ mask, disables IRQs when high
F	26	Privileged	FIRQ Mask, disables FIRQs when high
mode	[1:0]	Privileged	Processor mode 3 - Supervisor 2 - Interrupt 1 - Fast Interrupt 0 - User

7 Cache

The Amber cache size is optimized to use FPGA Block RAMs. Each way has 256 lines of 16 bytes. 256 lines x 16 bytes x 2 ways = 8k bytes. The address tag is 20 bits. Each cache can be configured with either 2, 3, 4 or 8 ways.

Table 16 Cache Specification

Ways	2	3	4	**8**
Lines per way	256	256	256	256
Words per line	4	4	4	4
Total words	2048	3072	4096	8192
Total bytes	8192	12288	16384	32768
FPGA 9K Block RAMs	8 + 2 = 10	12 + 3 = 15	16 + 4 = 20	32 + 8 = 40

8 Amber Project

The Amber project is a complete processor system implemented on an FPGA development board. The purpose of the project is to provide an evironment that gives an example usage of the Amber 2 core, and supports a set of tests that verify the correct functionality of the code. This is especially important if modificatiosn to the core are made.

8.1 Amber Port List

The following table gives the port list for the Amber 2x core. The Amber 23 and Amber 25 cores have identical port lists.

Table 17 Amber 2x Core Port List

Name	Width	Direction	Description
i_clk	1	in	Clock input. The core only has a single clock. The Wishbone interface also works on this clock.
i_irq	1	in	Interrupt request, active high. Causes the core to switch to IRQ mode and jump to the IRQ address vector when asserted. The switch does not occur until the end of the current instruction. For example if the core is executing a stm instruction it could take 40 or 50 cycles to complete this instruction. Once the instruction has completed the core will jump to the IRQ vector and execute the instruction at that location.
i_firq	1	in	Fast Interrupt request, active high. Causes the core to switch to FIRQ mode and jump to the FIRQ address vector when asserted. Again the core makes the switch after the current instruction has completed.
i_system_rdy	1	in	Connected to the stall signal that stalls the decode and execute stages of the core. The system uses this signal to freeze the core until the DDR3 main memory initialization has completed.
Wishbone Interface			
o_wb_adr	32	out	Byte address. Note that the core only generates 26-bit instruction addresses but can generate full 32-bit data addresses.
o_wb_sel	4	out	Byte enable for writes. Bit 0 corresponds to byte 0 which is bits [7:0] on the data buses.
o_wb_we	1	out	Write enable, active high.
i_wb_dat	32	in	Read data. Active when i_wb_ack is asserted in a read cycle.
o_wb_dat	32	out	Write data. Active when o_wb_stb is high.
o_wb_cyc	1	out	Holds bus ownership during multi-cycle accesses.
o_wb_stb	1	out	Per-cycle strobe.
i_wb_ack	1	in	Used to terminate read and write accesses.
i_wb_err	1	in	Used to indicate an error on an access. Currently not used within the Amber 2 core.

8.2 Amber 23 Verilog Files

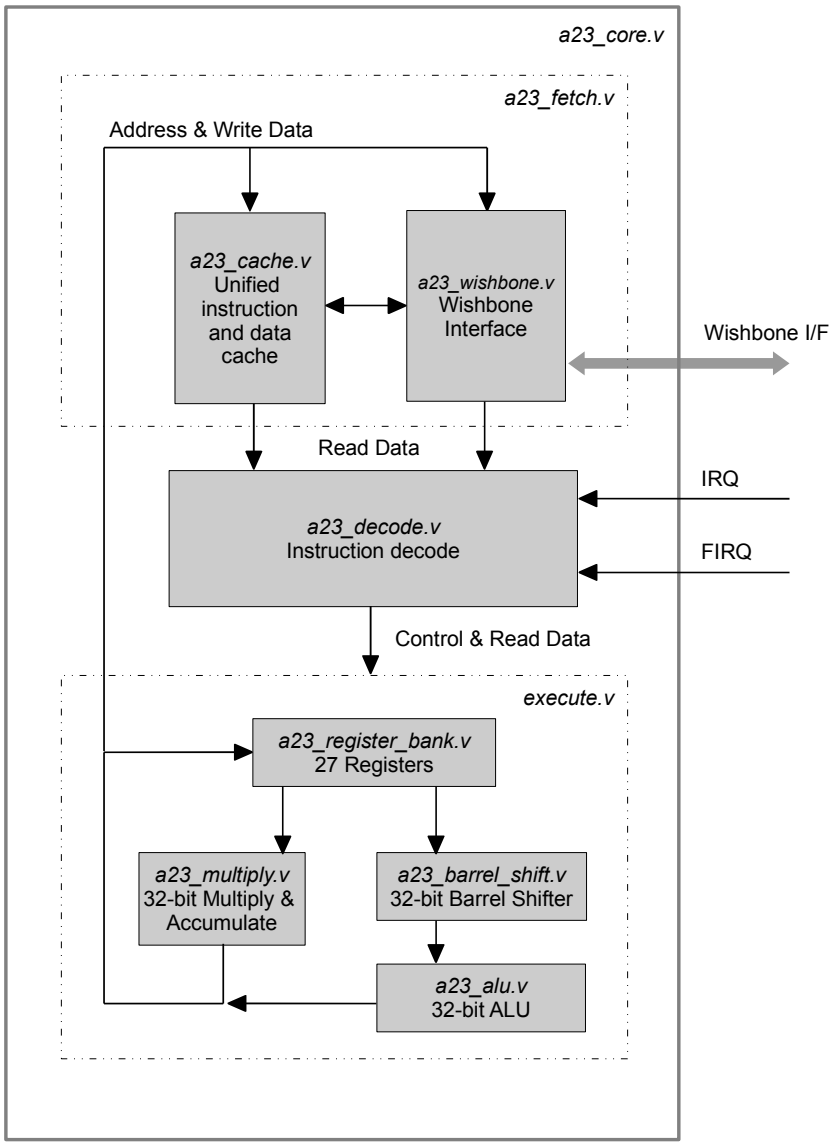
The following table describes each Verilog source file in the Amber 2 core. These files are located in $AMBER_BASE/hw/vlog/amber.

Table 18 Amber 23 Core Source Files

Name	Description
a23_config_definesv	Defines used to configure the amber core. The number of ways in the cache is configurable. Also contains a set of debug switches which enable debug messages to be printed during simulation.
a23_localparams.v	Local parameters used in various amber source files.
a23_wishbone.v	The Wishbone interface connecting the Execute stage and Cache to the rest of the system. Instantiated in Fetch.
a23_alu.v	The arithmetic logic unit. Includes a 32-bit 2's compliment adder/subtractor as well as logical functions such as AND and XOR.
a23_functions.v	Common Verilog functions.
a23_core.v	Top-level Amber module.
a23_barrel_shifter.v	32-bit barrel shifter instantiated in Execute.
a23_cache.v	Synthesizable cache. Instantiated in Fetch. Cache misses cause the core to stall. The cache then issues a quad-word read on the wishbone bus, starting with the word that missed, and wrapping at the quad-word boundary.
a23_coprocessor.v	Co-processor 15 registers and control signals. Instantiated in Amber.
a23_decode.v	The instruction decode pipeline stage. Instantiated in Amber.
a23_decompile.v	The decompiler. This is a non-synthesizable debug module. It creates the amber.dis file which lists every instruction executed by the core.
a23_execute.v	The execute pipeline stage. Instantiated in Amber. It contains the alu, multiply, and register_bank sub-modules.
a23_fetch.v	The Fetch stage. This contains the Cache and Wishbone interface modules. It is instantiated in Amber.
a23_multiply.v	32-bit 2's compliment multiply and multiply-accumulate unit. Uses the Booth algorithm and takes 34 cycles to complete a signed multiply-accumulate operation but is quite small in logic area.
a23_register_bank.v	Contains all 27 registers r0 to r15 for each mode of operation. Registers are implemented as real flipflops in the FPGA. This allows multiple read and write access to the bank simultaneously.

The following diagram shows the Verilog module structure within the Amber 2 core.

Figure 5 - *Amber 23 Core Verilog Structure*



8.3 Project Directory Structure

The following table describes the directories and sub-directories located under $AMBER_BASE.

Table 19 Project directory structure

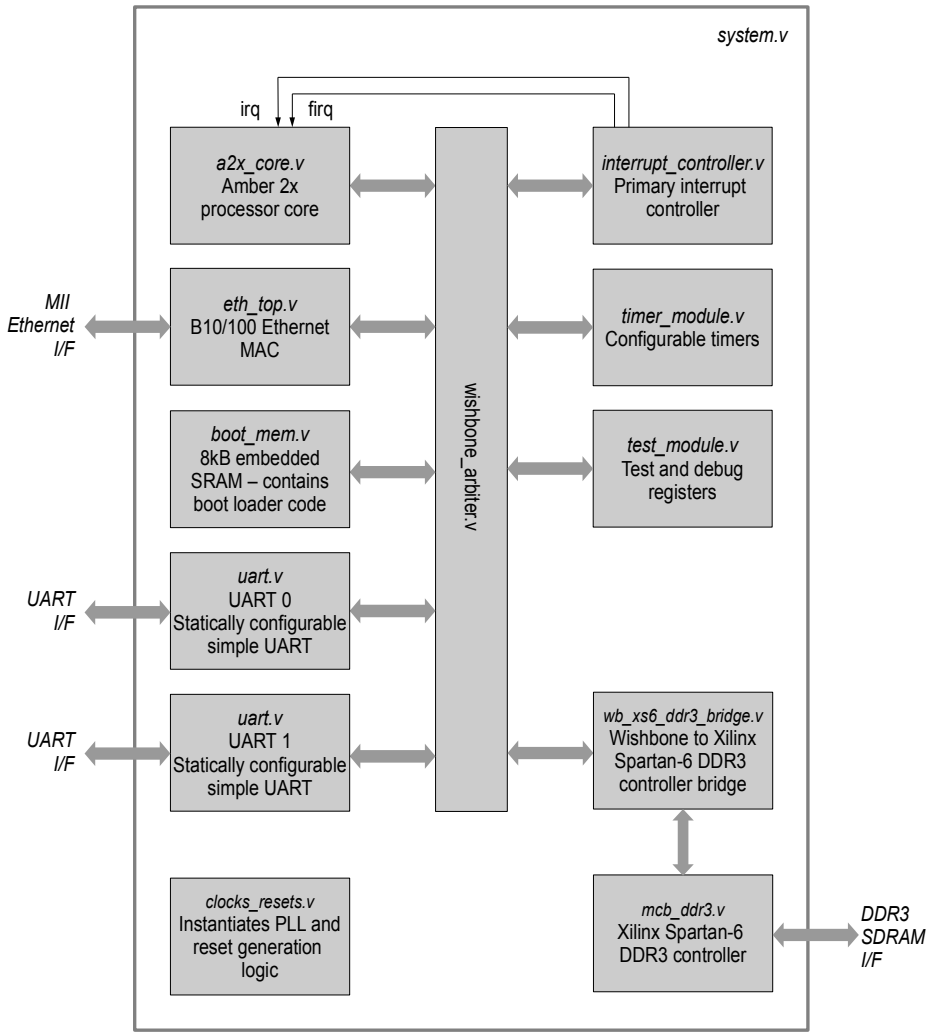
Directory	Description
doc	Contains all project documentation.
hw	Contains all Verilog source files, simulations and synthesis scripts, and hardware test source files.
hw/fpga	Files relating to FPGA synthesis.
hw/fpga/bin	Contains the FPGA synthesis makefile and supporting scripts.
hw/fpga/bitfiles	This directory is created during the FPGA synthsis process. It is used to store the final bitfile generated at the end of the FPGA syntheis process.

Directory	Description
hw/fpga/log	This directory is created during the FPGA synthsis process. It is used to store log files for each step of the FPGA synthesis process.
hw/fpga/work	This directory is created during the FPGA synthsis process. It is used to store temporary files created during the FPGA synthsis process. These files get erased when a new synthess run is started.
hw/isim	Where tests are run from. The Xilinx iSim Verilog simulator work directory, wave dump and any other simulation output files go in here.
hw/tests	Holds a set of hardware tests written in assembly. These tests focus on verifying the correct operation of the instruction set. If any modifications are made to the Amber core it is important that these tests still pass.
hw/tools	Holds scripts used to run Verilog simulations.
hw/vlog	Verilog source files.
hw/vlog/amber23	Amber 23 core Verilog source files.
hw/vlog/amber25	Amber 25 core Verilog source files.
hw/vlog/ethmac	The Ethernet MAC Verilog source files. These files come from the Opencores Ethmac project and are reproduced here for convenience.
hw/vlog/lib	Hardware libary Verilog files including memory models. The Amber project provides a simple generic library that is normally used for simulations. It also provides some wrappers for Xilinx library elements.
hw/vlog/system	FPGA system Verilog source files.
hw/vlog/tb	Testbench Verilog files.
hw/vlog/xs6_ddr3	Xilinx Spartan-6 DDR3 controller Verilog files go in here. These are not provided with the project for copyright reasons. They are needed to implement the Amber system on a Spartan-6 development board and must be generated in Xilinx Coregen.
hw/vlog/xv6_ddr3	Xilinx Virtex-6 DDR3 controller Verilog files go in here. These are not provided with the project for copyright reasons. They are needed to implement the Amber system on a Virtex-6 development board and must be generated in Xilinx Coregen.
sw	Contains C source files for applications that run on the Amber system, as well as some utilities that aid in debugging the system.
sw/boot-loader-serial	C, assembly sources and a makefile for the serial-port boot-loader application.
sw/boot-loader-ethmac	C, assembly sources and a makefile for the ethernet-port boot-loader application. This application supports telnet for control and status, and tftp for uploading elf executable files.
sw/hello-world	C, assembly source and a makefile for a simple stand-alone application example.
sw/include	Common C, assembly and makefile include files.
sw/mini-libc	C, assembly sources and a makefile to build the object that comprise a very small and limited stand-alone replacement for the libc library.
sw/tools	Shell scripts and C source files for compile and debug utilities.
sw/vmlinux	Contains the .mem and .dis files for the vmlinux simulation.

8.4 Amber FPGA System

The FPGA system included with the Amber project is a complete embedded processor system which included all peripherals needed to run Linux, including UART, timers and an Ethernet (MII) port. The following diagram shows the entire system.

Figure 6 - *Amber FPGA System*



All the Verilog source code was specifically developed for this project with the exception of the following modules;

- *ddr3.v.* The Xilinx Spartan-6 DDR3 controller was generated by the Xilinx Coregen tool. The files are not included with the project for copyright reasons. It is up to the user to optain the ISE software from Xilinx and generate the correct memory controller. Note that Wishbone bridge modules are included that support both the Xilinx Spartan-6 DDR3 controller and the Virtex-6 controller.
- *eth_top.v.* This module is from the Opencores Ethernet MAC 10/100 Mbps project. The Verilog code is included for convenience. It has not been modified, except to provide a memory module for the Spartan-6 FPGA.

9 Verilog simulations

9.1 Installing the Amber project

If you have not already done so, you need to download the Amber project from Opencores.org. The Amber project includes all the Verilog source files, tests written in assembly, a boot loader application written in C and scripts to compile, simulate and synthesize the code. You can either download a tar.gz file from the Opencores website or better still, connect to the Opencores Subversion server to download the project. This can be done on a Linux PC as follows;

```
mkdir /<your amber install path>/
cd /<your amber install path>/
svn --username <your opencores account name> --password <your opencores password> \
co http://opencores.org/ocsvn/amber/amber/trunk
```

9.2 Installing the Compiler

Tests need to be compiled before you can run simulations. You need to install a GNU cross-compiler to do this. The easiest way to install the GNU tool chain is to download a ready made package. Code Sourcery provides a free one. To download the Code Sourcery package, go to this page
http://www.codesourcery.com/sgpp/lite/arm

You need to register and will be sent an email to access the download area. Select the **GNU/Linux** version and then the **IA32 GNU/Linux** Installer. Once the package is installed, add the following to your .bashrc file, where the PATH is set to where you install the Code Sourcery GNU package.

```
# Change /proj/amber to where you saved the amber package on your system
export AMBER_BASE=/<your amber install path>/trunk

# Change /opt/Sourcery to where the package is installed on your system
PATH=/<your code sourcery install path>/bin:${PATH}

# AMBER_CROSSTOOL is the name added to the start of each GNU tool in
# the Code Sourcery bin directory. This variable is used in various makefiles to set
# the correct tool to compile code for the Amber core
export AMBER_CROSSTOOL=arm-none-linux-gnueabi

# Xilinx ISE installation directory
# This should be configured for you when you install ISE.
# But check that is has the correct value
# It is used in the run script to locate the Xilinx library elements.
export XILINX=/opt/Xilinx/14.5/ISE
```

9.2.1 GNU Tools Usage

It's important to remember to use the correct switches with the GNU tools to restrict the ISA to the set of instructions supported by the Amber 2 core. The switches are already set in the makefiles included with the Amber 2 core. Here are the switches to use with gcc (arm-none-linux-gnueabi-gcc);

```
-march=armv2a -mno-thumb-interwork
```

These switches specify the correct version of the ISA, and tell the compiler not to create bx instructions. Here is the switch to use with the GNU linker, arm-none-linux-gnueabi-ld;

```
 --fix-v4bx
```

This switch converts any bx instructions (which are not supported) to 'mov pc, lr'. Here is an example usage from the boot-loader make process;

```
arm-none-linux-gnueabi-gcc -c -Os -march=armv2a -mno-thumb-interwork -ffreestanding
   -I../include   -c -o boot-loader.o boot-loader.c
arm-none-linux-gnueabi-gcc -I../include    -c -o start.o start.S
arm-none-linux-gnueabi-gcc -c -Os -march=armv2a -mno-thumb-interwork -ffreestanding
   -I../include   -c -o crc16.o crc16.c
arm-none-linux-gnueabi-gcc -c -Os -march=armv2a -mno-thumb-interwork -ffreestanding
   -I../include   -c -o xmodem.o xmodem.c
arm-none-linux-gnueabi-gcc -c -Os -march=armv2a -mno-thumb-interwork -ffreestanding
   -I../include   -c -o elfsplitter.o elfsplitter.c
arm-none-linux-gnueabi-ld -Bstatic -Map boot-loader.map  --strip-debug --fix-v4bx -o boot-
   loader.elf -T sections.lds boot-loader.o start.o crc16.o xmodem.o elfsplitter.o
   ../mini-libc/printf.o ../mini-libc/libc_asm.o ../mini-libc/memcpy.o
arm-none-linux-gnueabi-objcopy -R .comment -R .note boot-loader.elf
../tools/amber-elfsplitter boot-loader.elf > boot-loader.mem
../tools/amber-memparams.sh boot-loader.mem boot-loader_memparams.v
arm-none-linux-gnueabi-objdump -C -S -EL boot-loader.elf > boot-loader.dis
```

A full list of compile switches for gcc can be found here;
http://gcc.gnu.org/onlinedocs/gcc-4.5.2/gcc/ARM-Options.html#ARM-Options

And for ld here;
http://sourceware.org/binutils/docs-2.21/ld/ARM.html#ARM

9.3 Running Simulations

You should be able to use any Verilog-2001 compatible simulator to run simulations of the Amber 2 Core. The project comes with run scripts and project files for the free Xilinx Webpack ISim 14.5 simulator.

Example usage:

```
[conor@lab isim]$ cd $AMBER_BASE/hw/isim
[conor@lab isim]$ ./run.sh hello-world
   Test hello-world, type 4
   make -s -C ../mini-libc MIN_SIZE=1
   arm-none-linux-gnueabi-gcc -c -Os -march=armv2a -mno-thumb-interwork -ffreestanding
   -I../include   -c -o boot-loader-serial.o boot-loader-serial.c
   arm-none-linux-gnueabi-ld -Bstatic -Map boot-loader-serial.map  --strip-debug --fix-
   v4bx -o boot-loader-serial.elf -T sections.lds boot-loader-serial.o start.o crc16.o
   xmodem.o elfsplitter.o ../mini-libc/printf.o ../mini-libc/libc_asm.o ../mini-
   libc/memcpy.o
   arm-none-linux-gnueabi-objcopy -R .comment -R .note boot-loader-serial.elf
   ../tools/amber-elfsplitter boot-loader-serial.elf > boot-loader-serial.mem
   ../tools/amber-memparams32.sh boot-loader-serial.mem boot-loader-serial_memparams32.v
   ../tools/amber-memparams128.sh boot-loader-serial.mem boot-loader-
   serial_memparams128.v
   arm-none-linux-gnueabi-objdump -C -S -EL boot-loader-serial.elf > boot-loader-
   serial.dis
   ../tools/check_mem_size.sh boot-loader-serial.mem "@000020"
   make -s -C ../mini-libc MIN_SIZE=1
   Running: /tools/Xilinx/14.5/ISE_DS/ISE/bin/lin/unwrapped/fuse tb -o amber-test.exe
   -prj amber-isim.prj -d BOOT_MEM_FILE="../../sw/boot-loader-serial/boot-loader-
   serial.mem" -d BOOT_MEM_PARAMS_FILE="../../sw/boot-loader-serial/boot-loader-
   serial_memparams32.v" -d MAIN_MEM_FILE="../../sw/hello-world/hello-world.mem" -d
   AMBER_LOG_FILE="tests.log" -d AMBER_TEST_NAME="hello-world" -d AMBER_SIM_CTRL=4 -d
   AMBER_TIMEOUT=0 -d AMBER_LOAD_MAIN_MEM -incremental -i ../vlog/lib -i ../vlog/system
   -i ../vlog/amber23 -i ../vlog/amber25 -i ../vlog/tb
```

```
ISim P.58f (signature 0xfbc00daa)
Number of CPUs detected in this system: 4
Turning on mult-threading, number of parallel sub-compilation jobs: 8
Determining compilation order of HDL files
Analyzing Verilog file "../vlog/system/boot_mem32.v" into library work
Analyzing Verilog file "../vlog/system/boot_mem128.v" into library work
Analyzing Verilog file "../vlog/system/clocks_resets.v" into library work
Analyzing Verilog file "../vlog/system/interrupt_controller.v" into library work
Analyzing Verilog file "../vlog/system/system.v" into library work
Analyzing Verilog file "../vlog/system/test_module.v" into library work
Analyzing Verilog file "../vlog/system/timer_module.v" into library work
Analyzing Verilog file "../vlog/system/uart.v" into library work
Analyzing Verilog file "../vlog/system/wb_xs6_ddr3_bridge.v" into library work
Analyzing Verilog file "../vlog/system/wishbone_arbiter.v" into library work
Analyzing Verilog file "../vlog/system/afifo.v" into library work
Analyzing Verilog file "../vlog/system/ddr3_afifo.v" into library work
Analyzing Verilog file "../vlog/system/ethmac_wb.v" into library work
Analyzing Verilog file "../vlog/system/main_mem.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_clockgen.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_crc.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_fifo.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_maccontrol.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_macstatus.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_miim.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_outputcontrol.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_random.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_receivecontrol.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_registers.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_register.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_rxaddrcheck.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_rxcounters.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_rxethmac.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_rxstatem.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_shiftreg.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_spram_256x32.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_top.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_transmitcontrol.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_txcounters.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_txethmac.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_txstatem.v" into library work
Analyzing Verilog file "../vlog/ethmac/eth_wishbone.v" into library work
Analyzing Verilog file "../vlog/ethmac/xilinx_dist_ram_16x32.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_alu.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_barrel_shift.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_cache.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_coprocessor.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_core.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_decode.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_decompile.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_execute.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_fetch.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_multiply.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_register_bank.v" into library work
Analyzing Verilog file "../vlog/amber23/a23_wishbone.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_alu.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_barrel_shift.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_shifter.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_coprocessor.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_core.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_dcache.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_decode.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_decompile.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_execute.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_fetch.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_icache.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_mem.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_multiply.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_register_bank.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_wishbone.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_wishbone_buf.v" into library work
Analyzing Verilog file "../vlog/amber25/a25_write_back.v" into library work
Analyzing Verilog file "../vlog/lib/generic_iobuf.v" into library work
Analyzing Verilog file "../vlog/lib/generic_sram_byte_en.v" into library work
Analyzing Verilog file "../vlog/lib/generic_sram_line_en.v" into library work
Analyzing Verilog file "../vlog/tb/tb_uart.v" into library work
Analyzing Verilog file "../vlog/tb/eth_test.v" into library work
Analyzing Verilog file "../vlog/tb/dumpvcd.v" into library work
Analyzing Verilog file "../vlog/tb/tb.v" into library work
Starting static elaboration
Completed static elaboration
Fuse Memory Usage: 41692 KB
Fuse CPU Usage: 1220 ms
Compiling module clocks_resets
Compiling module generic_sram_line_en(DATA_WIDTH=...
Compiling module generic_sram_byte_en(DATA_WIDTH=...
```

```
   Compiling module a23_cache_default
   Compiling module a23_wishbone
   Compiling module a23_fetch
   Compiling module a23_decompile_2
   Compiling module a23_decode
   Compiling module a23_barrel_shift
   Compiling module a23_alu
   Compiling module a23_multiply
   Compiling module a23_register_bank
   Compiling module a23_execute
   Compiling module a23_coprocessor
   Compiling module a23_core
   Compiling module eth_clockgen
   Compiling module eth_shiftreg
   Compiling module eth_outputcontrol
   Compiling module eth_miim
   Compiling module eth_register(RESET_VALUE=8'b0)
   Compiling module eth_register(RESET_VALUE=8'b1010...
   Compiling module eth_register(WIDTH=1,RESET_VALUE...
   Compiling module eth_register(WIDTH=7,RESET_VALUE...
   Compiling module eth_register(WIDTH=7,RESET_VALUE...
   Compiling module eth_register(WIDTH=7,RESET_VALUE...
   Compiling module eth_register(RESET_VALUE=8'b0110...
   Compiling module eth_register(RESET_VALUE=8'b0100...
   Compiling module eth_register(WIDTH=6,RESET_VALUE...
   Compiling module eth_register(WIDTH=4,RESET_VALUE...
   Compiling module eth_register(WIDTH=3,RESET_VALUE...
   Compiling module eth_register(RESET_VALUE=8'b0110...
   Compiling module eth_register(WIDTH=1)
   Compiling module eth_register(WIDTH=5,RESET_VALUE...
   Compiling module eth_register(WIDTH=16,RESET_VALU...
   Compiling module eth_registers
   Compiling module eth_receivecontrol
   Compiling module eth_transmitcontrol
   Compiling module eth_maccontrol
   Compiling module eth_txcounters
   Compiling module eth_txstatem
   Compiling module eth_crc
   Compiling module eth_random
   Compiling module eth_txethmac
   Compiling module eth_rxstatem
   Compiling module eth_rxcounters
   Compiling module eth_rxaddrcheck
   Compiling module eth_rxethmac
   Compiling module generic_sram_byte_en(DATA_WIDTH=...
   Compiling module eth_spram_256x32
   Compiling module eth_fifo(DEPTH=16,CNT_WIDTH=5)
   Compiling module eth_wishbone
   Compiling module eth_macstatus
   Compiling module eth_top
   Compiling module generic_iobuf
   Compiling module generic_sram_byte_en(DATA_WIDTH=...
   Compiling module boot_mem32
   Compiling module uart(WB_DWIDTH=32,WB_SWIDTH=4)
   Compiling module test_module(WB_DWIDTH=32,WB_SWID...
   Compiling module timer_module(WB_DWIDTH=32,WB_SWI...
   Compiling module interrupt_controller(WB_DWIDTH=3...
   Compiling module main_mem(WB_DWIDTH=32,WB_SWIDTH=...
   Compiling module wishbone_arbiter(WB_DWIDTH=32,WB...
   Compiling module ethmac_wb(WB_DWIDTH=32,WB_SWIDTH...
   Compiling module system
   Compiling module eth_test
   Compiling module tb_uart_default
   Compiling module dumpvcd
   Compiling module tb
   Time Resolution for simulation
is 1ps.
   Waiting for 1 sub-compilation(s) to finish...
   Compiled 68 Verilog Units
   Built simulation executable amber-test.exe
   Fuse Memory Usage: 89580 KB
   Fuse CPU Usage: 2120 ms
   GCC CPU Usage: 1200 ms
   ISim P.58f (signature 0xfbc00daa)
   WARNING: A WEBPACK license was found.
   WARNING: Please use Xilinx License Configuration Manager to check out a full ISim
   license.
   WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more
   information on the differences between the Lite and the Full version.
   This is a Lite version of ISim.
   Time resolution is 1 ps
   Simulator is doing circuit initialization process.
   Load boot memory from ../../sw/boot-loader-serial/boot-loader-serial.mem
   Read in 2053 lines
   log file tests.log, timeout 0, test name hello-world
```

```
Load main memory from ../../sw/hello-world/hello-world.mem
Read in 9116 lines
Finished circuit initialization process.
Amber Boot Loader v20130428143120
j 0x00008000

Hello, World!

--------------------------------------------------------------------------------
Amber Core
      > User         FIRQ         IRQ          SVC
r0       0x00000010
r1       0x00008dfc
r2       0x00000000
r3       0x00000000
r4       0x0c008003
r5       0xdeadbeef
r6       0xdeadbeef
r7       0xdeadbeef
r8       0xdeadbeef   0xdeadbeef
r9       0xdeadbeef   0xdeadbeef
r10      0x00000011   0xdeadbeef
r11      0xf0000000   0xdeadbeef
r12      0x00001ecc   0xdeadbeef
r13      0x08000000   0xdeadbeef   0xdeadbeef   0x01ffffb0
r14 (lr) 0x00008020   0xdeadbeef   0xdeadbeef   0x600003fb
r15 (pc) 0x00008490

Status Bits: N=0, Z=1, C=1, V=0, IRQ Mask 0, FIRQ Mask 0, Mode = User
--------------------------------------------------------------------------------

++++++++++++++++++++
Passed hello-world 47634 ticks
++++++++++++++++++++
Stopped at time : 1191327500 ps : File "/proj/amber_trunk_working/hw/vlog/tb/tb.v"
Line 503
```

9.4 Simulation output files

9.4.1 Disassembly Output File

The disassembly file, amber.dis, is generated by default during a simulation. It is located in the $AMBER_BASE/hw/sim directory. This file is very useful for debugging software as it shows every instruction executed by the core and the result of all load and store operations.

This file is generated by default. To turn off generation, comment the line where AMBER_DECOMPILE is defined in $AMBER_BASE/hw/vlog/amber/amber_config_defines.v.

Below is an example of the dissassembly output file. The first column gives the time that the instruction was executed. The time is specified in sys_clk ticks. The second column gives the address of the instruction being executed and the next column gives the instruction. If an instruction is not executed because of a conditional execution code, this is marked with a '–' character in front of the instruction. For load and store instructions, the actual memory access is given below the instruction. This is the complete listing for the add test.

```
  264         0:   mov     r1,  #3
  267         4:   mov     r2,  #1
  270         8:   add     r3,  r1,  r2
  273         c:   cmp     r3,  #4
  276        10:  -movne   r10, #10
  279        14:  -bne     b4
  282        18:   mov     r4,  #0
```

```
     285        1c:   mov     r5,  #0
     288        20:   add     r6,  r5,  r4
     291        24:   cmp     r6,  #0
     294        28:  -movne   r10, #20
     297        2c:  -bne     b4
     300        30:   mov     r7,  #0
     303        34:   mvn     r8,  #0
     306        38:   add     r9,  r7,  r8
     309        3c:   cmn     r9,  #1
     312        40:  -movne   r10, #30
     315        44:  -bne     b4
     318        48:   mvn     r1,  #0
     321        4c:   mov     r2,  #0
     324        50:   add     r3,  r1,  r2
     327        54:   cmn     r3,  #1
     330        58:  -movne   r10, #40
     333        5c:  -bne     b4
     336        60:   mvn     r4,  #0
     339        64:   mvn     r5,  #0
     342        68:   add     r6,  r4,  r5
     345        6c:   cmn     r6,  #2
     348        70:  -movne   r10, #50
     351        74:  -bne     b4
     354        78:   mvn     r7,  #0
     357        7c:   mvn     r8,  #254
     360        80:   add     r9,  r7,  r8
     363        84:   cmn     r9,  #256
     366        88:  -movne   r10, #60
     369        8c:  -bne     b4
     372        90:   ldr     r1, [pc, #60]
     377              read    addr d4, data 7fffffff
     381        94:   mov     r2,  #1
     384        98:   adds    r3,  r1,  r2
     387        9c:  -bvc     b4
     390        a0:   ldr     r0, [pc, #48]
     395              read    addr d8, data 80000000
     399        a4:   cmp     r0,  r3
     402        a8:  -movne   r10, #70
     405        ac:  -bne     b4
     408        b0:   b       c0
     410              jump    from b0 to c0, r0 80000000, r1 7fffffff
     417        c0:   ldr     r11, [pc, #8]
     422              read    addr d0, data f0000000
     426        c4:   mov     r10, #17
     429        c8:   str     r10, [r11]
     432              write   addr f0000000, data 00000011, be f
```

9.4.2

Figure 7 - *GTKWave waveform viewer*

9.4.3 Program Trace Utility

A utility is provided that traces all function calls made during a Verilog simulation. Here is an example usage;

```
cd $AMBER_BASE/hw/sim
run ethmac-test
ln -s ../../sw/tools/amber-jumps.sh jumps
jumps ethmac-test
```

This produces the following output. The left column gives the time of the event. The next colum gives the name of the calling function. The next column gives the value of the r0 register. This register holds the first parameter passed in function calls. The next column gives the name of the function called.

```
   276031 u main ->                              ( 00008dec, ) printf u
   276104 u printf ->                            ( 07ffff8c, ) print u
   276311 u print ->                             ( 00000053, ) _outbyte u
   276411   print <-                             ( 00000053, )
```

```
etc.
```

9.5 Hardware Tests

The Amber package contains a set of tests which are used to verify the correct operation of all the instructions, interrupts, the cache and peripherals. The tests are written in assembly. Several of the tests were added when a specific bug was found while debugging the core. To run one of the tests, use run <test-name>, e.g.

```
cd $AMBER_BASE/hw/sim
run barrel_shift
```

Each test generates pass or fail when it completes, e.g.

```
# ++++++++++++++++++++
# Passed barrel_shift
# ++++++++++++++++++++
```

To run the complete test suite;

```
cd $AMBER_BASE/hw/sim
run -a
```

Once the run is complete look at the output file hw-tests.log in the $AMBER_BASE/hw/sim/ directory to check the results. All tests should pass.

The following table describes each test. The source files for these tests are in the directory $AMBER_BASE/hw/tests.

Table 20 Amber Core Hardware Verification Tests

Name	Description
adc	Tests the adc instruction. Adds 3 32-bit numbers using adc and checks the result.
addr_ex	Tests an address exception interrupt. Sets the pc to 0x3fffffc and executes a nop. The pc then increments to 0x4000000 triggering an address exception.
add	Tests the add instruction. Runs through a set of additions of positive and negative numbers, checking that the results are correct. Also tests that the 's' flag on the instruction correctly sets the condition flags.
barrel_shift_rs	Tests the barrel shift operation with a mov instruction, when the shift amount is a register value. Test that shift of 0 leaves Rm unchanged. Tests that a shift of > 32 sets Rm and carry out to 0.
barrel_shift	Tests the barrel shift operation with a mov instruction when the shift amount is an immediate value.Tests lsl, lsr and ror.
bcc	Tests branch on carry clear.
bic_bug	Test added to catch specific bug with the bic instruction. The following instruction stored the result in r3, instead of r2 tst r2, r0, lsl r3 bicne r2, r2, r0, lsl r3
bl	Test Branch and Link instruction. Checks that the correct return address is stored in the link register (r14).
cache1	Contains a long but simple code sequence. The entire sequence can fit in the cache. This sequence is executes 4 times, so three times it will execute from the cache. Test passes if sequence executes correctly.
cache2	Tests simple interactin between cached data and uncached instruction accesses.
cache3	Tests that the cache can write to and read back multiple times from 2k words in sequence in

Name	Description
	memory - the size of the cache.
cacheable_area	Tests the cacheable area co-processor function.
cache_flush	Tests the cache flush function. Does a flush in the middle of a sequence of data reads. Checks that all the data reads are correct.
cache_swap_bug	Tests the interaction between a swap instruction and the cache. Runs through a main loop multiple times with different numbers of nop instructions before the swp instruction to test a range of timing interactions between the cache state machine and the swap instruction.
cache_swap	Fills up the cache and then does a swap access to data in the cache. That data should be invalidated. Check by reading it again.
change_mode	Tests teq, tst, cmp and cmn with the p flag set. Starts in supervisor mode, changes to Interrupt mode then Fast Interrupt mode, then supervisor mode again and finally User mode.
change_sbits	Change status bits. Tests movs where the destination register is r15, the pc. Depending on the processor mode and whether the s bit is set or not, some or none of the status bits will change.
ddr31	Word accesses to random addresses in DDR3 memory. The test creates a list of addresses in an area of boot_mem. It then writes to all addresses with data value equal to address. Finally it reads back all locations checking that the read value is correct.
ddr32	Tests byte read and write accesses to DDR3 memory.
ddr33	Test back to back write-read accesses to DDR3 memory.
ethmac_mem	Tests wishbone access to the internal memory in the Ethernet MAC module.
ethmac_reg	Tests wishbone access to registers in the Ethernet MAC module.
ethmac_tx	Tests ethernet MAC frame transmit and receive functions and Ethmac DMA access to hiboot mem. Ethmac is put in loopback mode and a packet is transmitted and received.
firq	Executes 20 FIRQs at random times while executing a small loop of code. The interrupts are triggered using a ransom timer. Test checks the full set of FIRQ registers (r8 to r14) and will only pass if all interrupts are handled correctly.
flow_bug	The core was illegally skipping an instruction after a sequence of 3 conditional not-execute instructions and 1 conditional execute instruction.
flow1	Tests instruction and data flow. Specifically tests that a stm writing to cached memory also writes all data through to main memory.
flow2	Tests that a stream of str instrutions writing to cached memory works correctly.
flow3	Tests ldm where the pc is loaded which causes a jump. At the same time the mode is changed. This is repeated with the cache enabled.
hiboot_mem	Tests wishbone read and write access to hi (non-cachable) boot SRAM.
inflate_bug	A load store sequence was found to not execute correctly.
irq	Tests running a simple algorithm to add a bunch of numbers and check that the result is correct. This algorithm runs 80 times. During this, a whole bunch of IRQ interrupts are triggered using the random timer.
ldm_stm_onetwo	Tests ldm and stm of single registers with cache enabled. Tests ldm and stm of 2 registers with cache enabled.
ldm1	Tests the standard form of ldm.
ldm2	Tests ldm where the user mode registers are loaded whilst in a privileged mode.
ldm3	Tests ldm where the status bits are also loaded.
ldm4	Tests the usage of ldm in User Mode where the status bits are loaded. The s bit should be ignored in User Mode.
ldr	Tests ldr and ldrb with all the different addressing modes.
ldr_atr_pc	Tests lrd and str of r15.
mla	Tests the mla (multiply and accumulate) instruction.
mlas_bug	Bug with Multiply Accumulate. The flags were gettting set 1 cycle early.
movs_bug	Tests a movs followed by a sequence of ldr and str instructions with different condition fields.
mul	Tests the mul (multiply) instruction.
sbc	Tests the 'subtract with carry' instruction by doing 3 64-bit subtractions.
stm_stream	Generates as dense a stream of writes as possible to check that the memory subsystem can cope with this worst case.

Name	Description
stm1	Tests the normal operation of the stm instruction.
stm2	Test jumps into user mode, loads some values into registers r8 - r14, then jumps to FIRQ and saves the user mode registers to memory.
strb	Tests str and strb with different indexing modes.
sub	Tests sub and subs.
swi	Tests the software interrupt – swi.
swp_lock_bug	Bug broke an instruction read immediately after a swp instruction.
swp	Tests swp and swpb.
uart_reg	Tests wishbone read and write access to the Amber UART registers.
uart_rxint	Tests the UART receive interrupt function. Some text is sent from the test_uart to the uart and an interrupt generated.
uart_rx	Tests the UART receive function.
uart_tx	Uses the tb_uart in loopback mode to verify the transmitted data.
undefined_ins	Tests Undefined Instruction Interrupt. Fires a few unsupported floating point unit (FPU) instructions into the core. These cause undefined instruction interrupts when executed.

9.6 C Programs

In addition to the short assembly language tests, some longer programs written in C are included with the Amber system. These can be used to further test and verify the system, or as a basis to develop your own applications.

The source code for these programs is in $AMBER_BASE/sw.

9.6.1 Serial Boot Loader

This is located in $AMBER_BASE/sw/boot-loader-serial. It can be run in simulation as follows;

```
cd $AMBER_BASE/hw/isim
./run.sh boot-loader-serial
```

The simulation output looks like the following;

```
# Test boot-loader, log file boot-loader.log
# Load boot memory from ../../sw/boot-loader/boot-loader.mem
# Read in 1928 lines
# Amber Boot Loader v20110202130047
# Commands
# l                             : Load elf file
# b <address>                   : Load binary file to <address>
# d <start address> <num bytes> : Dump mem
# h                             : Print help message
# j                             : Execute loaded elf, jumping to 0x00080000
# p <address>                   : Print ascii mem until first 0
# r <address>                   : Read mem
# s                             : Core status
# w <address> <value>           : Write mem
# r 0  0000000c
# r 1  00001b76
# r 2  00000000
# r 3  00000000
# r 4  deadbeef
# r 5  deadbeef
# r 6  deadbeef
# r 7  deadbeef
# r 8  deadbeef
# r 9  deadbeef
# r10  deadbeef
```

```
# r11  deadbeef
# r12  00000048
# r13  600002f7
# sp   01ffff80
# pc   600002f3
#
# -------------------------------------------------------------------------
# Amber Core
#          User         FIRQ         IRQ        > SVC
# r0       0x00000001
# r1       0x00001c35
# r2       0x00000000
# r3       0x00000000
# r4       0xdeadbeef
# r5       0xdeadbeef
# r6       0xdeadbeef
# r7       0xdeadbeef
# r8       0xdeadbeef   0xdeadbeef
# r9       0xdeadbeef   0xdeadbeef
# r10      0x00000011   0xdeadbeef
# r11      0xf0000000   0xdeadbeef
# r12      0x00000048   0xdeadbeef
# r13      0xdeadbeef   0xdeadbeef   0xdeadbeef   0x01ffffc0
# r14 (lr) 0xdeadbeef   0xdeadbeef   0xdeadbeef   0x20000763
# r15 (pc) 0x00001250
#
# Status Bits: N=0, Z=1, C=1, V=0, IRQ Mask 0, FIRQ Mask 0, Mode = Supervisor
# -------------------------------------------------------------------------
#
# ++++++++++++++++++++
# Passed boot-loader
# ++++++++++++++++++++
```

The boot loader is used to download longer applications onto the FPGA development board via the UART port and using Hyper Terminal on a host Windows PC.

9.6.2 Hello World

This is located in $AMBER_BASE/sw/hello-world. It can be run in simulation as follows;

```
cd $AMBER_BASE/hw/isim
./run.sh hello-world
```

This is a very simple example of a stand alone C program. The printf function it uses is contained in $AMBER_BASE/sw/mini-libc, so that it can run on an FPGA without access to a real libc library file.

9.6.3 Ethmac Boot Loader

This is located in $AMBER_BASE/sw/boot-loader-ethmac. This is an 'over the network' boot loader. It supports telnet for command and status, and tftp for uploading executable programs (as elf files) to run on the FPGA.

The IP address is hard-coded in $AMBER_BASE/sw/boot-loader-ethmac/packet.c, line 56. To change it, edit that file and rebuild the FPGA, creating a new bitfile.

Here's an example usage of the boot-loader;

```
[conor@lab ~]$ telnet 192.168.0.17
   Trying 192.168.0.17...
   Connected to 192.168.0.17.
   Escape character is '^]'.
   Amber Processor Boot Loader
   > s
   Socket ID           0
   Packets received    10
```

```
    Packets transmitted 9
    Packets resent      0
    TCP checksum errors 0
    Counterparty IP 192.168.0.52
    Counterparty Port 55318
    Malloc pointer 0x01223600
    Malloc count 531
    Uptime 21 seconds
    >
```

9.7 Linux

A memory file is provided to run a simulation of Linux booting. The main reason for providing this file is to have a long test to further validate the correct operation of the core. This file was created from a modified version of the 2.4.27 kernel with the patch-2.4.27-vrs1.bz2 patch file applied and then some modifications made to source files to support the specific hardware in the Amber 2 FPGA.

The vmlinux.mem memory file contains an embedded ext2 format ramdisk image which contains the hello-world program, but renamed as /sbin/init. The kernel mounts the ramdisk as /dev/root and runs init. This program prints "Hello, World" and writes the test pass value to the simulation control register. To run this simulation;

```
cd $AMBER_BASE/hw/sim
run vmlinux
```

This simulation takes about 6 million ticks to run to completion, or between 5 minutes and an hour of wall time depending on your simulator and PC. The following is the output from this simulation;

```
# Amber Boot Loader v20110117211518
# j 0x2080000
#
# Linux version 2.4.27-vrs1 (conor@server) (gcc version 4.5.1 (Sourcery G++ Lite 2010.09-
   50) ) #354 Tue Feb 1 17:56:00 GMT 2011
# CPU: Amber 2 revision 0
# Machine: Amber-FPGA-System
# On node 0 totalpages: 1024
# zone(0): 1024 pages.
# zone(1): 0 pages.
# zone(2): 0 pages.
# Kernel command line: console=ttyAM0 mem=32M root=/dev/ram
# Calibrating delay loop... 19.91 BogoMIPS
# Memory: 32MB = 32MB total
# Memory: 31136KB available (493K code, 195K data, 32K init)
# Dentry cache hash table entries: 4096 (order: 0, 32768 bytes)
# Inode cache hash table entries: 4096 (order: 0, 32768 bytes)
# Mount cache hash table entries: 4096 (order: 0, 32768 bytes)
# Buffer cache hash table entries: 8192 (order: 0, 32768 bytes)
# Page-cache hash table entries: 8192 (order: 0, 32768 bytes)
# POSIX conformance testing by UNIFIX
# Linux NET4.0 for Linux 2.4
# Based upon Swansea University Computer Society NET3.039
# Starting kswapd
# ttyAM0 at MMIO 0x16000000 (irq = 1) is a WSBN
# pty: 256 Unix98 ptys configured
# RAMDISK driver initialized: 16 RAM disks of 208K size 1024 blocksize
# NetWinder Floating Point Emulator V0.97 (double precision)
# RAMDISK: ext2 filesystem found at block 8388608
# RAMDISK: Loading 200 blocks [1 disk] into ram disk... done.
# Freeing initrd memory: 200K
# VFS: Mounted root (ext2 filesystem) readonly.
# Freeing init memory: 32K
# Hello, World!
```

```
#
# ------------------------------------------------------------------------------
# Amber Core
#        > User         FIRQ         IRQ          SVC
# r0       0x00000010
# r1       0x0080ee00
# r2       0x00000000
# r3       0x00000000
# r4       0x00000000
# r5       0x00000000
# r6       0x00000000
# r7       0x00000000
# r8       0x00000000   0xdeadbeef
# r9       0x00000000   0xdeadbeef
# r10      0x00000011   0xdeadbeef
# r11      0xf0000000   0xdeadbeef
# r12      0x00000000   0xdeadbeef
# r13      0x019fff40   0xdeadbeef   0x0210bca4   0x02161fe8
# r14 (lr) 0x00000000   0xdeadbeef   0x220a437f   0x0080e428
# r15 (pc) 0x0080e800
#
# Status Bits: N=0, Z=1, C=1, V=0, IRQ Mask 0, FIRQ Mask 0, Mode = User
# ------------------------------------------------------------------------------
#
# ++++++++++++++++++++
# Passed vmlinux
# ++++++++++++++++++++
```

The program trace utility can be used to trace the Linux execution, as follows;

```
cd $AMBER_BASE/hw/sim
ln -s ../../sw/tools/amber-jumps.sh jumps
jumps vmlinux
```

10 FPGA Synthesis

A makefile is provided that performs synthesis of the system to a Xilinx Spartan-6 FPGA. To use this makefile you must have Xilinx ISE installed. I have tested it with ISE v14.5. The makefile is quite flexible. To see all its options, type;

```
cd $AMBER_BASE/hw/fpga/bin
make help
```

To use the script to perform a complete synthesis run from start to finish and generate a bitfile;

```
cd $AMBER_BASE/hw/fpga/bin
chmod +x *.sh
make new
```

The script performs the following steps

1. Compiles the boot loader program in $AMBER_BASE/sw/boot-loader, to ensure the latest version goes into the boot_mem ram blocks.
2. Runs xst to synthesize the top-level Verilog file $AMBER_BASE/hw/vlog/system/system.v and everything inside it.
3. Runs ngbbuild to create the initial FPGA netlist.
4. Runs map to do placement.
5. Runs par to do routing.
6. Runs bitgen to create an FPGA bitfile in the bitfile directory.
7. Runs trce to do timing analysis on the finished FPGA.

The Spartan-6 FPGA target device is the default. To compile for the Virtex-6 FPGA, set VIRTEX6=1 on the command line, e.g.

```
cd $AMBER_BASE/hw/fpga/bin
make new VIRTEX6=1
```

The Amber 23 core is the default. To synthesize the Amber 25 core instead, set A25=1 on the command line, e.g.

```
cd $AMBER_BASE/hw/fpga/bin
make new A25=1
```

If the par step fails (timing or area constrains not met), you can rerun map and par with a different seed. Simply call the makefile again without the new switch. The makefile will automatically increment the seed, e.g.

```
cd $AMBER_BASE/hw/fpga/bin
```

```
make
```

The system clock speed is configured within the FPGA makefile, $AMBER_BASE/hw/fpga/bin/Makefile. To change it, change the value of AMBER_CLK_DIVIDER in that file. The system clock frequency is equal to the PLL's VCO clock frequency divided by AMBER_CLK_DIVIDER. By default it is set to 40MHz for Spartan-6 and 80MHz for Virtex-6.

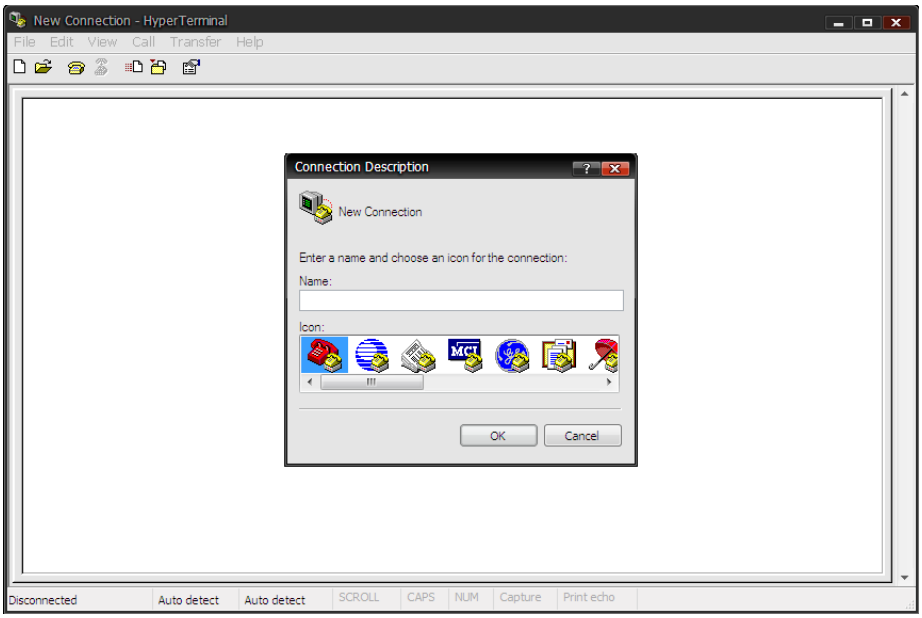
11 Using Boot-Loader

If you have a development board with a UART connection to a PC you can use boot-loader to download and run applications on the board. I have tested this with the Xilinx SP605 development board. It provides a UART connection via a USB port on the board.

11.1 Configure HyperTerminal

Run HyperTerminal on the PC. This is a free application supplied with Windows. In Windows XP it is available on the Start Menu under All Programs -> Accessories -> Communications -> HyperTerminal

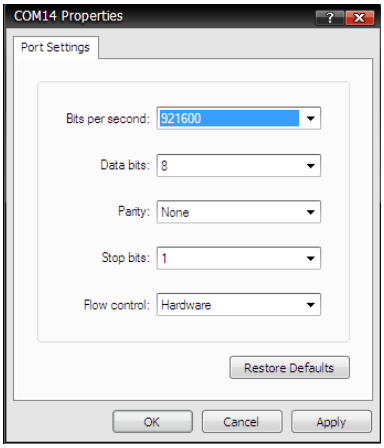
When HyperTerminal starts it brings up the new connection dialogue. The first screen of this dialogue asks you to name the connection. Name it anything you like.



On the next screen select the com port. This will depend on your PC. For me the correct port is COM14. Check the documentation for your FPGA board.

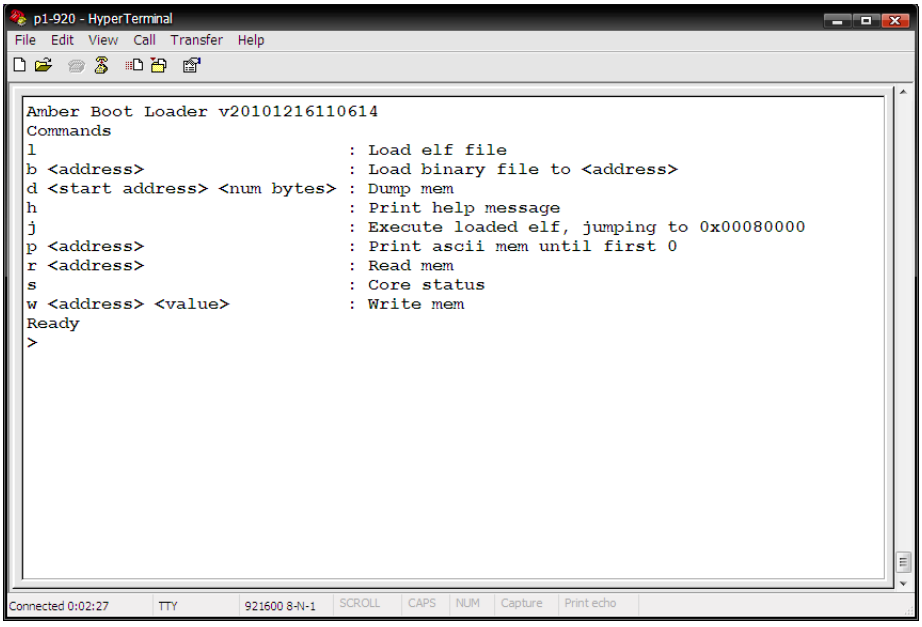
The final screen sets the connection speed and type. Select 921600 bits per second, 8

data bits, no parity bits, 1 stop bit and hardware flow control. This is the default speed of the UART and is configured within the Verilog code, in the file $AMBER_BASE/hw/vlog/system/system_config_defines.v. It can be changed prior to FPGA synthesis.



11.2 Configure the FPGA

Load the bitfile into the FPGA on the development board. This can be done using Xilinx iMPACT. Once the FPGA is configured the boot loader will print some messages via the UART interface onto the HyperTerminal screen, as follows;



You can now load and run applications using the boot loader. For example, to load the ethmac-test application, type 'l' and hit return. This puts the boot loader into a loop waiting to receive a file. Next select the Transfer-> Send File menu item on HyperTerminal. Select the 1K Xmodem protocol. Then click on browse and select the ethmac-test.elf file in $AMBER_BASE/sw/ethmac-test. The elf file in generated when you run make in that directory. The file downloads to the board. Type 'j' to run it.

12 License

All source code provided in the Amber package is release under the following license terms;

```
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```