

The diagram illustrates the pin connections for the Shield Header, Right Extra Pins, and Left Extra Pins. The Shield Header (J1, J7) connects to +3.3V, +6V, and GND. The Right Extra Pins (J8, J9) connect to +3.3V, GND, and +6V. The Left Extra Pins (J10) connect to +3.3V and GND.

**Shield Header (J1, J7):**

- J1:** Pin 10 (+3.3V), Pin 9 (P1\_01), Pin 8 (P0\_27), Pin 7 (P0\_10), Pin 6 (P1\_07), Pin 5 (P1\_06), Pin 4 (P0\_11), Pin 3 (P0\_09), Pin 2 (P0\_30), Pin 1 (GND).
- J7:** Pin 10 (+3.3V), Pin 9 (+6V), Pin 8 (P0\_03), Pin 7 (P0\_02), Pin 6 (P0\_05), Pin 5 (P0\_04), Pin 4 (P1\_10), Pin 3 (P1\_02), Pin 2 (P1\_03), Pin 1 (GND).

**Right Extra Pins (J8, J9):**

- J8:** Pin 4 (GND), Pin 3 (P0\_07), Pin 2 (P0\_06), Pin 1 (+3.3V).
- J9:** Pin 4 (+3.3V), Pin 3 (P0\_20), Pin 2 (P0\_25), Pin 1 (GND).

**Left Extra Pins (J10):**

- J10:** Pin 4 (+3.3V), Pin 3 (P0\_24), Pin 2 (P0\_23), Pin 1 (GND).

Diagram illustrating the pin configuration for the J6 connector (SWD) connected to the microcontroller:

- Pin 1: +BATT
- Pin 2: Vtref
- Pin 3: GND
- Pin 4: SWDCLK/TCK
- Pin 5: SWDIO/TMS
- Pin 6: SWO/TDO
- Pin 7: NC
- Pin 8: TDI

The figure displays four circuit diagrams for the DRV5015A1 comparators, labeled U1, U2, U4, and U5. Each circuit includes a 10nF capacitor (C1, C2, C7, C8) connected to a +3.3V supply and GND. The comparators are configured with VCC, GND, and OUT pins. The outputs are connected to P0\_31, P1\_11, P0\_21, and P1\_12 respectively.

The diagram shows the BT40 connector pinout with the following connections:

- H0-H3:** H0/GND, H1/GND, H2/GND, H3/GND.
- P102-SDA:** P1\_02 (1) to P102/SDA.
- P103-SCL:** P1\_03 (2) to P103/SCL.
- P00-XL1:** P0\_03 (3) to P00/XL1.
- P01-XL2:** P0\_04 (4) to P01/XL2.
- P004-AIN0:** P0\_04 (5) to P004/AIN0.
- P005-AIN1:** P0\_05 (6) to P005/AIN1.
- P002-NFC1:** P0\_02 (7) to P002/NFC1.
- P003-NFC2:** P0\_03 (8) to P003/NFC2.
- SWDIO:** P0\_30 (16) to SWDIO.
- SWCLK:** P0\_11 (15) to SWCLK.
- RESET:** P0\_09 (14) to RESET.
- P0\_30:** P0\_30 (13) to P0\_30.
- P0\_11:** P0\_11 (12) to P0\_11.
- P0\_09:** P0\_09 (11) to P0\_09.
- GND:** P0\_10 (10) to GND.
- VDD:** P0\_09 (9) to VDD.

MountingHole:MountingHole2-MountingHole2PadOnly

The diagram shows a 4-to-2 decoder circuit. It consists of two DMP2045U-7 comparators, Q4 and Q3. The inputs of Q4 are connected to +BATT and GND. The inputs of Q3 are connected to +BATT and GND. The outputs of Q4 and Q3 are connected to a 4-bit shift register. The circuit also includes a 10nF capacitor C20, a 100 ohm resistor R14, a switch SW1 (SW\_SPDT), and a battery BT1.