NEC

MOS INTEGRATED CIRCUIT

μPD161704A

1-CHIP DRIVER FOR 240 RGB x 320 DOT TFT-LCD WITH RAM

DESCRIPTION

The μPD161704A is a TFT-LCD 1-chip driver that includes display RAM.

This driver has 720-source outputs, 322-gate outputs (including 2-dummy outputs), a display RAM capacity of 1,382,400 bits (240 pixels x 18 bits x 320 lines) and can provide a 262,144-color display.

FEATURES

- TFT-LCD 1-chip driver with on-chip display RAM
- Logic power supply voltage: 2.3 V (Using internal regulator circuit)
- CPU/RGB interface voltage: 1.65 to 3.3 V
- Driver power supply voltage: 3.4 to 5.5 V
- Display RAM: 240 x 18 x 320 bits
- Driver outputs: 720 outputs (Source), 322 outputs (Gate, including 2 dummy)
- CPU interface: Three types of interfaces selectable
  - 6-/16-/18-bit RGB interface (Through mode, capture mode)
  - i80/M68 parallel interface (Selectable from 8-/16-/18-bit)
  - 16-/18-bit serial interface (No reading in serial interface mode)
- Colors: 262,144 colors/pixel
- On-chip timing generator
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD161704AP	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum on product quality, so please contact one of our sales representatives.

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The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

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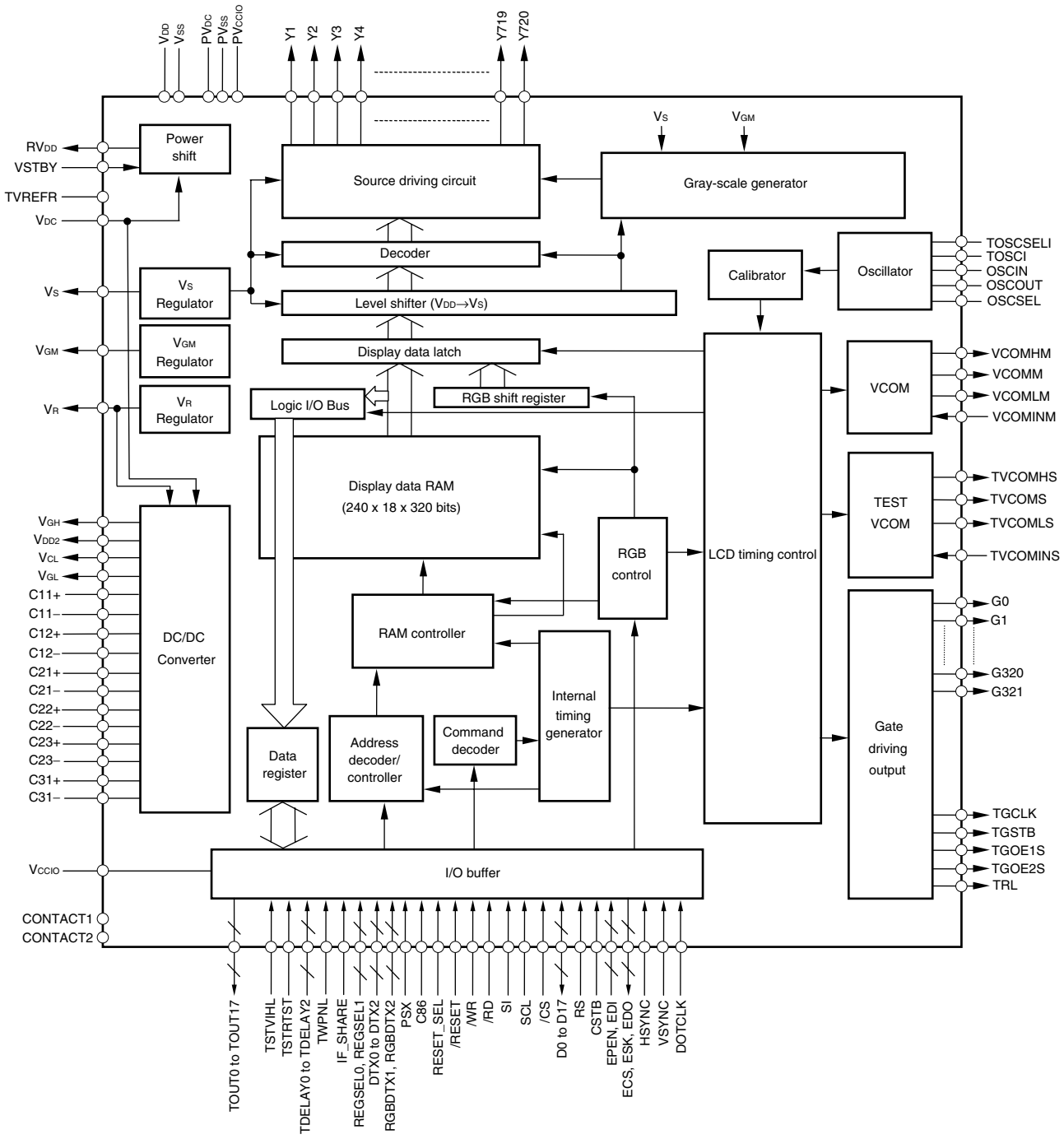
1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Pad Layout)

Chip size: 24.25 x 2.17 mm^2

Output bump size (Type A): 25 x 104 μm^2

Input bump size (Type B): 40 x 125 μm^2

Alignment mark (Mark center, unit: μm)

	X	Y
AM (Cross)	−11675.0	−950.0
AM (Cross)	11675.0	−950.0
AM (Circle)	11949.5	960.0
AM (Circle)	−11949.5	960.0

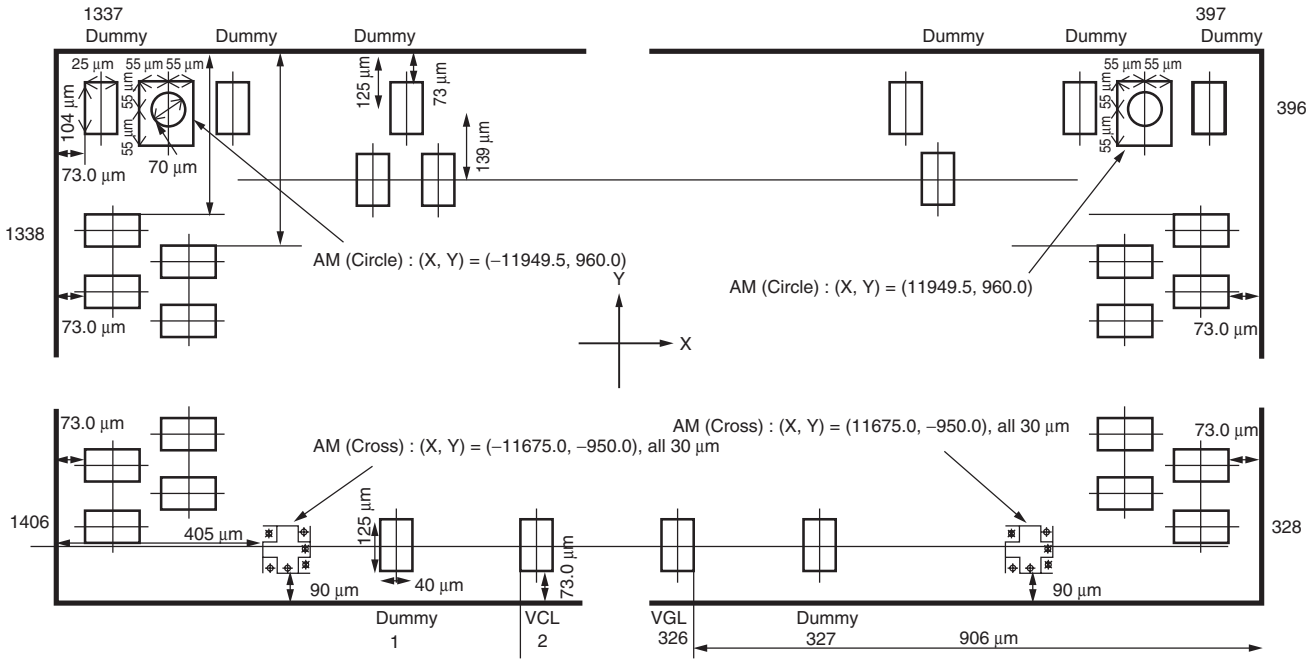


Table 2–1. Pad Coordinate (1/8)

PADTYPE: BUMP SIZE X = 40 um, Y = 125 um				
PAD pitch 70 um			BUMP	
PAD No.	PAD NAME	TYPE	X [um]	Y [um]
-	Alignment Mar	-	-11675.0	-950.0
1	Dummy	B	-11550.0	-949.5
2	VCL	B	-11480.0	-949.5
3	VCL	B	-11410.0	-949.5
4	VCL	B	-11340.0	-949.5
5	VCL	B	-11270.0	-949.5
6	C31-	B	-11200.0	-949.5
7	C31-	B	-11130.0	-949.5
8	C31-	B	-11060.0	-949.5
9	C31-	B	-10990.0	-949.5
10	C31+	B	-10920.0	-949.5
11	C31+	B	-10850.0	-949.5
12	C31+	B	-10780.0	-949.5
13	C31+	B	-10710.0	-949.5
14	C12-	B	-10640.0	-949.5
15	C12-	B	-10570.0	-949.5
16	C12-	B	-10500.0	-949.5
17	C12-	B	-10430.0	-949.5
18	C12-	B	-10360.0	-949.5
19	C12-	B	-10290.0	-949.5
20	C12+	B	-10220.0	-949.5
21	C12+	B	-10150.0	-949.5
22	C12+	B	-10080.0	-949.5
23	C12+	B	-10010.0	-949.5
24	C12+	B	-9940.0	-949.5
25	C12+	B	-9870.0	-949.5
26	C11-	B	-9800.0	-949.5
27	C11-	B	-9730.0	-949.5
28	C11-	B	-9660.0	-949.5
29	C11-	B	-9590.0	-949.5
30	C11-	B	-9520.0	-949.5
31	C11-	B	-9450.0	-949.5
32	C11+	B	-9380.0	-949.5
33	C11+	B	-9310.0	-949.5
34	C11+	B	-9240.0	-949.5
35	C11+	B	-9170.0	-949.5
36	C11+	B	-9100.0	-949.5
37	C11+	B	-9030.0	-949.5
38	VDD2	B	-8960.0	-949.5
39	VDD2	B	-8890.0	-949.5
40	VDD2	B	-8820.0	-949.5
41	VDD2	B	-8750.0	-949.5
42	VDD2	B	-8680.0	-949.5
43	VDD2	B	-8610.0	-949.5
44	VDD2	B	-8540.0	-949.5
45	VDD2	B	-8470.0	-949.5
46	VDD2	B	-8400.0	-949.5
47	VDD2	B	-8330.0	-949.5
48	TVREFR	B	-8260.0	-949.5
49	VGM	B	-8190.0	-949.5
50	VGM	B	-8120.0	-949.5
51	VGM	B	-8050.0	-949.5
52	VGM	B	-7980.0	-949.5
53	VGM	B	-7910.0	-949.5
54	VGM	B	-7840.0	-949.5
55	VS	B	-7770.0	-949.5
56	VS	B	-7700.0	-949.5
57	VS	B	-7630.0	-949.5
58	VS	B	-7560.0	-949.5
59	VS	B	-7490.0	-949.5
60	VS	B	-7420.0	-949.5
61	VR	B	-7350.0	-949.5
62	VR	B	-7280.0	-949.5
63	VR	B	-7210.0	-949.5
64	VR	B	-7140.0	-949.5
65	VR	B	-7070.0	-949.5
66	VCOMM	B	-7000.0	-949.5

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
328	Dummy	A	12000.0	-939.0
329	Dummy	A	11861.0	-914.0
330	Dummy	A	12000.0	-889.0
331	Dummy	A	11861.0	-864.0
332	Dummy	A	12000.0	-839.0
333	Dummy	A	11861.0	-814.0
334	Dummy	A	12000.0	-789.0
335	G161	A	11861.0	-764.0
336	G162	A	12000.0	-739.0
337	G163	A	11861.0	-714.0
338	G164	A	12000.0	-689.0
339	G165	A	11861.0	-664.0
340	G166	A	12000.0	-639.0
341	G167	A	11861.0	-614.0
342	G168	A	12000.0	-589.0
343	G169	A	11861.0	-564.0
344	G170	A	12000.0	-539.0
345	G171	A	11861.0	-514.0
346	G172	A	12000.0	-489.0
347	G173	A	11861.0	-464.0
348	G174	A	12000.0	-439.0
349	G175	A	11861.0	-414.0
350	G176	A	12000.0	-389.0
351	G177	A	11861.0	-364.0
352	G178	A	12000.0	-339.0
353	G179	A	11861.0	-314.0
354	G180	A	12000.0	-289.0
355	G181	A	11861.0	-264.0
356	G182	A	12000.0	-239.0
357	G183	A	11861.0	-214.0
358	G184	A	12000.0	-189.0
359	G185	A	11861.0	-164.0
360	G186	A	12000.0	-139.0
361	G187	A	11861.0	-114.0
362	G188	A	12000.0	-89.0
363	G189	A	11861.0	-64.0
364	G190	A	12000.0	-39.0
365	G191	A	11861.0	-14.0
366	G192	A	12000.0	11.0
367	G193	A	11861.0	36.0
368	G194	A	12000.0	61.0
369	G195	A	11861.0	86.0
370	G196	A	12000.0	111.0
371	G197	A	11861.0	136.0
372	G198	A	12000.0	161.0
373	G199	A	11861.0	186.0
374	G200	A	12000.0	211.0
375	G201	A	11861.0	236.0
376	G202	A	12000.0	261.0
377	G203	A	11861.0	286.0
378	G204	A	12000.0	311.0
379	G205	A	11861.0	336.0
380	G206	A	12000.0	361.0
381	G207	A	11861.0	386.0
382	G208	A	12000.0	411.0
383	G209	A	11861.0	436.0
384	G210	A	12000.0	461.0
385	G211	A	11861.0	486.0
386	G212	A	12000.0	511.0
387	G213	A	11861.0	536.0
388	G214	A	12000.0	561.0
389	G215	A	11861.0	586.0
390	G216	A	12000.0	611.0
391	G217	A	11861.0	636.0
392	G218	A	12000.0	661.0
393	G219	A	11861.0	686.0
394	G220	A	12000.0	711.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
865	Y361	A	50.0	960.0
866	Y362	A	25.0	821.0
867	Y363	A	0.0	960.0
868	Y364	A	-25.0	821.0
869	Y365	A	-50.0	960.0
870	Y366	A	-75.0	821.0
871	Y367	A	-100.0	960.0
872	Y368	A	-125.0	821.0
873	Y369	A	-150.0	960.0
874	Y370	A	-175.0	821.0
875	Y371	A	-200.0	960.0
876	Y372	A	-225.0	821.0
877	Y373	A	-250.0	960.0
878	Y374	A	-275.0	821.0
879	Y375	A	-300.0	960.0
880	Y376	A	-325.0	821.0
881	Y377	A	-350.0	960.0
882	Y378	A	-375.0	821.0
883	Y379	A	-400.0	960.0
884	Y380	A	-425.0	821.0
885	Y381	A	-450.0	960.0
886	Y382	A	-475.0	821.0
887	Y383	A	-500.0	960.0
888	Y384	A	-525.0	821.0
889	Y385	A	-550.0	960.0
890	Y386	A	-575.0	821.0
891	Y387	A	-600.0	960.0
892	Y388	A	-625.0	821.0
893	Y389	A	-650.0	960.0
894	Y390	A	-675.0	821.0
895	Y391	A	-700.0	960.0
896	Y392	A	-725.0	821.0
897	Y393	A	-750.0	960.0
898	Y394	A	-775.0	821.0
899	Y395	A	-800.0	960.0
900	Y396	A	-825.0	821.0
901	Y397	A	-850.0	960.0
902	Y398	A	-875.0	821.0
903	Y399	A	-900.0	960.0
904	Y400	A	-925.0	821.0
905	Y401	A	-950.0	960.0
906	Y402	A	-975.0	821.0
907	Y403	A	-1000.0	960.0
908	Y404	A	-1025.0	821.0
909	Y405	A	-1050.0	960.0
910	Y406	A	-1075.0	821.0
911	Y407	A	-1100.0	960.0
912	Y408	A	-1125.0	821.0
913	Y409	A	-1150.0	960.0
914	Y410	A	-1175.0	821.0
915	Y411	A	-1200.0	960.0
916	Y412	A	-1225.0	821.0
917	Y413	A	-1250.0	960.0
918	Y414	A	-1275.0	821.0
919	Y415	A	-1300.0	960.0
920	Y416	A	-1325.0	821.0
921	Y417	A	-1350.0	960.0
922	Y418	A	-1375.0	821.0
923	Y419	A	-1400.0	960.0
924	Y420	A	-1425.0	821.0
925	Y421	A	-1450.0	960.0
926	Y422	A	-1475.0	821.0
927	Y423	A	-1500.0	960.0
928	Y424	A	-1525.0	821.0
929	Y425	A	-1550.0	960.0
930	Y426	A	-1575.0	821.0
931	Y427	A	-1600.0	960.0

Table 2–1. Pad Coordinate (2/8)

PADTYPE: BUMP SIZE X = 40 um, Y = 125 um				
PAD pitch 70 um			BUMP	
PAD No.	PAD NAME	TYPE	X [um]	Y [um]
67	VCOMM	B	-6930.0	-949.5
68	VCOMM	B	-6860.0	-949.5
69	VCOMM	B	-6790.0	-949.5
70	VCOMM	B	-6720.0	-949.5
71	VCOMM	B	-6650.0	-949.5
72	VCOMM	B	-6580.0	-949.5
73	VCOMM	B	-6510.0	-949.5
74	Dummy	B	-6440.0	-949.5
75	VCOMINM	B	-6370.0	-949.5
76	VCOMHM	B	-6300.0	-949.5
77	VCOMHM	B	-6230.0	-949.5
78	VCOMHM	B	-6160.0	-949.5
79	VCOMHM	B	-6090.0	-949.5
80	VCOMHM	B	-6020.0	-949.5
81	Dummy	B	-5950.0	-949.5
82	Dummy	B	-5880.0	-949.5
83	Dummy	B	-5810.0	-949.5
84	Dummy	B	-5740.0	-949.5
85	Dummy	B	-5670.0	-949.5
86	Dummy	B	-5600.0	-949.5
87	VCOMLM	B	-5530.0	-949.5
88	VCOMLM	B	-5460.0	-949.5
89	VCOMLM	B	-5390.0	-949.5
90	VCOMLM	B	-5320.0	-949.5
91	VCOMLM	B	-5250.0	-949.5
92	Dummy	B	-5180.0	-949.5
93	Dummy	B	-5110.0	-949.5
94	Dummy	B	-5040.0	-949.5
95	Dummy	B	-4970.0	-949.5
96	Dummy	B	-4900.0	-949.5
97	Dummy	B	-4830.0	-949.5
98	Dummy	B	-4760.0	-949.5
99	Dummy	B	-4690.0	-949.5
100	VSS	B	-4620.0	-949.5
101	VSS	B	-4550.0	-949.5
102	VSS	B	-4480.0	-949.5
103	VSS	B	-4410.0	-949.5
104	VSS	B	-4340.0	-949.5
105	VSS	B	-4270.0	-949.5
106	VSS	B	-4200.0	-949.5
107	VSS	B	-4130.0	-949.5
108	VSS	B	-4060.0	-949.5
109	VSS	B	-3990.0	-949.5
110	VSS	B	-3920.0	-949.5
111	VSS	B	-3850.0	-949.5
112	VSS	B	-3780.0	-949.5
113	VSS	B	-3710.0	-949.5
114	VSS	B	-3640.0	-949.5
115	VSS	B	-3570.0	-949.5
116	VSS	B	-3500.0	-949.5
117	VSS	B	-3430.0	-949.5
118	VSS	B	-3360.0	-949.5
119	VSS	B	-3290.0	-949.5
120	VDC	B	-3220.0	-949.5
121	VDC	B	-3150.0	-949.5
122	VDC	B	-3080.0	-949.5
123	VDC	B	-3010.0	-949.5
124	VDC	B	-2940.0	-949.5
125	VDC	B	-2870.0	-949.5
126	VDC	B	-2800.0	-949.5
127	VDC	B	-2730.0	-949.5
128	VDC	B	-2660.0	-949.5
129	VDC	B	-2590.0	-949.5
130	VDC	B	-2520.0	-949.5
131	VDC	B	-2450.0	-949.5
132	VDC	B	-2380.0	-949.5
133	VDC	B	-2310.0	-949.5
134	VDC	B	-2240.0	-949.5
135	VDC	B	-2170.0	-949.5
136	VDCI	B	-2100.0	-949.5
137	VDCI	B	-2030.0	-949.5
138	VDCI	B	-1960.0	-949.5
139	VDCI	B	-1890.0	-949.5

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
395	Dummy	A	11861.0	736.0
396	Dummy	A	12000.0	761.0
397	Dummy	A	12039.5	960.0
-	Alignment Mar	-	11949.5	960.0
398	Dummy	A	11859.5	960.0
399	Dummy	A	11700.0	960.0
400	Dummy	A	11675.0	821.0
401	G221	A	11650.0	960.0
402	G222	A	11625.0	821.0
403	G223	A	11600.0	960.0
404	G224	A	11575.0	821.0
405	G225	A	11550.0	960.0
406	G226	A	11525.0	821.0
407	G227	A	11500.0	960.0
408	G228	A	11475.0	821.0
409	G229	A	11450.0	960.0
410	G230	A	11425.0	821.0
411	G231	A	11400.0	960.0
412	G232	A	11375.0	821.0
413	G233	A	11350.0	960.0
414	G234	A	11325.0	821.0
415	G235	A	11300.0	960.0
416	G236	A	11275.0	821.0
417	G237	A	11250.0	960.0
418	G238	A	11225.0	821.0
419	G239	A	11200.0	960.0
420	G240	A	11175.0	821.0
421	G241	A	11150.0	960.0
422	G242	A	11125.0	821.0
423	G243	A	11100.0	960.0
424	G244	A	11075.0	821.0
425	G245	A	11050.0	960.0
426	G246	A	11025.0	821.0
427	G247	A	11000.0	960.0
428	G248	A	10975.0	821.0
429	G249	A	10950.0	960.0
430	G250	A	10925.0	821.0
431	G251	A	10900.0	960.0
432	G252	A	10875.0	821.0
433	G253	A	10850.0	960.0
434	G254	A	10825.0	821.0
435	G255	A	10800.0	960.0
436	G256	A	10775.0	821.0
437	G257	A	10750.0	960.0
438	G258	A	10725.0	821.0
439	G259	A	10700.0	960.0
440	G260	A	10675.0	821.0
441	G261	A	10650.0	960.0
442	G262	A	10625.0	821.0
443	G263	A	10600.0	960.0
444	G264	A	10575.0	821.0
445	G265	A	10550.0	960.0
446	G266	A	10525.0	821.0
447	G267	A	10500.0	960.0
448	G268	A	10475.0	821.0
449	G269	A	10450.0	960.0
450	G270	A	10425.0	821.0
451	G271	A	10400.0	960.0
452	G272	A	10375.0	821.0
453	G273	A	10350.0	960.0
454	G274	A	10325.0	821.0
455	G275	A	10300.0	960.0
456	G276	A	10275.0	821.0
457	G277	A	10250.0	960.0
458	G278	A	10225.0	821.0
459	G279	A	10200.0	960.0
460	G280	A	10175.0	821.0
461	G281	A	10150.0	960.0
462	G282	A	10125.0	821.0
463	G283	A	10100.0	960.0
464	G284	A	10075.0	821.0
465	G285	A	10050.0	960.0
466	G286	A	10025.0	821.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
932	Y428	A	-1625.0	821.0
933	Y429	A	-1650.0	960.0
934	Y430	A	-1675.0	821.0
935	Y431	A	-1700.0	960.0
936	Y432	A	-1725.0	821.0
937	Y433	A	-1750.0	960.0
938	Y434	A	-1775.0	821.0
939	Y435	A	-1800.0	960.0
940	Y436	A	-1825.0	821.0
941	Y437	A	-1850.0	960.0
942	Y438	A	-1875.0	821.0
943	Y439	A	-1900.0	960.0
944	Y440	A	-1925.0	821.0
945	Y441	A	-1950.0	960.0
946	Y442	A	-1975.0	821.0
947	Y443	A	-2000.0	960.0
948	Y444	A	-2025.0	821.0
949	Y445	A	-2050.0	960.0
950	Y446	A	-2075.0	821.0
951	Y447	A	-2100.0	960.0
952	Y448	A	-2125.0	821.0
953	Y449	A	-2150.0	960.0
954	Y450	A	-2175.0	821.0
955	Y451	A	-2200.0	960.0
956	Y452	A	-2225.0	821.0
957	Y453	A	-2250.0	960.0
958	Y454	A	-2275.0	821.0
959	Y455	A	-2300.0	960.0
960	Y456	A	-2325.0	821.0
961	Y457	A	-2350.0	960.0
962	Y458	A	-2375.0	821.0
963	Y459	A	-2400.0	960.0
964	Y460	A	-2425.0	821.0
965	Y461	A	-2450.0	960.0
966	Y462	A	-2475.0	821.0
967	Y463	A	-2500.0	960.0
968	Y464	A	-2525.0	821.0
969	Y465	A	-2550.0	960.0
970	Y466	A	-2575.0	821.0
971	Y467	A	-2600.0	960.0
972	Y468	A	-2625.0	821.0
973	Y469	A	-2650.0	960.0
974	Y470	A	-2675.0	821.0
975	Y471	A	-2700.0	960.0
976	Y472	A	-2725.0	821.0
977	Y473	A	-2750.0	960.0
978	Y474	A	-2775.0	821.0
979	Y475	A	-2800.0	960.0
980	Y476	A	-2825.0	821.0
981	Y477	A	-2850.0	960.0
982	Y478	A	-2875.0	821.0
983	Y479	A	-2900.0	960.0
984	Y480	A	-2925.0	821.0
985	Y481	A	-2950.0	960.0
986	Y482	A	-2975.0	821.0
987	Y483	A	-3000.0	960.0
988	Y484	A	-3025.0	821.0
989	Y485	A	-3050.0	960.0
990	Y486	A	-3075.0	821.0
991	Y487	A	-3100.0	960.0
992	Y488	A	-3125.0	821.0
993	Y489	A	-3150.0	960.0
994	Y490	A	-3175.0	821.0
995	Y491	A	-3200.0	960.0
996	Y492	A	-3225.0	821.0
997	Y493	A	-3250.0	960.0
998	Y494	A	-3275.0	821.0
999	Y495	A	-3300.0	960.0
1000	Y496	A	-3325.0	821.0
1001	Y497	A	-3350.0	960.0
1002	Y498	A	-3375.0	821.0
1003	Y499	A	-3400.0	960.0
1004	Y500	A	-3425.0	821.0

Table 2–1. Pad Coordinate (3/8)

PADTYPE: BUMP SIZE X = 40 um, Y = 125 um				
PAD pitch 70 um			BUMP	
PAD No.	PAD NAME	TYPE	X [um]	Y [um]
140	VDCI	B	-1820.0	-949.5
141	VDCI	B	-1750.0	-949.5
142	VDCI	B	-1680.0	-949.5
143	VDCI	B	-1610.0	-949.5
144	VDCI	B	-1540.0	-949.5
145	VDCI	B	-1470.0	-949.5
146	RVDD	B	-1400.0	-949.5
147	RVDD	B	-1330.0	-949.5
148	RVDD	B	-1260.0	-949.5
149	RVDD	B	-1190.0	-949.5
150	RVDD	B	-1120.0	-949.5
151	RVDD	B	-1050.0	-949.5
152	VDD	B	-980.0	-949.5
153	VDD	B	-910.0	-949.5
154	VDD	B	-840.0	-949.5
155	VDD	B	-770.0	-949.5
156	VDD	B	-700.0	-949.5
157	VDD	B	-630.0	-949.5
158	TOSCI	B	-560.0	-949.5
159	TOSCSELI	B	-490.0	-949.5
160	OSCIN	B	-420.0	-949.5
161	OSCOUT	B	-350.0	-949.5
162	PVDC	B	-280.0	-949.5
163	OSCSEL	B	-210.0	-949.5
164	PVSS	B	-140.0	-949.5
165	RESET_SEL	B	-70.0	-949.5
166	PVCCIO	B	0.0	-949.5
167	EPEN	B	70.0	-949.5
168	EDI	B	140.0	-949.5
169	ECS	B	210.0	-949.5
170	ESK	B	280.0	-949.5
171	EDO	B	350.0	-949.5
172	CSTB	B	420.0	-949.5
173	D0	B	490.0	-949.5
174	TOUT0	B	560.0	-949.5
175	D1	B	630.0	-949.5
176	TOUT1	B	700.0	-949.5
177	D2	B	770.0	-949.5
178	TOUT2	B	840.0	-949.5
179	D3	B	910.0	-949.5
180	TOUT3	B	980.0	-949.5
181	D4	B	1050.0	-949.5
182	TOUT4	B	1120.0	-949.5
183	D5	B	1190.0	-949.5
184	TOUT5	B	1260.0	-949.5
185	D6	B	1330.0	-949.5
186	TOUT6	B	1400.0	-949.5
187	D7	B	1470.0	-949.5
188	TOUT7	B	1540.0	-949.5
189	D8	B	1610.0	-949.5
190	TOUT8	B	1680.0	-949.5
191	D9	B	1750.0	-949.5
192	TOUT9	B	1820.0	-949.5
193	D10	B	1890.0	-949.5
194	TOUT10	B	1960.0	-949.5
195	D11	B	2030.0	-949.5
196	TOUT11	B	2100.0	-949.5
197	D12	B	2170.0	-949.5
198	TOUT12	B	2240.0	-949.5
199	D13	B	2310.0	-949.5
200	TOUT13	B	2380.0	-949.5
201	D14	B	2450.0	-949.5
202	TOUT14	B	2520.0	-949.5
203	D15	B	2590.0	-949.5
204	TOUT15	B	2660.0	-949.5
205	D16	B	2730.0	-949.5
206	TOUT16	B	2800.0	-949.5
207	D17	B	2870.0	-949.5
208	TOUT17	B	2940.0	-949.5

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
467	G287	A	10000.0	960.0
468	G288	A	9975.0	821.0
469	G289	A	9950.0	960.0
470	G290	A	9925.0	821.0
471	G291	A	9900.0	960.0
472	G292	A	9875.0	821.0
473	G293	A	9850.0	960.0
474	G294	A	9825.0	821.0
475	G295	A	9800.0	960.0
476	G296	A	9775.0	821.0
477	G297	A	9750.0	960.0
478	G298	A	9725.0	821.0
479	G299	A	9700.0	960.0
480	G300	A	9675.0	821.0
481	G301	A	9650.0	960.0
482	G302	A	9625.0	821.0
483	G303	A	9600.0	960.0
484	G304	A	9575.0	821.0
485	G305	A	9550.0	960.0
486	G306	A	9525.0	821.0
487	G307	A	9500.0	960.0
488	G308	A	9475.0	821.0
489	G309	A	9450.0	960.0
490	G310	A	9425.0	821.0
491	G311	A	9400.0	960.0
492	G312	A	9375.0	821.0
493	G313	A	9350.0	960.0
494	G314	A	9325.0	821.0
495	G315	A	9300.0	960.0
496	G316	A	9275.0	821.0
497	G317	A	9250.0	960.0
498	G318	A	9225.0	821.0
499	G319	A	9200.0	960.0
500	G320	A	9175.0	821.0
501	G321	A	9150.0	960.0
502	Dummy	A	9125.0	821.0
503	Dummy	A	9100.0	960.0
504	Y1	A	9075.0	821.0
505	Y2	A	9050.0	960.0
506	Y3	A	9025.0	821.0
507	Y4	A	9000.0	960.0
508	Y5	A	8975.0	821.0
509	Y6	A	8950.0	960.0
510	Y7	A	8925.0	821.0
511	Y8	A	8900.0	960.0
512	Y9	A	8875.0	821.0
513	Y10	A	8850.0	960.0
514	Y11	A	8825.0	821.0
515	Y12	A	8800.0	960.0
516	Y13	A	8775.0	821.0
517	Y14	A	8750.0	960.0
518	Y15	A	8725.0	821.0
519	Y16	A	8700.0	960.0
520	Y17	A	8675.0	821.0
521	Y18	A	8650.0	960.0
522	Y19	A	8625.0	821.0
523	Y20	A	8600.0	960.0
524	Y21	A	8575.0	821.0
525	Y22	A	8550.0	960.0
526	Y23	A	8525.0	821.0
527	Y24	A	8500.0	960.0
528	Y25	A	8475.0	821.0
529	Y26	A	8450.0	960.0
530	Y27	A	8425.0	821.0
531	Y28	A	8400.0	960.0
532	Y29	A	8375.0	821.0
533	Y30	A	8350.0	960.0
534	Y31	A	8325.0	821.0
535	Y32	A	8300.0	960.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
1005	Y501	A	-3450.0	960.0
1006	Y502	A	-3475.0	821.0
1007	Y503	A	-3500.0	960.0
1008	Y504	A	-3525.0	821.0
1009	Y505	A	-3550.0	960.0
1010	Y506	A	-3575.0	821.0
1011	Y507	A	-3600.0	960.0
1012	Y508	A	-3625.0	821.0
1013	Y509	A	-3650.0	960.0
1014	Y510	A	-3675.0	821.0
1015	Y511	A	-3700.0	960.0
1016	Y512	A	-3725.0	821.0
1017	Y513	A	-3750.0	960.0
1018	Y514	A	-3775.0	821.0
1019	Y515	A	-3800.0	960.0
1020	Y516	A	-3825.0	821.0
1021	Y517	A	-3850.0	960.0
1022	Y518	A	-3875.0	821.0
1023	Y519	A	-3900.0	960.0
1024	Y520	A	-3925.0	821.0
1025	Y521	A	-3950.0	960.0
1026	Y522	A	-3975.0	821.0
1027	Y523	A	-4000.0	960.0
1028	Y524	A	-4025.0	821.0
1029	Y525	A	-4050.0	960.0
1030	Y526	A	-4075.0	821.0
1031	Y527	A	-4100.0	960.0
1032	Y528	A	-4125.0	821.0
1033	Y529	A	-4150.0	960.0
1034	Y530	A	-4175.0	821.0
1035	Y531	A	-4200.0	960.0
1036	Y532	A	-4225.0	821.0
1037	Y533	A	-4250.0	960.0
1038	Y534	A	-4275.0	821.0
1039	Y535	A	-4300.0	960.0
1040	Y536	A	-4325.0	821.0
1041	Y537	A	-4350.0	960.0
1042	Y538	A	-4375.0	821.0
1043	Y539	A	-4400.0	960.0
1044	Y540	A	-4425.0	821.0
1045	Y541	A	-4450.0	960.0
1046	Y542	A	-4475.0	821.0
1047	Y543	A	-4500.0	960.0
1048	Y544	A	-4525.0	821.0
1049	Y545	A	-4550.0	960.0
1050	Y546	A	-4575.0	821.0
1051	Y547	A	-4600.0	960.0
1052	Y548	A	-4625.0	821.0
1053	Y549	A	-4650.0	960.0
1054	Y550	A	-4675.0	821.0
1055	Y551	A	-4700.0	960.0
1056	Y552	A	-4725.0	821.0
1057	Y553	A	-4750.0	960.0
1058	Y554	A	-4775.0	821.0
1059	Y555	A	-4800.0	960.0
1060	Y556	A	-4825.0	821.0
1061	Y557	A	-4850.0	960.0
1062	Y558	A	-4875.0	821.0
1063	Y559	A	-4900.0	960.0
1064	Y560	A	-4925.0	821.0
1065	Y561	A	-4950.0	960.0
1066	Y562	A	-4975.0	821.0
1067	Y563	A	-5000.0	960.0
1068	Y564	A	-5025.0	821.0
1069	Y565	A	-5050.0	960.0
1070	Y566	A	-5075.0	821.0
1071	Y567	A	-5100.0	960.0
1072	Y568	A	-5125.0	821.0
1073	Y569	A	-5150.0	960.0

Table 2–1. Pad Coordinate (4/8)

PADTYPE: BUMP SIZE X = 40 um, Y = 125 um				
PAD pitch 70 um			BUMP	
PAD No.	PAD NAME	TYPE	X [um]	Y [um]
209	PVSS	B	3010.0	-949.5
210	TGOE1S	B	3080.0	-949.5
211	TGOE2S	B	3150.0	-949.5
212	TGCLK	B	3220.0	-949.5
213	TGSTB	B	3290.0	-949.5
214	TRL	B	3360.0	-949.5
215	PVSS	B	3430.0	-949.5
216	SI	B	3500.0	-949.5
217	PVCCIO	B	3570.0	-949.5
218	SCL	B	3640.0	-949.5
219	TDELAY0	B	3710.0	-949.5
220	CS	B	3780.0	-949.5
221	TDELAY1	B	3850.0	-949.5
222	RESET	B	3920.0	-949.5
223	TDELAY2	B	3990.0	-949.5
224	RS	B	4060.0	-949.5
225	TSTVIHL	B	4130.0	-949.5
226	WR	B	4200.0	-949.5
227	TSTRTST	B	4270.0	-949.5
228	RD	B	4340.0	-949.5
229	VSYNC	B	4410.0	-949.5
230	HSYNC	B	4480.0	-949.5
231	DOTCLK	B	4550.0	-949.5
232	PSX	B	4620.0	-949.5
233	PVCCIO	B	4690.0	-949.5
234	REGSEL0	B	4760.0	-949.5
235	REGSEL1	B	4830.0	-949.5
236	C86	B	4900.0	-949.5
237	DTX1	B	4970.0	-949.5
238	PVCCIO	B	5040.0	-949.5
239	DTX2	B	5110.0	-949.5
240	RGB_DTX2	B	5180.0	-949.5
241	DTX0	B	5250.0	-949.5
242	RGB_DTX1	B	5320.0	-949.5
243	PVCCIO	B	5390.0	-949.5
244	TWPNL	B	5460.0	-949.5
245	IF_SHARE	B	5530.0	-949.5
246	PVSS	B	5600.0	-949.5
247	VSTBY	B	5670.0	-949.5
248	VCCIO	B	5740.0	-949.5
249	VCCIO	B	5810.0	-949.5
250	VCCIO	B	5880.0	-949.5
251	VCCIO	B	5950.0	-949.5
252	VCCIO	B	6020.0	-949.5
253	PVDC	B	6090.0	-949.5
254	CONTACT1	B	6160.0	-949.5
255	CONTACT2	B	6230.0	-949.5
256	Dummy	B	6300.0	-949.5
257	Dummy	B	6370.0	-949.5
258	Dummy	B	6440.0	-949.5
259	Dummy	B	6510.0	-949.5
260	Dummy	B	6580.0	-949.5
261	Dummy	B	6650.0	-949.5
262	Dummy	B	6720.0	-949.5
263	Dummy	B	6790.0	-949.5
264	Dummy	B	6860.0	-949.5
265	Dummy	B	6930.0	-949.5
266	Dummy	B	7000.0	-949.5
267	Dummy	B	7070.0	-949.5
268	Dummy	B	7140.0	-949.5
269	Dummy	B	7210.0	-949.5
270	Dummy	B	7280.0	-949.5
271	Dummy	B	7350.0	-949.5
272	Dummy	B	7420.0	-949.5
273	Dummy	B	7490.0	-949.5
274	Dummy	B	7560.0	-949.5
275	Dummy	B	7630.0	-949.5

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
536	Y33	A	8275.0	821.0
537	Y34	A	8250.0	960.0
538	Y35	A	8225.0	821.0
539	Y36	A	8200.0	960.0
540	Y37	A	8175.0	821.0
541	Y38	A	8150.0	960.0
542	Y39	A	8125.0	821.0
543	Y40	A	8100.0	960.0
544	Y41	A	8075.0	821.0
545	Y42	A	8050.0	960.0
546	Y43	A	8025.0	821.0
547	Y44	A	8000.0	960.0
548	Y45	A	7975.0	821.0
549	Y46	A	7950.0	960.0
550	Y47	A	7925.0	821.0
551	Y48	A	7900.0	960.0
552	Y49	A	7875.0	821.0
553	Y50	A	7850.0	960.0
554	Y51	A	7825.0	821.0
555	Y52	A	7800.0	960.0
556	Y53	A	7775.0	821.0
557	Y54	A	7750.0	960.0
558	Y55	A	7725.0	821.0
559	Y56	A	7700.0	960.0
560	Y57	A	7675.0	821.0
561	Y58	A	7650.0	960.0
562	Y59	A	7625.0	821.0
563	Y60	A	7600.0	960.0
564	Y61	A	7575.0	821.0
565	Y62	A	7550.0	960.0
566	Y63	A	7525.0	821.0
567	Y64	A	7500.0	960.0
568	Y65	A	7475.0	821.0
569	Y66	A	7450.0	960.0
570	Y67	A	7425.0	821.0
571	Y68	A	7400.0	960.0
572	Y69	A	7375.0	821.0
573	Y70	A	7350.0	960.0
574	Y71	A	7325.0	821.0
575	Y72	A	7300.0	960.0
576	Y73	A	7275.0	821.0
577	Y74	A	7250.0	960.0
578	Y75	A	7225.0	821.0
579	Y76	A	7200.0	960.0
580	Y77	A	7175.0	821.0
581	Y78	A	7150.0	960.0
582	Y79	A	7125.0	821.0
583	Y80	A	7100.0	960.0
584	Y81	A	7075.0	821.0
585	Y82	A	7050.0	960.0
586	Y83	A	7025.0	821.0
587	Y84	A	7000.0	960.0
588	Y85	A	6975.0	821.0
589	Y86	A	6950.0	960.0
590	Y87	A	6925.0	821.0
591	Y88	A	6900.0	960.0
592	Y89	A	6875.0	821.0
593	Y90	A	6850.0	960.0
594	Y91	A	6825.0	821.0
595	Y92	A	6800.0	960.0
596	Y93	A	6775.0	821.0
597	Y94	A	6750.0	960.0
598	Y95	A	6725.0	821.0
599	Y96	A	6700.0	960.0
600	Y97	A	6675.0	821.0
601	Y98	A	6650.0	960.0
602	Y99	A	6625.0	821.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
1074	Y570	A	-5175.0	821.0
1075	Y571	A	-5200.0	960.0
1076	Y572	A	-5225.0	821.0
1077	Y573	A	-5250.0	960.0
1078	Y574	A	-5275.0	821.0
1079	Y575	A	-5300.0	960.0
1080	Y576	A	-5325.0	821.0
1081	Y577	A	-5350.0	960.0
1082	Y578	A	-5375.0	821.0
1083	Y579	A	-5400.0	960.0
1084	Y580	A	-5425.0	821.0
1085	Y581	A	-5450.0	960.0
1086	Y582	A	-5475.0	821.0
1087	Y583	A	-5500.0	960.0
1088	Y584	A	-5525.0	821.0
1089	Y585	A	-5550.0	960.0
1090	Y586	A	-5575.0	821.0
1091	Y587	A	-5600.0	960.0
1092	Y588	A	-5625.0	821.0
1093	Y589	A	-5650.0	960.0
1094	Y590	A	-5675.0	821.0
1095	Y591	A	-5700.0	960.0
1096	Y592	A	-5725.0	821.0
1097	Y593	A	-5750.0	960.0
1098	Y594	A	-5775.0	821.0
1099	Y595	A	-5800.0	960.0
1100	Y596	A	-5825.0	821.0
1101	Y597	A	-5850.0	960.0
1102	Y598	A	-5875.0	821.0
1103	Y599	A	-5900.0	960.0
1104	Y500	A	-5925.0	821.0
1105	Y601	A	-5950.0	960.0
1106	Y602	A	-5975.0	821.0
1107	Y603	A	-6000.0	960.0
1108	Y604	A	-6025.0	821.0
1109	Y605	A	-6050.0	960.0
1110	Y606	A	-6075.0	821.0
1111	Y607	A	-6100.0	960.0
1112	Y608	A	-6125.0	821.0
1113	Y609	A	-6150.0	960.0
1114	Y610	A	-6175.0	821.0
1115	Y611	A	-6200.0	960.0
1116	Y612	A	-6225.0	821.0
1117	Y613	A	-6250.0	960.0
1118	Y614	A	-6275.0	821.0
1119	Y615	A	-6300.0	960.0
1120	Y616	A	-6325.0	821.0
1121	Y617	A	-6350.0	960.0
1122	Y618	A	-6375.0	821.0
1123	Y619	A	-6400.0	960.0
1124	Y620	A	-6425.0	821.0
1125	Y621	A	-6450.0	960.0
1126	Y622	A	-6475.0	821.0
1127	Y623	A	-6500.0	960.0
1128	Y624	A	-6525.0	821.0
1129	Y625	A	-6550.0	960.0
1130	Y626	A	-6575.0	821.0
1131	Y627	A	-6600.0	960.0
1132	Y628	A	-6625.0	821.0
1133	Y629	A	-6650.0	960.0
1134	Y630	A	-6675.0	821.0
1135	Y631	A	-6700.0	960.0
1136	Y632	A	-6725.0	821.0
1137	Y633	A	-6750.0	960.0
1138	Y634	A	-6775.0	821.0
1139	Y635	A	-6800.0	960.0
1140	Y636	A	-6825.0	821.0

Table 2–1. Pad Coordinate (5/8)

PADTYPE: BUMP SIZE X = 40 um, Y = 125 um				
PAD pitch 70 um			BUMP	
PAD No.	PAD NAME	TYPE	X [um]	Y [um]
276	Dummy	B	7700.0	-949.5
277	Dummy	B	7770.0	-949.5
278	Dummy	B	7840.0	-949.5
279	Dummy	B	7910.0	-949.5
280	Dummy	B	7980.0	-949.5
281	Dummy	B	8050.0	-949.5
282	Dummy	B	8120.0	-949.5
283	Dummy	B	8190.0	-949.5
284	Dummy	B	8260.0	-949.5
285	Dummy	B	8330.0	-949.5
286	Dummy	B	8400.0	-949.5
287	Dummy	B	8470.0	-949.5
288	Dummy	B	8540.0	-949.5
289	Dummy	B	8610.0	-949.5
290	CONTACT3	B	8680.0	-949.5
291	CONTACT4	B	8750.0	-949.5
292	VGH	B	8820.0	-949.5
293	VGH	B	8890.0	-949.5
294	VGH	B	8960.0	-949.5
295	VGH	B	9030.0	-949.5
296	VGH	B	9100.0	-949.5
297	VGH	B	9170.0	-949.5
298	VGH	B	9240.0	-949.5
299	C21+	B	9310.0	-949.5
300	C21+	B	9380.0	-949.5
301	C21+	B	9450.0	-949.5
302	C21-	B	9520.0	-949.5
303	C21-	B	9590.0	-949.5
304	C21-	B	9660.0	-949.5
305	C22+	B	9730.0	-949.5
306	C22+	B	9800.0	-949.5
307	C22+	B	9870.0	-949.5
308	C22-	B	9940.0	-949.5
309	C22-	B	10010.0	-949.5
310	C22-	B	10080.0	-949.5
311	C23+	B	10150.0	-949.5
312	C23+	B	10220.0	-949.5
313	C23+	B	10290.0	-949.5
314	C23-	B	10360.0	-949.5
315	C23-	B	10430.0	-949.5
316	C23-	B	10500.0	-949.5
317	VGL	B	10570.0	-949.5
318	VGL	B	10640.0	-949.5
319	VGL	B	10710.0	-949.5
320	VGL	B	10780.0	-949.5
321	VGL	B	10850.0	-949.5
322	VGL	B	10920.0	-949.5
323	VGL	B	10990.0	-949.5
324	VGL	B	11060.0	-949.5
325	VGL	B	11130.0	-949.5
326	VGL	B	11200.0	-949.5
327	Dummy	B	11270.0	-949.5
-	**Alignment Mar**	-	11675.0	-950.0

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
603	Y100	A	6600.0	960.0
604	Y101	A	6575.0	821.0
605	Y102	A	6550.0	960.0
606	Y103	A	6525.0	821.0
607	Y104	A	6500.0	960.0
608	Y105	A	6475.0	821.0
609	Y106	A	6450.0	960.0
610	Y107	A	6425.0	821.0
611	Y108	A	6400.0	960.0
612	Y109	A	6375.0	821.0
613	Y110	A	6350.0	960.0
614	Y111	A	6325.0	821.0
615	Y112	A	6300.0	960.0
616	Y113	A	6275.0	821.0
617	Y114	A	6250.0	960.0
618	Y115	A	6225.0	821.0
619	Y116	A	6200.0	960.0
620	Y117	A	6175.0	821.0
621	Y118	A	6150.0	960.0
622	Y119	A	6125.0	821.0
623	Y120	A	6100.0	960.0
624	Y121	A	6075.0	821.0
625	Y122	A	6050.0	960.0
626	Y123	A	6025.0	821.0
627	Y124	A	6000.0	960.0
628	Y125	A	5975.0	821.0
629	Y126	A	5950.0	960.0
630	Y127	A	5925.0	821.0
631	Y128	A	5900.0	960.0
632	Y129	A	5875.0	821.0
633	Y130	A	5850.0	960.0
634	Y131	A	5825.0	821.0
635	Y132	A	5800.0	960.0
636	Y133	A	5775.0	821.0
637	Y134	A	5750.0	960.0
638	Y135	A	5725.0	821.0
639	Y136	A	5700.0	960.0
640	Y137	A	5675.0	821.0
641	Y138	A	5650.0	960.0
642	Y139	A	5625.0	821.0
643	Y140	A	5600.0	960.0
644	Y141	A	5575.0	821.0
645	Y142	A	5550.0	960.0
646	Y143	A	5525.0	821.0
647	Y144	A	5500.0	960.0
648	Y145	A	5475.0	821.0
649	Y146	A	5450.0	960.0
650	Y147	A	5425.0	821.0
651	Y148	A	5400.0	960.0
652	Y149	A	5375.0	821.0
653	Y150	A	5350.0	960.0
654	Y151	A	5325.0	821.0
655	Y152	A	5300.0	960.0
656	Y153	A	5275.0	821.0
657	Y154	A	5250.0	960.0
658	Y155	A	5225.0	821.0
659	Y156	A	5200.0	960.0
660	Y157	A	5175.0	821.0
661	Y158	A	5150.0	960.0
662	Y159	A	5125.0	821.0
663	Y160	A	5100.0	960.0
664	Y161	A	5075.0	821.0
665	Y162	A	5050.0	960.0
666	Y163	A	5025.0	821.0
667	Y164	A	5000.0	960.0
668	Y165	A	4975.0	821.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
1141	Y637	A	-6850.0	960.0
1142	Y638	A	-6875.0	821.0
1143	Y639	A	-6900.0	960.0
1144	Y640	A	-6925.0	821.0
1145	Y641	A	-6950.0	960.0
1146	Y642	A	-6975.0	821.0
1147	Y643	A	-7000.0	960.0
1148	Y644	A	-7025.0	821.0
1149	Y645	A	-7050.0	960.0
1150	Y646	A	-7075.0	821.0
1151	Y647	A	-7100.0	960.0
1152	Y648	A	-7125.0	821.0
1153	Y649	A	-7150.0	960.0
1154	Y650	A	-7175.0	821.0
1155	Y651	A	-7200.0	960.0
1156	Y652	A	-7225.0	821.0
1157	Y653	A	-7250.0	960.0
1158	Y654	A	-7275.0	821.0
1159	Y655	A	-7300.0	960.0
1160	Y656	A	-7325.0	821.0
1161	Y657	A	-7350.0	960.0
1162	Y658	A	-7375.0	821.0
1163	Y659	A	-7400.0	960.0
1164	Y660	A	-7425.0	821.0
1165	Y661	A	-7450.0	960.0
1166	Y662	A	-7475.0	821.0
1167	Y663	A	-7500.0	960.0
1168	Y664	A	-7525.0	821.0
1169	Y665	A	-7550.0	960.0
1170	Y666	A	-7575.0	821.0
1171	Y667	A	-7600.0	960.0
1172	Y668	A	-7625.0	821.0
1173	Y669	A	-7650.0	960.0
1174	Y670	A	-7675.0	821.0
1175	Y671	A	-7700.0	960.0
1176	Y672	A	-7725.0	821.0
1177	Y673	A	-7750.0	960.0
1178	Y674	A	-7775.0	821.0
1179	Y675	A	-7800.0	960.0
1180	Y676	A	-7825.0	821.0
1181	Y677	A	-7850.0	960.0
1182	Y678	A	-7875.0	821.0
1183	Y679	A	-7900.0	960.0
1184	Y680	A	-7925.0	821.0
1185	Y681	A	-7950.0	960.0
1186	Y682	A	-7975.0	821.0
1187	Y683	A	-8000.0	960.0
1188	Y684	A	-8025.0	821.0
1189	Y685	A	-8050.0	960.0
1190	Y686	A	-8075.0	821.0
1191	Y687	A	-8100.0	960.0
1192	Y688	A	-8125.0	821.0
1193	Y689	A	-8150.0	960.0
1194	Y690	A	-8175.0	821.0
1195	Y691	A	-8200.0	960.0
1196	Y692	A	-8225.0	821.0
1197	Y693	A	-8250.0	960.0
1198	Y694	A	-8275.0	821.0
1199	Y695	A	-8300.0	960.0
1200	Y696	A	-8325.0	821.0
1201	Y697	A	-8350.0	960.0
1202	Y698	A	-8375.0	821.0
1203	Y699	A	-8400.0	960.0
1204	Y700	A	-8425.0	821.0
1205	Y701	A	-8450.0	960.0
1206	Y702	A	-8475.0	821.0

Table 2–1. Pad Coordinate (6/8)

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
669	Y166	A	4950.0	960.0
670	Y167	A	4925.0	821.0
671	Y168	A	4900.0	960.0
672	Y169	A	4875.0	821.0
673	Y170	A	4850.0	960.0
674	Y171	A	4825.0	821.0
675	Y172	A	4800.0	960.0
676	Y173	A	4775.0	821.0
677	Y174	A	4750.0	960.0
678	Y175	A	4725.0	821.0
679	Y176	A	4700.0	960.0
680	Y177	A	4675.0	821.0
681	Y178	A	4650.0	960.0
682	Y179	A	4625.0	821.0
683	Y180	A	4600.0	960.0
684	Y181	A	4575.0	821.0
685	Y182	A	4550.0	960.0
686	Y183	A	4525.0	821.0
687	Y184	A	4500.0	960.0
688	Y185	A	4475.0	821.0
689	Y186	A	4450.0	960.0
690	Y187	A	4425.0	821.0
691	Y188	A	4400.0	960.0
692	Y189	A	4375.0	821.0
693	Y190	A	4350.0	960.0
694	Y191	A	4325.0	821.0
695	Y192	A	4300.0	960.0
696	Y193	A	4275.0	821.0
697	Y194	A	4250.0	960.0
698	Y195	A	4225.0	821.0
699	Y196	A	4200.0	960.0
700	Y197	A	4175.0	821.0
701	Y198	A	4150.0	960.0
702	Y199	A	4125.0	821.0
703	Y200	A	4100.0	960.0
704	Y201	A	4075.0	821.0
705	Y202	A	4050.0	960.0
706	Y203	A	4025.0	821.0
707	Y204	A	4000.0	960.0
708	Y205	A	3975.0	821.0
709	Y206	A	3950.0	960.0
710	Y207	A	3925.0	821.0
711	Y208	A	3900.0	960.0
712	Y209	A	3875.0	821.0
713	Y210	A	3850.0	960.0
714	Y211	A	3825.0	821.0
715	Y212	A	3800.0	960.0
716	Y213	A	3775.0	821.0
717	Y214	A	3750.0	960.0
718	Y215	A	3725.0	821.0
719	Y216	A	3700.0	960.0
720	Y217	A	3675.0	821.0
721	Y218	A	3650.0	960.0
722	Y219	A	3625.0	821.0
723	Y220	A	3600.0	960.0
724	Y221	A	3575.0	821.0
725	Y222	A	3550.0	960.0
726	Y223	A	3525.0	821.0
727	Y224	A	3500.0	960.0
728	Y225	A	3475.0	821.0
729	Y226	A	3450.0	960.0
730	Y227	A	3425.0	821.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
1207	Y703	A	-8500.0	960.0
1208	Y704	A	-8525.0	821.0
1209	Y705	A	-8550.0	960.0
1210	Y706	A	-8575.0	821.0
1211	Y707	A	-8600.0	960.0
1212	Y708	A	-8625.0	821.0
1213	Y709	A	-8650.0	960.0
1214	Y710	A	-8675.0	821.0
1215	Y711	A	-8700.0	960.0
1216	Y712	A	-8725.0	821.0
1217	Y713	A	-8750.0	960.0
1218	Y714	A	-8775.0	821.0
1219	Y715	A	-8800.0	960.0
1220	Y716	A	-8825.0	821.0
1221	Y717	A	-8850.0	960.0
1222	Y718	A	-8875.0	821.0
1223	Y719	A	-8900.0	960.0
1224	Y720	A	-8925.0	821.0
1225	Dummy	A	-8950.0	960.0
1226	Dummy	A	-8975.0	821.0
1227	Dummy	A	-9000.0	960.0
1228	Dummy	A	-9025.0	821.0
1229	Dummy	A	-9050.0	960.0
1230	Dummy	A	-9075.0	821.0
1231	Dummy	A	-9100.0	960.0
1232	Dummy	A	-9125.0	821.0
1233	G160	A	-9150.0	960.0
1234	G159	A	-9175.0	821.0
1235	G158	A	-9200.0	960.0
1236	G157	A	-9225.0	821.0
1237	G156	A	-9250.0	960.0
1238	G155	A	-9275.0	821.0
1239	G154	A	-9300.0	960.0
1240	G153	A	-9325.0	821.0
1241	G152	A	-9350.0	960.0
1242	G151	A	-9375.0	821.0
1243	G150	A	-9400.0	960.0
1244	G149	A	-9425.0	821.0
1245	G148	A	-9450.0	960.0
1246	G147	A	-9475.0	821.0
1247	G146	A	-9500.0	960.0
1248	G145	A	-9525.0	821.0
1249	G144	A	-9550.0	960.0
1250	G143	A	-9575.0	821.0
1251	G142	A	-9600.0	960.0
1252	G141	A	-9625.0	821.0
1253	G140	A	-9650.0	960.0
1254	G139	A	-9675.0	821.0
1255	G138	A	-9700.0	960.0
1256	G137	A	-9725.0	821.0
1257	G136	A	-9750.0	960.0
1258	G135	A	-9775.0	821.0
1259	G134	A	-9800.0	960.0
1260	G133	A	-9825.0	821.0
1261	G132	A	-9850.0	960.0
1262	G131	A	-9875.0	821.0
1263	G130	A	-9900.0	960.0
1264	G129	A	-9925.0	821.0
1265	G128	A	-9950.0	960.0
1266	G127	A	-9975.0	821.0
1267	G126	A	-10000.0	960.0
1268	G125	A	-10025.0	821.0

Table 2–1. Pad Coordinate (7/8)

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
731	Y228	A	3400.0	960.0
732	Y229	A	3375.0	821.0
733	Y230	A	3350.0	960.0
734	Y231	A	3325.0	821.0
735	Y232	A	3300.0	960.0
736	Y233	A	3275.0	821.0
737	Y234	A	3250.0	960.0
738	Y235	A	3225.0	821.0
739	Y236	A	3200.0	960.0
740	Y237	A	3175.0	821.0
741	Y238	A	3150.0	960.0
742	Y239	A	3125.0	821.0
743	Y240	A	3100.0	960.0
744	Y241	A	3075.0	821.0
745	Y242	A	3050.0	960.0
746	Y243	A	3025.0	821.0
747	Y244	A	3000.0	960.0
748	Y245	A	2975.0	821.0
749	Y246	A	2950.0	960.0
750	Y247	A	2925.0	821.0
751	Y248	A	2900.0	960.0
752	Y249	A	2875.0	821.0
753	Y250	A	2850.0	960.0
754	Y251	A	2825.0	821.0
755	Y252	A	2800.0	960.0
756	Y253	A	2775.0	821.0
757	Y254	A	2750.0	960.0
758	Y255	A	2725.0	821.0
759	Y256	A	2700.0	960.0
760	Y257	A	2675.0	821.0
761	Y258	A	2650.0	960.0
762	Y259	A	2625.0	821.0
763	Y260	A	2600.0	960.0
764	Y261	A	2575.0	821.0
765	Y262	A	2550.0	960.0
766	Y263	A	2525.0	821.0
767	Y264	A	2500.0	960.0
768	Y265	A	2475.0	821.0
769	Y266	A	2450.0	960.0
770	Y267	A	2425.0	821.0
771	Y268	A	2400.0	960.0
772	Y269	A	2375.0	821.0
773	Y270	A	2350.0	960.0
774	Y271	A	2325.0	821.0
775	Y272	A	2300.0	960.0
776	Y273	A	2275.0	821.0
777	Y274	A	2250.0	960.0
778	Y275	A	2225.0	821.0
779	Y276	A	2200.0	960.0
780	Y277	A	2175.0	821.0
781	Y278	A	2150.0	960.0
782	Y279	A	2125.0	821.0
783	Y280	A	2100.0	960.0
784	Y281	A	2075.0	821.0
785	Y282	A	2050.0	960.0
786	Y283	A	2025.0	821.0
787	Y284	A	2000.0	960.0
788	Y285	A	1975.0	821.0
789	Y286	A	1950.0	960.0
790	Y287	A	1925.0	821.0
791	Y288	A	1900.0	960.0
792	Y289	A	1875.0	821.0
793	Y290	A	1850.0	960.0
794	Y291	A	1825.0	821.0
795	Y292	A	1800.0	960.0
796	Y293	A	1775.0	821.0
797	Y294	A	1750.0	960.0
798	Y295	A	1725.0	821.0
799	Y296	A	1700.0	960.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
1269	G124	A	-10050.0	960.0
1270	G123	A	-10075.0	821.0
1271	G122	A	-10100.0	960.0
1272	G121	A	-10125.0	821.0
1273	G120	A	-10150.0	960.0
1274	G119	A	-10175.0	821.0
1275	G118	A	-10200.0	960.0
1276	G117	A	-10225.0	821.0
1277	G116	A	-10250.0	960.0
1278	G115	A	-10275.0	821.0
1279	G114	A	-10300.0	960.0
1280	G113	A	-10325.0	821.0
1281	G112	A	-10350.0	960.0
1282	G111	A	-10375.0	821.0
1283	G110	A	-10400.0	960.0
1284	G109	A	-10425.0	821.0
1285	G108	A	-10450.0	960.0
1286	G107	A	-10475.0	821.0
1287	G106	A	-10500.0	960.0
1288	G105	A	-10525.0	821.0
1289	G104	A	-10550.0	960.0
1290	G103	A	-10575.0	821.0
1291	G102	A	-10600.0	960.0
1292	G101	A	-10625.0	821.0
1293	G100	A	-10650.0	960.0
1294	G99	A	-10675.0	821.0
1295	G98	A	-10700.0	960.0
1296	G97	A	-10725.0	821.0
1297	G96	A	-10750.0	960.0
1298	G95	A	-10775.0	821.0
1299	G94	A	-10800.0	960.0
1300	G93	A	-10825.0	821.0
1301	G92	A	-10850.0	960.0
1302	G91	A	-10875.0	821.0
1303	G90	A	-10900.0	960.0
1304	G89	A	-10925.0	821.0
1305	G88	A	-10950.0	960.0
1306	G87	A	-10975.0	821.0
1307	G86	A	-11000.0	960.0
1308	G85	A	-11025.0	821.0
1309	G84	A	-11050.0	960.0
1310	G83	A	-11075.0	821.0
1311	G82	A	-11100.0	960.0
1312	G81	A	-11125.0	821.0
1313	G80	A	-11150.0	960.0
1314	G79	A	-11175.0	821.0
1315	G78	A	-11200.0	960.0
1316	G77	A	-11225.0	821.0
1317	G76	A	-11250.0	960.0
1318	G75	A	-11275.0	821.0
1319	G74	A	-11300.0	960.0
1320	G73	A	-11325.0	821.0
1321	G72	A	-11350.0	960.0
1322	G71	A	-11375.0	821.0
1323	G70	A	-11400.0	960.0
1324	G69	A	-11425.0	821.0
1325	G68	A	-11450.0	960.0
1326	G67	A	-11475.0	821.0
1327	G66	A	-11500.0	960.0
1328	G65	A	-11525.0	821.0
1329	G64	A	-11550.0	960.0
1330	G63	A	-11575.0	821.0
1331	G62	A	-11600.0	960.0
1332	G61	A	-11625.0	821.0
1333	G60	A	-11650.0	960.0
1334	Dummy	A	-11675.0	821.0
1335	Dummy	A	-11700.0	960.0
1336	Dummy	A	-11859.5	960.0
-	**Alignment Mar**	-	-11949.5	960.0

Table 2–1. Pad Coordinate (8/8)

PADTYPE: SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
800	Y297	A	1675.0	821.0
801	Y298	A	1650.0	960.0
802	Y299	A	1625.0	821.0
803	Y300	A	1600.0	960.0
804	Y301	A	1575.0	821.0
805	Y302	A	1550.0	960.0
806	Y303	A	1525.0	821.0
807	Y304	A	1500.0	960.0
808	Y305	A	1475.0	821.0
809	Y306	A	1450.0	960.0
810	Y307	A	1425.0	821.0
811	Y308	A	1400.0	960.0
812	Y309	A	1375.0	821.0
813	Y310	A	1350.0	960.0
814	Y311	A	1325.0	821.0
815	Y312	A	1300.0	960.0
816	Y313	A	1275.0	821.0
817	Y314	A	1250.0	960.0
818	Y315	A	1225.0	821.0
819	Y316	A	1200.0	960.0
820	Y317	A	1175.0	821.0
821	Y318	A	1150.0	960.0
822	Y319	A	1125.0	821.0
823	Y320	A	1100.0	960.0
824	Y321	A	1075.0	821.0
825	Y322	A	1050.0	960.0
826	Y323	A	1025.0	821.0
827	Y324	A	1000.0	960.0
828	Y325	A	975.0	821.0
829	Y326	A	950.0	960.0
830	Y327	A	925.0	821.0
831	Y328	A	900.0	960.0
832	Y329	A	875.0	821.0
833	Y330	A	850.0	960.0
834	Y331	A	825.0	821.0
835	Y332	A	800.0	960.0
836	Y333	A	775.0	821.0
837	Y334	A	750.0	960.0
838	Y335	A	725.0	821.0
839	Y336	A	700.0	960.0
840	Y337	A	675.0	821.0
841	Y338	A	650.0	960.0
842	Y339	A	625.0	821.0
843	Y340	A	600.0	960.0
844	Y341	A	575.0	821.0
845	Y342	A	550.0	960.0
846	Y343	A	525.0	821.0
847	Y344	A	500.0	960.0
848	Y345	A	475.0	821.0
849	Y346	A	450.0	960.0
850	Y347	A	425.0	821.0
851	Y348	A	400.0	960.0
852	Y349	A	375.0	821.0
853	Y350	A	350.0	960.0
854	Y351	A	325.0	821.0
855	Y352	A	300.0	960.0
856	Y353	A	275.0	821.0
857	Y354	A	250.0	960.0
858	Y355	A	225.0	821.0
859	Y356	A	200.0	960.0
860	Y357	A	175.0	821.0
861	Y358	A	150.0	960.0
862	Y359	A	125.0	821.0
863	Y360	A	100.0	960.0
864	Dummy	A	75.0	821.0

PADTYPE: BUMP SIZE X = 25 um, Y = 104 um				
GATE OUTPUTS 25 um pitch tartan				
PAD No.	PAD NAME	BUMP	X [um]	Y [um]
1337	Dummy	A	-12039.5	960.0
1338	Dummy	A	-12000.0	761.0
1339	Dummy	A	-11861.0	736.0
1340	G59	A	-12000.0	711.0
1341	G58	A	-11861.0	686.0
1342	G57	A	-12000.0	661.0
1343	G56	A	-11861.0	636.0
1344	G55	A	-12000.0	611.0
1345	G54	A	-11861.0	586.0
1346	G53	A	-12000.0	561.0
1347	G52	A	-11861.0	536.0
1348	G51	A	-12000.0	511.0
1349	G50	A	-11861.0	486.0
1350	G49	A	-12000.0	461.0
1351	G48	A	-11861.0	436.0
1352	G47	A	-12000.0	411.0
1353	G46	A	-11861.0	386.0
1354	G45	A	-12000.0	361.0
1355	G44	A	-11861.0	336.0
1356	G43	A	-12000.0	311.0
1357	G42	A	-11861.0	286.0
1358	G41	A	-12000.0	261.0
1359	G40	A	-11861.0	236.0
1360	G39	A	-12000.0	211.0
1361	G38	A	-11861.0	186.0
1362	G37	A	-12000.0	161.0
1363	G36	A	-11861.0	136.0
1364	G35	A	-12000.0	111.0
1365	G34	A	-11861.0	86.0
1366	G33	A	-12000.0	61.0
1367	G32	A	-11861.0	36.0
1368	G31	A	-12000.0	11.0
1369	G30	A	-11861.0	-14.0
1370	G29	A	-12000.0	-39.0
1371	G28	A	-11861.0	-64.0
1372	G27	A	-12000.0	-89.0
1373	G26	A	-11861.0	-114.0
1374	G25	A	-12000.0	-139.0
1375	G24	A	-11861.0	-164.0
1376	G23	A	-12000.0	-189.0
1377	G22	A	-11861.0	-214.0
1378	G21	A	-12000.0	-239.0
1379	G20	A	-11861.0	-264.0
1380	G19	A	-12000.0	-289.0
1381	G18	A	-11861.0	-314.0
1382	G17	A	-12000.0	-339.0
1383	G160	A	-11861.0	-364.0
1384	G15	A	-12000.0	-389.0
1385	G14	A	-11861.0	-414.0
1386	G13	A	-12000.0	-439.0
1387	G12	A	-11861.0	-464.0
1388	G11	A	-12000.0	-489.0
1389	G10	A	-11861.0	-514.0
1390	G9	A	-12000.0	-539.0
1391	G8	A	-11861.0	-564.0
1392	G7	A	-12000.0	-589.0
1393	G6	A	-11861.0	-614.0
1394	G5	A	-12000.0	-639.0
1395	G4	A	-11861.0	-664.0
1396	G3	A	-12000.0	-689.0
1397	G2	A	-11861.0	-714.0
1398	G1	A	-12000.0	-739.0
1399	G0	A	-11861.0	-764.0
1400	Dummy	A	-12000.0	-789.0
1401	Dummy	A	-11861.0	-814.0
1402	Dummy	A	-12000.0	-839.0
1403	Dummy	A	-11861.0	-864.0
1404	Dummy	A	-12000.0	-889.0
1405	Dummy	A	-11861.0	-914.0
1406	Dummy	A	-12000.0	-939.0

3. PIN FUNCTIONS

3.1 Power Supply System Pins

(1/2)

Symbol	Pin Name	Pad No.	I/O	Function
V_{DD}	Power supply for logic	152 to 157	–	Power supply pin for logic circuit. Connect to RV_{DD} pin.
RV_{DD}	Amp. output generator for internal logic power supply	146 to 151	–	Connect to V_{DD} pin, and capacitor between V_{SS}.
V_{CCIO}	CPU/RGB interface power supply	248 to 252	–	Power supply pin for CPU/RGB interface.
V_{DC}	DC/DC converter reference power supply	120 to 135	–	Reference power supply pin for DC/DC converter.
V_{SS}	Ground	100 to 119	–	Connect to ground on system.
V_S	V_S regulator output	55 to 60	–	Adjustment power supply voltage pin for source driver driving. The V_S output voltage can be changed by setting VSSEL0 to VSSEL2.
V_R	V_R regulator output	61 to 65	–	Reference adjustment power supply voltage pin for DC/DC converter. This pin can adjust power supply voltage (V_{GH}, V_{GL}) for gate driving. The V_R output voltage can be changed by setting VRSEL0 to VRSEL2.
V_{GM}	Power supply output for gamma and VCOM DA	49 to 54	Output	Gamma resistance and reference power supply output pin for VCOM DA. V_{GM} output voltage can be changed by setup of VSEL2 to VSEL0. Connect to capacitor between V_{SS}.
V_{DCI}	Power supply output for DC/DC converter	136 to 145	–	This is reference voltage output pin for V_{DD2}, V_{CL} boost. Connect to capacitor between V_{SS}.
V_{GH}	DC/DC converter output	292 to 298	–	Boost output voltage of DC/DC converter (V_R x 2 to V_R x 4). V_R voltage level is outputted 2 to 4 time of booster. The number of boost steps of V_{GH} is chosen by the connection method of VGHREF, VGHON0, VGHON1 registers and an external capacitor. The voltage level outputted from this pin is used as top voltage for gate drive. Connect the capacitor for boost between V_{SS}.
V_{DD2}	DC/DC converter output	38 to 47	–	Boost output voltage of DC/DC converter (V_{DCI} x 2 or x 3). V_{DCI} voltage level is outputted 2 times of booster. Connect the capacitor for boost between V_{SS}. Also, connect a schottky diode between V_{DC}.
V_{GL}	DC/DC converter output	317 to 326	–	Boost output voltage of DC/DC converter (V_R x –1 to V_R x –3). V_R voltage level is outputted –1 to –3 time of booster. The number of boost steps of V_{GL} is chosen by the connection method of VGLREF, VGLON0, VGLON1 registers and an external capacitor. The voltage level outputted from this pin is used as bottom voltage for gate drive. Connect the capacitor for boost and schottky diode between V_{SS}.
V_{CL}	DC/DC converter output	2 to 5	–	Boost output voltage of DC/DC converter (V_{DCI} x –1). V_{DCI} voltage level is outputted –1 time of booster. Control of V_{CL} of operation is controllable by the VCLON register. The voltage level outputted from this pin is used as voltage of the regulator for negative side voltage output of VCOM drive circuit. When unused VCOM drive circuit, give it as intact (setup VCLON = 0). Connect the capacitor for boost between V_{SS}.

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
C11+, C11– C12+, C12– C21+, C21– C22+, C22– C23+, C23– C31+, C31–	Capacitor connect pin for boost	32 to 37, 26 to 31, 20 to 25, 14 to 19, 299 to 301, 302 to 304, 305 to 307, 308 to 310, 311 to 313, 314 to 316, 10 to 13, 6 to 9	–	To connect booster for DC/DC converter. For detail of the connection of capacitor, refer to **7.7 Variable Boost Steps.** For the recommended values of the capacitance and withstanding voltage of each capacitor, refer to **7.10 Recommended Capacitance Values of External Capacitor.**
PV_{CCIO}	Mode setting	166, 217, 233, 238, 243	–	Pull-up power supply pin for mode setting
PV_{DC}	Mode setting	162, 253	–	Pull-up power supply pin for mode setting
PV_{SS}	Mode setting	164, 209, 215, 246	–	Pull-down power supply pin for mode setting

3.2 Logic System Pins

(1/3)

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>Pad No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>DTX0 to DTX2</td><td>CPU interface bus width selection</td><td>241, 237, 239</td><td>Input</td><td>This pin selects the bus width of the i80/M68 interface (it is invalid for the RGB interface).
<table>
<tr><th>DTX0</th><th>DTX1</th><th>DTX2</th><th>i80/M68 Parallel</th><th>Serial</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>18 bits</td><td>Setting prohibited</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>8 bits</td><td>Setting prohibited</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>8 bits</td><td>18 bits</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>8 bits</td><td>Setting prohibited</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>16 bits</td><td>16 bits</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>16 bits</td><td>Setting prohibited</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>16 bits</td><td>Setting prohibited</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>16 bits</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>RGB_DTX1, RGB_DTX2</td><td>RGB interface bus width selection</td><td>242, 240</td><td>Input</td><td>This pin selects the bus width of RGB interface (it is invalid for the CPU interface).
<table>
<tr><th>RGB_DTX1</th><th>RGB_DTX2</th><th>RGB Interface Bus Width</th></tr>
<tr><td>L</td><td>L</td><td>18 bits</td></tr>
<tr><td>L</td><td>H</td><td>16 bits</td></tr>
<tr><td>H</td><td>L</td><td>16 bits</td></tr>
<tr><td>H</td><td>H</td><td>6 bits</td></tr>
</table></td></tr>
<tr><td>PSX</td><td>CPU interface mode selection</td><td>232</td><td>Input</td><td>This pin selects the mode of the CPU interface.
L: i80/M68 interface, H: Serial interface</td></tr>
<tr><td>/CS</td><td>Chip select</td><td>220</td><td>Input</td><td>This pin is used for chip select signals. When /CS = L, the chip is active and can perform data I/O operations including command and data I/O.</td></tr>
<tr><td>/RESET</td><td>Reset</td><td>222</td><td>Input</td><td>When /RESET is L, an internal reset is performed. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.
/RESET is valid when pulse width is over 10 μs.</td></tr>
<tr><td>/RD
(E)</td><td>Read
(Enable)</td><td>228</td><td>Input</td><td>When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low.
When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations.</td></tr>
<tr><td>/WR
(R,/W)</td><td>Write
(Read/write)</td><td>226</td><td>Input</td><td>When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations.
When M68 series parallel data transfer (R,/W) has been selected, this pin is used to determine the direction of data transfer.
L: Write, H: Read</td></tr>
<tr><td>C86</td><td>Select interface</td><td>236</td><td>Input</td><td>This pin is used to switch between interface modes (i80 series CPU or M68 series CPU).
L: Selects i80 series CPU mode, H: Selects M68 series CPU mode</td></tr>
<tr><td>SI</td><td>Serial input</td><td>216</td><td>Input</td><td>This pin is data input of serial interface.</td></tr>
<tr><td>SCL</td><td>Serial clock</td><td>218</td><td>Input</td><td>This pin is clock input of serial interface.</td></tr>
</table>

(2/3)

Symbol	Pin Name	Pad No.	I/O	Function
D_0 to D_{17}	Data bus for both CPU and RGB interface	173, 175, 177, 179, 181, 183, 185, 187, 189, 191, 193, 195, 197, 199, 201, 203, 205, 207	I/O	These pins comprise 18-bit bi-directional data bus.
HSYNC	Horizontal sync signal	230	Input	This is the horizontal sync signal of the RGB interface.
VSYNC	Vertical sync signal	229	Input	This is the vertical sync signal of the RGB interface.
DOTCLK	Dot clock	231	Input	This is the dot clock signal of the RGB interface.
RS	Data/command selection	224	Input	When parallel data transfer has been selected, this pin is usually connected to the least significant bit of the standard CPU address bus and is used to distinguish between data from display data and commands. RS = L: Indicates that data from D_0 to D_{17} is command. RS = H: Indicates that data from D_0 to D_{17} is data.
CSTB	Frame synchronize signal	172	Output	This pin outputs signal synchronized frame leveled by interface power supply voltage (V_{CCIO}).
RESET_SEL	Reset selection signal	165	Input	This pin selects initialization of the register by /RESET pin input. H: Hard/command reset valid (In case of selecting register mode 1 or 3, only E2OPC [R68] and DC/DC operation setting [R24/R257] register is valid for hard reset. L: Only command reset is valid
REGSEL1, REGSEL0	Register mode selection	234, 235	Input	The μPD161704A builds in two registration tables and two register initialization modes. These modes can be chosen by setup of this pin. For more details about register mode, refer to **9. RESET.**
IF_SHARE	Data bus switch selection	245	Input	This pin selects the mode which uses the data bus D_0 to D_{17} for CPU access, or sharing it with the data bus of RGB interface. L: D_0 to D_{17} is interface only for CPU. H: D_0 to D_{17} is input pin only for RGB In case of selecting this mode, command transfer is available only for serial interface (both register read and data read are impossible).
OSCSEL	Oscillation signal select	163	Input	This pin is used to select the oscillation signal. L: Selects CR on-chip oscillator. H: Selects oscillator connected to external resistor
OSCIN	Oscillation signal	160	Input	This is the oscillation signal pin. OSCEL = H: Be sure to connect 36 kΩ resistor between OSCIN and OSCOUT pin. OSCEL = L: Leave OSCIN and OSCOUT pin open.
OSCOUT		161	Output	

REGSEL1	REGSEL0	Mode Setting
L	L	Register mode 1
L	H	Register mode 2
H	L	Register mode 3
H	H	Register mode 4

(3/3)

Symbol	Pin Name	Pad No.	I/O	Function
EPEN	Valid for external E^2PROM	167	Input	This pin selects valid or invalid for external E^2PROM. L: Valid for external E^2PROM H: Invalid for external E^2PROM
EDI	Data input for E^2PROM interface	168	Input	This pin is data input for E^2PROM interface. It is used for reading of the data of E^2PROM. It connects with DOUT (data out pin) of E^2PROM.
ECS	Chip select for E^2PROM interface	169	Output	This pin is used as the chip select pin for the E^2PROM interface. When ECS = H, the E^2PROM goes to active status, after which data is transferred. This pin is connected to the E^2PROM's CS (chip select) pin.
<R> ESK	Serial clock for E^2PROM interface	170	Output	This pin is CLK for E^2PROM interface. This is the E^2PROM clock for which has 8 divided circumferences in internal oscillator. In the fall of ESK, data is outputted from EDO to E^2PROM. It connects with CLK (shift clock pin) of E^2PROM.
EDO	Data output for E^2PROM interface	171	Output	This pin is data output for E^2PROM interface. Data is outputted to E^2PROM. It connects with DIN (data-in pin) of E^2PROM.

3.3 Driver Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
Y_1 to Y_{720}	Source output	504 to 863, 865 to 1224	Output	These pins are source output pins.
G_0 to G_{321}	Gate output	1399 to 1340, 1333 to 1233, 335 to 394, 401 to 501	Output	These pins are gate output pins (G_0 and G_{321} are dummy outputs).
VCOMHM	Common high-level output	76 to 80	Output	<COMONM [R30] = 1> Output high level of VCOM voltage. This pin changes voltage, corresponding DA0 to DA5 [R31], MCDA0 to MCDA6 [R32]. Connect to capacitor between V_{SS}. <COMONM [R30] = 0> This is open when not using.
VCOMLM	Common low-level output	87 to 91	Output	<COMONM [R30] = 1> Output low level of VCOM voltage. This pin changes voltage, corresponding DA0 to DA5 [R31], MCDA0 to MCDA6 [R32]. Connect to capacitor between V_{SS}. <COMONM [R30] = 0> This is open when not using.
VCOMM	VCOM output	66 to 73	Output	<COMONM [R30] = 1> Output VCOM voltage which synchronizing input VCINM. Connect to common pin of LCD panel. <COMONM [R30] = 0> This is open when not using.
VCOMINM	VCOM center voltage input	75	Input	This is VCOM center voltage input pin. When COMINM [R32] = 0, connect VCOMINM pin to PV_{SS}. <COMINM [R32] = 0> Internal D/A valid <COMINM [R32] = 1> VCOMINM input voltage valid

3.4 Test or Other Pins

Symbol	Pin Name	Pad No.	I/O	Function
CONTACT1 to CONTACT4	For Bump resistance measurement	254, 255, 290, 291	–	This is the pin used for Bump resistance measurement. CONTACT1, 2 and CONTACT3, 4 short-circuit inside IC, respectively. When not use it, leave open.
TOUT0 to TOUT17	Test output	174, 176, 178, 180, 182, 184, 186, 188, 190, 192, 194, 196, 198, 200, 202, 204, 206, 208	Output	This is output pin when IC is in test mode. Normally, leave it open.
TDELAY0 to TDELAY2, TSTRTST, TSTVIHL, TOSCI, TOSCSELI,	Test input	219, 221, 223, 227, 225, 158, 159,	Input	These input pins are to set up test mode of IC. Normally, connected it to V_{SS} or open.
VSTBY, TWPNL	Test input	247, 244	Input	This is input pin when IC is in test mode. Normally, connected it to V_{SS}.
TVREFR, TGCLK, TGSTB, TGOE1S, TGOE2S, TRL	Test output	48, 212, 213, 210, 211, 214	Output	This is output pin when IC is in test mode. Normally, leave it open.
DUMMY	Dummy	1, 74, 81 to 86, 92 to 99, 256 to 289, 327 to 334, 395 to 400, 502, 503, 864, 1225 to 1232, 1334 to 1339, 1400 to 1406	–	Dummy pin

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

(1/2)

Pin Name	Input Type	I/O	Power Supply	Recommended Connection of Unused Pins		Note
				Parallel Interface	Serial Interface	
PSX	Schmitt trigger	Input	V_{CCIO}	Mode setting pin		1
RGB_DTX1, RGB_DTX2	Schmitt trigger	Input	V_{CCIO}	Mode setting pin		1
DTX0 to DTX2	Schmitt trigger	Input	V_{CCIO}	Mode setting pin		1
REGSEL0, REGSEL1	Schmitt trigger + low path filter	Input	V_{CCIO}	Mode setting pin		1
IF_SHARE	Schmitt trigger	Input	V_{CCIO}	Mode setting pin		1
RS	Schmitt trigger	Input	V_{CCIO}	Register setting pin		–
/RD(E), /WR	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} (when i80 series interface)	Connect to V_{CCIO} or V_{SS}	1
C86	Schmitt trigger	Input	V_{CCIO}	Mode setting pin	Connect to V_{CCIO} or V_{SS}	1
D_0 to D_{17}	Schmitt trigger	I/O	V_{CCIO}	–	Connect to V_{SS}	–
SI, SCL	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} or V_{SS}	–	–
HSYNC	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} or V_{SS}		–
VSYNC	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} or V_{SS}		–
DOTCLK	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} or V_{SS}		–
/RESET	Schmitt trigger + low path filter	Input	V_{CCIO}	Always reset on power application		–
EPEN	Schmitt trigger	Input	V_{CCIO}	Mode setting pin		1
EDI	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} or V_{SS}		–
ECS	–	Output	V_{CCIO}	Leave open		–
ESK	–	Output	V_{CCIO}	Leave open		–
EDO	–	Output	V_{CCIO}	Leave open		–
CSTB	–	Output	V_{CCIO}	Leave open		–
RESET_SEL	Schmitt trigger	Input	V_{CCIO}	Connect to V_{CCIO} or V_{SS}		–
OSCIN	–	Input	V_{DC}	Leave open		–
OSCOUT	–	Output	V_{DC}	Leave open		–
OSCSEL	–	Input	V_{DC}	Mode setting pin		2
Y_1 to Y_{720}	–	Output	V_S	Leave open		–
G_0 to G_{321}	–	Output	V_{GH}, V_{GL}	Leave open		–

Notes 1. Connect to V_{CCIO} or V_{SS}, depending on the mode selected.

2. Connect to V_{DC} or V_{SS}, depending on the mode selected.

(2/2)

Pin Name	Input Type	I/O	Power Supply	Recommended Connection of Unused Pins		Note
				Parallel Interface	Serial Interface	
CONTACT1 to CONTACT4	–	–	–	Leave open		–
TOUT0 to TOUT17	–	Output	V_{CCIO}	Leave open		–
VSTBY	–	Output	V_{DC}	Connect to V_{SS}		–
TVREFR	–	Output	V_{DD}	Leave open		–
TWPNL	–	Output	V_{CCIO}	Connect to V_{SS}		–
TSTRTST	–	Input	V_{CCIO}	Connect to V_{SS} or open		–
TSTVIHL	–	Input	V_{CCIO}	Connect to V_{SS} or open		–
TOSCI	–	Input	V_{DC}	Connect to V_{SS} or open		–
TOSCSELI	–	Input	V_{DC}	Connect to V_{SS} or open		–
TDELAY0 to TDELAY2	–	Input	V_{CCIO}	Connect to V_{SS} or open		–
TGCLK, TGSTB, TGOE1S, TGOE2S, TRL	–	Input	–	Leave open		–

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type (Each common register mode)

The μPD161704A chip transfers data using a RGB interface (18/16/6-bit), i80/M68 parallel interface (18/16/8-bit), and serial interface (18/16-bit). The PSX, DTX0 to DTX2, RGB_DTX1, and RGB_DTX2 pins are used to select the modes shown in the Table 5–1 below. Note that the i80/M68 parallel interface and serial interface can write data to the display data RAM and registers, but that the RGB interface can write data only to the display data RAM.

Table 5–1. CPU Interface Mode (IF_SHARE = L)

PSX	DTX0	DTX1	DTX2	Mode	/RD (E)	/WR (R,/W)	C86	D_{17}, D_{16}	D_{15} to D_{10}	D_9	D_8	D_7 to D_1	D_0	SI, SCL
L	L	L	L	18-bit parallel	/RD (E)	/WR (R,/W)	C86	D_{17}, D_{16}	D_{15} to D_{10}	D_9	D_8	D_7 to D_1	D_0	Hi-Z Note
	H	L	L	16-bit parallel	/RD (E)	/WR (R,/W)	C86	Hi-Z Note	D_{15} to D_{10}	D_9	D_8	D_7 to D_1	D_0	Hi-Z Note
		H	H											
		H	L											
		L	H					D_{17}, D_{16}	D_{15} to D_{10}	Hi-Z Note	D_8	D_7 to D_1	Hi-Z Note	
	L	L	H	8-bit parallel	/RD (E)	/WR (R,/W)	C86	Hi-Z Note	Hi-Z Note	Hi-Z Note	Hi-Z Note	D_7 to D_1	D_0	Hi-Z Note
		H	L											
		H	H											
H	L	H	L	18-bit serial	X	X	X	Hi-Z Note	Hi-Z Note	Hi-Z Note	Hi-Z Note	Hi-Z Note	Hi-Z Note	SI, SCL
	H	L	L	16-bit serial										
Other then above				Setting prohibited										

Remark X: Don't care

Note Hi-Z: High impedance (low clamping inside)

Table 5–2. RGB Interface Mode (IF_SHARE = H)

PSX	RGB_DTX1	RGB_DTX2	Mode	/RD (E)	/WR (R,/W)	C86	SI, SCL	D_{17}, D_{16}	D_{15} to D_{13}	D_{12}	D_{11} to D_8	D_7 to D_1	D_0
L	X	X	–	/RD (E) Note2	/WR (R,/W) Note2	C86	Hi-Z Note1	D_{17}, D_{16}	D_{15} to D_{13}	D_{12}	D_{11} to D_8	D_7 to D_1	D_0
H	H	L	16-bit	X	X	X	SI, SCL	Hi-Z Note1	D_{15} to D_{13}	D_{12}	D_{11} to D_8	D_7 to D_1	D_0
	L	H						D_{17}, D_{16}	D_{15} to D_{13}	Hi-Z Note1	D_{11} to D_8	D_7 to D_1	Hi-Z Note1
	L	L	18-bit					D_{17}, D_{16}	D_{15} to D_{13}	D_{12}	D_{11} to D_8	D_7 to D_1	D_0
	H	H	6-bit					Hi-Z Note1	Hi-Z Note1	Hi-Z Note1	Hi-Z Note1	D_7, D_6: Hi-Z Note1 D_5 to D_1	D_0
Other then above				Setting prohibited									

Remark X: Don't care

Notes 1. Hi-Z: High impedance (low clamping inside)

2. When use it by IF_SHARE = H in parallel interface (PSX = L), use /CS, /RD (E) and /WR (R,/W) in non-active state.

5.1.2 Selection of data transfer mode

When the 18-bit parallel interface is selected, the length of 1 pixel is fixed to 18 bits. With the 16-bit or 8-bit parallel interface, however, the length of 1 pixel can be selected from 18 or 16 bits.

If the 16-bit or 8-bit parallel interface is selected, therefore, several modes of transferring data to the display RAM are selectable.

[16-bit parallel interface]

<When 1 pixel = 18 bits>

<1> Transferring 16-bit data transfer + 2-bit data transfer two times (DTX0 = H, DTX1 = H, DTX2 = H)

1 pixel = 18-bit data is divided into 16-bit data and 2-bit data for transfer, as shown in Figure 5–3.

<R> <2> Transferring 9 + 9-bit data transfer two times (DTX0 = H, DTX1 = H, DTX2 = L)

1 pixel = 18-bit data transfer by 2 times transmission of 9-bit data as shown in Figure 5–4.

<When 1 pixel = 16 bits>

<1> 16-bit data transfer (DTX0 = H, DTX2 = L, DTX3 = L)

Display data of 1 pixel is transferred by one transmission as shown in Figure 5–5 to 5–8. Because 1 pixel is 16 bits long, the number of display colors is limited to 65,536.

[8-bit parallel interface]

< When 1 pixel = 18 bits>

<1> Transferring 6 + 6 + 6-bit data three times (DTX0 = L, DTX1 = H, DTX2 = L)

1 pixel = 18-bit data is divided into three 6-bit data for transfer, as shown in Figure 5–9.

<2> Transferring 8 + 8 + 2-bit data three times (DTX0 = L, DTX1 = H, DTX2 = H)

1 pixel = 18-bit data transfer by 3 times transmission of 8-bit data transfer two times + 2-bit data transfer as shown in Figure 5–10.

<Where 1 pixel = 16 bits>

<1> Transferring 8 + 8 bit twice (DTX0 = L, DTX1 = L, DTX2 = H)

1 pixel is divided into two 8-bit data for transfer, as shown in Figure 5–11. Because 1 pixel is 16 bits long, the number of display colors is limited to 65,536.

1 pixel of the μPD161704A display RAM consists of 18 bits. If the 16-bit parallel interface is used to transfer 16 bits as 1 pixel (DTX1 = 0), therefore, the data transferred by the CPU (16 bits) runs short by 2 bits, and these 2 bits must be made up for.

For how to do this, refer to Figures 5–5, 5–6 and 5–11.

<R> **Table 5–3. Interfaces and Data Transfer Modes**

IF_SHARE = L

PSX	DTX0	DTX1	DTX2	RGB_DTX1	RGB_DTX2	Interface Mode	Number of Data of 1 Pixel	Mode of Transferring 1-Pixel Data
L	L	L	L	L/H Note	L/H Note	18-bit parallel	18-bit	18-bit transfer
		H	H			8-bit parallel	18-bit	Transferring 8+8+2-bit three times
		H	L					Transferring 6+6+6-bit three times
		L	H				16-bit	Transferring 8+8-bit two times
	H	H	H			16-bit parallel	18-bit	Transferring 16+2-bit two times
		H	L					Transferring 9+9-bit two times
		L	H				16-bit	16-bit transfer (D17 to D10, D8 to D1)
		L	L					16-bit transfer (D15 to D0)
H	H	L	L			16-bit serial	16-bit	16-bit transfer
	L	H	L			18-bit serial	18-bit	18-bit transfer

Note When IF_SHARE = L, both RGB_DTX1 and RGB_DTX2 setting are invalid.

IF_SHARE = H

PSX	DTX0	DTX1	DTX2	RGB_DTX1	RGB_DTX2	Interface Mode	Number of Data of 1 Pixel	Mode of Transferring 1-Pixel Data
H	L/H	L/H	L/H	H	L	–	16-bit	16-bit transfer (D15 to D0)
				L	H			16-bit transfer (D17 to D13, D11 to D1)
				L	L		18-bit	18-bit transfer
				H	H			Transferring 6-bit three times

Remark When it is not using serial interface, it regards as PSX = 0, therefore, DTX0 to DTX2 are “Don’t care”.

Figure 5–1. Relationship between Bus Data and Display RAM Data (18-bit parallel interface)

Data bus side

18-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–2. Relationship between Bus Data and Display RAM Data (18-bit RGB interface)

Data bus side

18-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–3. Relationship between Bus Data and Display RAM Data
(1-pixel/18-bit mode, 16-bit parallel interface (DTX0, DTX1, DTX2 = H, H, H))

Data bus side

16-bit data (at 1-byte)																2-bit data (at 2-byte)	
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Caution Data D_2 to D_{15} of the second byte are treated as invalid data when the 16-bit parallel interface is used.

Figure 5–4. Relationship between Bus Data and Display RAM Data
(1-pixel/18-bit mode, 16-bit parallel interface (DTX0, DTX1, DTX2 = H, H, L))

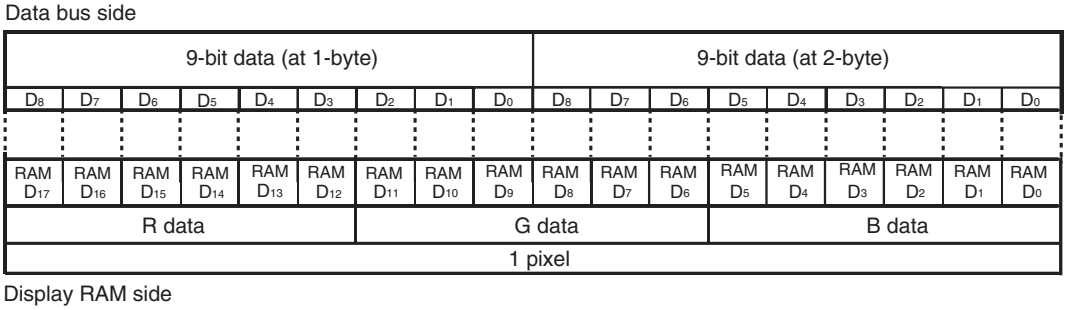
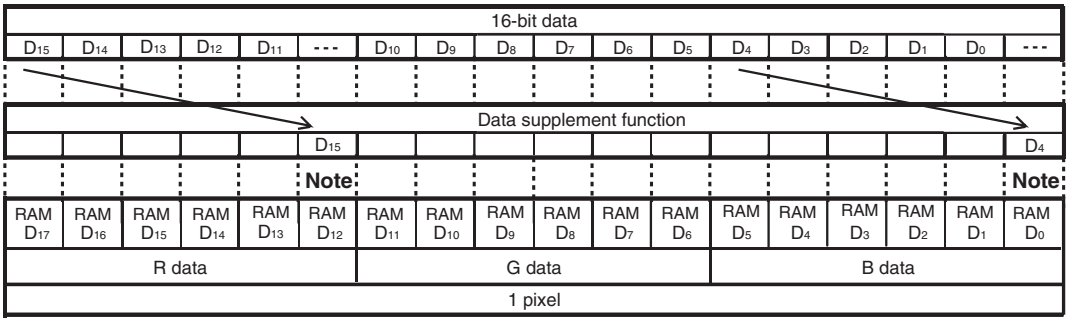
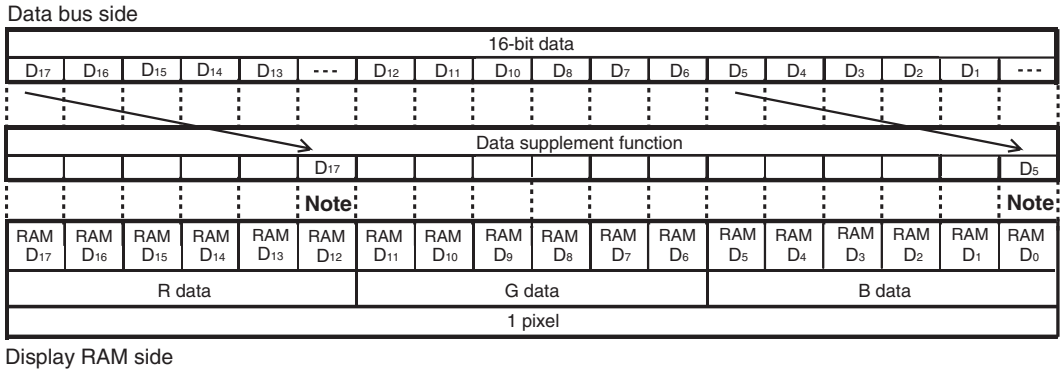


Figure 5–5. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode, 16-bit parallel interface (DTX0, DTX1, DTX2 = H, L, L))



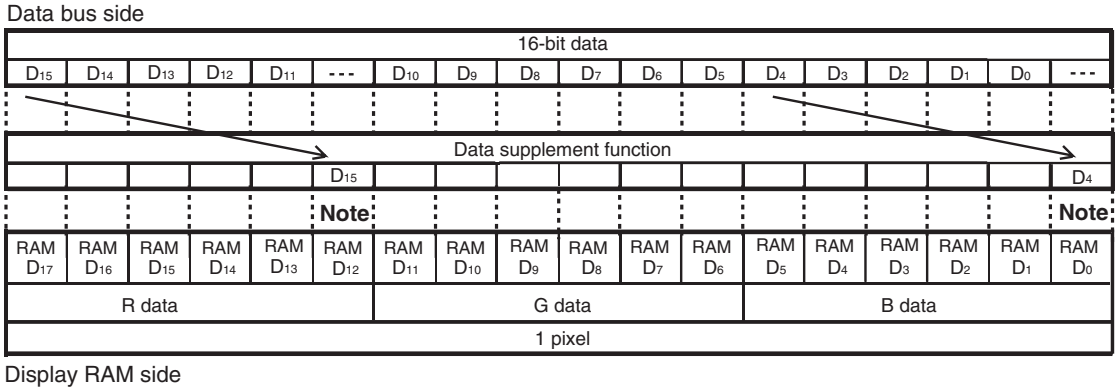
Note When in used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by D_{15} and D_4 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–6. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode, 16-bit parallel interface (DTX0, DTX1, DTX2 = H, L, H))



Note When in used 16-bit parallel interface (DTX0, DTX1, DTX2 = H, L, H), display RAM data D_{12} and D_0 are supplemented by D_{17} and D_5 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–7. Relationship between Bus Data and Display RAM Data
(16-bit RGB interface (RGB_DTX1, RGB_DTX2 = H, L))



Note When in used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by D_{15} and D_4 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–8. Relationship between Bus Data and Display RAM Data
(16-bit RGB interface (RGB_DTX1, RGB_DTX2 = L, H))

Data bus side

16-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	---	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	---
					D_{17}												D_5
					Note												**Note**
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are supplemented by D_{17} and D_5 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–9. Relationship between Bus Data and Display RAM Data
(1-pixel/18-bit mode, 8-bit parallel interface (DTX0, DTX1, DTX2 = L, H, L))

Data bus side

6-bit data (at 1-byte)						6-bit data (at 2-byte)						6-bit data (at 3-byte)					
D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Caution Display data D_6 and D_7 of the 8-bit parallel interface are treated as invalid data.

Figure 5–10. Relationship between Bus Data and Display RAM Data
(1-pixel/18-bit mode, 8-bit parallel interface (DTX0, DTX1, DTX2 = L, H, H))

Data bus side

8-bit data (at 1-byte)								8-bit data (at 2-byte)								2-bit data (at 3-byte)	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Caution Display data D_2 to D_7 of the 3 word treated as invalid data.

Figure 5–11. Relationship between Bus Data and Display RAM Data
(1-pixel/16-bit mode, 8-bit parallel interface (DTX0, DTX1, DTX2 = L, L, H))

Data bus side

8-bit data (at 1-byte)									8-bit data (at 2-byte)								
D_7	D_6	D_5	D_4	D_3	---	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	---
					Data supplement function												
					D_7												D_4
					Note												**Note**
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Note When in used 8-bit parallel interface, display RAM data D_0 and D_{12} are supplemented by bit D_7 of the first byte of the bus data and bit D_4 of the second byte of the bus data, and written to the display RAM as 18-bit data

Figure 5–12. Relationship between Bus Data and Display RAM Data (6-bit RGB interface)

Data bus side

6-bit data (at 1-byte)						6-bit data (at 2-byte)						6-bit data (at 3-byte)					
D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					

Display RAM side

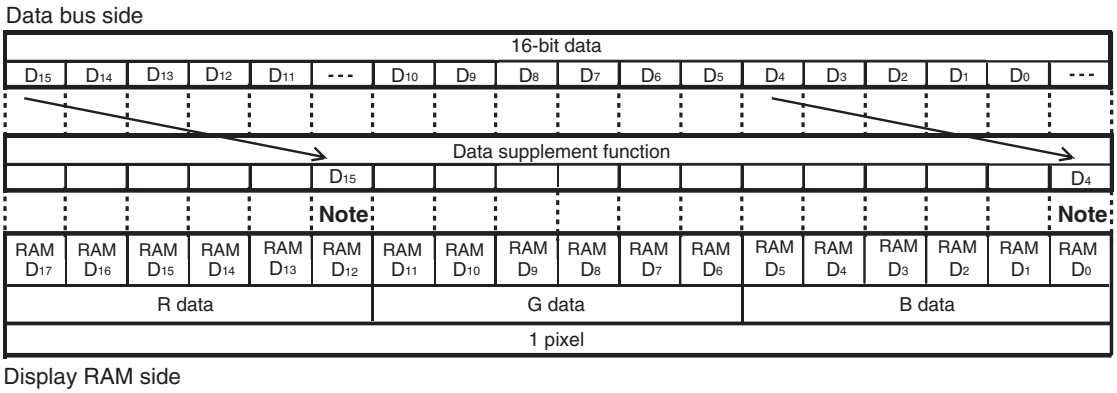
Figure 5–13. Relationship between Bus Data and Display RAM Data (18-bit serial interface)

Data bus side

18-bit data																	
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RAM D_{17}	RAM D_{16}	RAM D_{15}	RAM D_{14}	RAM D_{13}	RAM D_{12}	RAM D_{11}	RAM D_{10}	RAM D_9	RAM D_8	RAM D_7	RAM D_6	RAM D_5	RAM D_4	RAM D_3	RAM D_2	RAM D_1	RAM D_0
R data						G data						B data					
1 pixel																	

Display RAM side

Figure 5–14. Relationship between Bus Data and Display RAM Data (16-bit serial interface)



Note When in used 16-bit serial interface, display RAM data D_{12} and D_0 are supplemented by D_{15} and D_4 of bus data respectively, and written to the display RAM as 18-bit data.

Figure 5–15. 16-bit Parallel Interface Data Transfer (1-pixel/18-bit mode)

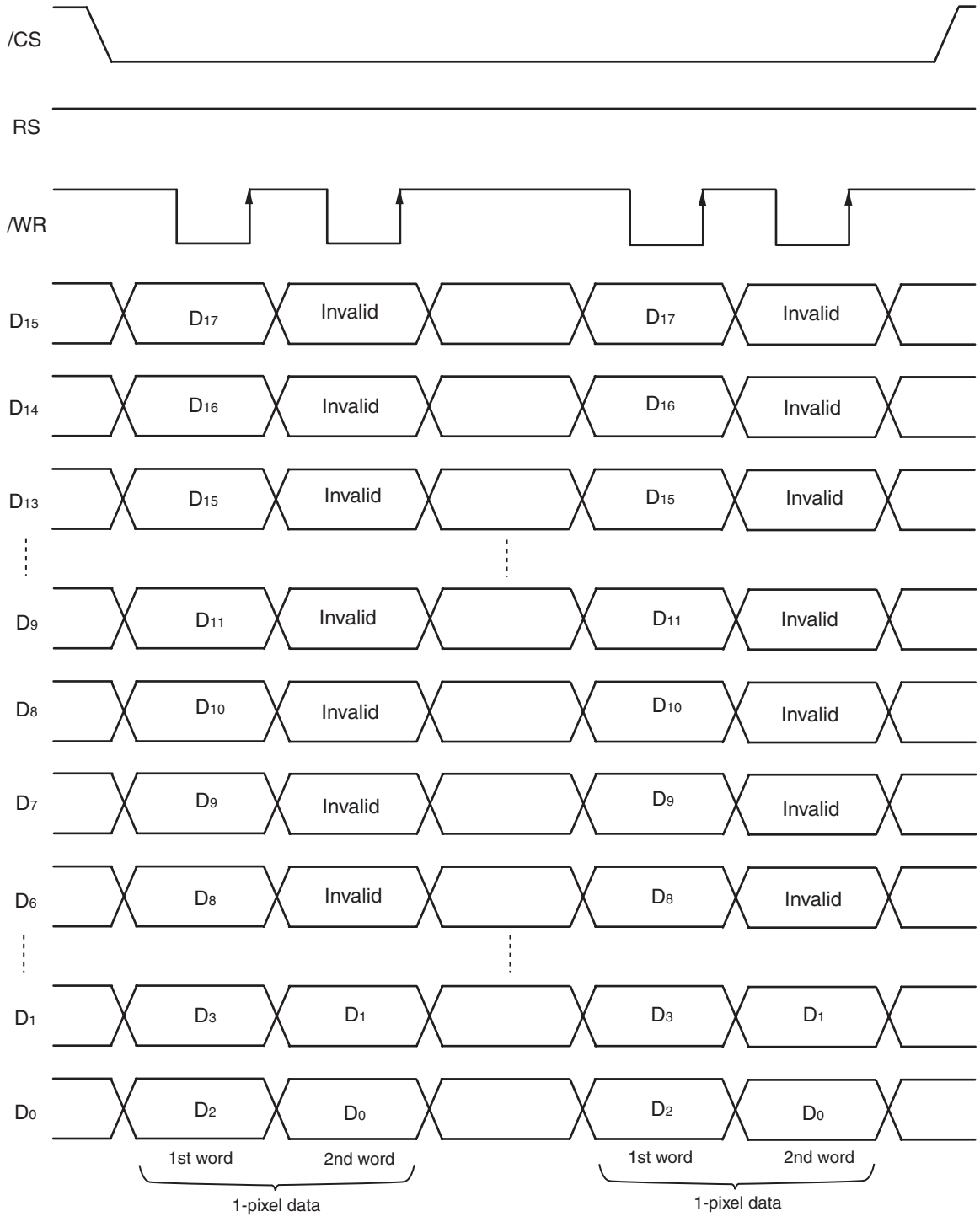


Figure 5–16. 8-bit Parallel Interface Data Transfer (1-pixel/16-bit mode)

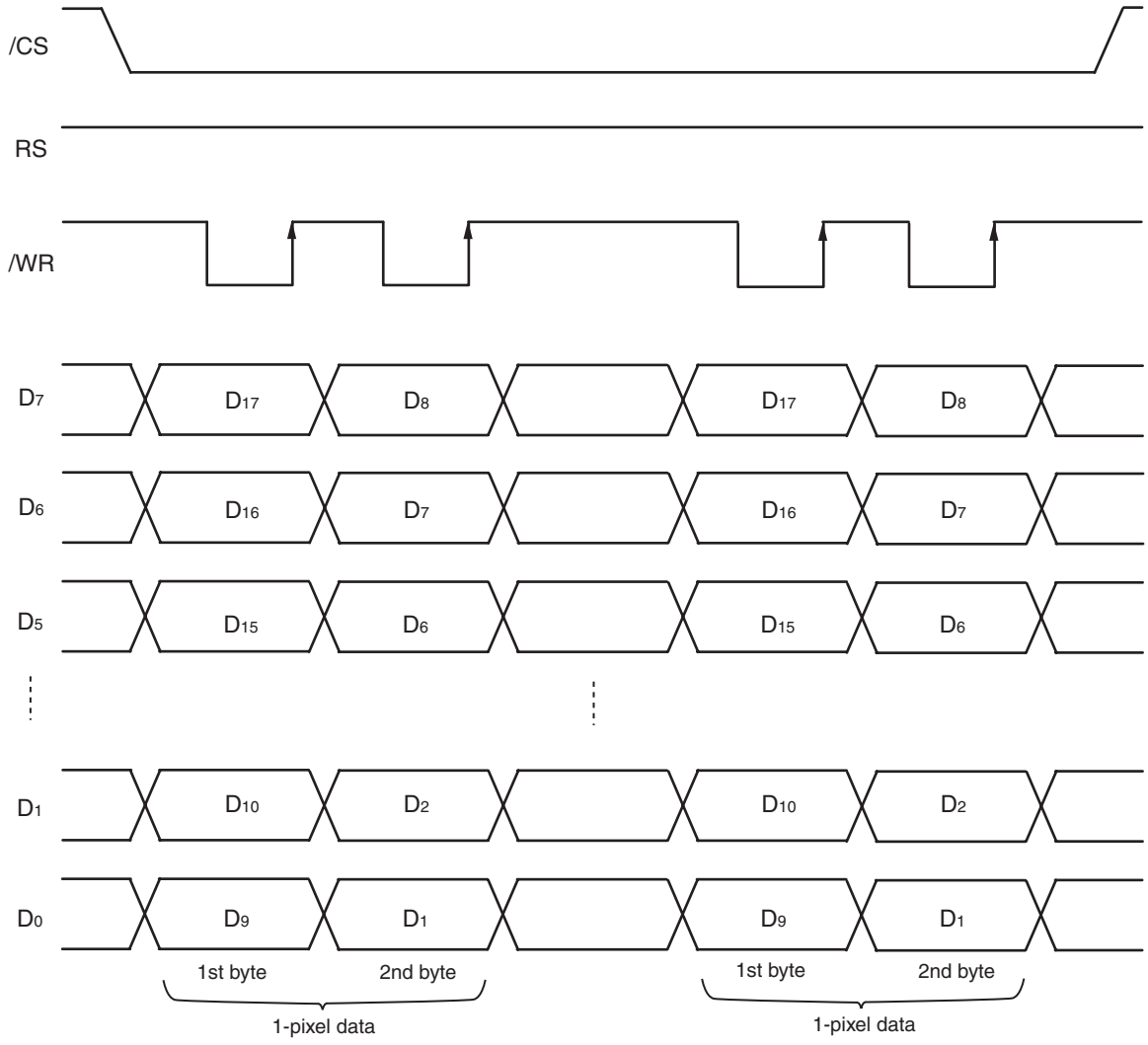


Figure 5–17. 8-bit Parallel Interface Data Transfer (1-pixel/18-bit mode)

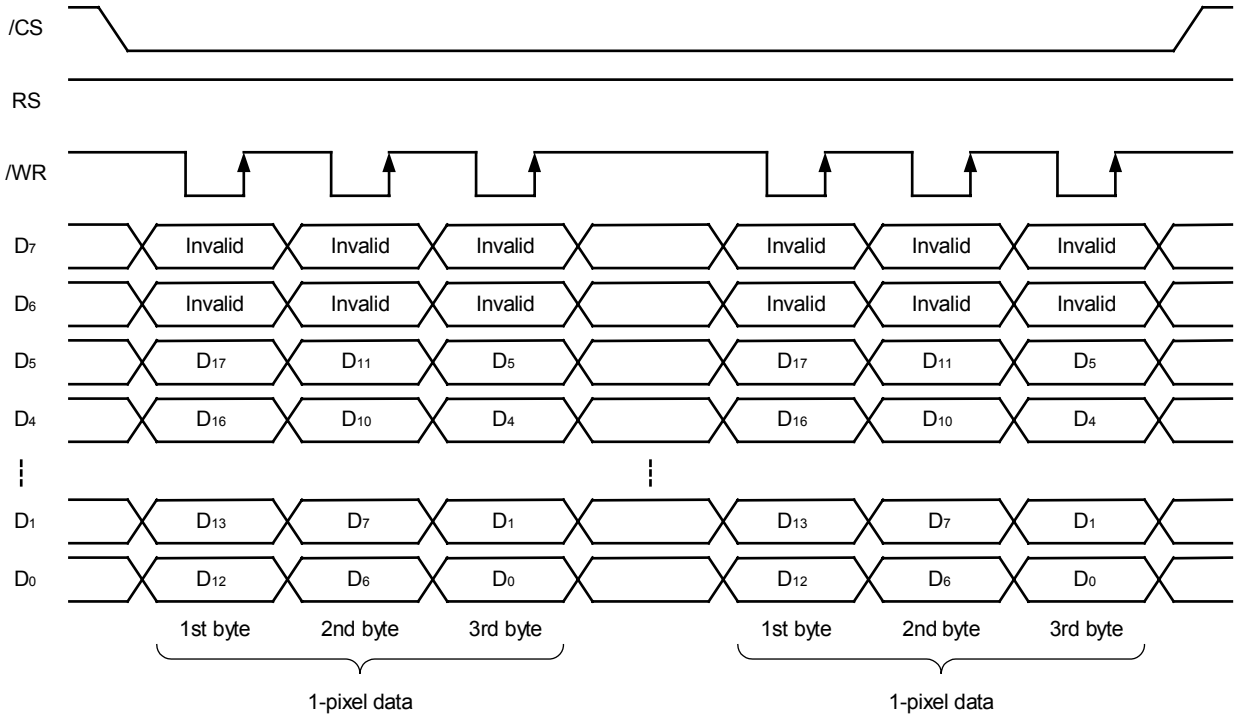
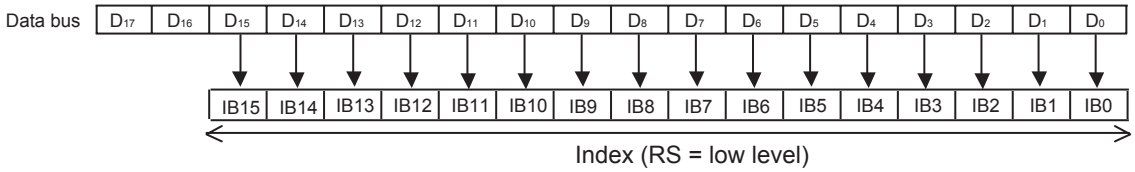
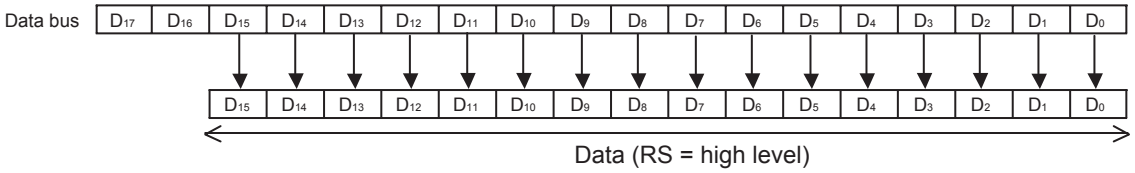


Figure 5–18. Relationship between Bus Data and Setting Data in 18-bit Parallel Interface Mode

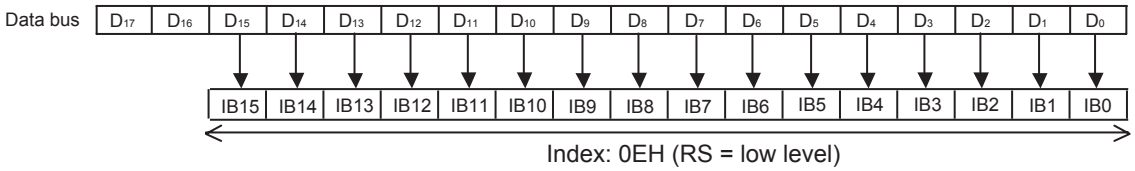
• 18-bit parallel interface

<Read/write in command>





<Read/write in display data (1 pixel = 18-bit) >



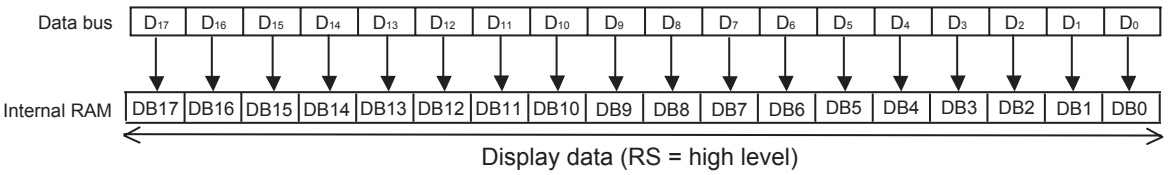
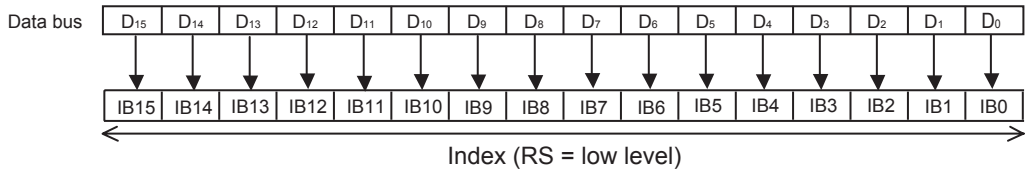
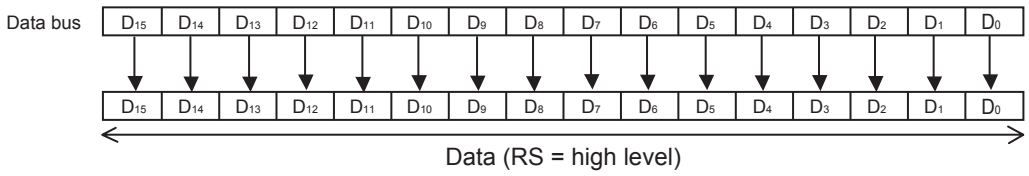


Figure 5–19. Relationship between Bus Data and Setting Data in 16-bit Parallel Interface Mode (except for DTX0, DTX1, DTX2 = H, L, L)

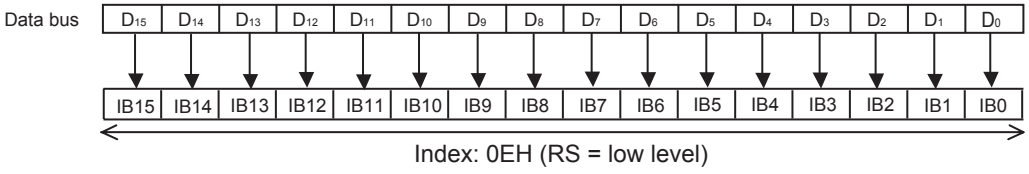
• 16-bit parallel interface

<Read/write in command>





<Read/write in display data (1 pixel = 16-bit) >



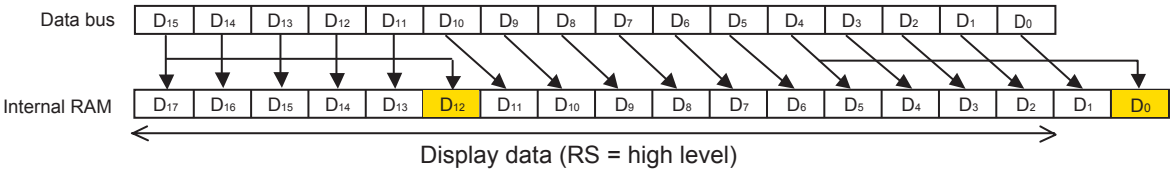
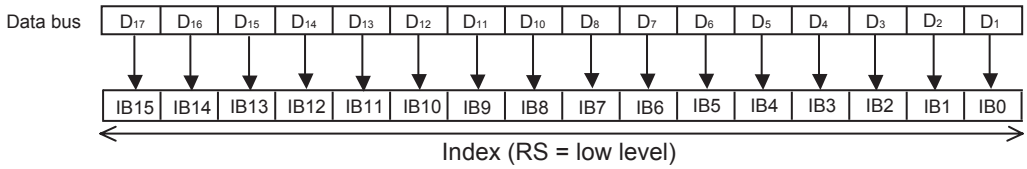
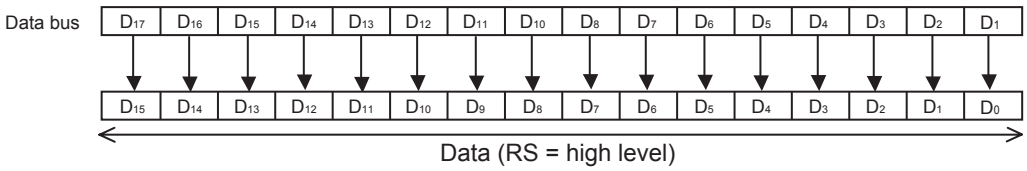


Figure 5–20. Relationship between Bus Data and Setting Data in 16-bit Parallel Interface Mode (DTX0, DTX1, DTX2 = H, L, H)

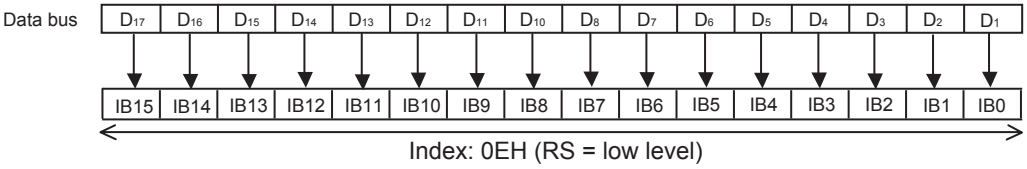
• 16-bit parallel interface

<Read/write in command>





<Read/write in display data (1 pixel = 16-bit) >



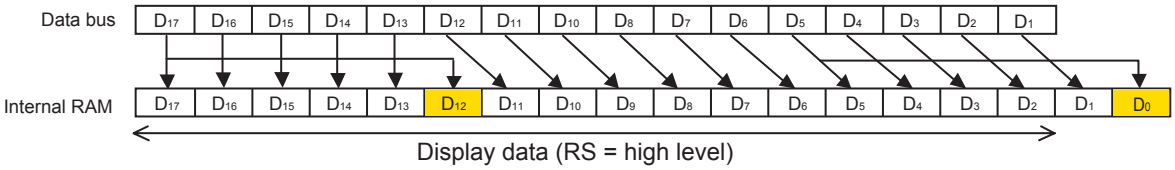
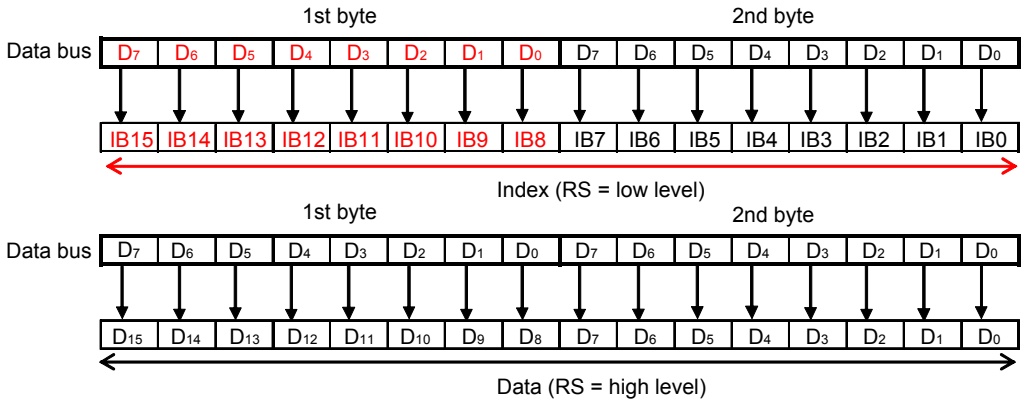


Figure 5–21. Relationship between Bus Data and Setting Data in 8-bit Parallel Interface Mode

8-bit parallel interface

<Read/write in command>



<Read/write in display data (1 pixel = 16-bit) >

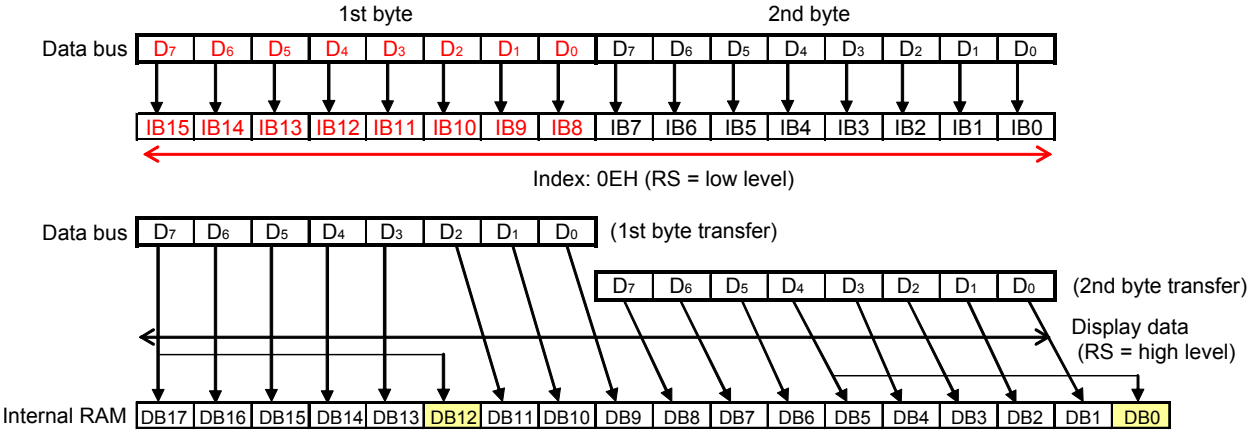
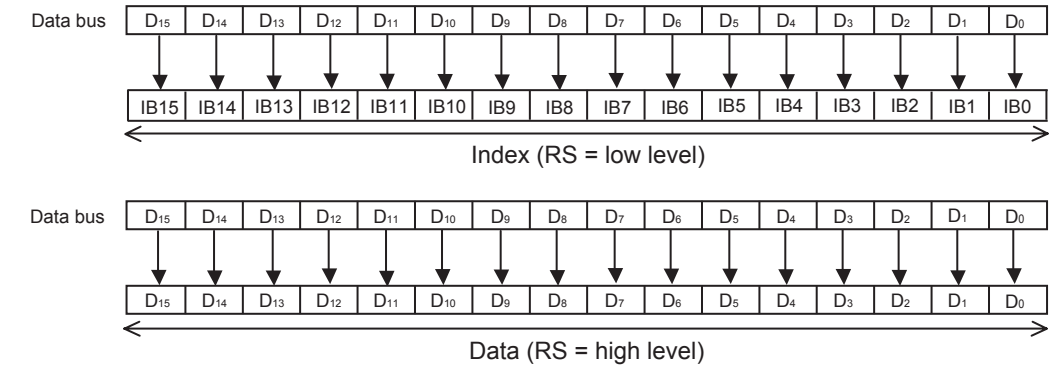


Figure 5–22. Relationship between Bus Data and Setting Data in 16-bit Serial Interface Mode

• 16-bit serial interface

<Write in command>



<Write in display data (1 pixel = 16-bit) >

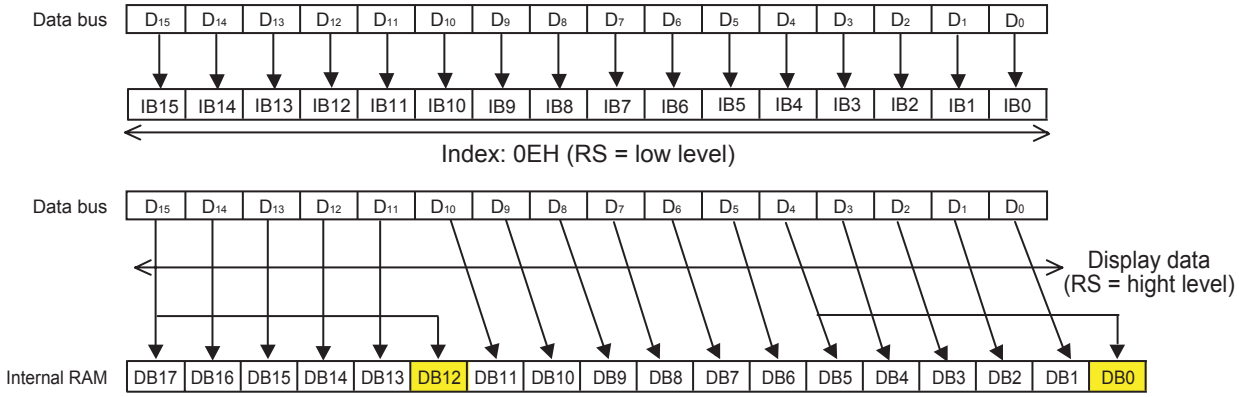
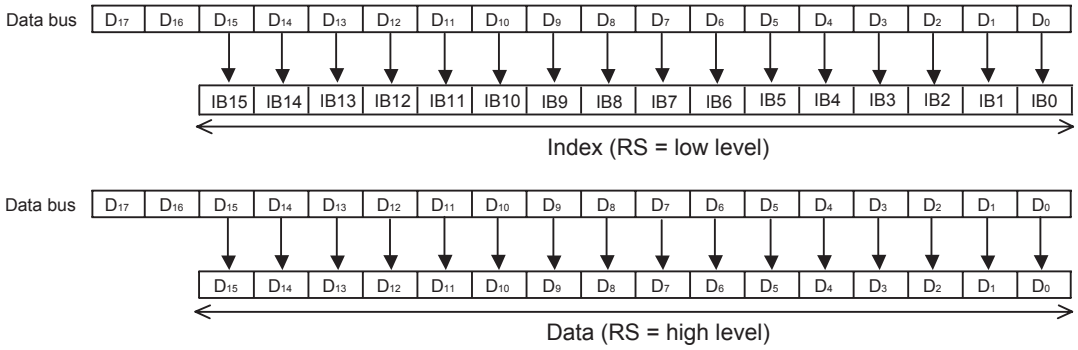


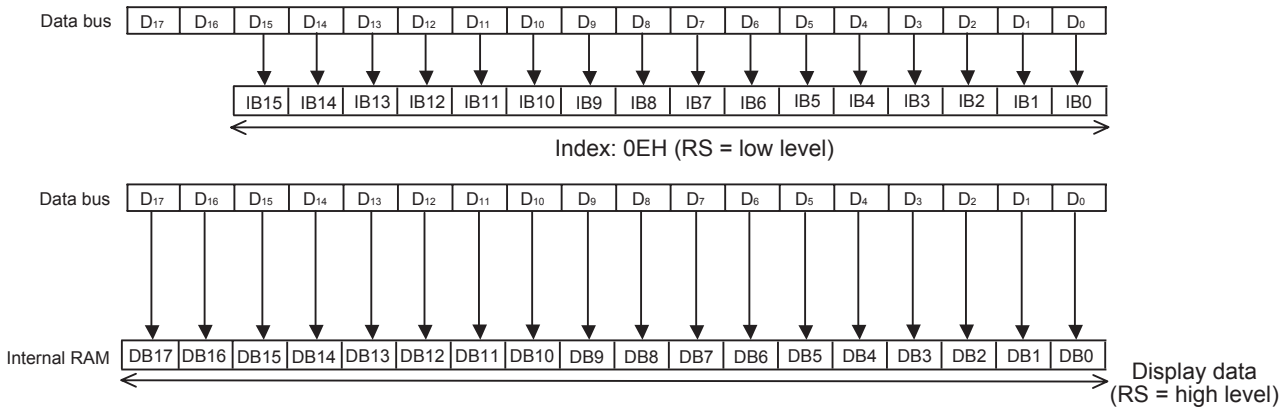
Figure 5–23. Relationship between Bus Data and Setting Data in 18-bit Serial Interface Mode

• 18-bit serial interface

<Write in command>



<Write in display data (1 pixel = 18-bit)>



5.1.3 RGB interface (Each common register mode)

The μPD161704A can be directly connected to the RGB interface when NWRGB (bit D_2) of R2 register is set to 1.

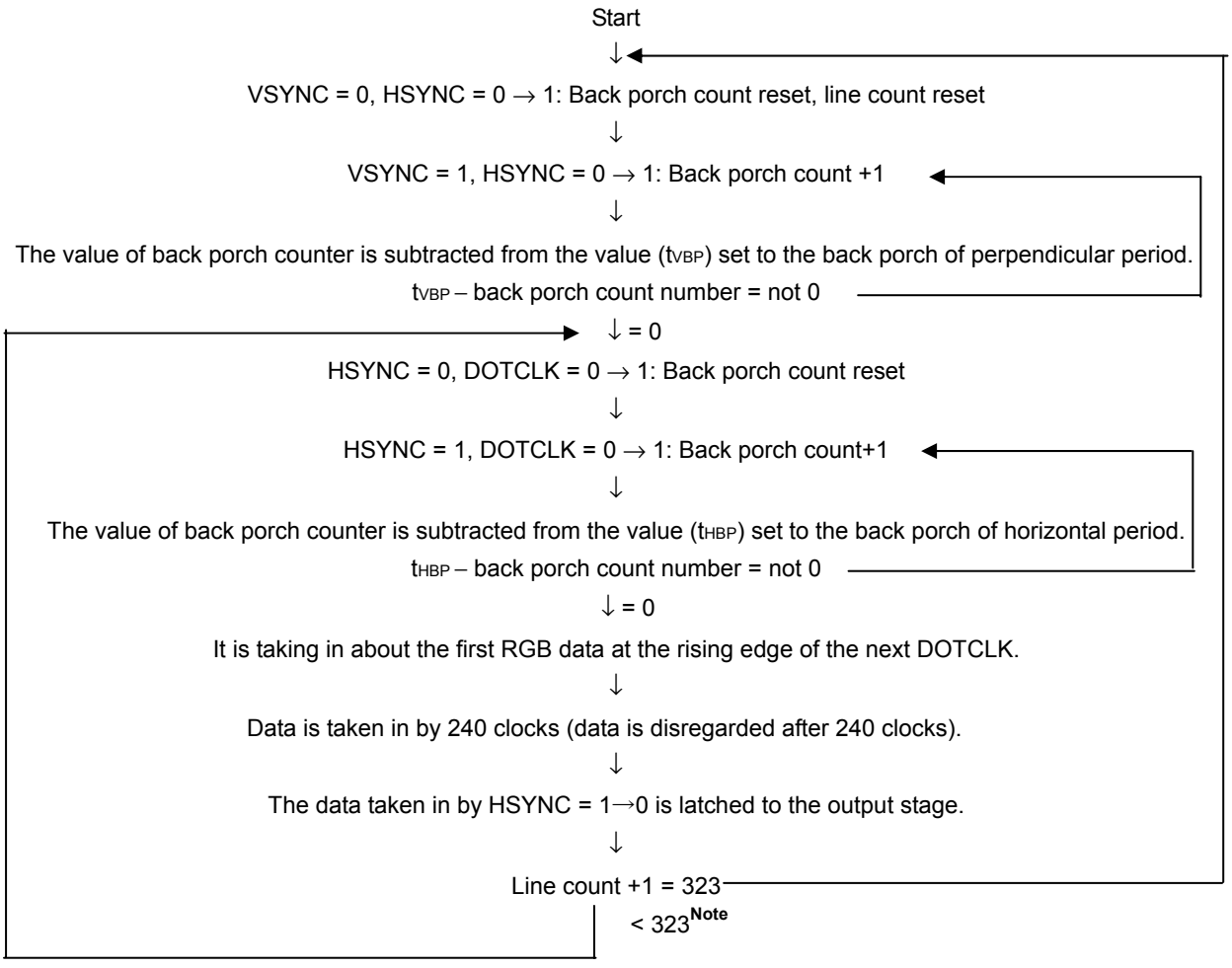
The HSYNC and VSYNC signals establish synchronization in the horizontal and vertical direction, respectively, and data input to the data bus (D_{17} to D_0) is latched in synchronization with DOTCLK. For the electrical specifications, refer to **11. ELECTRICAL SPECIFICATIONS**.

When the RGB interface is selected, the display output timing can be selected from <HSYNC/VSYNC/DOTCLK> or <internal oscillation clock>. It can also be selected whether the data input from the RGB interface is to be written to the display RAM or not.

The mode in which the data input from the RGB interface is not written to the display data RAM and is used for display output is called the through mode (the display output timing is generated by HSYNC/VSYNC/DOTCLK).

The mode in which the data input from the RGB interface is written to the display data RAM for display output is called the capture mode. In the capture mode, the display output timing can be selected from < HSYNC/VSYNC/DOTCLK > or <internal oscillation clock>.

Movement of μPD161704A when making display output timing into <HSYNC/VSYNC/DOTCLK> is as follows.



Note 323 = 320-display line + 3-dummy line

Remark When VSYNC and HSYNC are low active and DOTCLK is latched (VSEG, HSEG and DCKEG pins are L and BPSEL = 0, respectively) about data in the rising edge.

Caution As for low active and VSYNC and HSYNC, DOTCLK latch data by the rising edge when RGB 18/16-bit mode is selected. Moreover, low active is latched by the rising edge of the 3rd shot at the time of RGB 6-bit mode selection, and, as for DOTCLK, VSYNC and HSYNC latch data.

In addition, an RGB data invalid mode is also available. In this mode, data input from a motion picture chip via the RGB interface is ignored. Note that only data input from the RGB interface is ignored in this mode and that access from the i80/M68 parallel interface and serial interface is possible.

<R> However, mode selection operates NWRGB, RGBS, and DISPCK bits of R2 register on shown as follows.

Table 5–4. RGB Interface Mode Selection

R2			RGB Interface		
NWRGB D_2	RGBS D_1	DISPCK D_0	Mode	Display Output Timing Clock	Writing from RGB Interface to Display Data RAM
1	0	0/1	Through mode	HSYNC/VSYNC/DOTCLK	No
1	1	1	Capture mode	HSYNC/VSYNC/DOTCLK	Yes
1	1	0		Internal oscillation clock	
0	0/1	1	RGB data invalid mode	HSYNC/VSYNC/DOTCLK	No
		0		Internal oscillation clock	

When capture mode is selected, DOTCLK is used as a write-in signal to a display data RAM. In addition, X addresses of an address pointer are reset by the HSYNC signal, and an increment is carried out by DOTCLK. Y address is reset by the VSYNC signal and an increment is carried out by HSYNC signal.

The blanking period can be set by the horizontal back porch register and vertical back porch register. When in RGB 6-bit mode, the value which increased the value of a level back porch register 3 times comes back porch period.

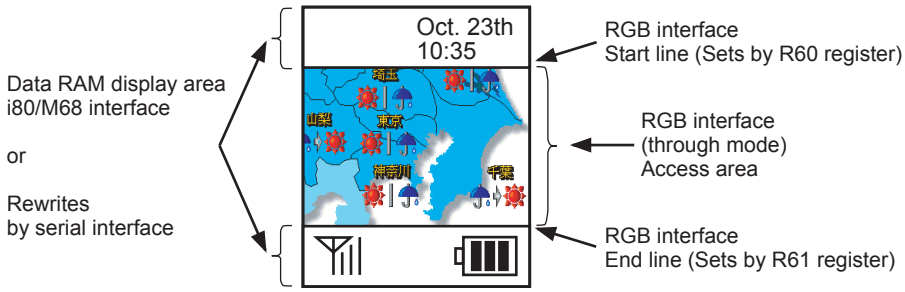
The active levels of HSYNC and VSYNC can be set. In addition, the active level of DOTCLK can also be set. In the through mode, however, the partial function and window access mode cannot be used.

[Example of using RGB interface]

<Through mode>

In the through mode, the area to be displayed by the RGB interface is specified by the RGB interface start line register (RGBST [8:0], R16) and RGB interface end line register (RGBED [8:0], R17). The data written to the display data RAM are displayed in areas other than the RGB interface area. In the through mode, the display data RAM and registers can be accessed (written or read) by the i80/M68 interface or serial interface when an access is made by the RGB interface.

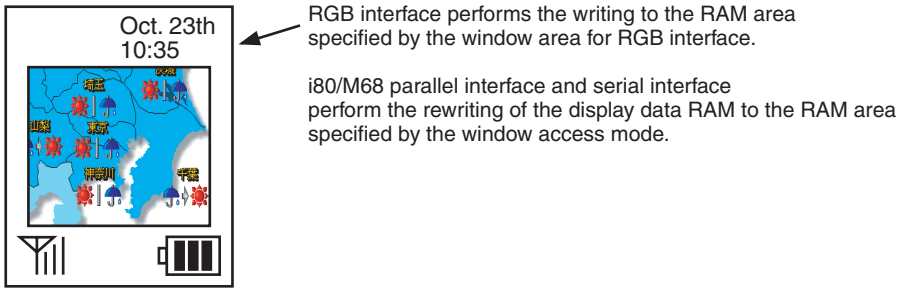
Therefore, an operation such as rewriting the time or antenna by a base band IC while inputting motion picture data from a DSP via the RGB interface can be performed.



<Capture mode>

In the capture mode, the area set in the window access mode is written by the RGB interface (CAPXMIN [7:0], CAPXMAX [7:0], CAPYMIN [8:0], CAPYMAX [8:0], R18 to R21).

Even in this mode, the i80/M68 parallel interface or serial interface, which are shared with the RGB interface, can be used. Note, however, that data can be written to a register while the RGB interface is accessed, but that the RAM cannot be accessed. Make sure that only one of these accesses is made (shift to the RGB data invalid mode so that RGB data is not input).

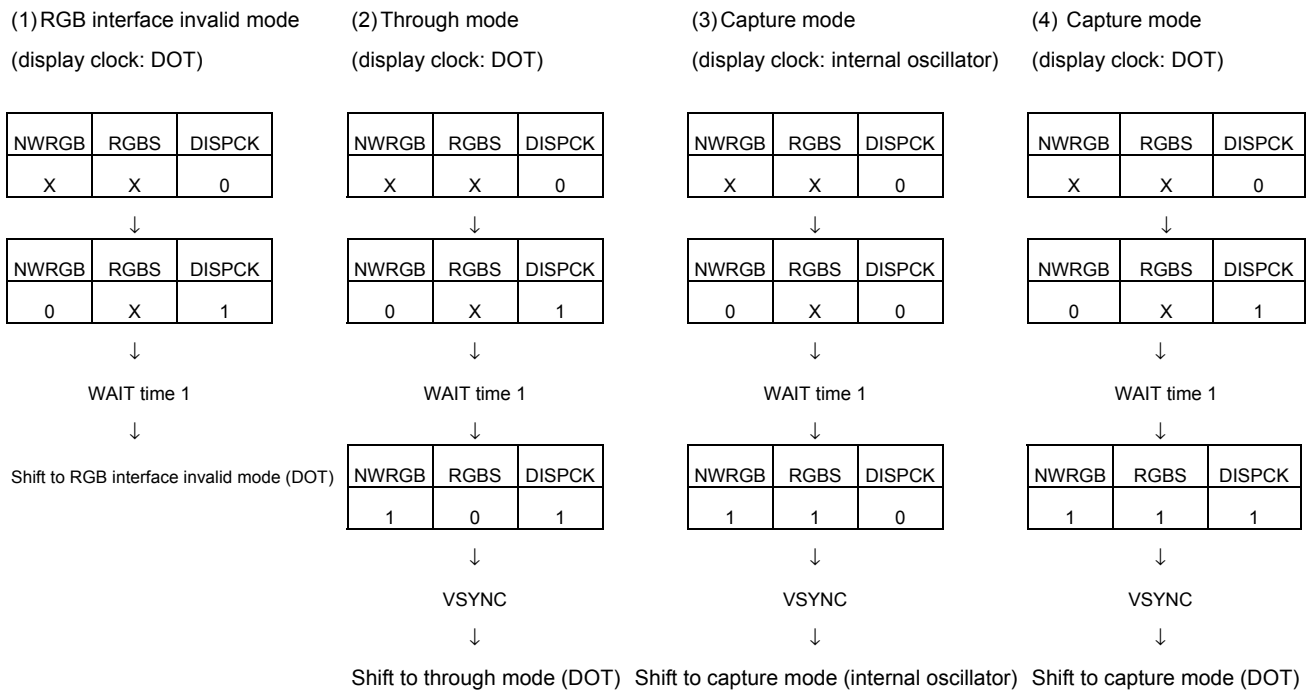


<Notes on using RGB interface>

<1> Be sure to input data from the RGB interface every frame.

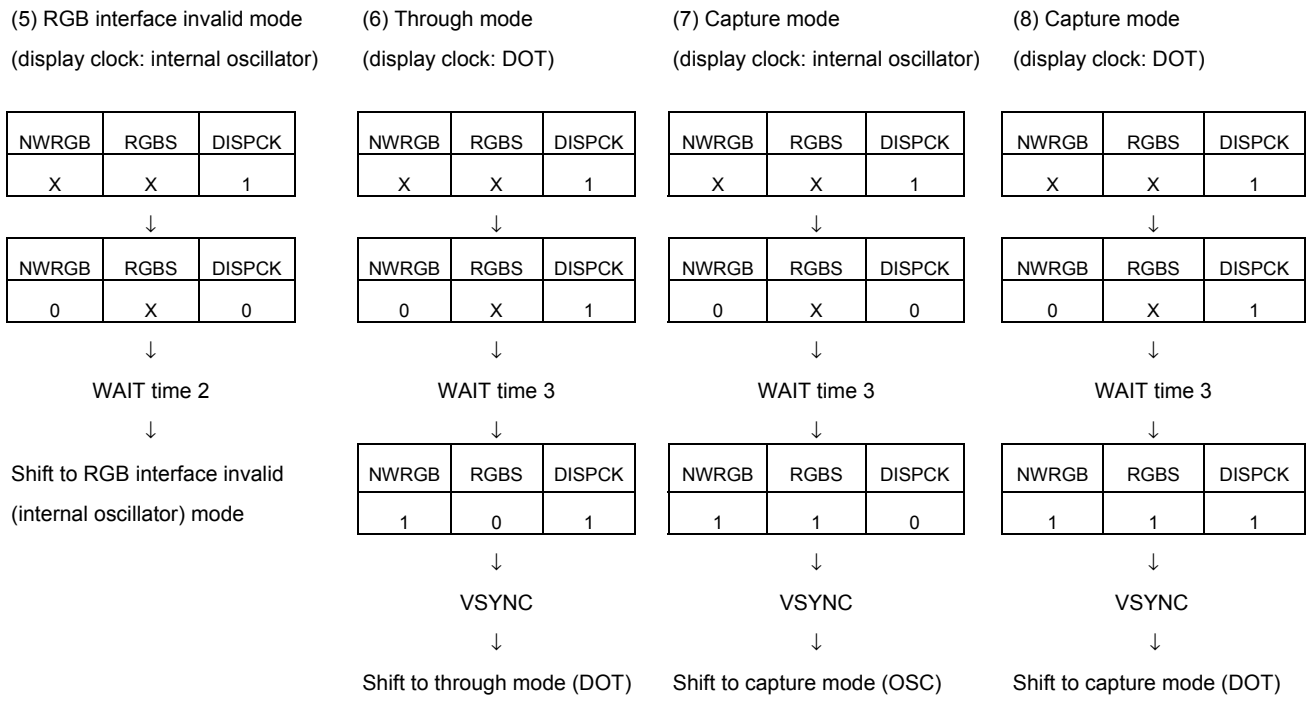
<2> When changing the mode (e.g., from the through mode to the capture mode, and vice versa), issue defined mode of selection command after once always setting RGB invalid mode.

<3> It is a shift flow from the time of internal oscillation use (DISPCK [R2] = 0) to each mode as a display clock.



Remark WAIT time 1: Set sufficient time of one or more frames.

<4> It is a shift flow from the time of DOTCLK use (DISPCK [R2] = 1) to each mode as a display clock.



Remarks 1. WAIT time 2: External clock for two frames is required.

2. WAIT time 3: External clock + VSYNC for one frame is required.

<5> Data (back porch period is included) of one line should be set within the period of HSYNC to HSYNC.

<6> Data (back porch period is included) of one frame should be set within the period of VSYNC to VSYNC.

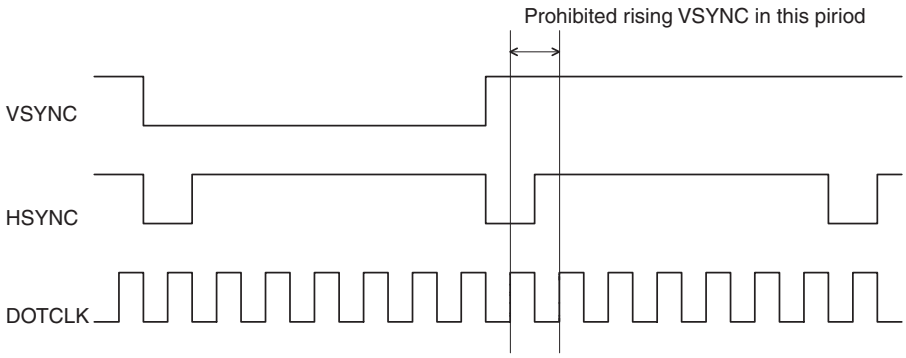
<7> INC function cannot be used about the writing to the display data RAM at the time of capture mode. However, ADX and an ADR function can be used.

<8> A setup of XA [7:0], YA [8:0], XMN [7:0], XMX [7:0], YMN [8:0], YMX [8:0], R6 to R11 is invalid at the time of RGB interface mode (since these are set up of CPU interface).

<9> The period from "the DOTCLK standup after falling of HSYNC" to "the standup of DOTCLK after HSYNC standup" should not start VSYNC. For more details, refer to the next Figure 5–24.

<R> **Figure 5–24. Example of HSYNC, VSYNC, and DOTCLK Input Timing (both HSYNC and VSYNC are low active, and data latch by DOTCLK rising edge)**

(1) BPSEL = 0



(2) BPSEL = 1

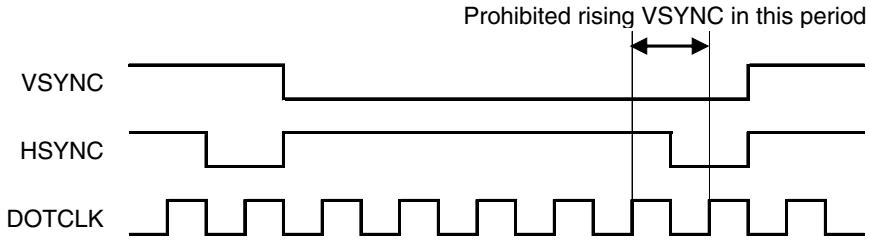


Figure 5–25. HSYNC and VSYNC Input Image Figure (when both HSYNC and VSYNC are high active)

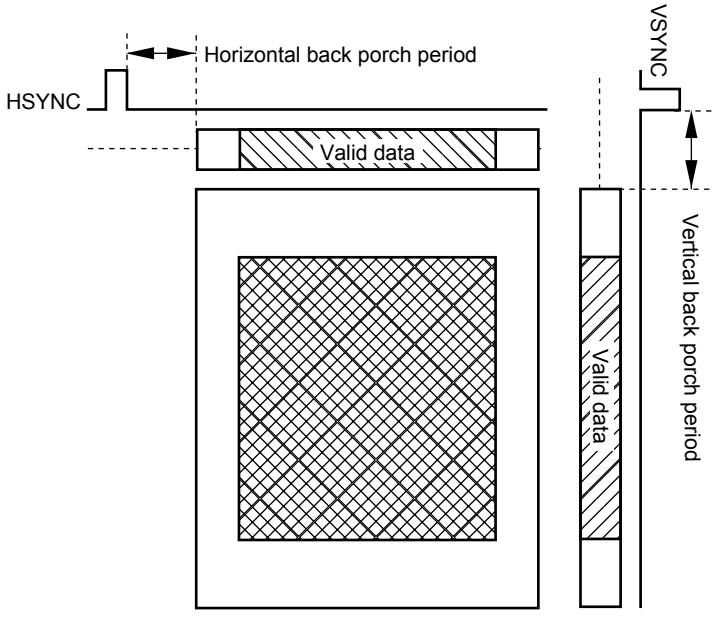
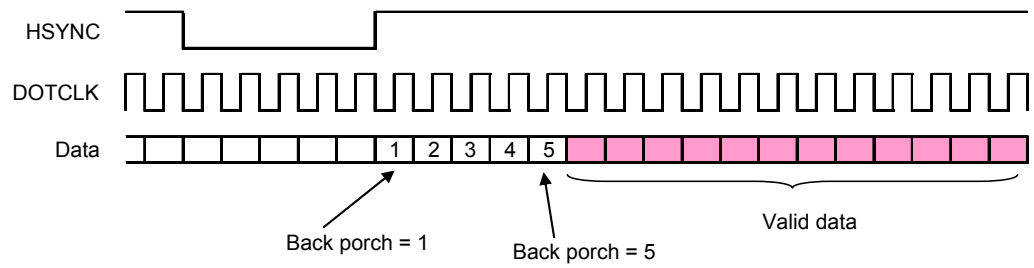


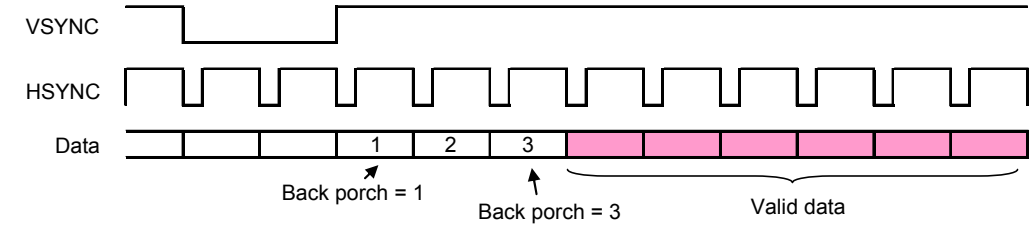
Figure 5–26. RGB Interface Horizontal Period and Vertical Period Back Porch

Horizontal period back porch (Example of back porch number = 5)

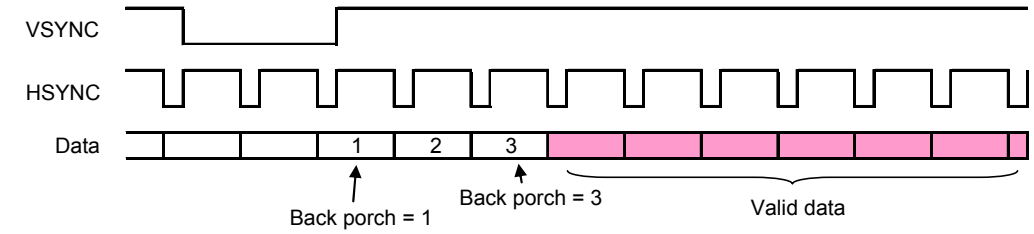


Vertical period back porch (Example of back porch number = 3)

BPSEL (R112) = 20H



BPSEL (R112) = 21H



5.1.4 i80/M68 parallel interface (Each common register mode)

When the parallel interface has been selected, setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (Refer to Table 5–5 below).

Table 5–5.

C86	Mode	/RD (E)	/WR (R,/W)
H	M68 series CPU	E	R, /W
L	i80 series CPU	/RD	/WR

The data bus signal is identified according to the combination of the /RD (E), and /WR (R,/W) signals, as shown in the following Table 5–6.

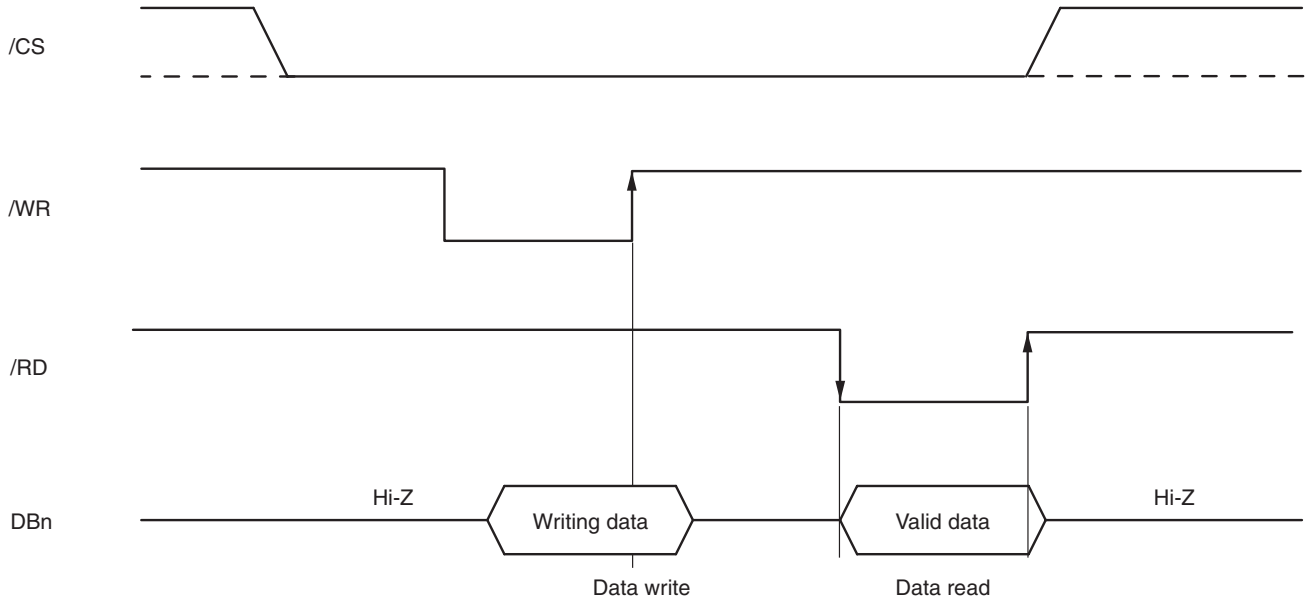
Table 5–6.

M68 Series CPU	i80 Series CPU		Function
R,/W	/RD	/WR	
H	L	H	Read display data
L	H	L	Write display data

(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μPD161704A at L period of the /WR signal. The data is output to the data bus when the /RD signal is L.

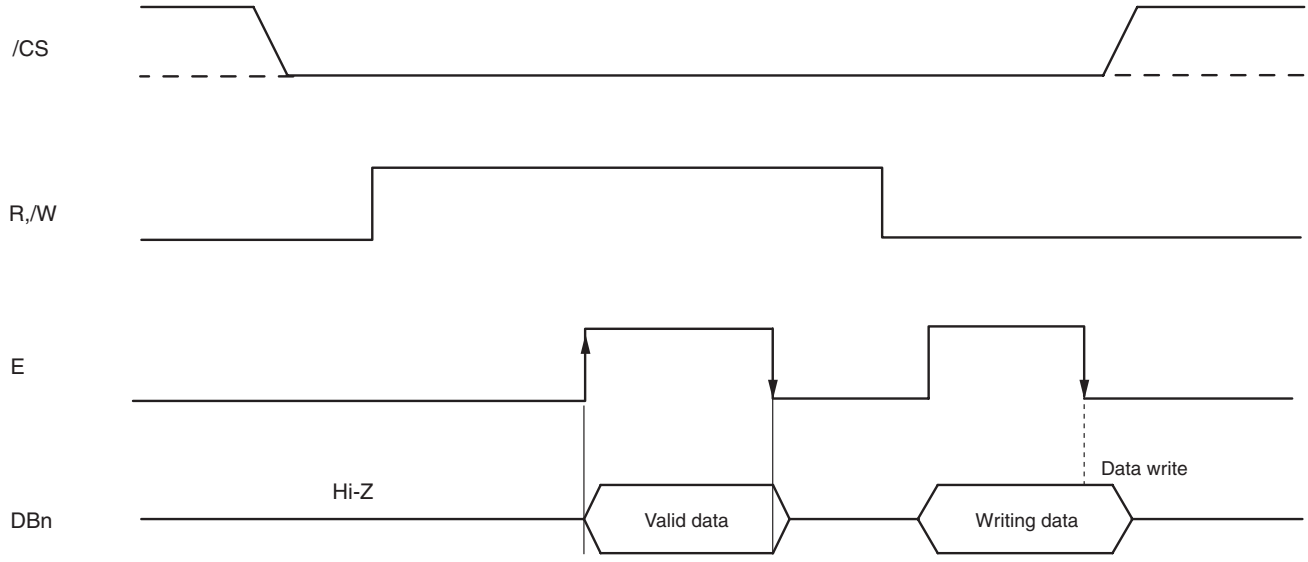
Figure 5–27. i80 Series Interface Data Bus Status



(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the H period of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

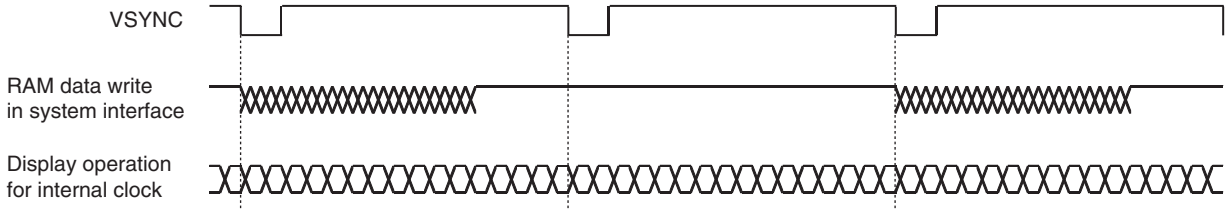
Figure 5–28. M68 Series Interface Data Bus Status



5.1.5 VSYNC interface (Each common register mode)

The VSYNC interface in which the video display is possible is built in only by i80/M68 conventional parallel interface and a conventional frame synchronized signal (VSYNC).

By setting up with VIMD = 1, VSYNC interface comes usable. In VSYNC interface, internal display operation is synchronized by the frame synchronized signal (VSYNC). From i80/M68 interface, it abolishes that the data before rewriting and the data after rewriting are intermingled in one frame by writing display data in RAM at a write-in speed more than fixed speed from internal display operation.



In addition, if VSYNC comes active, being simultaneous (the above figure falling of VSYNC), when the writing from a system interface to RAM begins to be performed, it is necessary to write in data above the speed computed by the following expression of relations.

<R> In this mode, secure to keep width over 1 H MIN. for VSYNC active width.

[RAM write-in speed]

RAM write-in speed (MIN.) [Hz] < 1/ {one-line time (calibration time) / the number of one-line write-in data}

Remark The number of 1 line write-in data is the number of data for one line transmitted from CPU.

[Example 1 of calculation] When writing in data of 320 pixel of 240 RGB,

- Rewriting pixel size : 240 RGB x 320
- Interface : 16-bit package transmission
- One-line time : 51 μs (frame frequency of 60 Hz)

RAM write-in speed minimum value = 1/ (51 μs/240) = 4.62 MHz (when not taking variation in a calibration into consideration)

5.1.6 Serial interface (Each common register mode)

When the serial interface has been selected, if the chip is active (/CS = L), serial data input (SI) and serial clock input (SCL) can be received. When 18-bit serial interface is used, serial data is read from D_{17} and then from D_{16} to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighteenth serial clock's rising edge and is then converted to parallel data for processing.

When 16-bit serial interface is used, serial data is read from D_{15} and then from D_{14} to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the sixteenth serial clock's rising edge and is then converted to parallel data for processing.

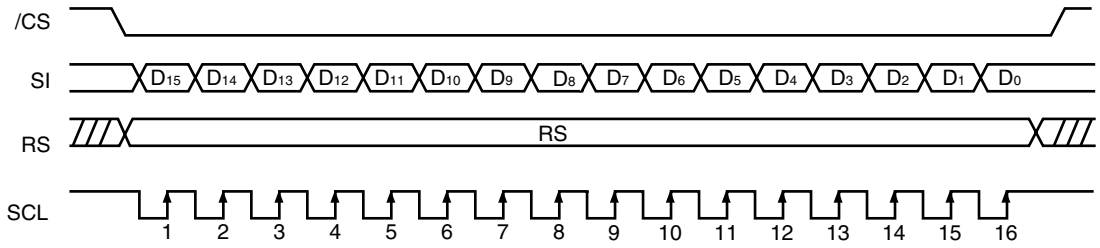
Also, like using parallel interface, serial interface can judge what it is by RS input.

RS = L	RS = H
Index	Data

Remark When it writes in display RAM, it is possible by selecting specified register number same as register.

The serial interface signal chart is shown below.

Figure 5–29. Serial Interface Signal Chart (16-bit serial interface)



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

2. The data read function is disabled during serial interface mode.

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. We recommend checking operation with the actual device.

5.1.7 Chip select (Each common register mode)

The μPD161704A has a chip select pin (/CS). The CPU parallel interface and serial interface can be used only when /CS = L. When the chip select pin is inactive, D_0 to D_{17} are set to high impedance (invalid) and input of RS, /RD, or /WR is not active.

Therefore, keep the chip select pin active for 1 cycle period of data transfer (until a read/write operation has been completed once in the parallel interface mode).

It is not necessary to keep the chip select signal active when successively transferring data. It may be non-active between data transfer operations.

5.1.8 Access to display data RAM and internal registers (Each common register mode)

Figures 5–30 to 5–34 show read/write accesses to the display data RAM and write accesses to internal registers 8-, 16-, and 18-bit parallel interface modes and serial interface mode.

Note that the display data RAM and registers can't read operation in the serial interface mode.

When the CPU accessed the μPD161704A, the CPU only has to satisfy the AC standard requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take WAIT time into consideration.

However, in the vertical writing (INC = 1) which an address is changed in the direction of Y and written in it, note that the cycle time is severe rather than the case of the horizontal writing (INC = 0).

Figure 5–30. Read/Write in 16-/18-Bit Parallel Interface Mode

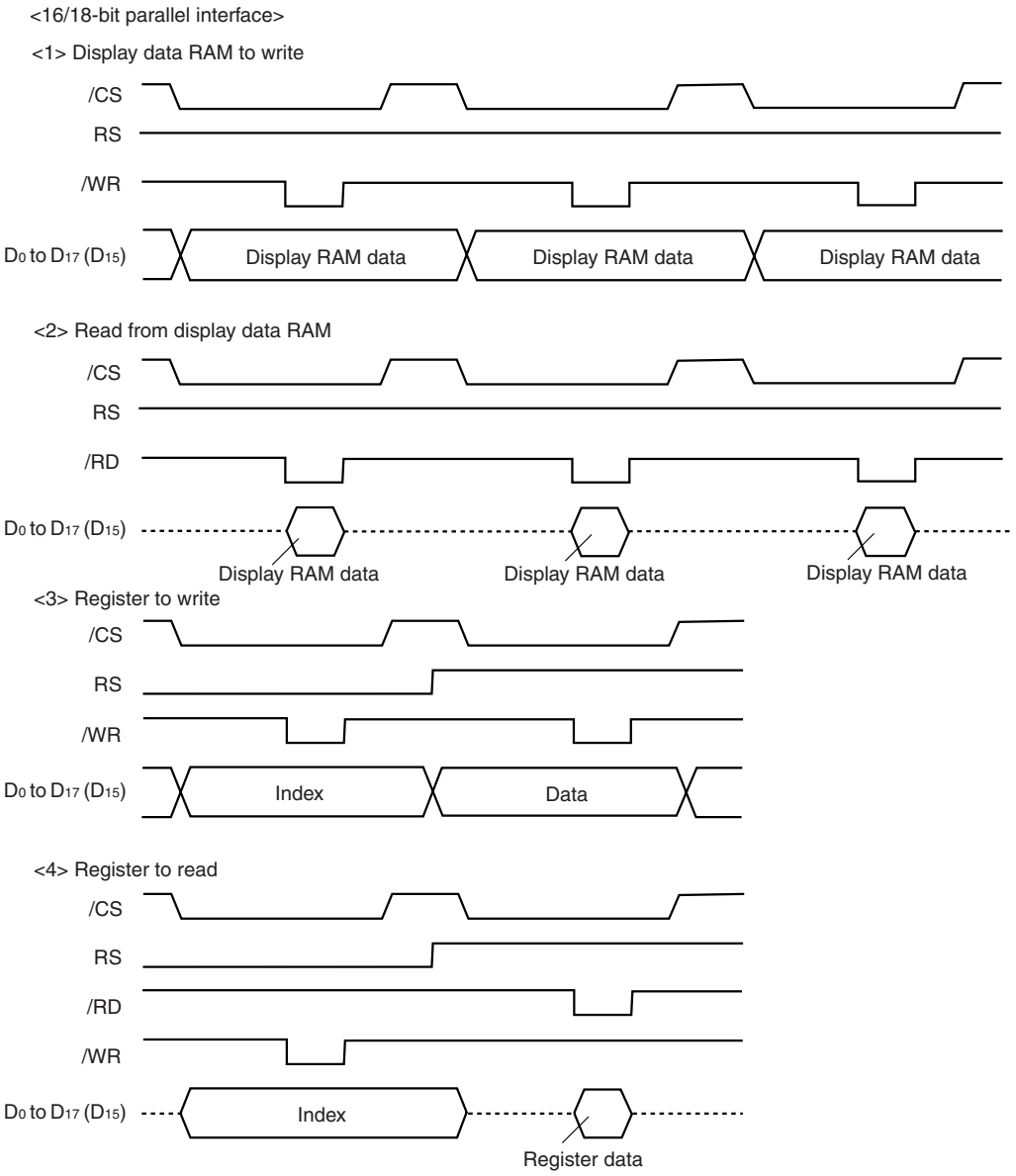
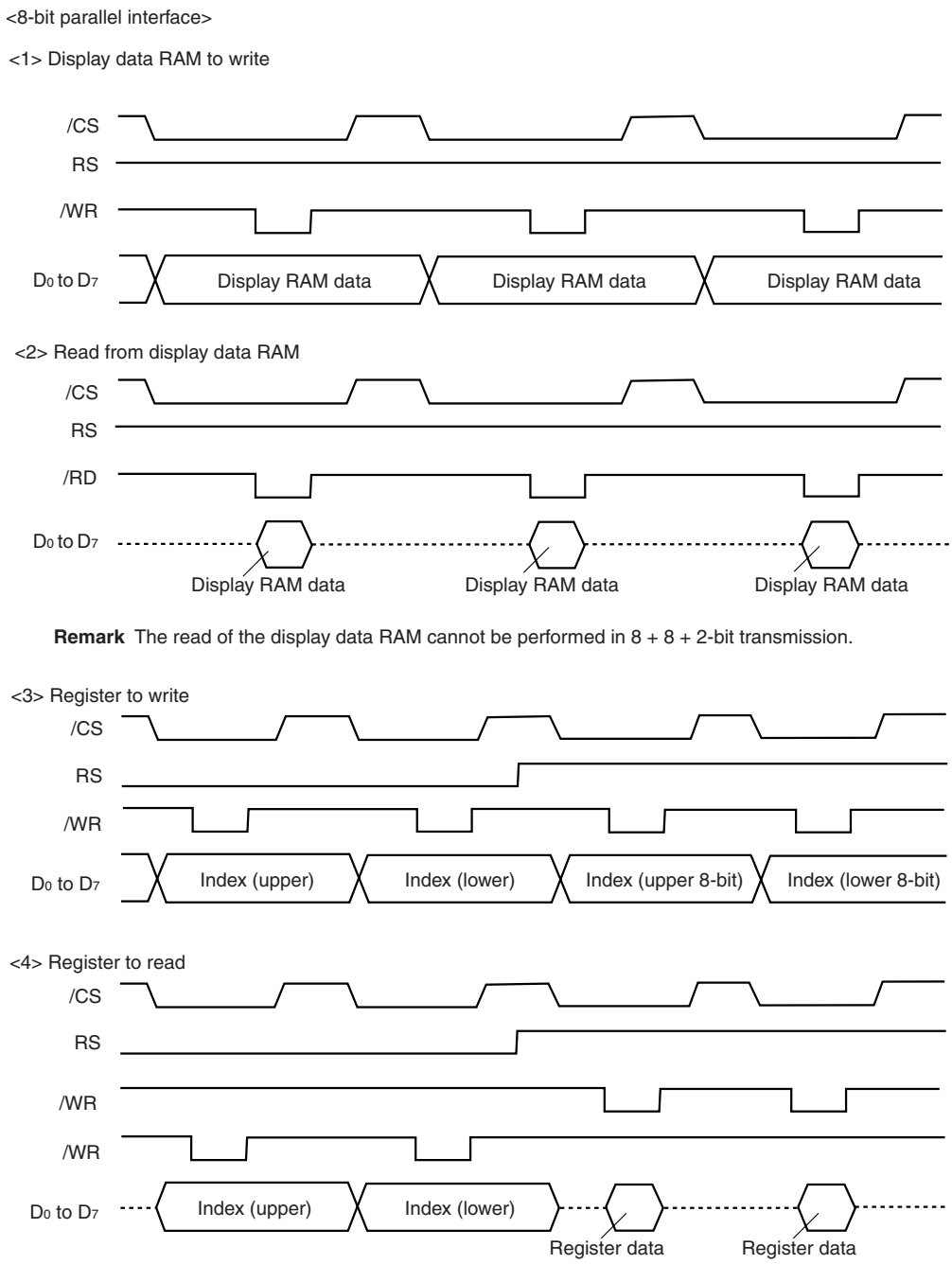


Figure 5–31. Read/Write in 8-Bit Parallel Interface Mode



Remark The read of the display data RAM cannot be performed in 8 + 8 + 2-bit transmission.

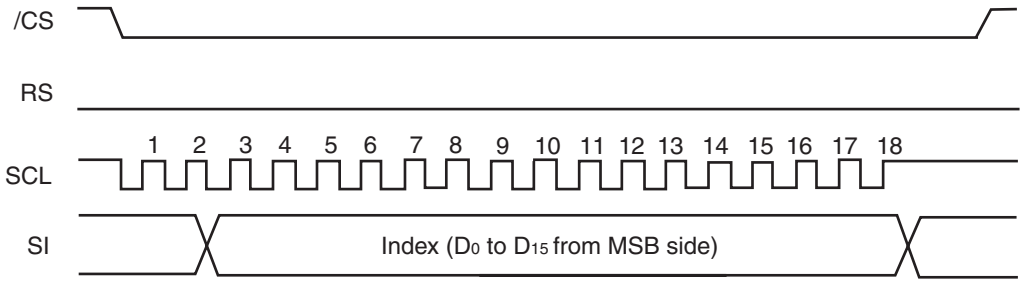
Cautions 1. While setting the writing to a register, set it the fixed input of the low level to RS pin. While setting the writing to a register, "index (upper 8 bit) + (bottom 8 bit)" period is pointed out.

2. While setting the writing to display data RAM, set it the fixed input of the high level to RS pin. While setting the writing to display data RAM, a "data transfer for 1 pixel (1 register)" period is pointed out.

3. When use 8-bit parallel interface, RS pin always start transfer after hard reset release, after set up 100 ns MIN. input of high level.

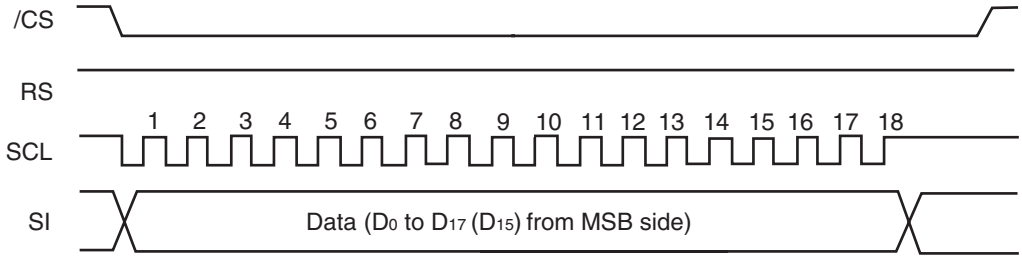
Figure 5–32. 18-bit Serial Interface Mode

<1> Index to write



Remark 16 bits of lower are used as an index among serial input data.

<2> Data to write



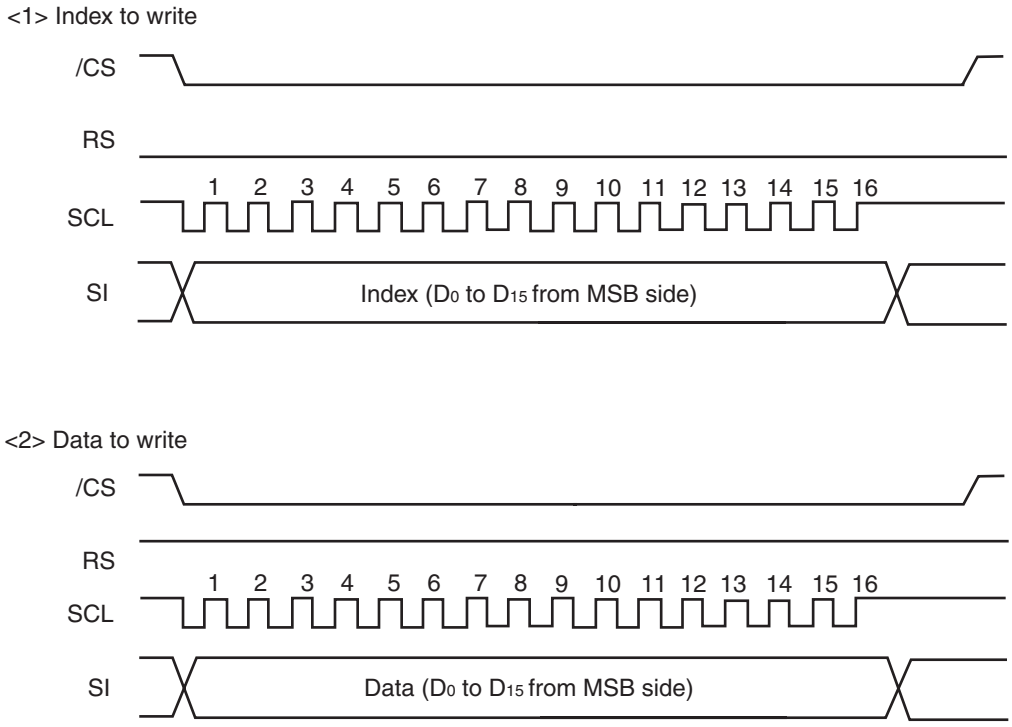
Remark In the case of register data, 16 bits of lower of serial data are used.

Cautions 1. While setting the writing to index, set it the fixed the low level to RS pin.

2. While setting the writing to data, set it the fixed output of the high level to RS pin.

3. When write in register, setting value of D_{17} and D_{16} are assigned to empty (Don't care) bit.

Figure 5–33. 16-bit Serial Interface Mode

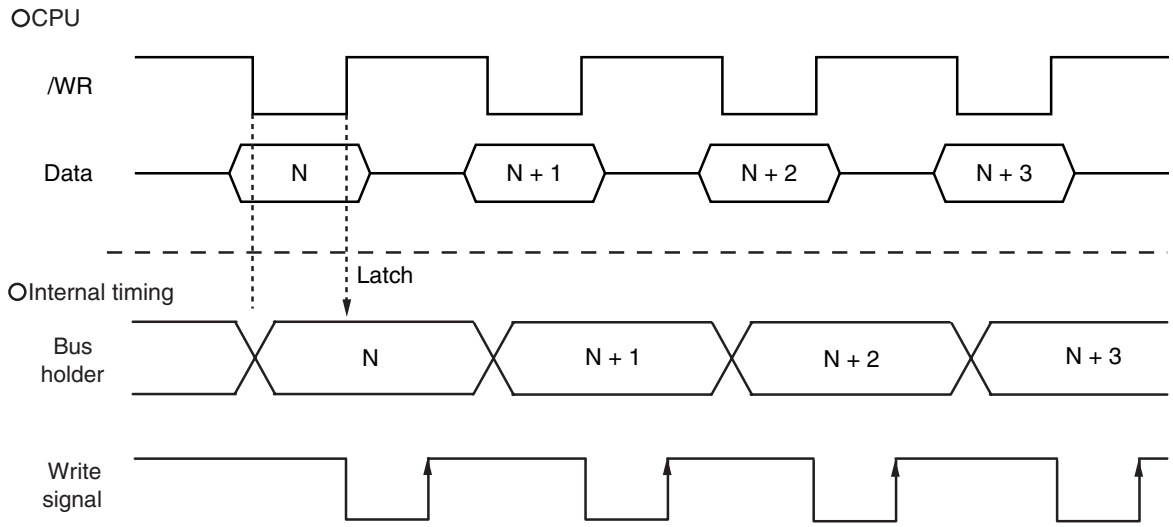


Cautions 1. While setting the writing to index, set it the fixed output of the low level to RS pin.

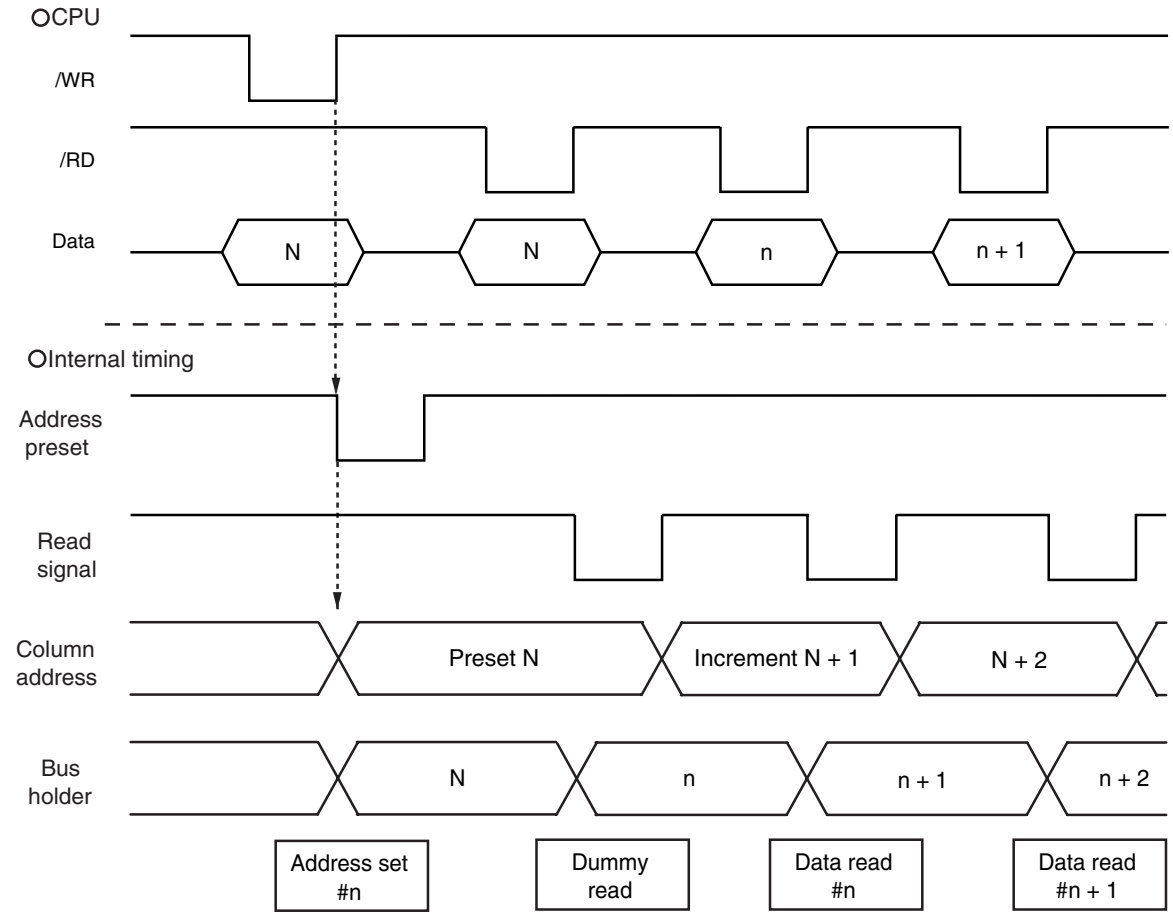
2. While setting the writing to data, set it the fixed output of the high level to RS pin.

Figure 5–34. Image of Internal Access to Display RAM

Writing



Reading



5.2 Display Data RAM (Each common register mode)

This RAM stores dot data for display and consists of 240 x 320 x 18 bits. Any address of this RAM can be accessed by specifying X address and Y address.

Display data RAM construction refers to Figure 5–35.

Figure 5–35. Display Data RAM

D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R data						G data						B data					
Pixel 1 (= 1 X address)																	

LCD panel									
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	00H	01H	02H	03H	04H	05H	06H	07H	

5.2.1 X address circuit

X address of the display data RAM is specified by using the X address register (XA [7:0], R6) as shown in Figure 5–36.

The specified X address is incremented by one each time display data is written or read.

In the X address increment mode, the X address is incremented up to EFH. If more display data is written or read, the Y address is incremented, and the X address returns to 00H.

The relationship between the X address and source output can be inverted by the ADX [R1] flag of the display setting register 2 as shown in Figure 5–36. The input data can be rotated 90 degrees and displayed by changing the ADY function and address increment direction between X and Y.

5.2.2 Y address circuit

Y address of the display data RAM is specified by using the Y address register (YA [8:0], R7).

The Y address is incremented each by one when one each time display is written or read and X address is incremented to last address.

When the Y address has been incremented up to 13FH and the X address up to the final address, if further display data is read or written, the X address return to 00H and Y addresses return to 000H.

As shown in Figure 5–36, the relationship between the Y address and gate output can be inverted by the ADY [R1] flag of the display setting register 2. The data written to the display can be rotated 90 degrees and output by changing the ADX function and address increment switch direction between X and Y.

Table 5–7. Data Access Control (INC) Setting

INC [R5]	Setting
0	When data access, X directions an address continuing an increment or a decrement is carried out.
1	When data access, Y directions an address continuing an increment or a decrement is carried out.

Figure 5–36. Example of 90-Degree Rotation

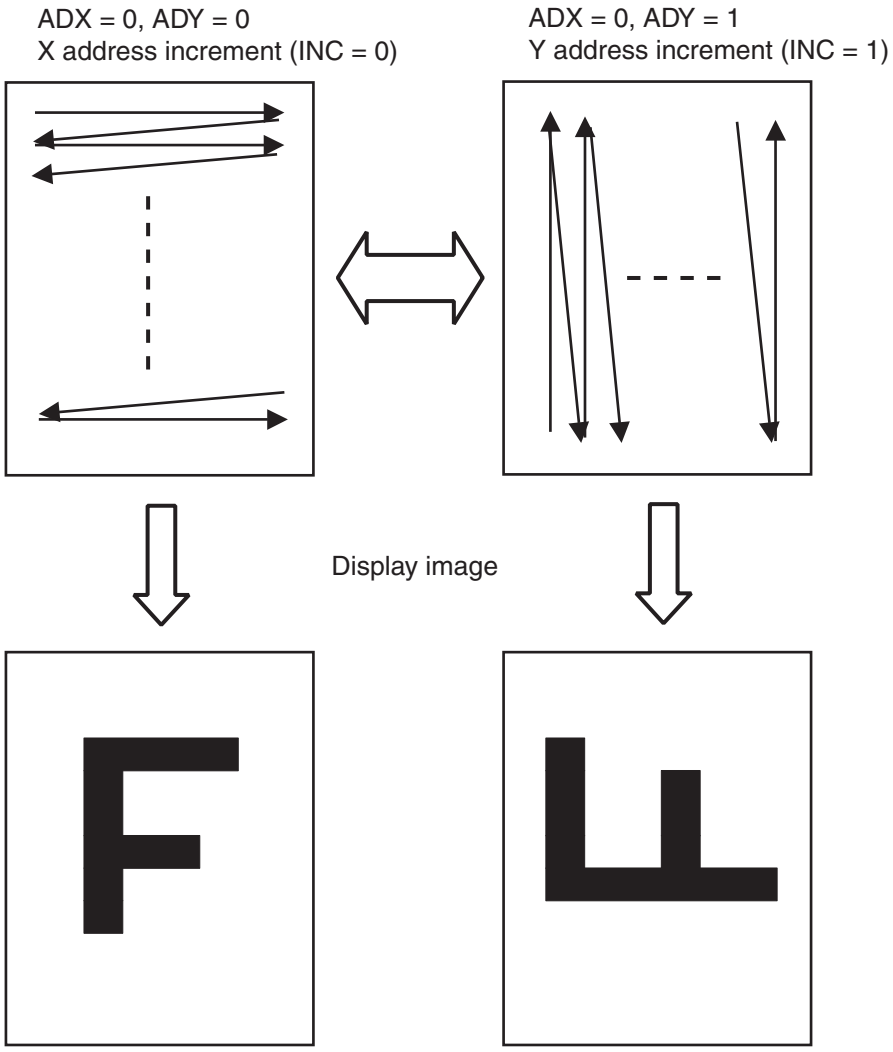
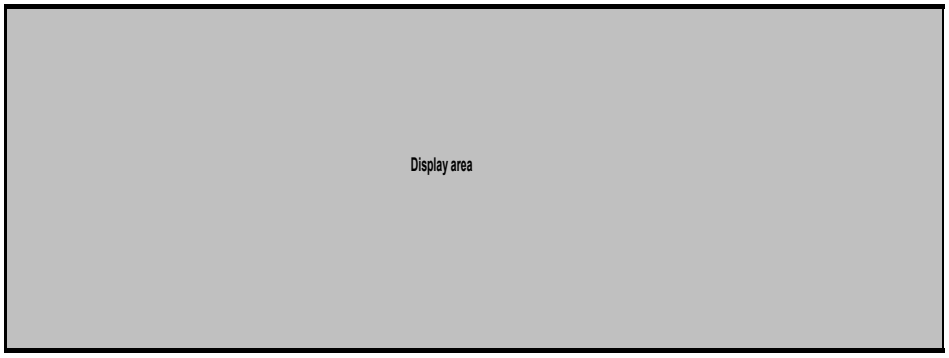


Figure 5–37. The μPD161704A RAM Addressing

1) ADX = 0

Source output	ADC = L	Y1	Y2	Y3	Y4	Y5	Y6	---	---	Y715	Y716	Y717	Y718	Y719	Y720
	ADC = H	Y720	Y719	Y718	Y717	Y716	Y715	---	---	Y6	Y5	Y4	Y3	Y2	Y1
	X-address	000H			001H			---	---	13EH			13FH		
		D [17:12]	D [11:6]	D [5:0]	D [17:12]	D [11:6]	D [5:0]	---	---	D [17:12]	D [11:6]	D [5:0]	D [17:12]	D [11:6]	D [5:0]
		1st pixel			2nd pixel			---	---	239th pixel			240th pixel		

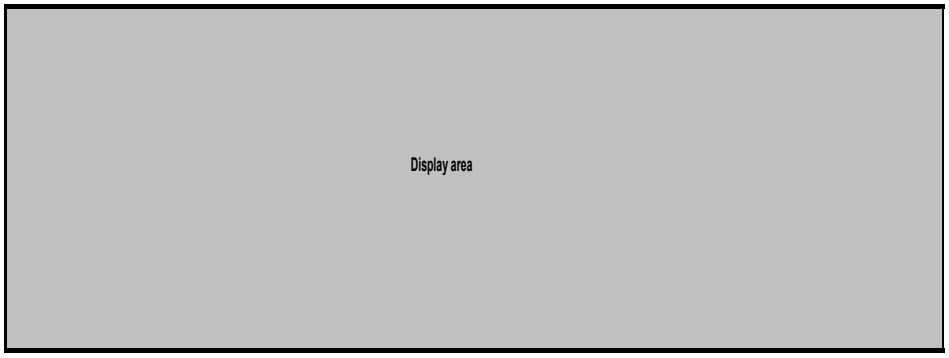
Gate output			
R,/L = L	R,/L = H	Y-address	
		ADR = L	ADR = H
G0	G321	(Dummy line)	
G1	G320	000H	13FH
G2	G319	001H	13EH
:	:	:	:
:	:	:	:
G159	G162	09EH	0A1H
G160	G161	09FH	0A0H
G161	G160	0A0H	09FH
G162	G159	0A1H	09EH
:	:	:	:
:	:	:	:
G319	G2	13EH	001H
G320	G1	13FH	000H
G321	G0	(Dummy line)	



2) ADX = 1

Source output	ADC = L	Y1	Y2	Y3	Y4	Y5	Y6	---	---	Y715	Y716	Y717	Y718	Y719	Y720
	ADC = H	Y720	Y719	Y718	Y717	Y716	Y715	---	---	Y6	Y5	Y4	Y3	Y2	Y1
	X-address	13FH			13EH			---	---	001H			000H		
		D [17:12]	D [11:6]	D [5:0]	D [17:12]	D [11:6]	D [5:0]	---	---	D [17:12]	D [11:6]	D [5:0]	D [17:12]	D [11:6]	D [5:0]
		240th pixel			239th pixel			---	---	2nd pixel			1st pixel		

Gate output			
R,/L = L	R,/L = H	Y-address	
		ADR = L	ADR = H
G0	G321	(Dummy line)	
G1	G320	000H	13FH
G2	G319	001H	13EH
:	:	:	:
:	:	:	:
G159	G162	09EH	0A1H
G160	G161	09FH	0A0H
G161	G160	0A0H	09FH
G162	G159	0A1H	09EH
:	:	:	:
:	:	:	:
G319	G2	13EH	001H
G320	G1	13FH	000H
G321	G0	(Dummy line)	



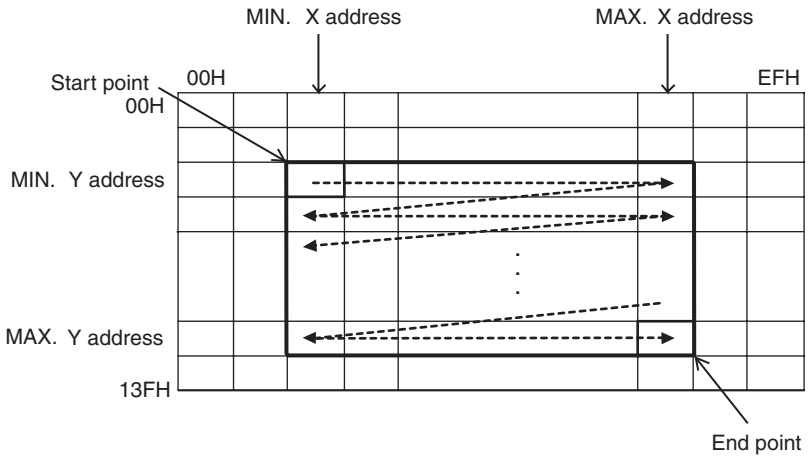
5.2.3 Arbitrary address area access (Window access mode (WAS))

With the μPD161704A, which can also access only the RAM address area specified arbitrarily.

First, select the area to be accessed by using the MIN.·X/Y address registers [R8, R10] and MAX.·X/Y address registers [R9, R11]. When WAS [R5] of data access control register is set to 1, the window access mode is then selected. The address scanning setting is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register and Y address register.

The data input from the RGB interface in the through mode of the RGB interface cannot be used in the window access mode.

Figure 5–38. Example of Incrementing Address when in Window Access Mode



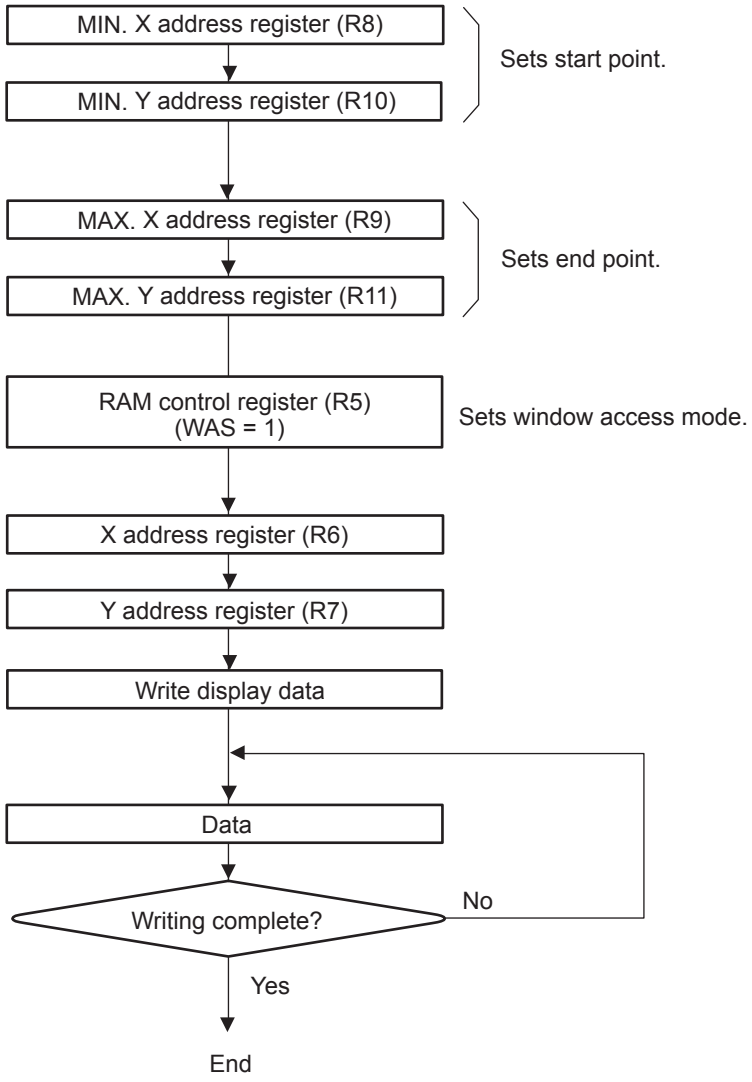
Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

Item	Address Relationship
X address	00H ≤ MIN.·X address [R8] ≤ X address (XA [7:0]< R6) ≤ EFH 00H ≤ X address (XA [7:0], R6) ≤ MAX.·X address [R9] ≤ EFH However, MIN.·X address [R8] < MAX.·X address [R9]
Y address	00H ≤ MIN.·Y address [R10]≤ Y address (YA [8:0], R7) ≤ 13FH 00H ≤ Y address (YA [8:0], R7) ≤ MAX.·Y address [R11] ≤ 13FH However, MIN.·Y address [R10]< MAX.·Y address [R11]

2. If invalid address data is set as the MIN./MAX.· address, operation is not guaranteed.

A set up of MIN.·X address register, MIN.·Y address register, MAX.·X address register, MAX.·Y address register can be set up in any order different.

Figure 5–39. Example of Sequence in Window Access Mode

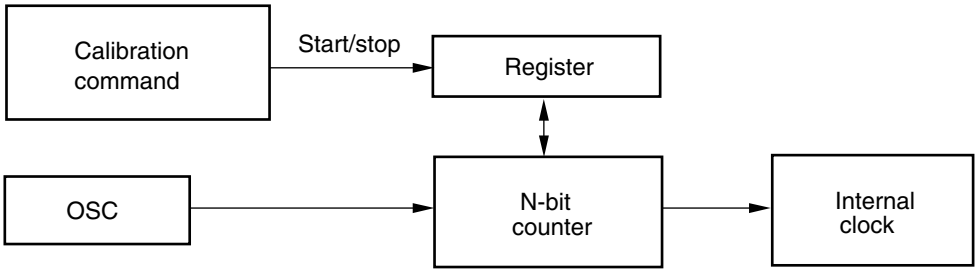


5.3 Oscillator (Each common register mode)

The μPD161704A has a CR oscillator (with external R), which generate the display clock. When OSCSEL is L, an internal resistance mode for oscillator is selected. On the other hand, leave both OSCIN and OCSOUT pin open. When OSCSEL is H, an external resistance mode for oscillator is selected. At the time of external resistance mode, connect 36 kΩ on resistance between OSC_{IN} and OSC_{OUT} pin.

This oscillator also has a calibration function, which is available by itself to set the number of frame frequency of display driving. Frame frequency calibration is set by calibration register (OC [R45]). The time to drive one line (1H) is set by the calibration start (OC = 1) and stop (OC = 0) commands.

Figure 5–40. Frame Frequency Calibration

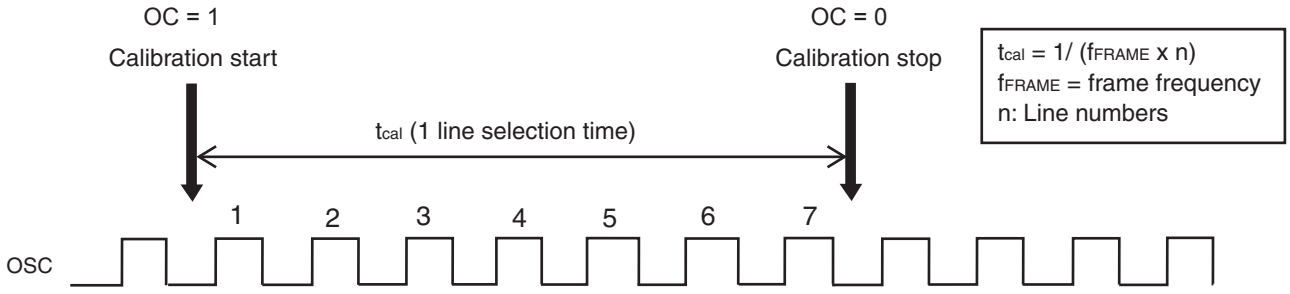


The calibration function involves counting the clock number of oscillation circuit generated between the start and stop signals (set as OC = 1) and storing that number in a register. The number of oscillation clocks is then continually compared with this register value in subsequent operations, and the time of the clock number stored in the register is set as 1 line selection time, and used as the internal reference clock.

By this function, even if the frequency of an oscillation circuit varies, frame frequency can be kept constant.

Using the time to set calibration (t_{cal}) can be selected either t_{cal} or t_{cal} x 2 through LTS [R1] register.

Figure 5–41. Calibration Function Timing (LTS = 0)



5.4 Display Timing Generator (Each common register mode)

The display timing generator generates the timing signals for the internal timing of the source driver and for the gate driver.

5.4.1 Horizontal period

Each following signal is controlled by register setup.

<GOE1 signal>

GOE1 standup timing register [GOST [7:0]] GOE1 falling timing register [GOED [7:0]] performs output timing control of GOE1 signal.

<VCOM signal>

It changes commonly, VCOM changes by the timing register [VMCHG [7:0]], and timing is controlled.

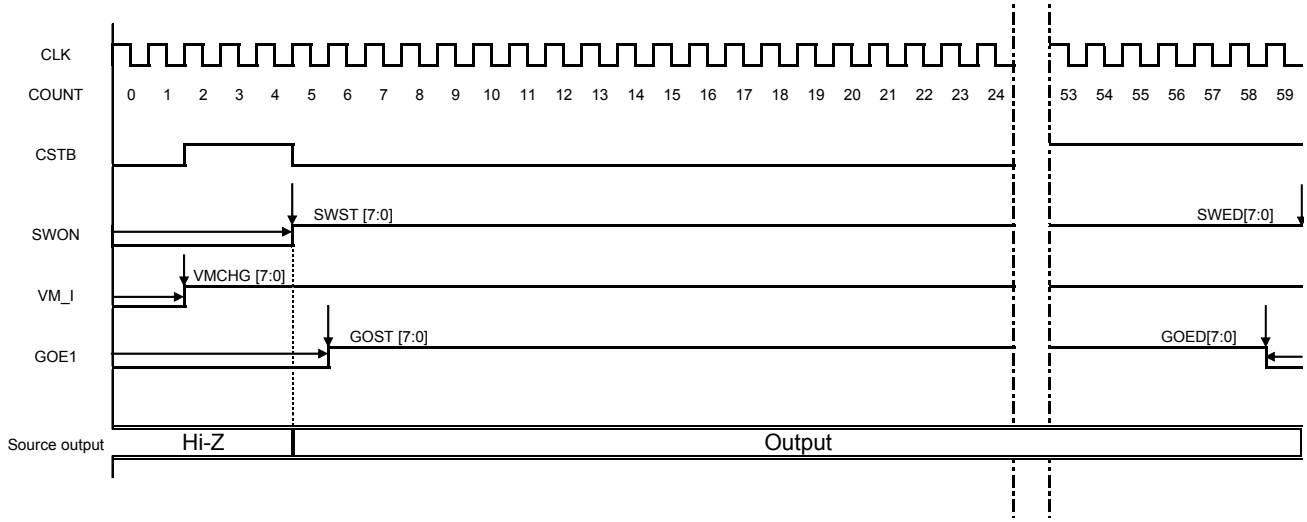
<Driving start timing>

A drive start and end timing are set up by the drive timing register [SWST [7:0], SWED [7:0]].

In addition, about SWST [7:0], VMCHG [7:0], and GOST [7:0], it sets of a level period up to what clock a signal changes flatly period (left side from 0 clock on below figure). Moreover, SWED [7:0] and GOED [7:0] set up to what count a signal changes from the last of a level.

Remark The setting value of GOST [7:0] and SWST [7:0] comes the same operation as an initial value, when the value below an initial value is set up.

<R> Horizontal period timing chart



Caution The Horizontal period is decided by setting the number of direct level period clocks as BCNT [7:0] of a calibration or calibration register. In addition, although arbitrary values can usually be set up, when the DOTCLK display of the RGB interface is used, set up BCNT [7:0] register with [3BH]. The display may be confused when a setup of those other than BCNT [7:0] = 3BH is performed at the time of the DOTCLK display of the RGB interface.

5.4.2 Vertical period

The output timings for normal operation, for normal operation → STBY input mode, for STBY status → return to normal operation, are shown figure as follows.

Figure 5–42. During Normal Operation (during line inversion)

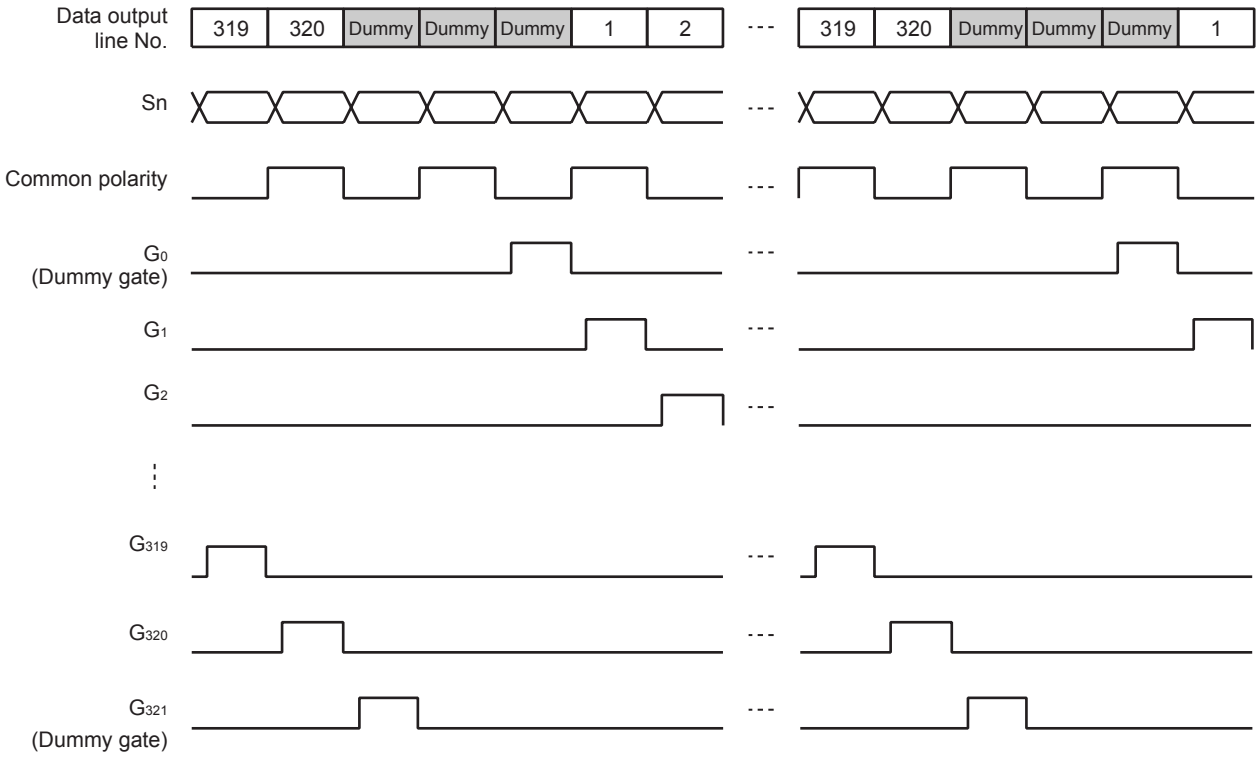
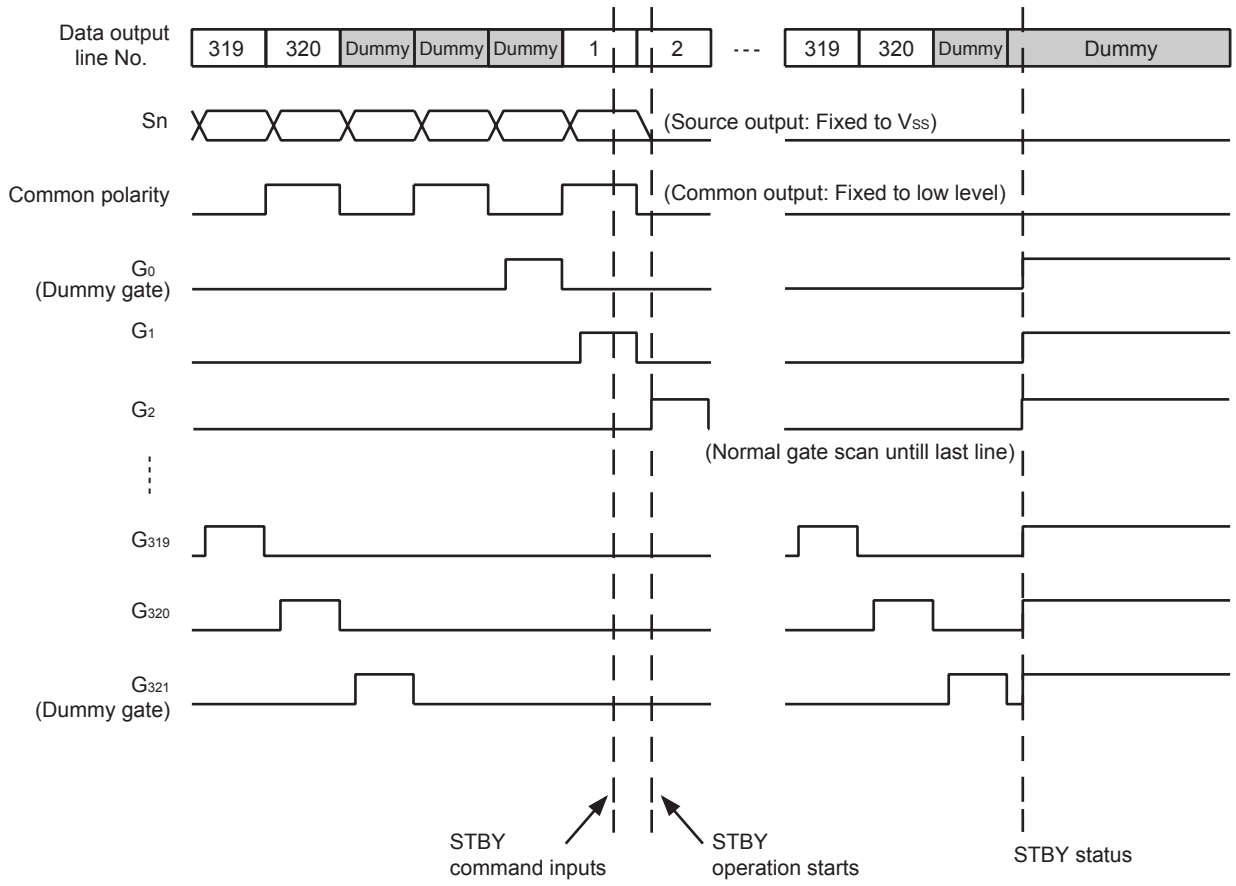
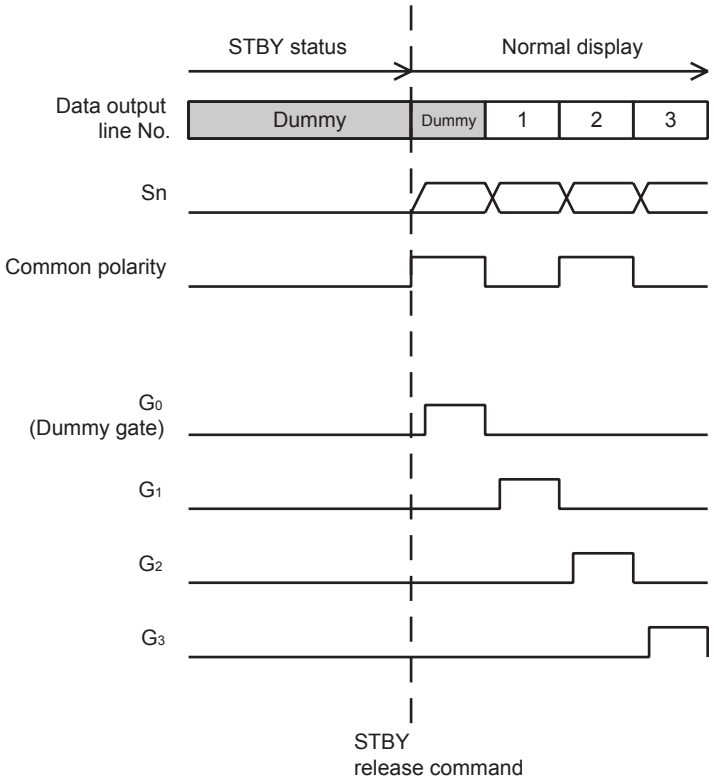


Figure 5–43. Normal Operation → STBY Input Mode (during line inversion)



Caution Oscillator does not stop only by the STBY command (Since it is necessary to output booster clock to power supply IC).

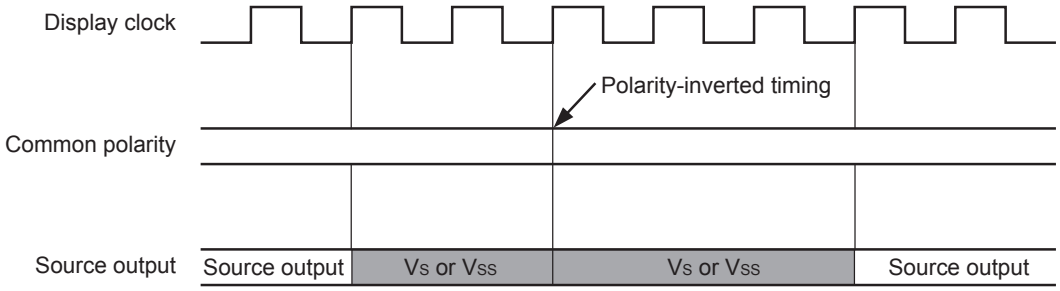
Figure 5–44. STBY Status → Return to Normal Operation (during line inversion)



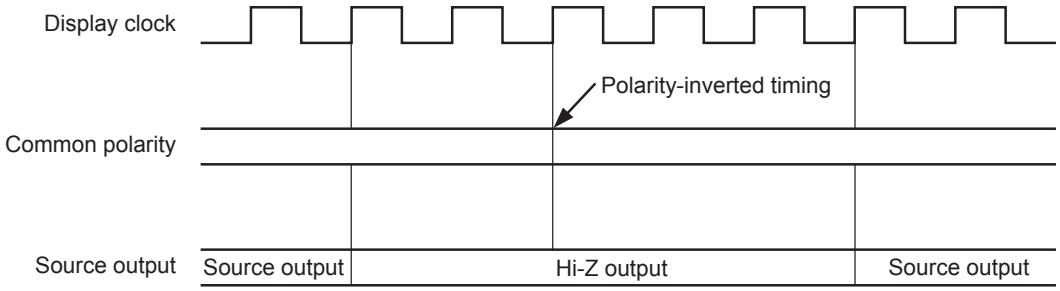
5.4.3 About source output of dummy period

In the μPD161704A, it is possible to set up the source output during dummy period by SOUT_MODE 1 and SOUT_MODE0 registers.

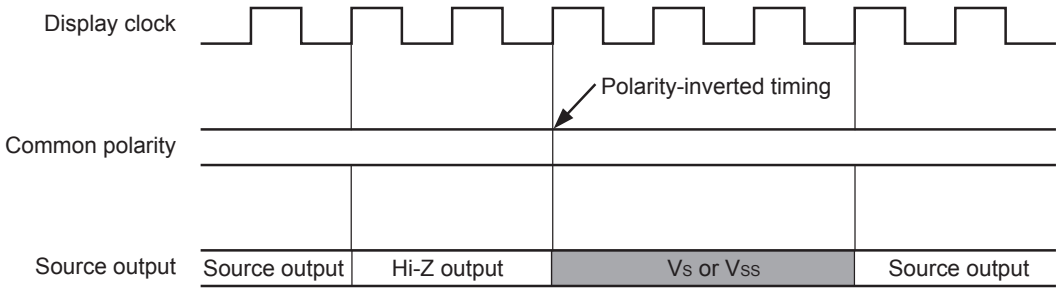
In the case of SOUT_MODE1, SOUT_MODE0 = 0, 0
As for the source output in the dummy period, V_S (when common = L) or V_{SS} (when common = H) is outputted by common polarity.



In the case of SOUT_MODE1, SOUT_MODE0 = 0, 1 or 1, 1
As for the source output in the dummy period, Hi-Z is outputted.



In the case of SOUT_MODE1, SOUT_MODE0 = 1, 0
As for the source output in the dummy period, Hi-Z is outputted before common polarity inversion and V_S or V_{SS} is outputted by common polarity as well as the case of "0, 0" after common polarity inversion.



5.5 γ-Curve Correction Circuit (Each common register mode)

The μPD161704A includes γ-curve correction circuit. It is possible to adjust inclination of γ- amplitude by register setup. Each register of the register setup (GPH [6:0], R36, GPL [6:0], R38, GNH [6:0], R37, and GNL [6:0], R39) performs amplitude of γ-curve of positive and negative polarity. Moreover, fine tuning is set to G3SW [R82] register = 1, and the register setup (GM1P [5:0], R97, GM2P [5:0], R99, GM3P [5:0], R101, GM3N [5:0], R98, GM2N [5:0], R100, and GM1N [5:0], R102) performs it.

Figure 5–45. γ-Curve Correction Circuit (Positive polarity, GRES = 0)

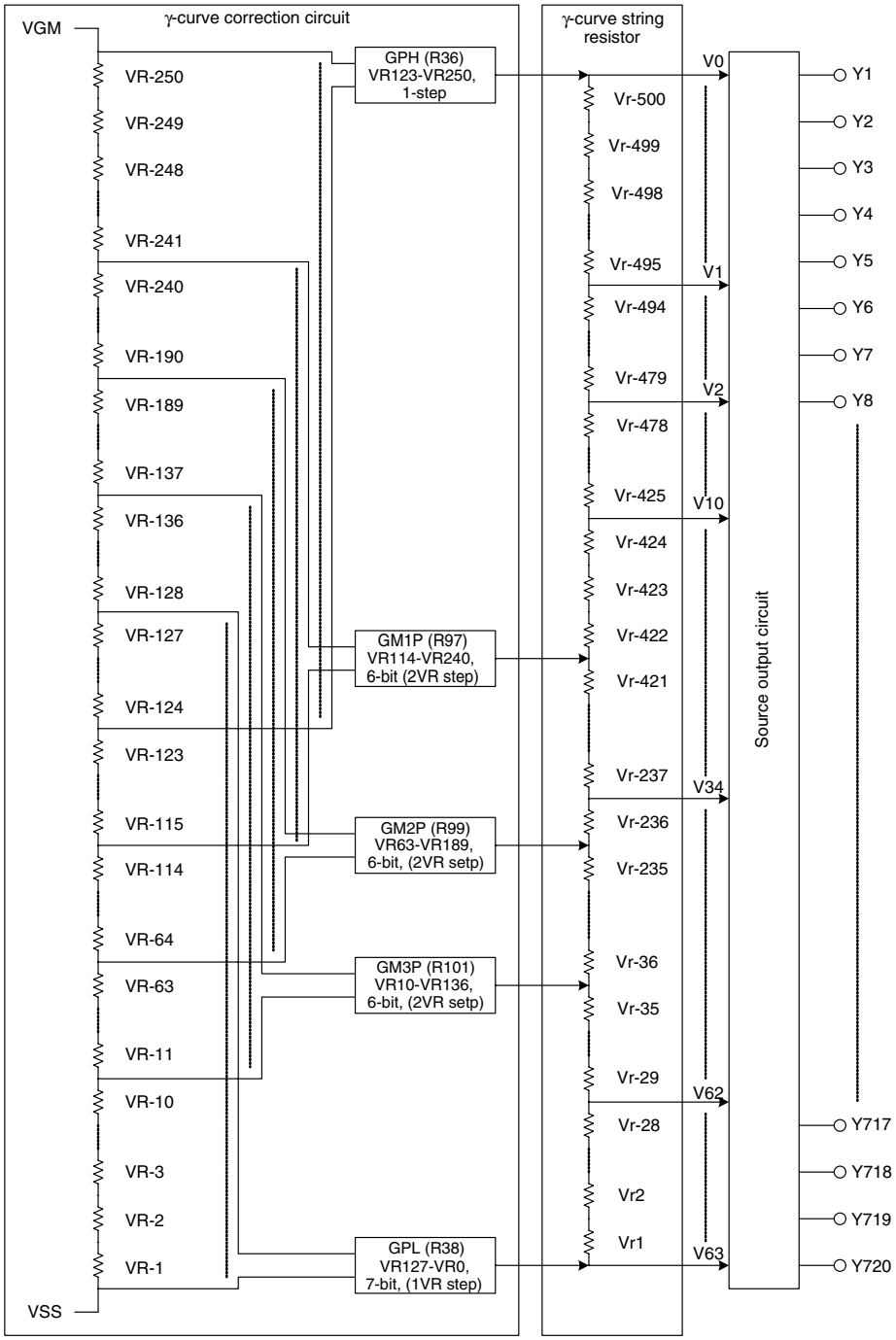
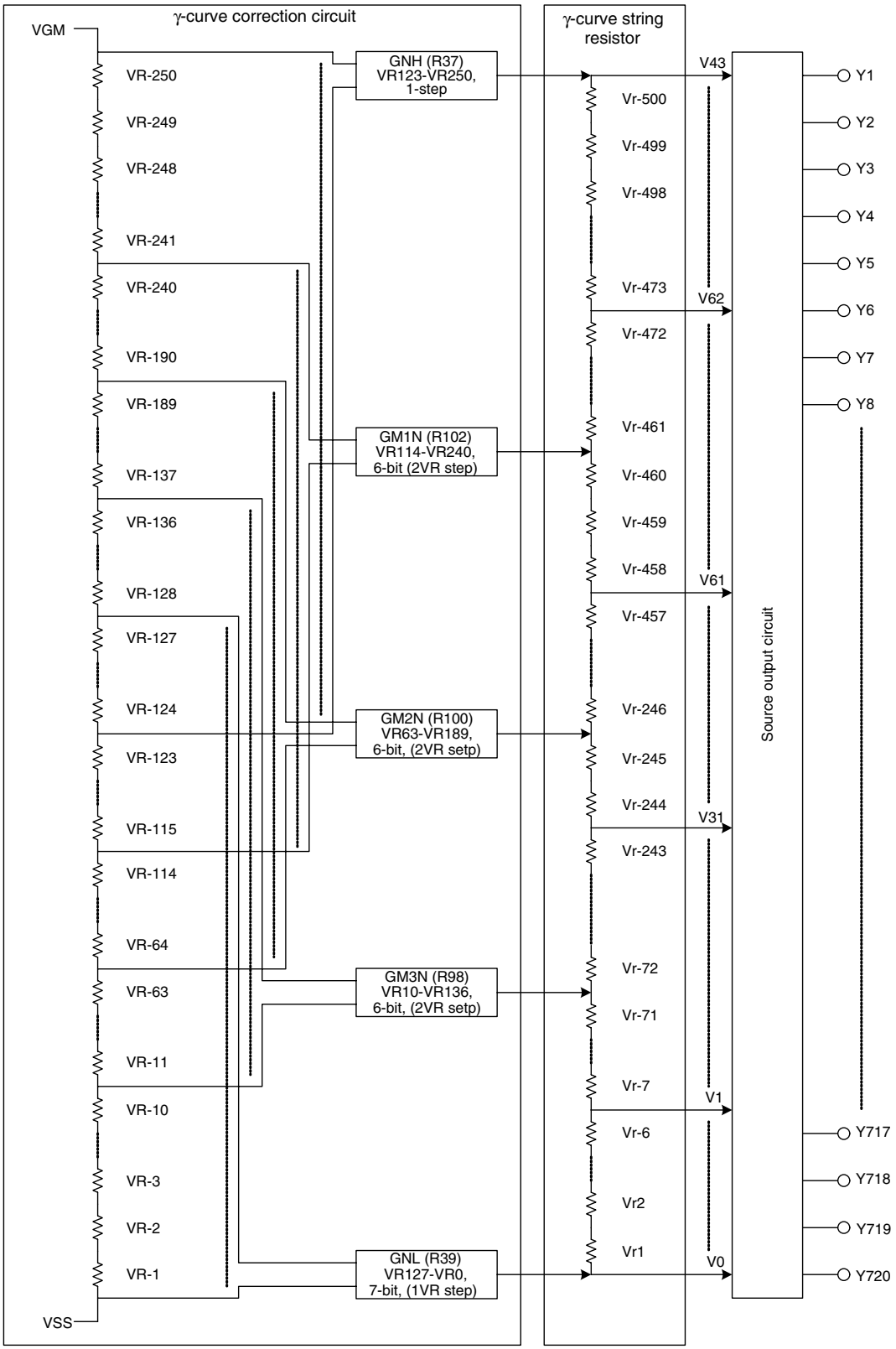


Figure 5–46. γ-Curve Correction Circuit (Negative polarity, GRES = 0)



A setup of the gray-scale voltage (Vr) in each gray-scale mode is as follows.

(1) GRES = 0: Default

1 V_r is positive polarity: (VPH–VPL)/500 and negative polarity: (VNH–VNL)/500.

Gray-scale Mode		Positive Polarity	Negative Polarity
64 gray-scale	2 gray-scale	V_r	V_r
0	0	500	0
1		494	6
2		486	14
3		478	22
4		470	30
5		462	38
6		454	46
7		446	54
8		439	61
9		432	68
10		424	76
11		416	84
12		408	92
13		400	100
14		392	108
15		384	116
16		376	124
17		367	133
18		358	142
19		348	152
20		339	161
21		330	170
22		322	178
23		314	186
24		306	194
25		299	201
26		292	208
27		285	215
28		278	222
29		271	229
30		264	236
31		257	243

Gray-scale Mode		Positive Polarity	Negative Polarity
64 gray-scale	2 gray-scale	V_r	V_r
32		250	250
33		243	257
34		236	264
35		229	271
36		223	277
37		217	283
38		211	289
39		205	295
40		199	301
41		193	307
42		187	313
43		181	319
44		175	325
45		169	331
46		163	337
47		157	343
48		151	349
49		145	355
50		138	362
51		131	369
52		124	376
53		117	383
54		109	391
55		101	399
56		93	407
57		84	416
58		75	425
59		66	434
60		55	445
61		43	457
62		28	472
63	1	0	500

(2) GRES = 1

1 V_r is positive polarity: (VPH–VPL)/500 and Negative polarity: (VNH–VNL)/500.

Gray-scale Mode		Positive Polarity	Negative Polarity
64 gray-scale	2 gray-scale	V_r	V_r
0	0	500	0
1		493	5
2		485	13
3		477	21
4		468	28
5		460	36
6		452	43
7		444	51
8		436	58
9		428	66
10		420	74
11		412	81
12		404	89
13		396	96
14		388	104
15		380	112
16		372	120
17		363	129
18		353	138
19		342	148
20		333	157
21		324	165
22		316	173
23		308	181
24		300	188
25		292	195
26		285	201
27		278	208
28		271	215
29		264	222
30		258	228
31		251	235

Gray-scale Mode		Positive Polarity	Negative Polarity
64 gray-scale	2 gray-scale	V_r	V_r
32		245	241
33		239	248
34		232	254
35		225	260
36		219	266
37		213	272
38		207	279
39		201	285
40		194	291
41		188	298
42		181	304
43		175	311
44		169	317
45		163	323
46		157	330
47		150	337
48		144	343
49		137	350
50		131	356
51		124	363
52		117	371
53		110	378
54		103	386
55		96	394
56		88	403
57		80	412
58		71	421
59		62	431
60		53	443
61		41	455
62		27	471
63	1	0	500

Table 5–8. γ-amplifier Connection Place

Positive Polarity	
GPH	Vr 500
GM1P	Vr 421
GM2P	Vr 235
GM3P	Vr 36
GPL	Vr 0

Negative Polarity	
GNH	Vr 500
GM1N	Vr 460
GM2N	Vr 245
GM3N	Vr 71
GNL	Vr 0

1 VRn = Vs/250 (20 mV step when Vs = 5 V)

GPH	GM1P	GM2P	GM3P	GPL	VRn	Vs = 5 V (V)
GNH	GM1N	GM2N	GM3N	GNL		
7-bit	6-bit	6-bit	6-bit	7-bit		
				00H	0	0.000
				01H	1	0.020
				:	:	:
			00H	0AH	10	0.200
			–	0BH	11	0.220
			01H	0CH	12	0.240
			:	:	:	:
		00H	–	3FH	63	1.260
		–	1BH	40H	64	1.280
		01H	–	41H	65	1.300
		:	:	:	:	:
	00H	–	34H	72H	114	2.280
	–	1AH		73H	115	2.300
	01H	–	35H	74H	116	2.320
	:	:	:	:	:	:
00H	–	1EH	–	7BH	123	2.460
01H	05H	–	39H	7CH	124	2.480
02H	–	1FH	–	7DH	125	2.500
03H	06H	–	3AH	7EH	126	2.520
04H	–	20H	–	7FH	127	2.540
:	:	:	:		:	:
0BH	0AH	–	3EH		134	2.680
0CH	–	24H	–		135	2.700
0DH	0BH	–	3FH		136	2.720
:	:	:			:	:
40H	–	3EH			187	3.740
41H	25H	–			188	3.760
42H	–	3FH			189	3.780
:	:				:	:
73H	3EH				238	4.760
74H	–				239	4.780
75H	3FH				240	4.800
:					:	:
7EH					249	4.980
7FH					250	5.000

Table 5–9. Gray-scale (Upper side) Bias Current Setup

GAN2	GAN1	GAN0	Current Value (magnification)
0	0	0	0.5
0	0	1	1.0 (default)
0	1	0	1.5
0	1	1	2.0
1	0	0	3.0
1	0	1	4.0
1	1	0	6.0
1	1	1	7.5

Table 5–10. Gray-scale (Bottom side) Bias Current Setup

GAP2	GAP1	GAP0	Current Value (magnification)
0	0	0	0.5
0	0	1	1.0 (default)
0	1	0	1.5
0	1	1	2.0
1	0	0	3.0
1	0	1	4.0
1	1	0	6.0
1	1	1	7.5

Table 5–11. γ-amplifier Bias Current Setup

GI2	GI1	GI0	Current Value (magnification)
0	0	0	0.5
0	0	1	1.0 (default)
0	1	0	1.5
0	1	1	2.0
1	0	0	2.5
1	0	1	3.0
1	1	0	3.5
1	1	1	4.0

5.6 Partial Display Mode (Each common register mode)

The μPD161704A is provided with a function that allows sections within the screen to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register, the number of lines in the area to be displayed is set using the partial non-display area line count register.

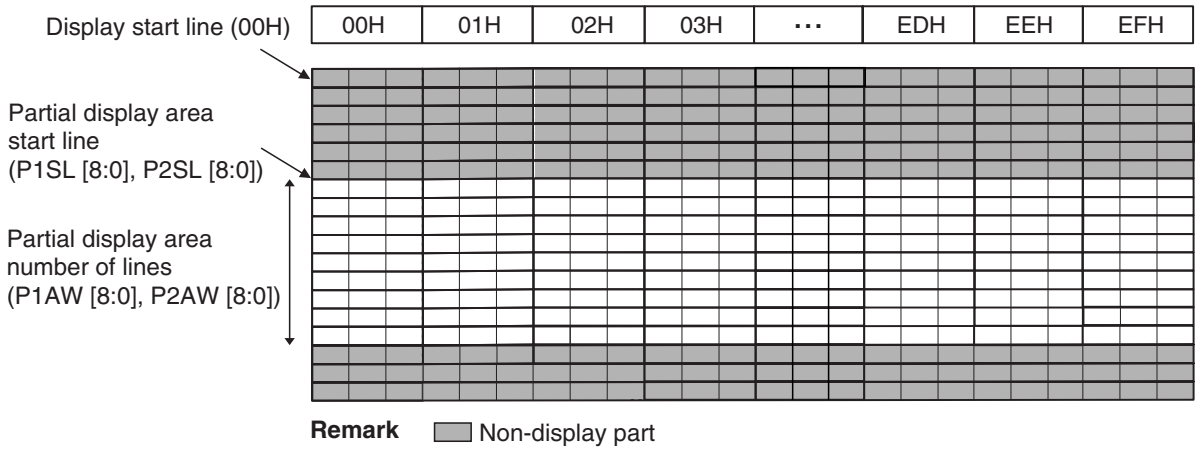
Moreover, the address of the image data displayed on partial display area can be specified by the partial display area display area address register (P1SA [8:0], P2SA [8:0]).

A setup of color is possible for partial non-displaying area at partial non-displaying area setting register. If "1" is set in the partial display area line count registers, the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by P1SL [8:0] and P1AW [8:0] is called partial 1, and the non-display area indicates by P2SL [8:0] and P2AW [8:0] is called partial 2. The partial 2 setting is enabled only when the partial 1 setting has been performed (when P1AW [8:0] ≠ 0). Therefore, to set only one area as a non-display area, perform only the setting for partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-color mode.

Figure 5–47. Partial Display Mode



Cautions 1. The specified partial areas must not directly overlap, and the partial 1 area and partial 2 area must be separated by at least one line. If the areas overlap, only the partial 1 settings are valid, and partial display is not performed for the partial 2 area.

2. When setting the partial display areas, be sure to observe the following relationship.

P1AW [8:0] (P2AW [8:0]) ≤ "13FH" (Setting gate line number – 1)

The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode

DISP1 = 1 or DISP0 = 1	<1> Display OFF
↓	
PSEL setting PGX setting (PSEL =0)	<2> Partial non-display area setting register Note1
↓	
Display data overwrite (for partial display)	<3> Display data overwrite Note1
↓	
P1SL [8:0] setting P2SL [8:0] setting	<4> Partial display area start line setting Note1
↓	
P1AW [8:0] setting P2AW [8:0] setting	<5> Partial display area line count setting Note1
↓	
P1SA [8:0] setting P2SA [8:0] setting	<6> Partial display are RAM address setting Note1
↓	
GS setting	<7> Partial display are color setting Note1
↓	
DTY = 1	<8> Partial display mode Note2
↓	
DISP1 = 0 and DISP0 = 0	<9> Display ON

Notes 1. <2> to <7> can be executed in any order.

2. <8> must be executed after <4> to <6> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode

DISP1 = 1 or DISP0 = 1	<1> Display OFF
↓	
Display data overwrite (for normal display)	<2> Display data overwrite Note
↓	
GS setting	<3> Display area color setting
↓	
DTY = 0	<4> Normal display mode Note
↓	
DISP1 = 0 and DISP0 = 0	<5> Display ON

Note <2> to <4> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)

DISP1 = 1 or DISP0 = 1	<1> Display OFF
↓	
Display data overwrite	<2> Display data overwrite Note1, 2
↓	
P1SL [8:0] setting P2SL [8:0] setting	<3> Partial display area start line setting Note1
↓	
P1AW [8:0] setting P2AW [8:0] setting	<4> Partial display area line count setting Note1
↓	
P1SA [8:0] setting P2SA [8:0] setting	<5> Partial display are RAM address setting Note1
↓	
DTY = 1	<6> Partial display mode Note3
↓	
DISPn = 0	<7> Display ON

Notes 1. <2> to <5> can be executed in any order.

2. Execute <2> only when necessary.

3. <6> must be executed after <3> to <5> have been set.

(4) Partial display setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Partial display area start line register (P1SL [8:0], P2SL [8:0])	00H	Specifies Y address 00H
Partial display area line count register (P1AW [8:0], P2AW [8:0])	A0H	Sets an area of 160 lines
Partial display area RAM address register (P1SA [8:0], P2SA [8:0])	00H	Specified Y address 00H

Setting A-2

Register	Setting Value	Details of Setting Value
Partial display area start line register (P1SL[8:0], P2SL[8:0])	A0H	Specifies Y address A0H
Partial display area line count register (P1AW[8:0], P2AW[8:0])	A0H	Sets an area of 160 lines
Partial display area RAM address register (P1SA[8:0], P2SA[8:0])	A0H	Specifies Y address A0H

Setting A-3

Register	Setting Value	Details of Setting Value
Partial display area start line register (P1SL [8:0], P2SL [8:0])	50H	Specifies Y address 50H
Partial display area line count register (P1AW [8:0], P2AW [8:0])	A0H	Sets an area of 160 lines
Partial display area RAM address register (P1SA [8:0], P2SA [8:0])	50H	Specifies Y address 50H

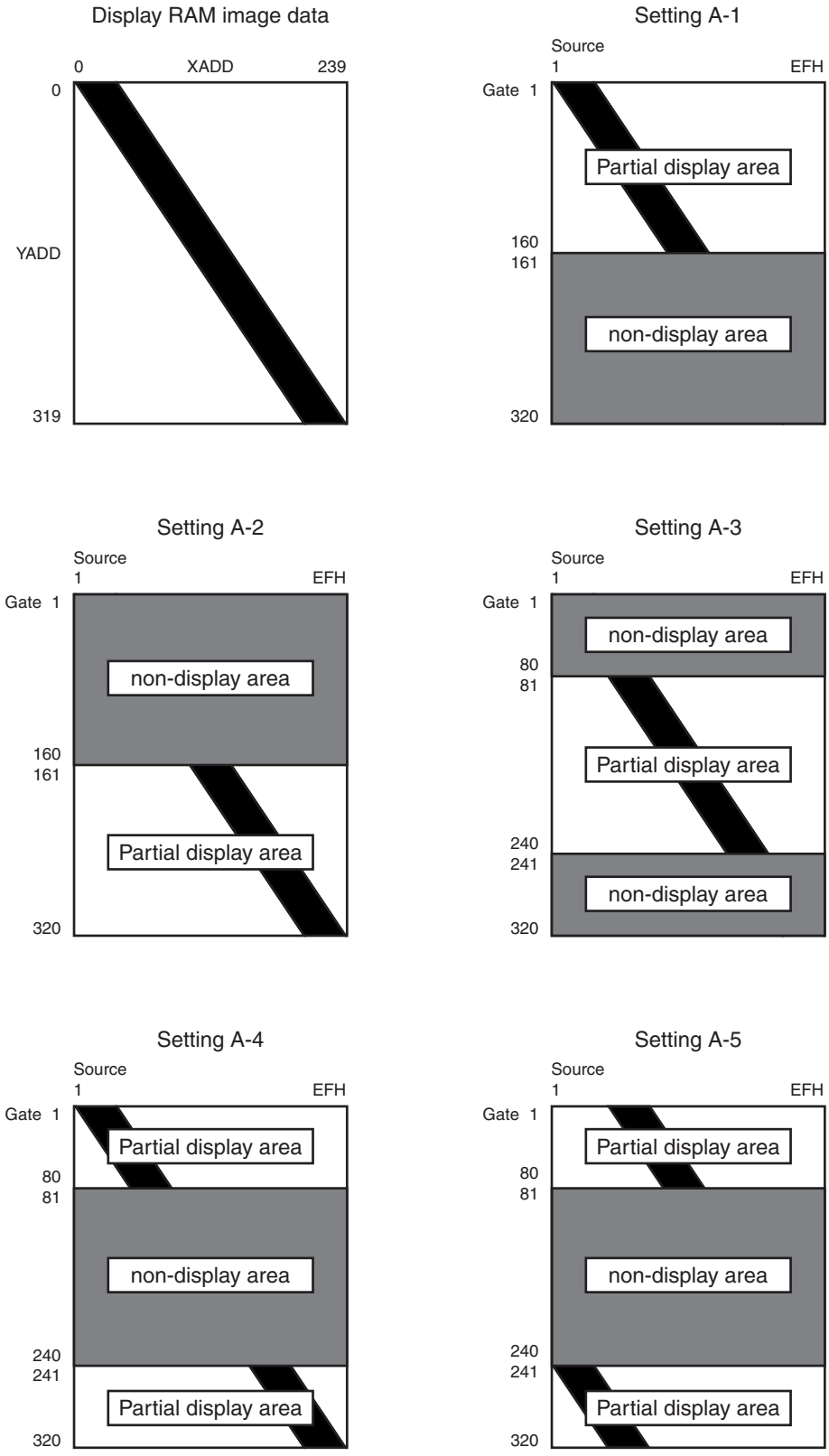
Setting A-4

Register	Setting Value	Details of Setting Value
Partial display area start line register (P1SL [8:0], P2SL [8:0])	F0H	Specifies Y address F0H
Partial display area line count register (P1AW [8:0], P2AW [8:0])	A0H	Sets an area of 160 lines
Partial display area RAM address register (P1SA [8:0], P2SA [8:0])	F0H	Specifies Y address F0H

Setting A-5

Register	Setting Value	Details of Setting Value
Partial display area start line register (P1SL [8:0], P2SL [8:0])	F0H	Specifies Y address F0H
Partial display area line count register (P1AW [8:0], P2AW [8:0])	A0H	Sets an area of 160 lines
Partial display area RAM address register (P1SA [8:0], P2SA [8:0])	00H	Specifies Y address 00H

Figure 5–48. Partial Display Setting



5.7 Stand-by (Each common register mode)

The μPD161704A has a stand-by function.

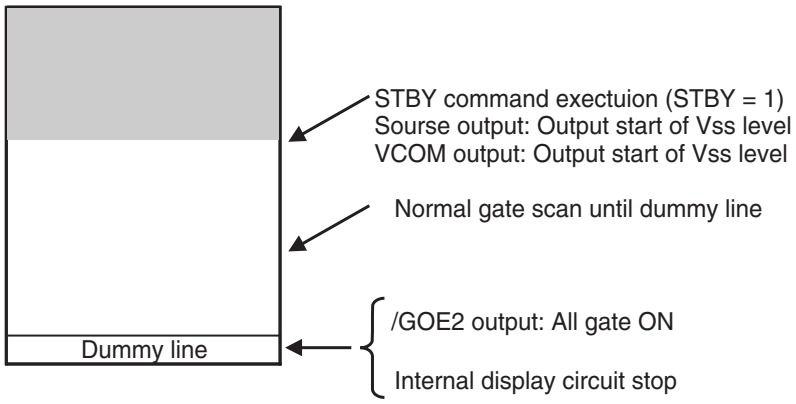
By setting STBY register = 1, and during the frame dummy line interval, all gate outputs are set to ON, from output to V_{SS}, VCOM to V_{SS}, and the panel charge is discharged. By setting DCON register = 0 after all gate outputs have become ON, regulator OFF and DC/DC converter OFF are executed, and by setting OSCON register = 0, full stand-by mode is entered after the internal oscillator stops.

<Stand-by sequence>

STBY register = 1
↓
(Wait in one frame period)
↓
DCON register = 0
↓
OSCON register = 0

The transition from the stand-by mode to the regular mode is the opposite sequence from the stand-by sequence, and is executed in the order of OSCON = 1, DCON = 1, and STBY = 0.

Figure 5–49. Outline of Operation During Stand-by Mode Execution



Remarks 1. In the stand-by mode (STBY = 1), display data RAM access, display data RAM hold, and register access are possible even during DC/DC converter OFF and internal oscillation stop, as long as power is supplied to V_{DD}, V_{CCIO}, and V_{DC}.

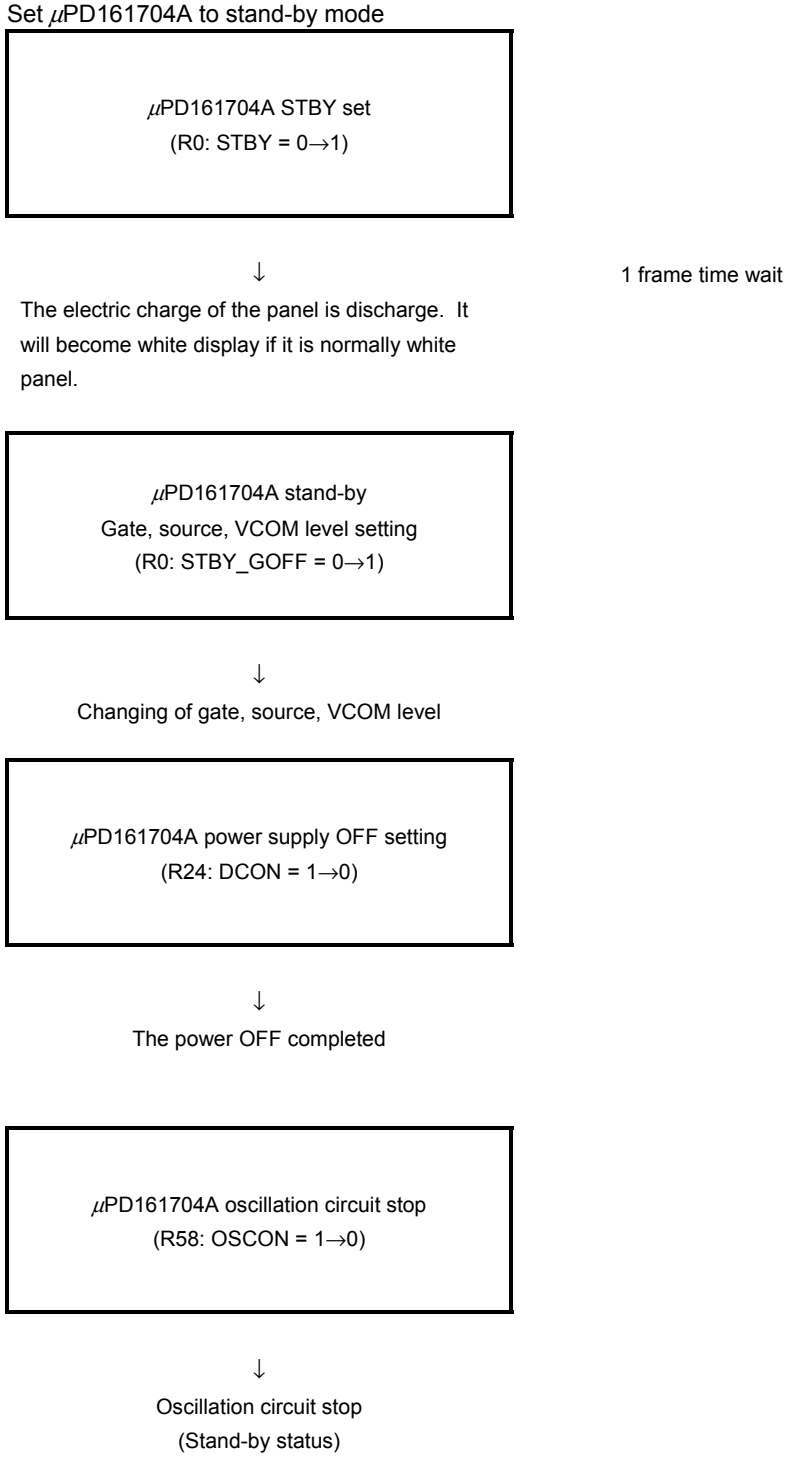
2. If STBY_GOFF = 1, gate, source, and VCOM level can be set up as follows.

Gate level: V_{GL}
Source level: Hi-Z
VCOM level: V_{SS}

5.7.1 Stand-by sequence

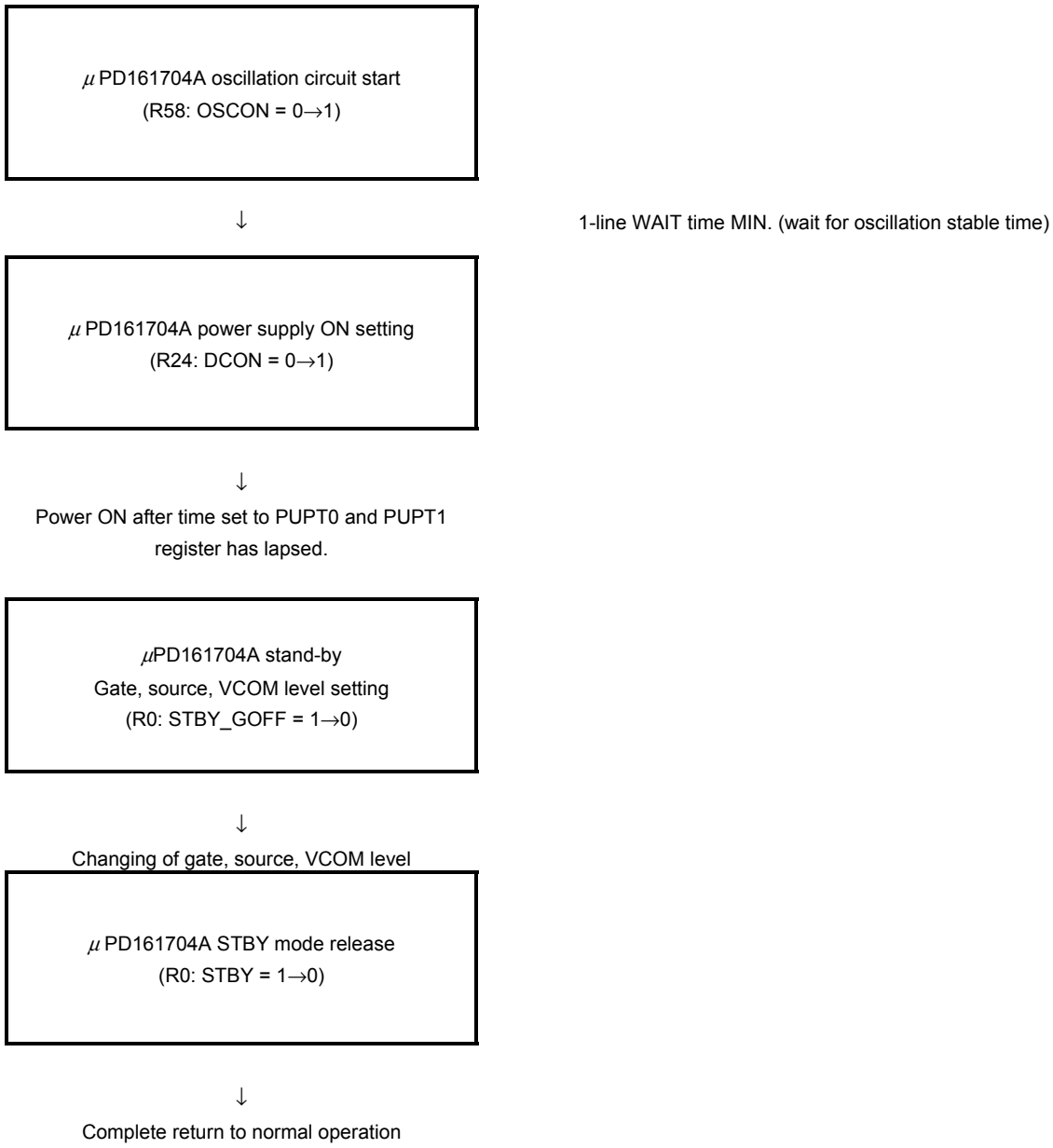
As power supply control, the example of a sequence at the time of performing an internal sequence is shown.

Set μPD161704A to stand-by mode



5.7.2 Stand-by release sequence

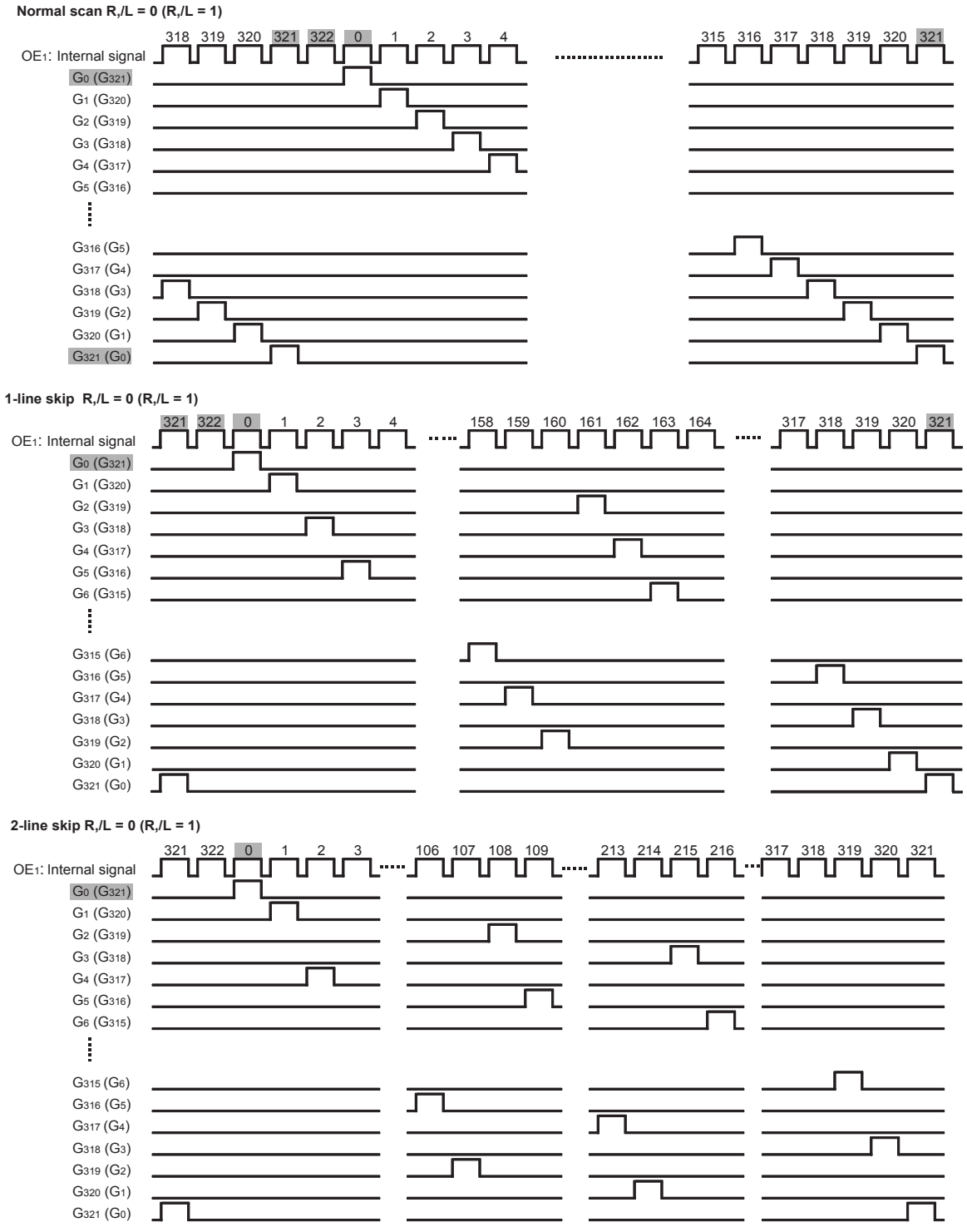
As power supply control, the example of a sequence at the time of performing an internal sequence is shown.



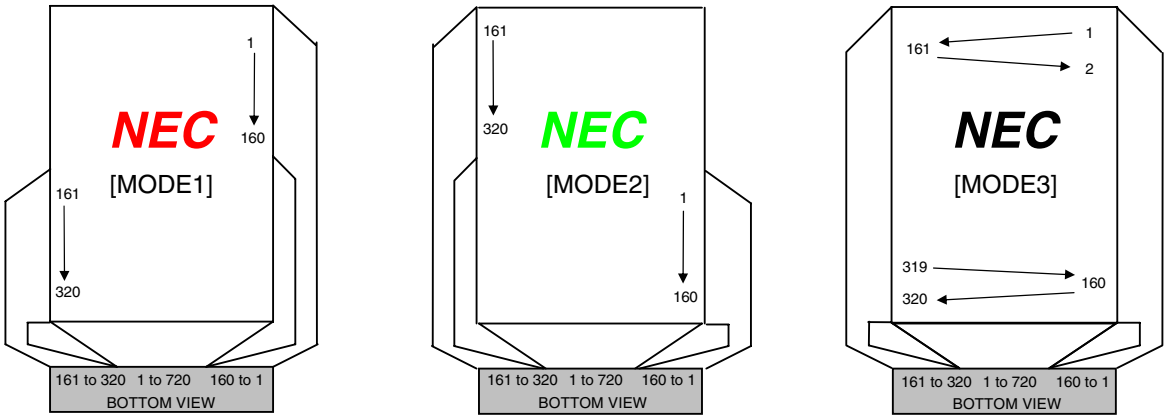
5.8 Gate Driver Control (Each common register mode)

The μPD161704A builds in 322 gate output circuits, and outputs a scanning signal according to display timing.

Figure 5–50. Gate Scan Waveform



Remark G_0 and G_{321} are dummy line.



R,/L = Scan direction of gate “L” 1 → 320
R,/L = Scan direction of gate “H” 320 → 1

SCN1 = ”0”, SCN = ”0”: Panel connection mode ”MODE1”
SCN1 = ”0”, SCN = ”1”: Panel connection mode ”MODE2”
SCN1 = ”1”, SCN = ”0”: Panel connection mode ”MODE3”
SCN1 = ”1”, SCN = ”1”” Setting prohibited

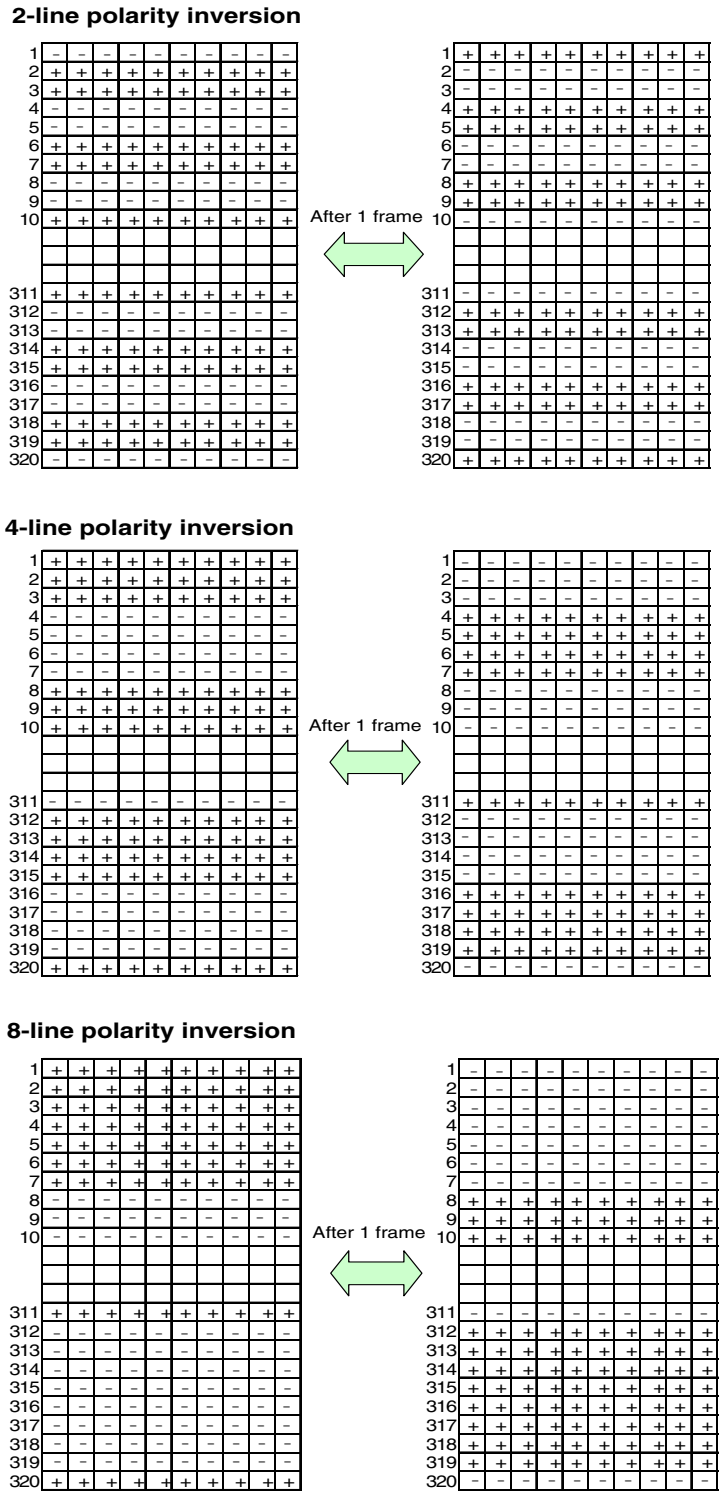
NLINE1 = ”0”, NLINE0 = ”0”: 1-line inversion
NLINE1 = ”0”, NLINE0 = ”1”: 2-line inversion
NLINE1 = ”1”, NLINE0 = ”0”: 4-line inversion
NLINE1 = ”1”, NLINE0 = ”1”: 8-line inversion

GSCAN1 = ”0”, GSCAN0 = ”0”: Line inversion
GSCAN1 = ”0”, GSCAN0 = ”1”: Frame inversion
GSCAN1 = ”1”, GSCAN0 = ”0”: Skip inversion 1D
GSCAN1 = ”1”, GSCAN0 = ”1”: Skip inversion 2B

5.8.1 Inverting n lines

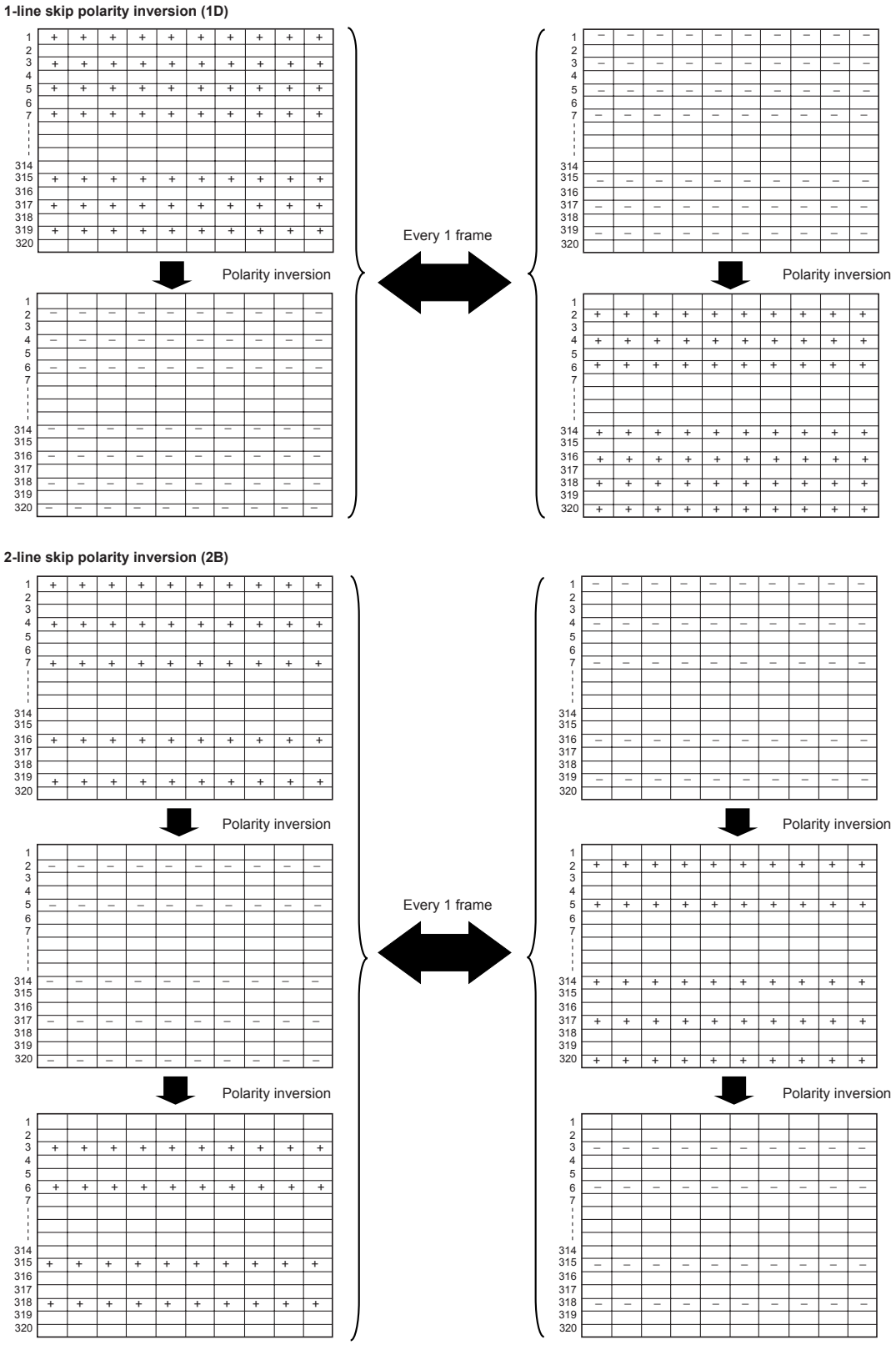
The inversion operation is executed by the number of lines n set to the NLINE [1:0] register. Figure 5–50 shows the inversion operation when 2, 4, and 8 is set as the number of lines n.

Figure 5–51. Example of Inverting n Lines



5.8.2 Skip polarity inversion

Figure 5–52. Skip Polarity Inversion



5.8.3 Gate scan function

Three types of scan methods can be selected for the gate scan operation. Make the selection using GSCAN0 and GSCAN1 register. The scan operations corresponding to the settings of the GSCAN0 and GSCAN1 register are shown in Table 5−12.

Table 5–12. Selecting Gate Scan Function

GSCAN1	GSCAN0	Scan Function	Operation
0	0	Common line inversion (n line inversion)	Inverts the number of lines set by the NLINE [1:0] register R51 = 0,0: Inverts 1 line, R51 = 1,0: Inverts 4 lines R51 = 0,1: Inverts 2 line, R51 = 1,1: Inverts 8 lines
0	1	Common frame inversion	Performs inversion every frame.
1	0	Skip inversion 1D **Note**	Skips and inverts 1 line and common inversion is carried out in a cycle of 1/2 frame. For details, refer to **Figure 5–53**.
1	1	Skip inversion 2B **Note**	Skips and inverts 1 line and common inversion is carried out in a cycle of 1/3 frame. For details, refer to **Figure 5–54**.

Note It cannot be used at the time of the through mode/capture mode selection of RGB interface.

Moreover, the scan direction of the gate can be vertically inverted every frame, as specified by R,/L register.
The setting is as follows.

Table 5–13. Selecting Inversion Direction

R,/L	Operation
0	Scans the gate from the top to the bottom. Line 1 → Line 320
1	Scans the gate from the bottom to the top. n frames: Line 320 → line 1

Also, eight kinds shown below can be selected as scanning mode of the non-display area at the time of partial operation.

Table 5–14. Partial Non-display Area Scan Mode

GSM	GSMLN [2:0]	Scan Mode
0	X, X, X	Same scan cycle as partial display area
1	0, 0, 0	Partial non-display area doesn't scan
1	0, 0, 1	Partial non-display area scans every 3 frames.
1	0, 1, 0	Partial non-display area scans every 5 frames.
1	0, 1, 1	Partial non-display area scans every 7 frames.
1	1, 0, 0	Partial non-display area scans every 9 frames.
1	1, 0, 1	Partial non-display area scans every 11 frames.
1	1, 1, 0	Partial non-display area scans every 13 frames.
1	1, 1, 1	Partial non-display area scans every 15 frames.

5.8.4 Skip inversion

One or two line is skipped and inverted. Figure 5–53 and 5–54 show specific waveforms.

Figure 5–53. Skip Inversion 1D

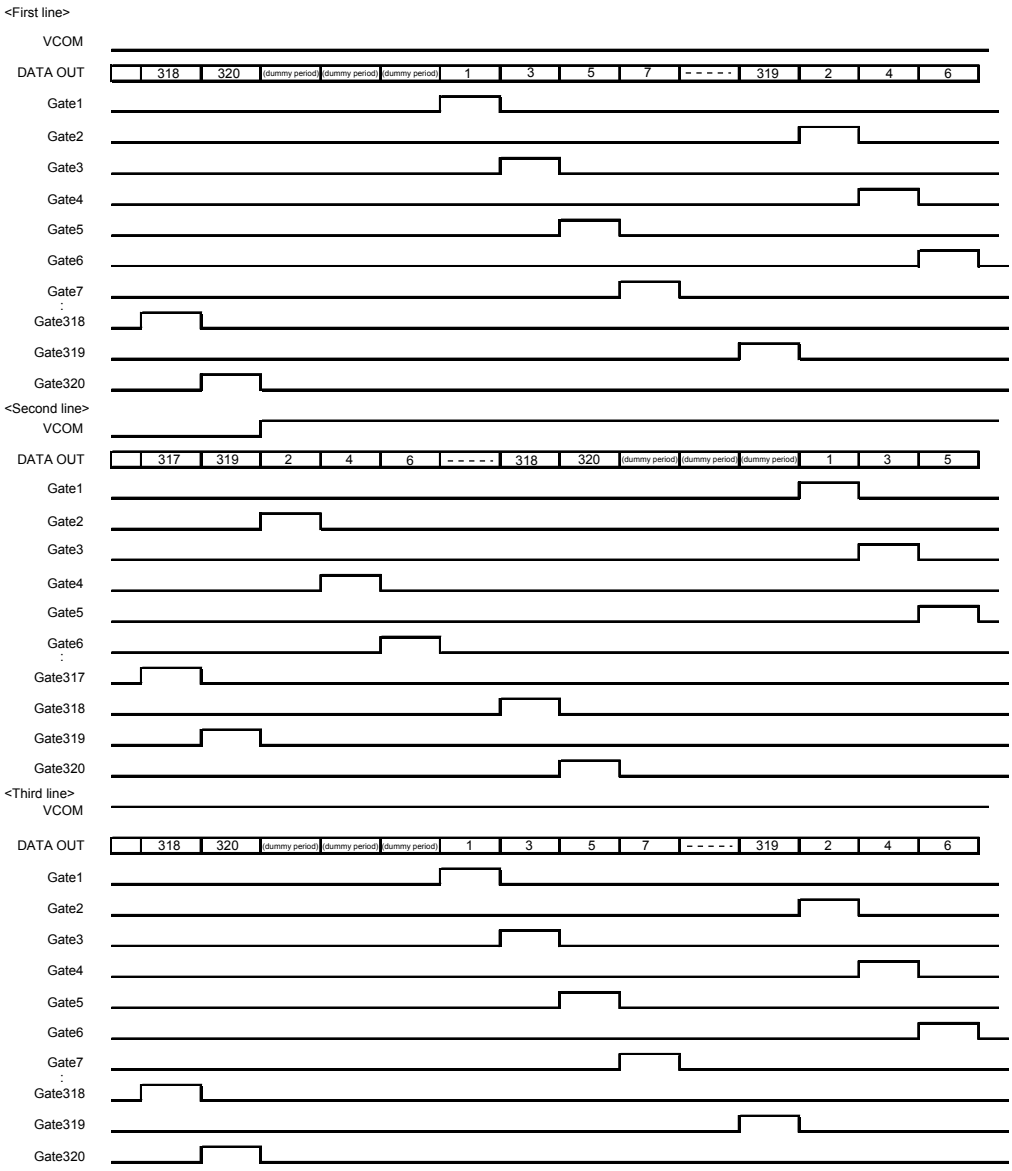
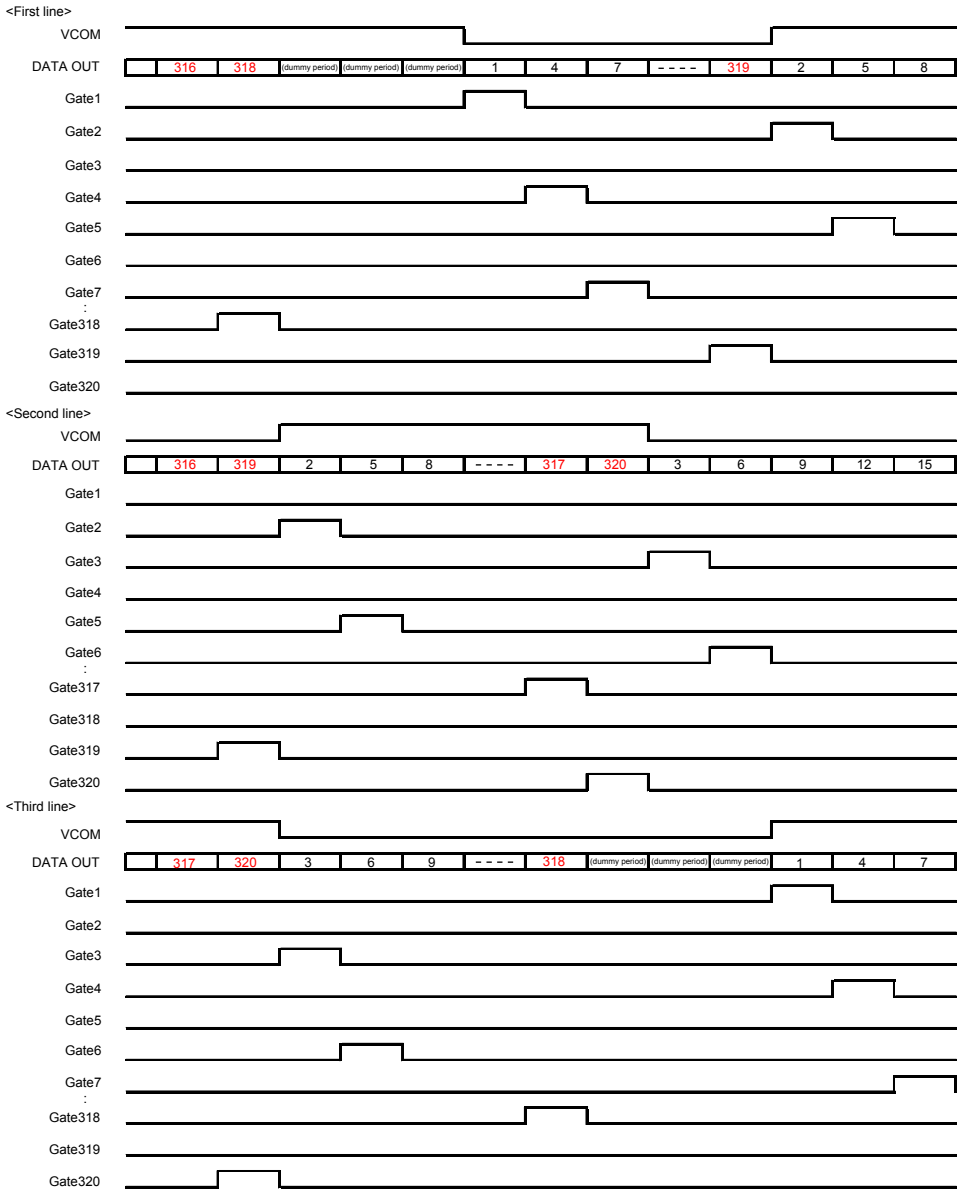


Figure 5–54. Skip Inversion 2B



6. E²PROM INTERFACE

The μPD161704A builds in the interface function to E²PROM corresponding to the micro-wire interface.

However, the capacity of E²PROM corresponds only 2 K and 4 K bit article.

6.1 The μPD161704A and E²PROM Connection

Connection with E²PROM is made as shown in the following figure.

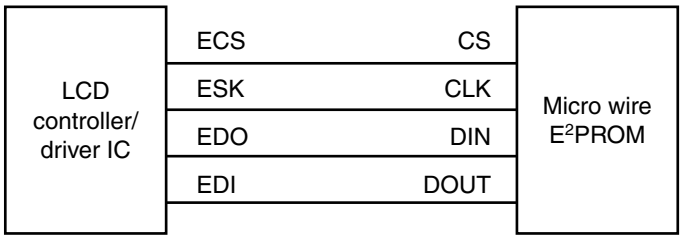


Table 6–1. LCD Controller Side Signal

Pin	Function
ECS	Chip select signal over E²PROM. With outputting ECS = 1, E²PROM is made into an active state and data is transmitted after that. It connects with CS (chip select pin) of E²PROM.
<R> ESK	Clock signal over E²PROM. In falling of ESK, data is outputted from EDO to E²PROM. It connects with CLK (shift clock pin) of E²PROM. This is the E²PROM clock for which has 8 divided circumferences in internal oscillator.
EDO	Data output pin. Data is outputted to E²PROM. It connects with DIN (data in pin) of E²PROM
EDI	Data input pin. It is used for reading of the data of E²PROM and a BUSY/READY check. It connects with DOUT (data out pin) of E²PROM.

<R> **6.2 Each Operation**

The μPD161704A can perform writing of register data, reading of a register date and elimination of E^2PROM data to E^2PROM. Selection of each operation is performed using R68 register.

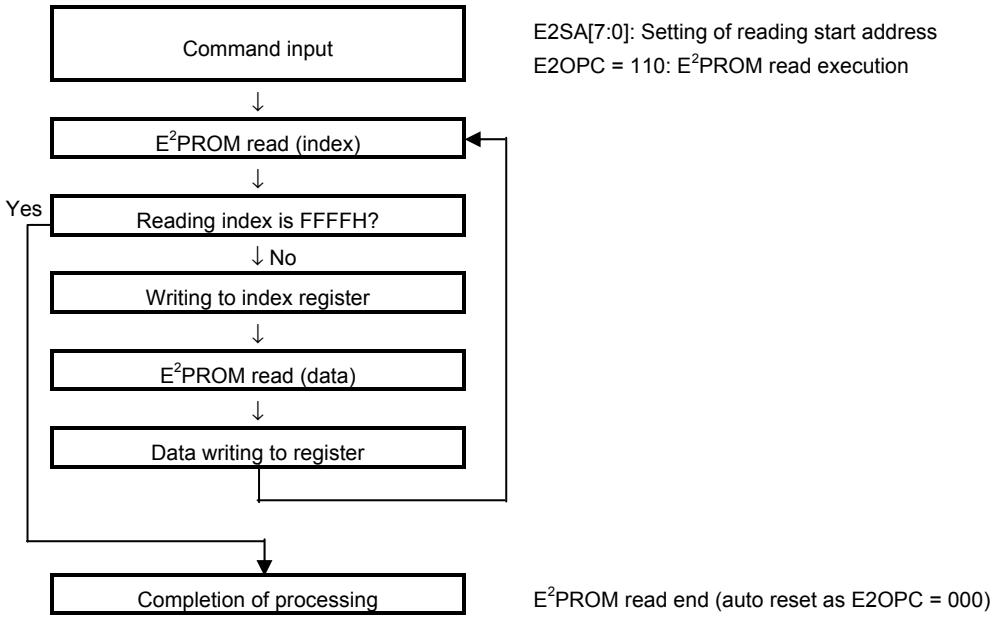
R68 Register			E^2PROM Command
E2OPC2	E2OPC1	E2OPC0	
0	0	0	Setting prohibited
0	0	1	EPSAVE: Writing to E^2PROM
0	1	0	MASKON: Permission of the writing and elimination to E^2PROM **Note**
0	1	1	MASKOF: Prohibition of the writing and elimination to E^2PROM
1	0	0	EPCLR: All area elimination of E^2PROM
1	0	1	EPWALL: FFH is written in all the area of E^2PROM
1	1	0	EPREAD: Reading from E^2PROM
1	1	1	Setting prohibited

Note Only when making it E2OPC [2:0] = 0, 1, 0 before setting a value as E2OPC, it is necessary to set E2EN [7:0] register as AAH. The signal of the permission of writing and elimination to E^2PROM as for E2OPC [2:0] = 0, 1, 0 is not transmitted not setting E2EN [7:0] register to AAH. In addition, when E2EN [7:0] register sets up Index in addition to E2OPC [2:0] or E2EN [7:0], it is reset by 00H.

In addition, explain each operation as follows.

[E^2PROM read command: Reading from E^2PROM]

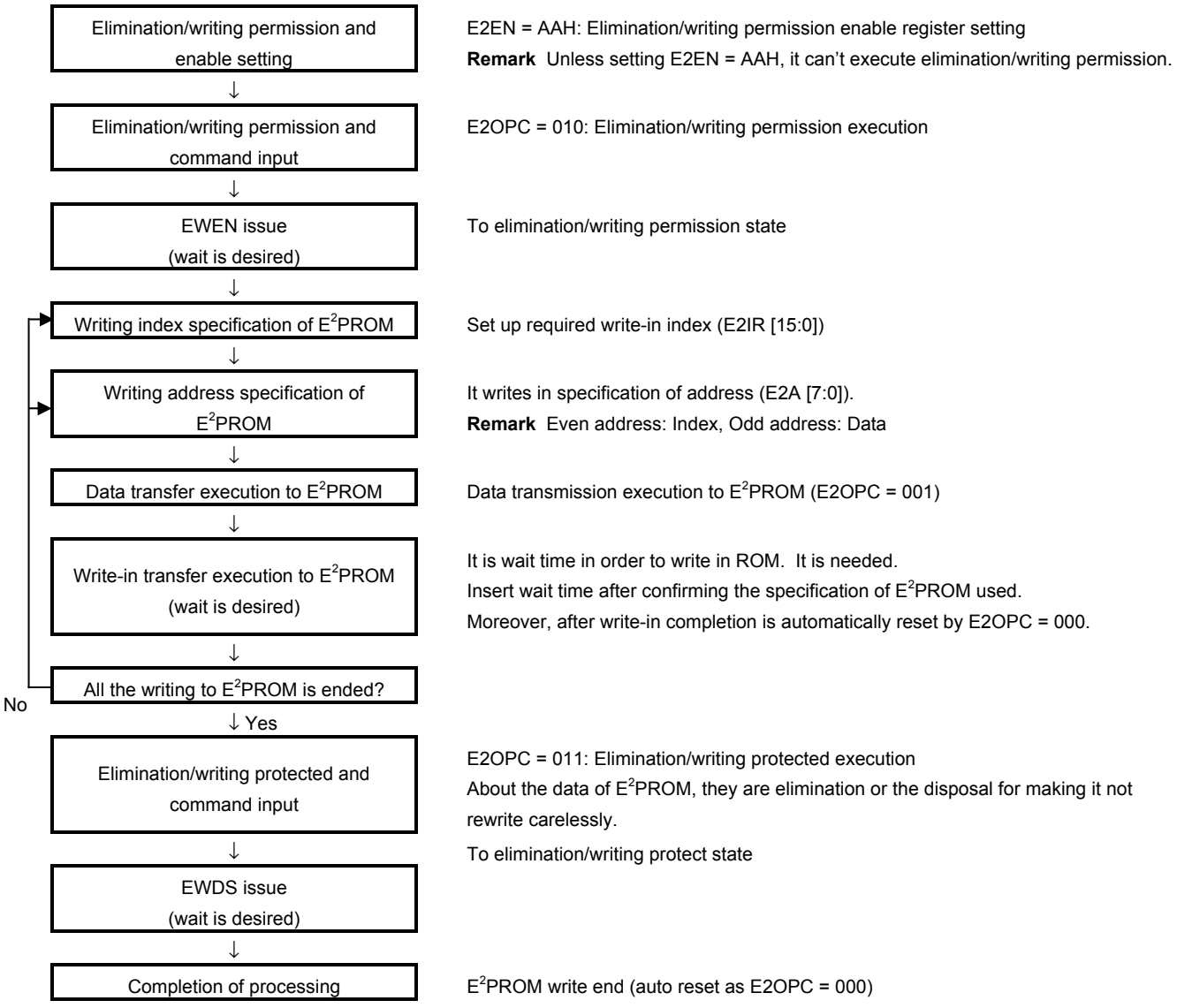
From the "E^2PROM address" set as "the E^2PROM reading start address register (E2SA [7:0])", it reads in order of "index (D_0 to D_{15}: Index" + "Data (D_0 to D_{15})" and the register data stored in E^2PROM is saved to the applicable index of the μPD161704A. In addition, reading operation is continuously performed until it reads the reading end ID (Index area wrote by E^2PROM is FFFFH).



[EPSAVE command: Writing of the data to E^2PROM]

The register data of the μPD161704A, data is written in the E^2PROM address based on E2A [7:0] with corresponding E2IR [15:0].

In addition, when an E^2PROM address is set as an even number address, an index is written in, and data is written in when it is set as an odd number address. Moreover, write the data corresponding to the index in the next address of the E^2PROM address in which the index was written.



[MASKON command: Writing/elimination permission to E^2PROM]

Elimination/writing to E^2PROM is permitted.

Elimination/writing permission and enable setting	E2EN = AAH: Elimination/writing permission and enable register setting **Remark** Unless setting E2EN = AAH, it can't execute elimination/writing permission.
↓	
Elimination/writing permission and command input	E2OPC = 010: Elimination/writing permission execution
↓	
EWEN <Erase Write ENable> issue (wait is desired)	E^2PROM to an elimination/writing permission state
↓	
Completion of elimination/writing permission processing	E^2PROM elimination / write-in permission end (auto reset as E2OPC = 000)

[MASKOF: Writing protected to E^2PROM]

Elimination/writing to E^2PROM are protected (Reading of data is possible).

Elimination/writing protection and Command input	E2OPC = 010: Elimination/writing protection execution
↓	
EWDS <Erase Write DiSable> issue (wait is desired)	E^2PROM to an elimination/writing protection state
↓	
Completion of elimination/writing permission processing	E^2PROM elimination / write-in permission end (auto reset as E2OPC = 000)

[EPCLR command: E^2PROM elimination]

The data of E^2PROM is initialized.

Elimination/writing permission and enable setting	E2EN = AAH: Elimination/writing permission and enable register setting **Remark** Unless setting E2EN = AAH, it can't execute elimination/writing permission.
↓	
Elimination/writing permission and command input	E2OPC = 010: Elimination/writing permission execution
↓	
EWEN <Erase Write ENable> issue (wait is desired)	E^2PROM to an elimination/writing permission state
↓	
E^2PROM elimination and command input	E^2PROM elimination execute (E2OPC = 100)
↓	
ERAL <ERase ALl> issue (wait is desired)	All data elimination of E^2PROM
↓	
Elimination/writing protection and Command input	E2OPC = 010: Elimination/writing protection execution
↓	
EWDS <Erase Write DiSable> issue (wait is desired)	E^2PROM to an elimination/writing protection state
↓	
Completion of processing of E^2PROM elimination	E^2PROM elimination end (auto reset as E2OPC = 000)

[EPWALL]

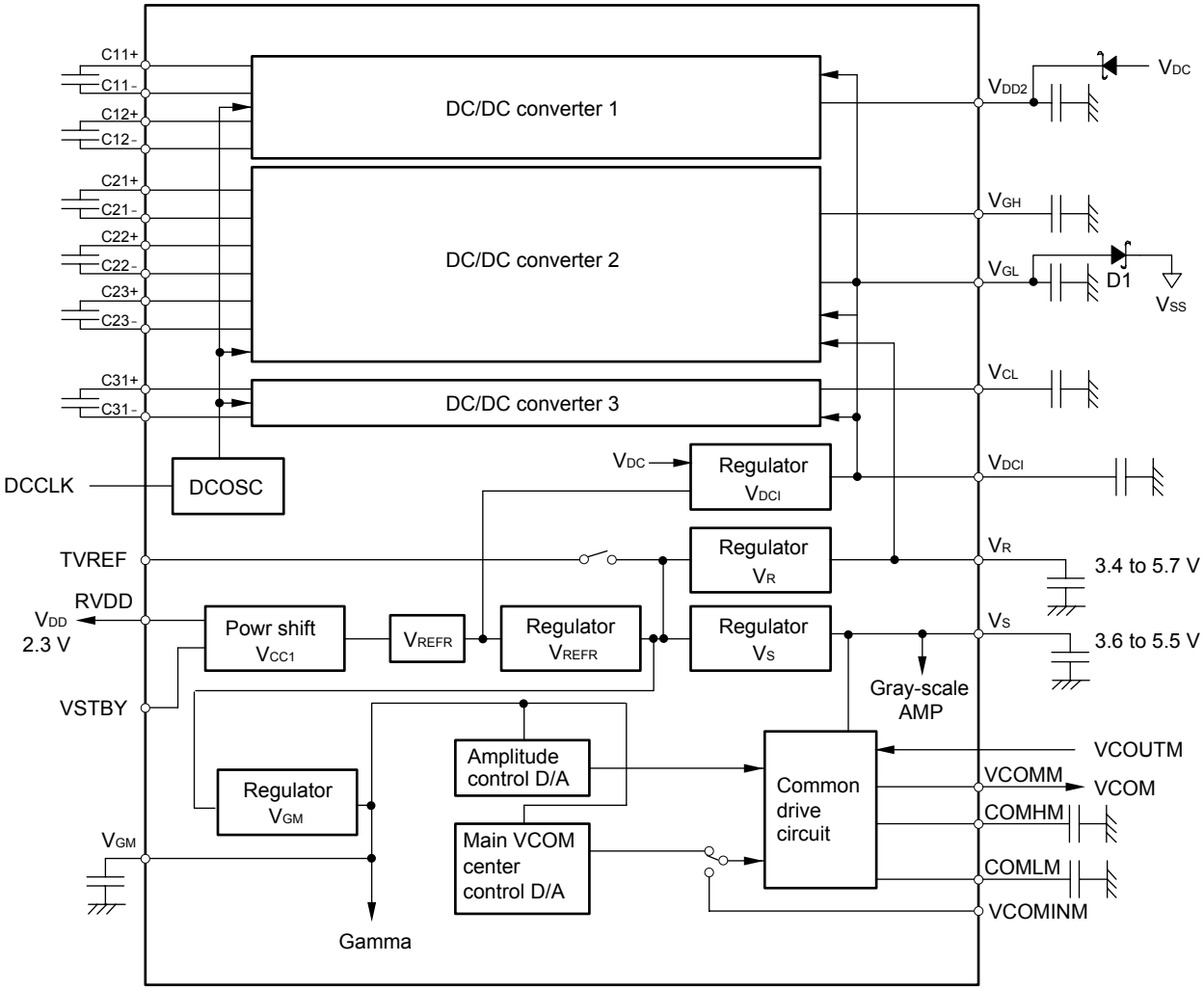
FFFFH is written in all the data of E^2PROM.

At the time of E^2PROM initialization, it reads to all E^2PROM data, an end command (FFFFH) is written and the infinite loop of reading by the noise etc. is prevented.

Elimination/writing permission and enable setting	E2EN = AAH: Elimination/writing permission and enable register setting **Remark** Unless setting E2EN = AAH, it can't execute elimination/writing permission.
↓	
Elimination/writing permission and command input	E2OPC = 010: Elimination/writing permission execution
↓	
EWEN <Erase Write ENable> issue (wait is desired)	E^2PROM to an elimination/writing permission state
↓	
All area FFFFH write-in command input	All area FFFFH write-in execution (E2OPC = 101)
↓	
WRAL <WRite ALl> issue (wait is desired)	Write in FFFFH to all address of E^2PROM
↓	
Elimination/writing protection and Command input	E2OPC = 011: Elimination/writing protection execution
↓	
EWDS <Erase Write DiSable> issue (wait is desired)	E^2PROM to an elimination/writing protection state
↓	
Completion of processing of all area E^2PROM write-in	E^2PROM all area write-in end (auto reset as E2OPC = 000)

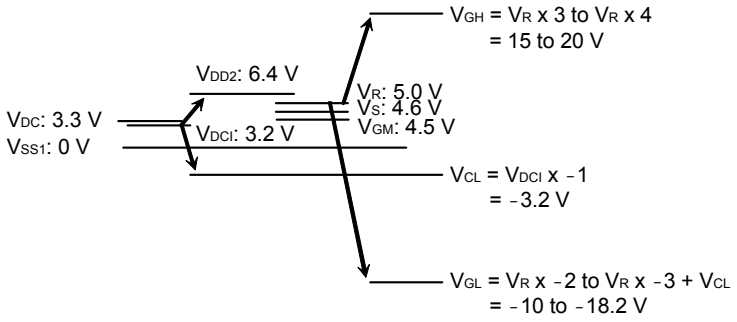
7. POWER SUPPLY CONTROL

DC/DC, VCOM block diagram

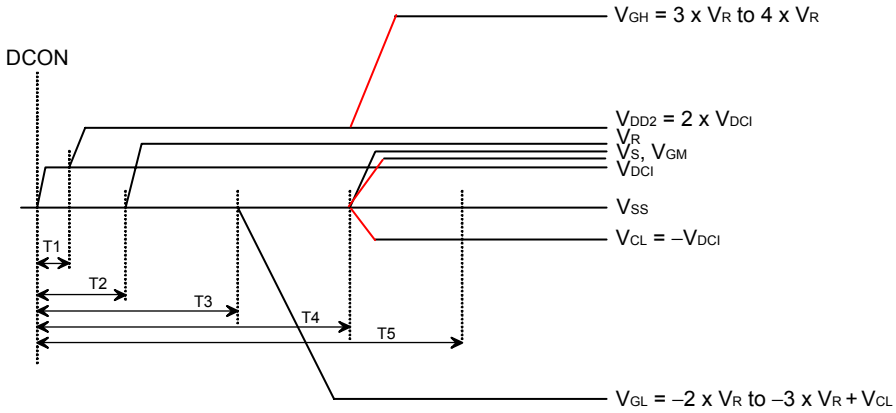


7.1 Boost Voltage Construction

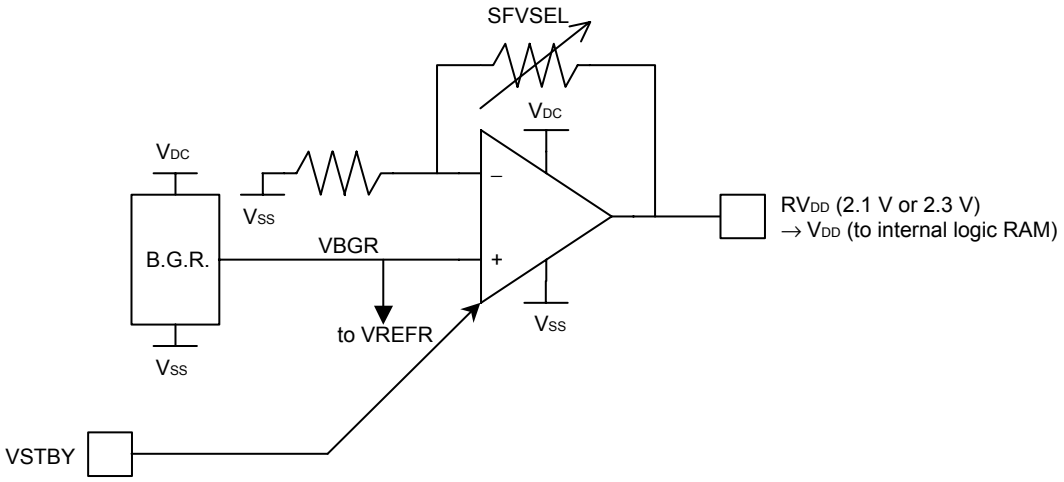
The boost voltage generated is shown below.



7.2 Boost Voltage Auto Start and Rising Order

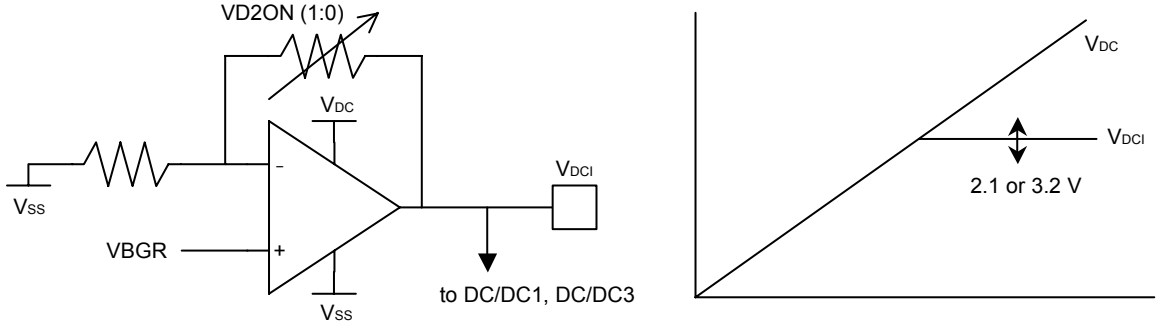


7.3 Power Shift Circuit



VSTBY	SFVSEL	Function
0 (V_{SS})	0	Regulator ON, RV_{DD} = 2.1 V (Test mode)
0 (V_{SS})	1	Regulator ON, RV_{DD} = 2.3 V (Default)
1 (V_{DC})	–	Regulator OFF, RV_{DD} = Hi-Z (Test mode)

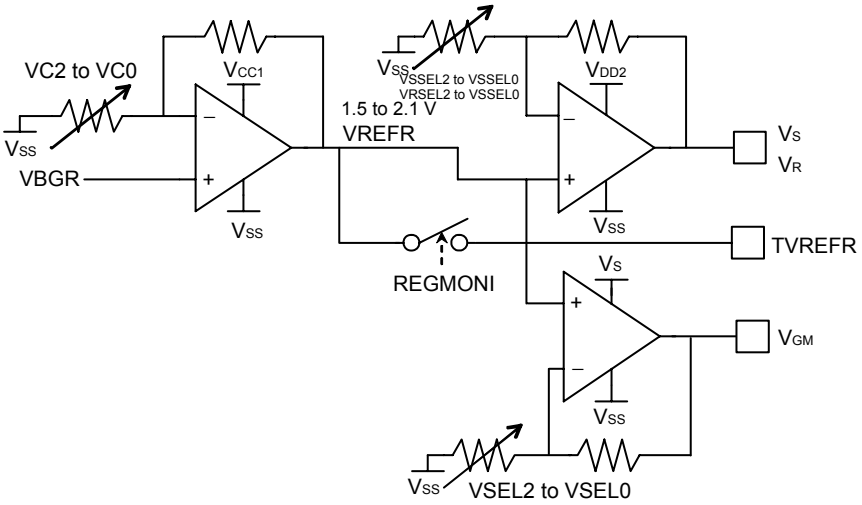
7.4 V_{DCI} Circuit



VD2ON1	V_{DCI} (Limit value)
0 (2 times boost)	V_{DCI} = 3.2 V
1 (3 times boost)	V_{DCI} = 2.1 V

7.5 V_S_AMP Circuit, V_R_AMP Circuit and V_{GM}_AMP Circuit

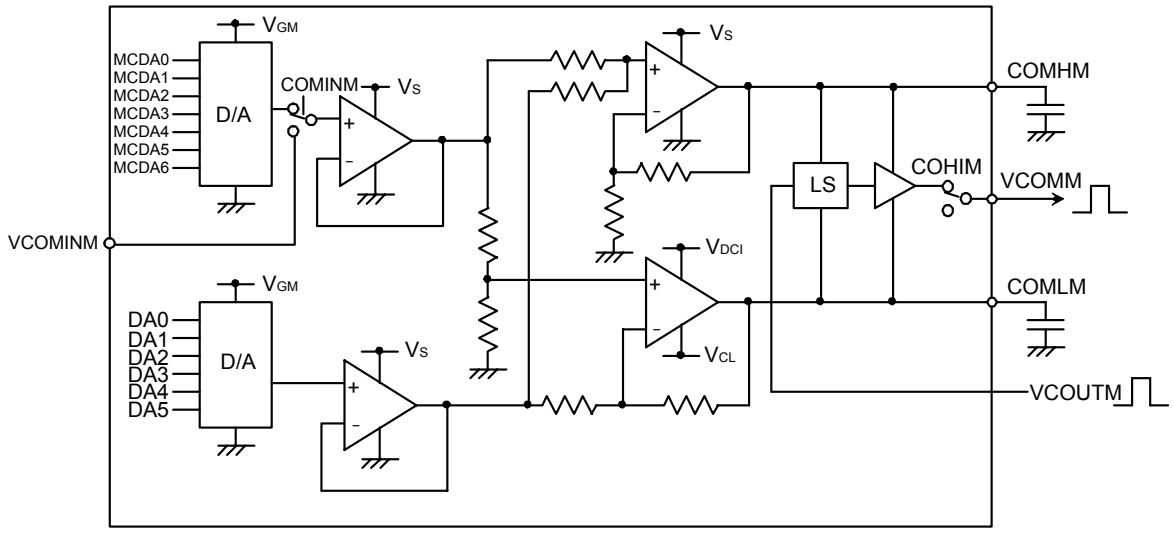
V_S, V_R and V_{GM} generating amplifier circuit is shown below.



Refer to **7.8 Mode Description** for the relation of each output voltage and register.

7.6 Common Drive Circuit

The common drive circuit is shown below.

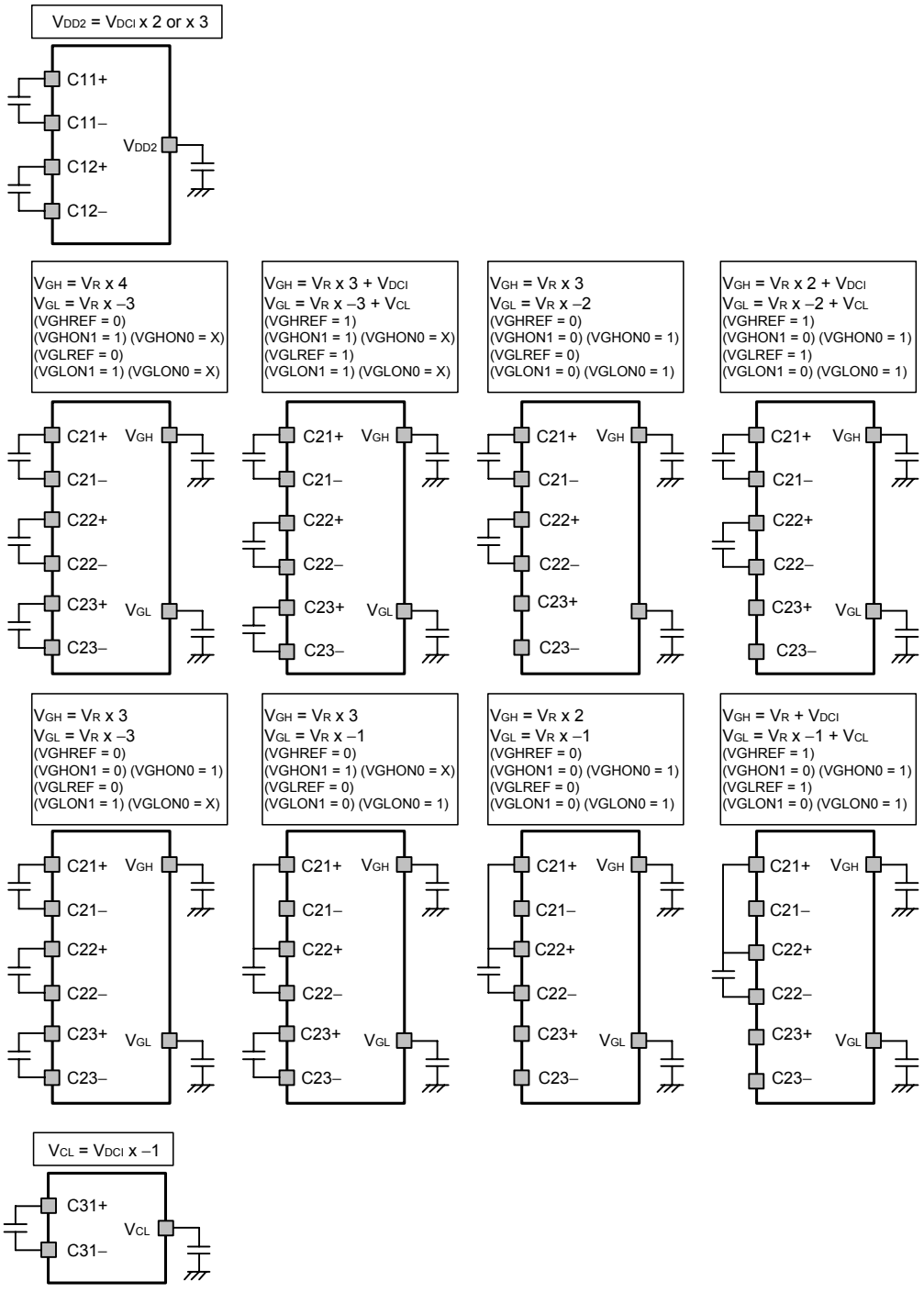


7.7 Variable Boost Steps

The number of boost step V_{DD2} is fixed to V_{DCI} x 2 or x 3. It sets up by VD2ON1 and VD2ON0 register.

The boost steps of V_{GH}, V_{GL} and V_{CL} are selected according to how the external capacitor is connected and by VGHON1 and VGHON0, VGLON1 and VGLON0, VGHREF, and VGLREF registers.

The example of connection is shown below.



7.8 Mode Description

7.8.1 DC/DC converter control

DCON	VD2ON1	VD2ON0	DC1HZ	State of V_{DD2}
0	x	x	0	V_{DC}
0	x	x	1	Hi-Z
1	0	0	0	V_{DC}
1	0	0	1	Hi-Z
1	0	1	x	V_{DCI} x 2 boost
1	1	x	x	V_{DCI} x 3 boost

DCON	VGHREF	VGHON1	VGHON0	VGLON1	VGLON0	DC2HZ	State of V_{GH}
0	x	x	x	x	x	0	$V_{GH} = V_{DD2}$
0	x	x	x	x	x	1	V_{GH} = Hi-Z
1	x	0	0	x	x	0	$V_{GH} = V_{DD2}$
1	x	0	0	0	0	1	V_{GH} = Hi-Z
1	0	0	1	x	x	x	$V_{GH} = V_R$ x 2 boost + V_R
1	0	1	x	x	x	x	$V_{GH} = V_R$ x 3 boost + V_R
1	1	0	1	x	x	x	$V_{GH} = V_R$ x 2 boost + V_{DCI}
1	1	1	x	x	x	x	$V_{GH} = V_R$ x 3 boost + V_{DCI}

DCON	VGLREF	VGLON1	VGLON0	VGHON1	VGHON0	DC2HZ	State of V_{GL}
0	x	x	x	x	x	0	$V_{GL} = V_{SS}$
0	x	x	x	x	x	1	V_{GL} = Hi-Z
1	x	0	0	x	x	0	$V_{GL} = V_{SS}$ ($V_{GL} = V_{CL}$ when V_{CL}= ON)
1	x	0	0	0	0	1	V_{GL} = Hi-Z
1	0	0	1	x	x	x	$V_{GL} = V_R$ x –2 boost
1	0	1	x	x	x	x	$V_{GL} = V_R$ x –3 boost
1	1	0	1	x	x	x	$V_{GL} = V_R$ x –2 boost + V_{CL}
1	1	1	x	x	x	x	$V_{GL} = V_R$ x –3 boost + V_{CL}

DCON	VCLON	DC3HZ	State of V_{CL}
0	x	0	$V_{CL} = V_{SS}$
0	x	1	V_{CL} = Hi-Z
1	0	0	$V_{CL} = V_{SS}$
1	0	1	V_{CL} = Hi-Z
1	1	x	V_{DCI} x –1 boost

7.8.2 DC/DC frame synchronous selection

DCFRM	DC/DC Operation
0	Asynchronous to frame signal
1	Synchronous to frame signal

7.8.3 DC/DC operation frequency selection

LPM	FS1	FS0	LFS1	LFS0	V_{DD2} and V_{CL} Operation Frequency
0	0	0	–	–	DCCLK/1
0	0	1	–	–	DCCLK/2
0	1	0	–	–	DCCLK/4
0	1	1	–	–	DCCLK/8
1	–	–	0	0	DCCLK/1
1	–	–	0	1	DCCLK/2
1	–	–	1	0	DCCLK/4
1	–	–	1	1	DCCLK/8

LPM	FS3	FS2	LFS3	LFS2	V_{GH} and V_{GL} Operation Frequency
0	0	0	x	x	DCCLK/1
0	0	1	x	x	DCCLK/2
0	1	0	x	x	DCCLK/4
0	1	1	x	x	DCCLK/8
1	x	x	0	0	DCCLK/1
1	x	x	0	1	DCCLK/2
1	x	x	1	0	DCCLK/4
1	x	x	1	1	DCCLK/8

7.8.4 DC/DC converter power ON time selection

PONM	PON	PUPT1	PUPT0	V_{DD2} Boost	V_R ON	V_{GL} Boost	V_{GH}/V_{CL} Boost V_S/V_{GM} Boost	
1	x	0	0	16/DCCLK	0.5 x 128/DCCLK	1.5 x 128/DCCLK	2.5 x 128/DCCLK	Internal sequence
1	x	0	1	16/DCCLK	0.5 x 256/DCCLK	1.5 x 256/DCCLK	2.5 x 256/DCCLK	Internal sequence
1	x	1	0	16/DCCLK	0.5 x 512/DCCLK	1.5 x 512/DCCLK	2.5 x 512/DCCLK	Internal sequence
1	x	1	1	16/DCCLK	0.5 x 1024/DCCLK	1.5 x 1024/DCCLK	2.5 x 1024/DCCLK	Internal sequence
0	1	x	x	External input	External input	External input	External input	External sequence
0	0	x	x	–	–	–	–	Normal mode

7.8.5 Division ratio selection of the DC/DC converter at power ON

PONM	PON	DUPF1	DUPF0	Division Ratio of the DC/DC Converter OSC Frequency
1	x	0	0	Internal sequence OSC = DCCLK/1
1	x	0	1	Internal sequence OSC = DCCLK/2
1	x	1	0	Internal sequence OSC = DCCLK/4
1	x	1	1	Internal sequence OSC = DCCLK/8
0	1	0	0	External sequence OSC = DCCLK/1
0	1	0	1	External sequence OSC = DCCLK/2
0	1	1	0	External sequence OSC = DCCLK/4
0	1	1	1	External sequence OSC = DCCLK/8
0	0	x	x	Valid of FS0, FS1, FS3, and FS4 setting

7.8.6 V_{REFR} regulator selection output

RGON	VC2	VC1	VC0	V_{REFR}
0	x	x	x	V_{REFR} regulator OFF (V_{REFR} = Hi-Z)
1	0	0	0	1.50 V
1	0	0	1	1.60 V
1	0	1	0	1.70 V
1	0	1	1	1.80 V
1	1	0	0	1.90 V
1	1	0	1	2.00 V
1	1	1	0	2.05 V
1	1	1	1	2.10 V

<R> **7.8.7 V_{GM} regulator selection output**

RGON	VSHI	VSEL2	VSEL1	VSEL0	V_{GM}			
					V_{GM}	V_{REFR} = 1.5 V	V_{REFR} = 2.0 V	V_{REFR} = 2.1 V
0	x	x	x	x	V_{GM} regulator OFF (V_{GM} = V_{SS})			
1	1	x	x	x	V_{GM} regulator OFF (V_{GM} = Hi-Z)			
1	0	0	0	0	V_{REFR} x 2.200	3.30	4.40	4.62
1	0	0	0	1	V_{REFR} x 2.250	3.38	4.50	4.73
1	0	0	1	0	V_{REFR} x 2.300	3.45	4.60	4.83
1	0	0	1	1	V_{REFR} x 2.350	3.53	4.70	4.94
1	0	1	0	0	V_{REFR} x 2.400	3.60	4.80	5.04
1	0	1	0	1	V_{REFR} x 2.450	3.68	4.90	5.15
1	0	1	1	0	V_{REFR} x 2.500	3.75	5.00	5.25
1	0	1	1	1	V_{REFR} x 2.550	3.83	5.10	5.36

7.8.8 V_S regulator selection output

RGON	VSHI	VSSEL2	VSSEL1	VSSEL0	V_S			
					V_S	V_{REFR} = 1.5 V	V_{REFR} = 2.0 V	V_{REFR} = 2.1 V
0	x	x	x	x	V_S regulator OFF (V_S = V_{SS})			
1	1	x	x	x	V_S regulator OFF (V_S = Hi-Z)			
1	0	0	0	0	V_{REFR} x 2.425	3.64	4.85	5.09
1	0	0	0	1	V_{REFR} x 2.450	3.68	4.90	5.15
1	0	0	1	0	V_{REFR} x 2.475	3.71	4.95	5.20
1	0	0	1	1	V_{REFR} x 2.500	3.75	5.00	5.25
1	0	1	0	0	V_{REFR} x 2.525	3.79	5.05	5.30
1	0	1	0	1	V_{REFR} x 2.550	3.83	5.10	5.36
1	0	1	1	0	V_{REFR} x 2.575	3.86	5.15	5.41
1	0	1	1	1	V_{REFR} x 2.600	3.90	5.20	5.46

7.8.9 V_R regulator selection output

RGONR	VRHI	VRSEL2	VRSEL1	VRSEL0	V_R			
					V_R	V_{REFR} = 1.5 V	V_{REFR} = 2.0 V	V_{REFR} = 2.1 V
0	x	x	x	x	V_R regulator OFF (V_R = V_{SS})			
1	1	x	x	x	V_R regulator OFF (V_R = Hi-Z)			
1	0	0	0	0	V_{REFR} x 2.250	3.38	4.50	4.73
1	0	0	0	1	V_{REFR} x 2.400	3.60	4.80	5.04
1	0	0	1	0	V_{REFR} x 2.450	3.68	4.90	5.15
1	0	0	1	1	V_{REFR} x 2.500	3.75	5.00	5.25
1	0	1	0	0	V_{REFR} x 2.525	3.79	5.05	5.30
1	0	1	0	1	V_{REFR} x 2.550	3.83	5.10	5.36
1	0	1	1	0	V_{REFR} x 2.600	3.90	5.20	5.46
1	0	1	1	1	V_{REFR} x 2.700	4.05	5.40	5.67

7.8.10 V_{DCI} regulator selection output

VDCION	VDCIHZ	VDCISEL	VD2ON1	V_{DCI} (Limit value)
1	x	x	0	3.2 V
1	x	x	1	2.1 V
0	1	x	x	Hi-Z
0	0	0	x	V_{DC}
0	0	1	x	V_{SS}

7.8.11 RV_{DD} regulator selection output

VSTBY	SFVSEL	RV_{DD}
V_{SS}	0	2.1 V
V_{SS}	1	2.3 V
V_{DC}	x	Hi-Z

7.8.12 V_S, V_R Amp. current selection

RGON, RGONR	LPM	ACS1	ACS0	LACS1	LACS0	V_S Status	V_R Status	State of Circuit Current
1	0	0	0	x	x	Output	Output	Amp. current = x 1
1	0	0	1	x	x	Output	Output	Amp. current = x 2
1	0	1	0	x	x	Output	Output	Amp. current = x 3
1	0	1	1	x	x	Output	Output	Amp. current = x 6
1	1	x	x	0	0	Output	Output	Amp. current = x 0.25
1	1	x	x	0	1	Output	Output	Amp. current = x 0.5
1	1	x	x	1	0	Output	Output	Amp. current = x 1.0
1	1	x	x	1	1	Output	Output	Amp. current = x 1.5

7.8.13 VCOMM output control

COMONM	COHIM	COHIS	STBY	STBY GOFF	CDA_AMP	VCOMHM/ VCOMLM AMP	VCOMM	Gate
0	x	x	0	0	OFF	OFF	Hi-Z	ON
1	1	x	0	0	ON	OFF	Hi-Z	ON
1	0	x	0	0	ON	ON	ON	ON
1	0	x	1	0	ON	ON	VCOMLM	V_{GH}
1	0	x	1	1	ON	ON	V_{SS}	V_{GL}
x	0	0	1	1	ON	ON	V_{SS}	V_{GL}

7.8.14 VCOMM output capability control

COMONM	COHIM1	COHIM0	COMP1	COMP0	VCOMM
1	1	x	0	0	VCOMM capability = x 1 mode
1	1	x	0	1	VCOMM capability = x 1.5 mode
1	1	x	1	0	VCOMM capability = x 2 mode
1	1	x	1	1	VCOMM capability = x 2.5 mode

7.8.15 VCOM Amp. current selection

COMONM	LPM	COMCS1	COMCS0	LCOMCS1	LCOMCS0	VCOMHM-AMP, VCOMLM-AMP	State of Circuit Current
0	x	x	x	x	x	OFF	Amp., CS power OFF
1	0	0	0	x	x	ON	Amp. current = x 1
1	0	0	1	x	x	ON	Amp. current = x 2
1	0	1	0	x	x	ON	Amp. current = x 3
1	0	1	1	x	x	ON	Amp. current = x 7
1	1	x	x	0	0	ON	Amp. current = x 0.25
1	1	x	x	0	1	ON	Amp. current = x 0.5
1	1	x	x	1	0	ON	Amp. current = x 1.0
1	1	x	x	1	1	ON	Amp. current = x 1.5

7.8.16 VCOMM center adjustment selection

Setting by COMINM (D7 of R32), this register can select the setting method of common drive waveform VCOMM center voltage.

When COMINM = 1 is set, input directly VCOMM center voltage to VCOMINM pin outside IC.

COMINM	VCOMM Center Adjustment
0	Internal D/A valid (R32 valid setting)
1	Valid of VCOMINM input center level voltage

7.8.17 VCOM output amplitude adjustment

This is used to adjust the output amplitude of main/sub VCOMM output. The VCOM output amplitude voltage ($VCOM_{p-p}$) can be adjusted as shown by the expression below using VCOM amplitude control register (R31), which is the output voltage of a D/A converter circuit for which V_{GM} is the reference potential.

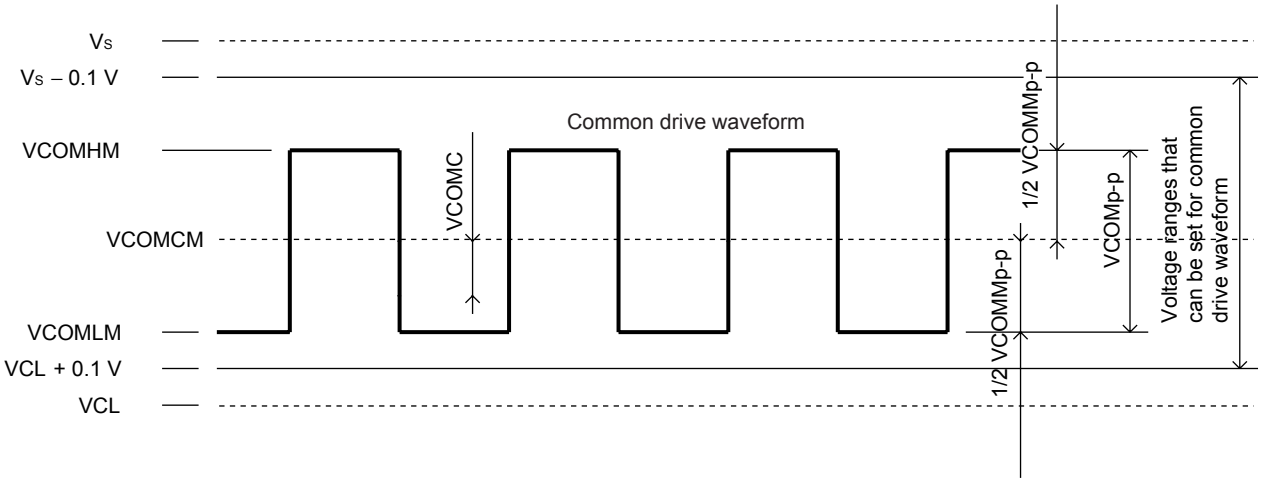
$$VCOMM_{p-p} = V_{GM} \times \{3/5 + \{3.15/5 \times (DA_{R31}/63)\}\}$$

Remark DA_{R31}: R31 setting values

The values of R31 that can be set are determined by the relationship of booster voltages V_{DD2} and V_{CL} to the potential level of the actual common drive waveform after VCOMM center adjustment.

Set the VCOMM output amplitude voltage, the VCOMM output center potential voltage setting level according to VCOMM center level control register (R32), or the VCOM output center potential input from VCOMINM in the relationships shown in the Figure 7–1.

Figure 7–1. Voltage Ranges that can be Set for Common Drive Waveform



<Conditions on common drive waveform voltage settings>

$3\ V \le VCOMM_{p-p} \le 5.5\ V$ ($VCOMM_{p-p}$ is not dependent on V_{DD2} and V_S)

$V_S \ge VCOMHM \ge VCOMLM \ge V_{CL}$

Remark $VCOMHM = 1/2\ VCOMM_{p-p} + VCOMCM$

$VCOMLM = VCOMCM – 1/2\ VCOMM_{p-p}$

VCOMCM: R32 setting values [COMINM (R32) = 0] or VCOMINM input voltage level [COMINM (R32) = 1]

Table 7–1. VCOM Output Amplitude Voltage ($VCOM_{p-p}$) Adjustment and D/A Converter Setting Values

DA5	DA4	DA3	DA2	DA1	DA0	DA_{R31}	$VCOM_{p-p}$ (Sample of V_{GM} = 5 V)
0	0	0	0	0	0	0	3.00 V
0	0	0	0	0	1	1	3.05 V
0	0	0	0	1	0	2	3.10 V
:	:	:	:	:	:	:	:
1	1	0	0	1	0	50	5.50 V
1	1	0	0	1	1	51	5.55 V (setting prohibited under here)
:	:	:	:	:	:	:	:
1	1	1	1	0	1	61	6.05 V (setting prohibited)
1	1	1	1	1	0	62	6.10 V (setting prohibited)
1	1	1	1	1	1	63	6.15 V (setting prohibited)

Remark The variable range of VCOMM output amplitude is set to V_{CL} + 0.1 V to V_S – 0.1 V. Also, use $VCOM_{p-p}$ to come a setup between 3.0 V and 5.5 V.

7.8.18 VCOMM output center adjustment

This is used to adjust the center potential level of VCOMM output. By VCOMM center level adjustment register (R32, R33), VCOMM output center potential voltage (VCOMCM) can adjust the output voltage, or the D/A converter circuit which makes V_{GM} reference potential so that it may be below formula.

$$VCOMCM = V_{GM} \times \{1/5 + \{2/5 \times (DA/127)\}\}$$

Remark DA: R32 setting values or R33 setting values

Table 7–2. VCOMM Output Center Potential Voltage (VCOMCM) and D/A Converter Setting Values

MCDA6	MCDA5	MCDA4	MCDA3	MCDA2	MCDA1	MCDA0	D/A	VCOMCM (V_{GM} = 5 V)
0	0	0	0	0	0	0	0	1.000 V
0	0	0	0	0	0	1	1	1.016 V
0	0	0	0	0	1	0	2	1.031 V
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	1	125	2.968 V
1	1	1	1	1	1	0	126	2.984 V
1	1	1	1	1	1	1	127	3.000 V

Remark The range in which the VCOMM output center can be varied is restricted by the output voltage of V_S and V_{CL}.

7.9 Value of Wiring Resistance to Each Pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Table 7–3. Recommended Wiring Resistor Values

Pin Name	Wiring Resistor Values (Ω)
V_{SS}	< 10
V_{DC}	< 10
V_{DCI}	< 10
RV_{DD}	< 10
V_S	< 10
V_R	< 10
V_{GM}	< 10
V_{GH}	< 50
V_{DD2}	< 10
V_{GL}	< 10
V_{CL}	< 10
VCOMHM	< 10
VCOMLM	< 10
VCOMM	< 10
C11+	< 10
C11–	< 10
C12+	< 10
C12–	< 10
C21+	< 50
C21–	< 50
C22+	< 50
C22–	< 50
C23+	< 50
C23–	< 50
C31+	< 10
C31–	< 10

7.10 Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Table 7–4. Recommended Values of External Capacitor

Pin Name	Recommended Value of Capacitors (μF)	Withstanding Voltage (V)
V_{DC}	1 to 4.7	6.3 or more
V_{DCI}	1 to 4.7	6.3 or more
RV_{DD}	1 to 4.7	6.3 or more
V_S	1 to 4.7	6.3 or more
V_R	1 to 4.7	10 or more
V_{GM}	1 to 4.7	6.3 or more
V_{GH}	0.47 to 1	25 or more
V_{DD2}	1 to 4.7	10 or more
V_{GL}	0.47 to 1	25 or more
V_{CL}	1 to 4.7	6.3 or more
VCOMHM	1 to 4.7	6.3 or more
VCOMLM	1 to 4.7	6.3 or more
C11+, C11–	1 to 4.7	6.3 or more
C12+, C12–	1 to 4.7	6.3 or more
C21+, C21–	0.47 to 1	10 or more
C22+, C22–	0.47 to 1	10 or more
C23+, C23–	0.47 to 1	10 or more
C31+, C31–	1 to 4.7	6.3 or more

7.11 Shottky Diode Specification

The recommended specification of the external shottky diode are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Connection Place	Connect by low resistance (10 Ω or less) between V_{GL}-V_{SS} and between V_{DC}-V_{DD2}
V_F	0.5 V (200 mA) or less
V_R	30 V or more
I_R	5 μA or less

8. POWER SUPPLY INJECTION/INTERCEPTION

The example of power ON/OFF sequence in the μPD161704A chip set is indicated.

8.1 Example of the □PD161704A Power ON Sequence

The example of sequence is indicated. It is the case that the simple sequence is used.

Input hard-reset to μPD161704A

↓

μPD161704A register reset

μPD161704A command reset
(R3 register)

R3

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1

↓

μPD161704A oscillator start

μPD161704A internal oscillator start
(R58 register)

R58

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1

↓

MIN. 1 line period (It is for the waiting for oscillation stable time)

μPD161704A γ-setting

μPD161704A γ-setting
(If you need it, you set it.)

R36 to R39, R82, R83, R97 to R102

Setting of R36 to R39, R82, R83 and R97 to R102 are in random order.

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	X	X	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A Horizontal period timing setting

μPD161704A horizontal period timing setting
(If you need it, you set it)

R77 to R79

Setting of R77 to R79 are in random order.

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	X	X	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

LCD display area setting

μPD161704A LCD display area setting
(R41-R44 register)

↓

R41 to R44 Setting of R41 to R44 are in random order.

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	X	X	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

Window setting

μPD161704A window setting
(R8-R11 register)

↓

R8 to R11 Setting of R8 to R11 are in random order.

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	X	X	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A window mode setting
(R5 register)

↓

R5

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	1	0	X	0	0

X: Set in accordance with the usage conditions.

↓

μPD161704A write address setting
(R6, R7 register)

↓

R6, R7 Setting of R6 and R7 are in random order.

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	X	X	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A display data input

RS	D15	D14	D13	D12	D11	D10	D9	D8
H	X	X	X	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

Power supply setting

μPD161704A power supply setting (R25 register)

R25

	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	1	0	0	0

↓

μPD161704A power supply setting (R26 register)

R26

	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting (R27 register)

R27

	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	1	0	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting (R28 register)

R28

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	1	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting (R29 register)

R29

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting
(R30 register)

R30

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	X	X	0	0	0	1

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting
(R31 register)

R31

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting
(R32 register)

R32

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	X

X: Set in accordance with the usage conditions.

↓

μPD161704A power supply setting
(R24 register)

R24

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	1	1	1	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	1

X: Set in accordance with the usage conditions.

↓

Power supply ON after the time set by PUPT0/PUPT1 in R27 is passed.

Display start setting

μPD161704A GOE1, GOE2 signal start
(R59 register)

R59

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1

↓

After time of 1-flame is passed, the display color is all white of all black.

μPD161704A display setting
(R0 register)

R0

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	X	0	0	0	0	0

X: Set in accordance with the usage conditions.

After DISP0 and DISP1 are released, normal RAM data is display.

8.2 Example of the μPD161704A Power OFF Sequence

The example of sequence is indicated. It is the case that the internal sequence is used.

Set μPD161704A in stand-by mode

μPD161704A stand-by mode setting 1
(R0 register)

R0

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	1	0	X	X

X: Set in accordance with the usage conditions.

↓

2 flame time wait

Panel is discharged. In case that the panel is normally white, the display color is white.

μPD161704A stand-by mode setting 2
(R0 register)

R0

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	1	1	X	X

X: Set in accordance with the usage conditions.

↓

Source output = Hi-Z, VCOM output = V_{SS}, GATE output = Low level. The stress to the panel at the time of stand-by can be stopped.

μPD161704A power off setting
(R24 register)

R24

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	X	X	X	X	X
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	X	0

X: Set in accordance with the usage conditions.

↓

Power OFF!

μPD161704A internal oscillator stop
(R58 register)

R26

RS	D15	D14	D13	D12	D11	D10	D9	D8
L	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0

↓

Power OFF is completed!!
(Stand-by is completed)

9. RESET

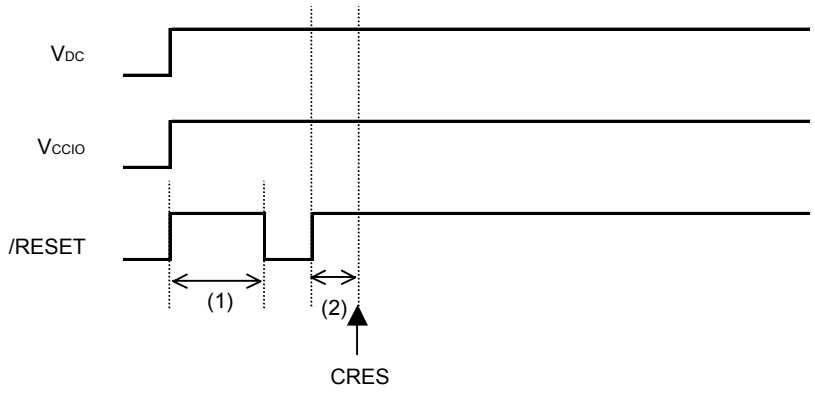
If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

Moreover, /RESET pin input can also be changed into the state of a default setup of each register by setting RESET_SEL pin to "H." However, the registers which will be in the state of a default setup by the register mode set up by REGSEL1 and REGSEL0 pin input differ.

Table 9–1. Relationship Register which Register Mode and Default State by REGSEL1, REGSEL0 pin and RESET_SEL pin

REGSEL1	REGSEL0	Register Mode	RESET_SEL	Register which becomes Default setup with /RESET Pin
L	L	1	L	E2OPC [2:0]
			H	E2OPC [2:0], R24 register
L	H	2	L	E2OPC [2:0]
			H	All register (same as reset command)
H	L	3	L	E2OPC [2:0]
			H	E2OPC [2:0], R257 register
H	H	4	L	E2OPC [2:0]
			H	All register (same as reset command)

Figure 9–1. Caution at the time of Power Injection

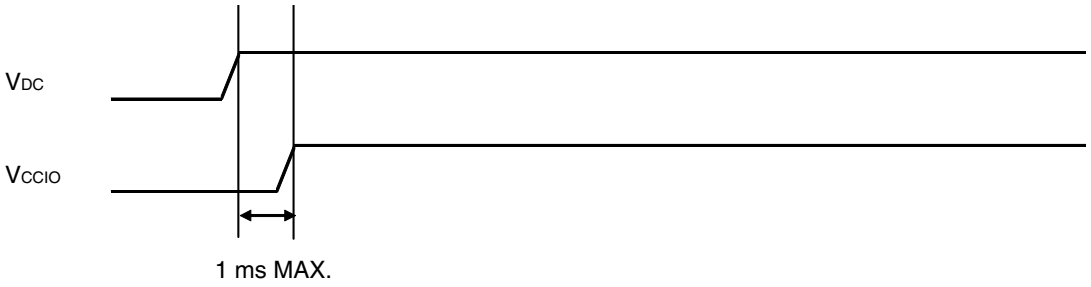


In addition, set up as short as possible time (1) until it applies hardware reset from a power supply injection at the time of a power supply injection. The /RESET pin is set to L from before the power supply injection, and if it rises after a power supply injection, it is not necessary to care about the time of (1). In between until it restricts at the time of low temperature and applies hardware reset, since an internal setup of a power supply system is unstable, an over-current may flow.

When using it by setup which does not reset a register in hardware reset (RESET_SEL = L), set up about time (1) until it applies hardware reset from a power supply injection (set up also about time (2) until it applies command reset from hardware reset release) as short (1 μs MIN.) as possible. Since an internal setup of a power supply system is unstable, an over-current may flow, until it restricts at the time of low temperature and command reset is inputted.

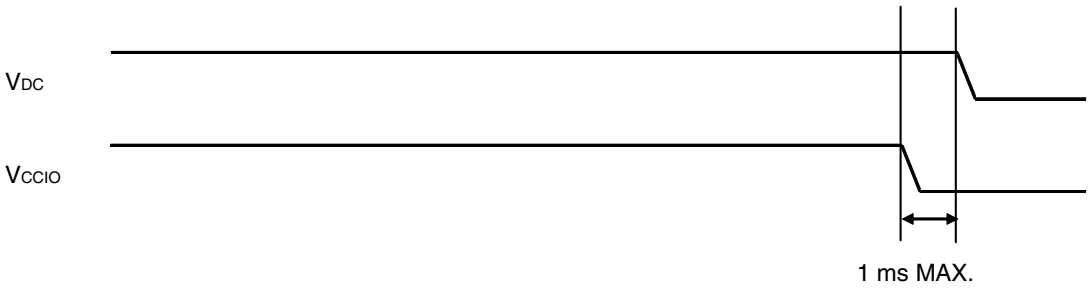
<R> 10. POWER SUPPLY INJECTION/ITERCEPTION ORDER

10.1 Recommendation Power Supply Injection Order



Caution After V_{CCIO} power supply injection, if it is in the state of V_{DC} = 0 V, the state of I/O pin will become unfixed.

10.2 Recommendation Power Supply Interception Order



Cautioin If it will be in the state of V_{DC} = 0 V during V_{CCIO} power supply injection, the state of I/O pin will become unfixed.

11. COMMAND

11.1 Command List

(it supplements about the view of a table)

Register mode 1, 2

Index		Data																Description
10 HEX.	16 HEX.	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
000	0000									DISP1	DISP0	ADC	DTY	STBY			GSMD	Display setting register 1
										1								Display data all 1 output (0: Normal, 1: All 1 fixed [6'h3F])
											0							Display data all 0 output (0: Normal, 1: All 0 fixed [6'h00])
												0						RAM write control (X direction, both R and B are switchable) (0: Y1 to Y768, 1: Y768 to Y1)
													0					Partial display (0: Normal display, 1: Partical display)
														0				Display OFF (0: Normal display, 1: Display OFF)
																	0	Partial non-display area gate scan (0: Normal operation, 1: Stop)

Initialization in reset

Register name

Register mode 1, 2

(1/3)

Index		Data																Description
10 HEX.	16 HEX.	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
000	0000									DISP1	DISP0	ADC	DTY	STBY	STBY_SOFF	LPM	GSM	Display setting register £ ±
										1								Display data all 1 output (0: Normal, 1: All 1 fixed [6'h3F]£ ©
											0							Display data all 0 output (0: Normal, 1: All 0 fixed [6'h00]£ ©
												0						RAM write control (X direction, both R and B are switchable) (0: Y1 to Y720, 1: Y720 to Y1)
													0					Partial display (0: Normal display, 1: Partial display)
														0				Display OFF (0: Normal operation, 1: Display OFF)
															0			Stand-by fixed status control (0: As usual, 1: Source = Hi-Z, gate = All OFF, common = VSS)
																0		Low power mode (0: Normal mode, 1: Low power mode)
																	0	Gate scan on partial non-display area (0: Normal operation, 1: Stop)
001	0001									ADX	ADY		BGR			LTS		Display setting register 2
										0								RAM X address direction inversion (0: Normal, 1: Inversion)
											0							RAM Y address direction inversion (0: Normal, 1: Inversion)
												0						Test register (0 fixed)
													0					RGB data inversion (both R and B are switchable) (0: Normal, 1: Inversion)
																0		Frame frequency 1/2 (= 1 line time x 2) (0: Normal, 1: 1/2)
002	0002										DCKEG	VSEG	HSEG	VIMD	NWRGB	RGBS	DISPCK	RGB interface register
											0							DOTCLK active direction (0: Rising edge, 1: Falling edge)
												0						VSYNC active direction (0: L active, 1: H active)
													0					HSYNC active direction (0: L active, 1: H active)
														0				VSYNC interface mode (0: OSC or RGB interface display, 1: VSYNC interface display)
															0			RGB interface mode (0: RGB invalid, 1: RGB valid)
																0		RGB interface mode (0: Through mode, 1: Capture mode)
																	0	Display clock (0: OSC, 1: DOTCLK)
003	0003																CRES	Soft reset
																	0	Soft reset (reset pulse occurs by writing in "1")
004	0004																GS	Color mode
																	0	GS = 0: 260-k color (64 gray scale), GS = 1: 8 color (2 gray scale)
005	0005												WAS	DINV	INC			RAM control register
												0						Test register £ 0 fixed)
													0					Window access control (0: Normal access, 1: Window access)
														0				RAM write, read data inversion (0: Normal, 1: Data inversion)
															0			RAM address counter control (0: Count to X direction, 1: Count to Y direction)
																0		Test register (0 fixed)
																	0	Test register (0 fixed)
006	0006									XA[7]	XA[6]	XA[5]	XA[4]	XA[3]	XA[2]	XA[1]	XA[0]	RAM X address
										0	0	0	0	0	0	0	0	
007	0007								YA[8]	YA[7]	YA[6]	YA[5]	YA[4]	YA[3]	YA[2]	YA[1]	YA[0]	RAM Y address
									0	0	0	0	0	0	0	0	0	
008	0008									XMN[7]	XMN[6]	XMN[5]	XMN[4]	XMN[3]	XMN[2]	XMN[1]	XMN[0]	Minimum X address in window access mode
										0	0	0	0	0	0	0	0	
009	0009									XMX[7]	XMX[6]	XMX[5]	XMX[4]	XMX[3]	XMX[2]	XMX[1]	XMX[0]	Maximum X address in window access mode
										1	1	1	0	1	1	1	1	
010	000A								YMN[8]	YMN[7]	YMN[6]	YMN[5]	YMN[4]	YMN[3]	YMN[2]	YMN[1]	YMN[0]	Minimum Y address in window access mode
									0	0	0	0	0	0	0	0	0	
011	000B								YMX[8]	YMX[7]	YMX[6]	YMX[5]	YMX[4]	YMX[3]	YMX[2]	YMX[1]	YMX[0]	Maximum Y address in window access mode
									1	0	0	1	1	1	1	1	1	
012	000C			0	0	0	0	0	0	0	0	0	0	0	0	0	0	Test register (0 fixed)
013	000D			0	0	0	0	0	0	0	0	0	0	0	0	0	0	Test register (0 fixed)
014	000E																	RAM Write index
015	000F																	
016	0010																PSEL	Partial non-display area display setting
																	0	Partial non-display area display setting (0: Specified color, 1: RAM data 8-color display)
017	0011														PGR	PGG	PGB	Partial non-display area display setting
															0			Partial non-display area [R] specified color setting (0:6'h00； ¢:6'h3F)
																0		Partial non-display area [G] specified color setting (0:6'h00； ¢:6'h3F)
																	0	Partial non-display area [B] specified color setting (0:6'h00； ¢:6'h3F)
018	0012								P1SL[8]	P1SL[7]	P1SL[6]	P1SL[5]	P1SL[4]	P1SL[3]	P1SL[2]	P1SL[1]	P1SL[0]	Partial 1 display area start line
									0	0	0	0	0	0	0	0	0	
019	0013								P2SL[8]	P2SL[7]	P2SL[6]	P2SL[5]	P2SL[4]	P2SL[3]	P2SL[2]	P2SL[1]	P2SL[0]	Partial 2 display area start line
									0	0	0	0	0	0	0	0	0	
020	0014								P1AW[8]	P1AW[7]	P1AW[6]	P1AW[5]	P1AW[4]	P1AW[3]	P1AW[2]	P1AW[1]	P1AW[0]	Partial 1 display area line number
									0	0	0	0	0	0	0	0	0	
021	0015								P2AW[8]	P2AW[7]	P2AW[6]	P2AW[5]	P2AW[4]	P2AW[3]	P2AW[2]	P2AW[1]	P2AW[0]	Partial 2 display area line number
									0	0	0	0	0	0	0	0	0	
022	0016								P1SA[8]	P1SA[7]	P1SA[6]	P1SA[5]	P1SA[4]	P1SA[3]	P1SA[2]	P1SA[1]	P1SA[0]	Partial 1 display area start line display RAM address
									0	0	0	0	0	0	0	0	0	
023	0017								P2SA[8]	P2SA[7]	P2SA[6]	P2SA[5]	P2SA[4]	P2SA[3]	P2SA[2]	P2SA[1]	P2SA[0]	Partial 2 display area start line display RAM address
									0	0	0	0	0	0	0	0	0	
024	0018				VDCION	RGONR	RGON	VCLON	VGLREF	VGLON[1]	VGLON[0]	VGHREF	VGHON[1]	VGHON[0]	VD2ON[1]	VD2ON[0]	DCON	DC/DC operation setting
					0	0	0	0	0	0	0	0	0	0	0	0	0	
025	0019									VDCISEL	VDCIHZ	VRHI	VSHI	DCFRM	DC3HZ	DC2HZ	DC1HZ	DC/DC output setting
										0	0	0	0	1	0	0	0	
026	001A									LFS[3]	LFS[2]	LFS[1]	LFS[0]	FS[3]	FS[2]	FS[1]	FS[0]	DC/DC frequency setting
										0	1	0	1	0	1	0	1	
027	001B											PONM	PON	DUPF[1]	DUPF[0]	PUPT[1]	PUPT[0]	DC/DC rising setting
												1	0	0	0	1	0	
028	001C				SFVSEL	VSEL[2]	VSEL[1]	VSEL[0]	VRSEL[2]	VRSEL[1]	VRSEL[0]	VSSEL[2]	VSSEL[1]	VSSEL[0]	VC[2]	VC[1]	VC[0]	Regulator voltage setting
					1	0	0	0	0	1	1	0	1	1	1	0	1	
029	001D								REGMON	LCDMCS[1]	LCDMCS[0]	COMCS[1]	COMCS[0]	LACS[1]	LACS[0]	ACS[1]	ACS[0]	Regulator current setting
									0	0	0	0	0	0	0	1	0	
030	001E											COMP[1]	COMP[0]		COMHIM		COMONM	VCOM output setting

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031	001F										DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	VCOM amplitude setting
											0	0	0	0	0	0	
032	0020								COMINM	CDA[6]	CDA[5]	CDA[4]	CDA[3]	CDA[2]	CDA[1]	CDA[0]	VCOMM cencter setting
									0	0	0	0	0	0	0	0	
033	0021																
034	0022																
035	0023																
036	0024									GPH[6]	GPH[5]	GPH[4]	GPH[3]	GPH[2]	GPH[1]	GPH[0]	amplitude setting
										1	1	1	1	1	1	1	
037	0025									GNH[6]	GNH[5]	GNH[4]	GNH[3]	GNH[2]	GNH[1]	GNH[0]	amplitude setting
										1	1	1	1	1	1	1	
038	0026									GPL[6]	GPL[5]	GPL[4]	GPL[3]	GPL[2]	GPL[1]	GPL[0]	amplitude setting
										0	0	0	0	0	0	0	
039	0027									GNL[6]	GNL[5]	GNL[4]	GNL[3]	GNL[2]	GNL[1]	GNL[0]	amplitude setting
										0	0	0	0	0	0	0	
040	0028																
041	0029								LCDXMIN[7]	LCDXMIN[6]	LCDXMIN[5]	LCDXMIN[4]	LCDXMIN[3]	LCDXMIN[2]	LCDXMIN[1]	LCDXMIN[0]	[LCDSIZE] X MIN. size set
									0	0	0	0	0	0	0	0	
042	002A							LCDYMIN[8]	LCDYMIN[7]	LCDYMIN[6]	LCDYMIN[5]	LCDYMIN[4]	LCDYMIN[3]	LCDYMIN[2]	LCDYMIN[1]	LCDYMIN[0]	[LCDSIZE] Y MIN. size set
								0	0	0	0	0	0	0	0	0	
043	002B								LCDXMAX[7]	LCDXMAX[6]	LCDXMAX[5]	LCDXMAX[4]	LCDXMAX[3]	LCDXMAX[2]	LCDXMAX[1]	LCDXMAX[0]	[LCDSIZE] X MAX. size set
									1	1	1	0	1	1	1	1	
044	002C							LCDYMAX[8]	LCDYMAX[7]	LCDYMAX[6]	LCDYMAX[5]	LCDYMAX[4]	LCDYMAX[3]	LCDYMAX[2]	LCDYMAX[1]	LCDYMAX[0]	[LCDSIZE] Y MAX. size set
								1	0	0	1	1	1	1	1	1	
045	002D															OC	Calibration register
																0	Calibration start/stop (0: Stop, 1: Start)
046	002E								BCNT[7]	BCNT[6]	BCNT[5]	BCNT[4]	BCNT[3]	BCNT[2]	BCNT[1]	BCNT[0]	Basical clock for 1 line (BASECOUNT[7:0]) number specified
									0	0	0	0	0	0	0	0	
047	002F																
048	0030																
049	0031																
050	0032													R	L	SCN1	SCN0	Gate scan setting
														0				Gate scan direction (0: O1 to O320, 1: O320 to O1)
																0	0	Gate signal panel connection setting
051	0033															NLINE[1]	NLINE[0]	n line inversion line number
																0	0	Line inversion line number
																		{NLINE1,NLINE0} = 0, 0: 1 line inversion, 0, 1: 2 line inversion, 1,0: 4 line inversion, 1,1: 8 line inversion
052	0034													GSMLN[2]	GSMLN[1]	GSMLN[0]		Gate scan in partial mode
														0	0	0		Gate scan in partial mode
																		{GSMLN2,1,0} = 0, 00,: scan stop, 0,0,1: 3-frame cycle, 0,1,0: 5-frame cycle ...
																		… 1,1,0: 13-frame cycle, 1,1,1: 15-frame cycle}
053	0035																PNFRM	Polarity inversion on partial non-display area
																	0	Polarity inversion on partial non-display area (0: Line inversion, 1: Frame inversion)
054	0036																	
055	0037															GSCAN[1]	GSCAN[0]	Line inversion/frame inversion/interlace setting
																0	0	Interlace display
																		{GSCAN1,GSCAN0} = 0,0: n line inversion, 0,1: Frame inversion, 1,0: Skip 1D, 1,1: Skip 2B
056	0038																	
057	0039																	
058	003A																OSCON	Oscillator control
																	0	Oscillator control (0:oscillator stop, 1: oscillator operation)
059	003B															GOE2ON	GOE1ON	Gate scan operation setting register
																0		Gate "H" fixed function (0: Normal operation, 1: Gate all "H")
																	0	Gate "L" fixed function (0: Gate all "L", 1: Normal operation)
060	003C							RGBST[8]	RGBST[7]	RGBST[6]	RGBST[5]	RGBST[4]	RGBST[3]	RGBST[2]	RGBST[1]	RGBST[0]	RGB interface through mode display start line
								0	0	0	0	0	0	0	0	0	
061	003D							RGBED[8]	RGBED[7]	RGBED[6]	RGBED[5]	RGBED[4]	RGBED[3]	RGBED[2]	RGBED[1]	RGBED[0]	RGB interface through mode display end line
								0	0	0	0	0	0	0	0	0	
062	003E								HBP[3]	HBP[2]	HBP[1]	HBP[0]	VBP[3]	VBP[2]	VBP[1]	VBP[0]	RGB interface backporch period setting
									0	0	0	1					Horizontal backporch period
													0	0	0	1	Vertical backporch period
063	003F								CAPXMIN[7]	CAPXMIN[6]	CAPXMIN[5]	CAPXMIN[4]	CAPXMIN[3]	CAPXMIN[2]	CAPXMIN[1]	CAPXMIN[0]	Minimum X address in RGB interface capture mode window access
									0	0	0	0	0	0	0	0	
064	0040								CAPXMAX[7]	CAPXMAX[6]	CAPXMAX[5]	CAPXMAX[4]	CAPXMAX[3]	CAPXMAX[2]	CAPXMAX[1]	CAPXMAX[0]	Maximum X address in RGB interface capture mode window access
									1	1	1	0	1	1	1	1	
065	0041								CAPYMIN[7]	CAPYMIN[6]	CAPYMIN[5]	CAPYMIN[4]	CAPYMIN[3]	CAPYMIN[2]	CAPYMIN[1]	CAPYMIN[0]	Minimum Y address in RGB interface capture mode window access
								0	0	0	0	0	0	0	0	0	
066	0042								CAPYMAX[7]	CAPYMAX[6]	CAPYMAX[5]	CAPYMAX[4]	CAPYMAX[3]	CAPYMAX[2]	CAPYMAX[1]	CAPYMAX[0]	Maximum Y address in RGB interface capture mode window access
								1	0	0	1	1	1	1	1	1	
067	0043																
068	0044													E2OPC[2]	E2OPC[1]	E2OPC[0]	E2PROM operation
														0	0	0	E2PROM operation start
069	0045								E2EN[7]	E2EN[6]	E2EN[5]	E2EN[4]	E2EN[3]	E2EN[2]	E2EN[1]	E2EN[0]	E2PROM operation 2
									0	0	0	0	0	0	0	0	E2PROM write permission enable register
070	0046								E2A[7]	E2A[6]	E2A[5]	E2A[4]	E2A[3]	E2A[2]	E2A[1]	E2A[0]	E2PROM write address specified
									0	0	0	0	0	0	0	0	
071	0047	E2IR[15]	E2IR[14]	E2IR[13]	E2IR[12]	E2IR[11]	E2IR[10]	E2IR[9]	E2IR[8]	E2IR[7]	E2IR[6]	E2IR[5]	E2IR[4]	E2IR[3]	E2IR[2]	E2IR[1]	E2IR[0]	E2PROM write index register specified
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

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072	0048									E2ID[23]	E2ID[22]	E2ID[21]	E2ID[20]	E2ID[19]	E2ID[18]	E2ID[17]	E2ID[16]	Product information register [23:16]
										0	0	0	0	0	0	0	0	
073	0049									E2ID[15]	E2ID[14]	E2ID[13]	E2ID[12]	E2ID[11]	E2ID[10]	E2ID[9]	E2ID[8]	Product information register [15:8]
										0	0	0	0	0	0	0	0	
074	004A									E2ID[7]	E2ID[6]	E2ID[5]	E2ID[4]	E2ID[3]	E2ID[2]	E2ID[1]	E2ID[0]	Product information register [7:0]
										0	0	0	0	0	0	0	0	
075	004B									E2SA[7]	E2SA[6]	E2SA[5]	E2SA[4]	E2SA[3]	E2SA[2]	E2SA[1]	E2SA[0]	E2PROM read start address specified
										0	0	0	0	0	0	0	0	
076	004C																	
077	004D	GOED[7]	GOED[6]	GOED[5]	GOED[4]	GOED[3]	GOED[2]	GOED[1]	GOED[0]	GOST[7]	GOST[6]	GOST[5]	GOST[4]	GOST[3]	GOST[2]	GOST[1]	GOST[0]	GOE1 change position setting
		0	0	0	0	0	0	0	1									GOE1 falling position setting
										0	0	0	0	0	1	0	1	GOE1 rising position setting
078	004E									VMCHG[7]	VMCHG[6]	VMCHG[5]	VMCHG[4]	VMCHG[3]	VMCHG[2]	VMCHG[1]	VMCHG[0]	COM(VM) polarity switch position
										0	0	0	0	0	0	0	1	
079	004F	SWED[7]	SWED[6]	SWED[5]	SWED[4]	SWED[3]	SWED[2]	SWED[1]	SWED[0]	SWST[7]	SWST[6]	SWST[5]	SWST[4]	SWST[3]	SWST[2]	SWST[1]	SWST[0]	SWON change position
		0	0	0	0	0	0	0	0									SWON falling edge position
										0	0	0	0	0	1	0	0	SWON rising edge position
080	0050																	
081	0051																	
082	0052									GI[2]	GI[1]	GI[0]			GRES		G3SW	circuit setting 1
										0	0	1						amplifier bias current （set up for magnification, using a default state as 1)
																		{GI2,1,0} = 0,0,0: 0.5 time, 0,0,1: 1 time, 0,1,0: 1.5 time, 0,1,1: 2 time
																		1,0,0: 2.5 time, 1,0,1: 3 time, 1,1,0: 3.5 time, 1,1,1: 4 time
															0			resistance switch
																	0	middle amplifier (0: OFF, 1: ON)
083	0053										GAP[2]	GAP[1]	GAP[0]		GAN[2]	GAN[1]	GAN[0]	circuit setting 2
											0	0	1					Gray scale amp. 0 to 31-gray scale bias current control （set up for maginfication, using a default state as 1)
																		{GAP2 to 0} = 0,0,0: 0.5 time, 0,0,1: 1 time, 0,1,0: 1.5 time, 0,1,1: 2 time
																		1,0,0: 3 time, 1,0,1: 4 time, 1,1,0: 6 time, 1,1,1: 7.5 time
															0	0	1	Gray scale amp. 32 to 63-gray scale bias current control (set up for magnification, using a default state as 1)
																		{GAP2 to 0} = 0,0,0: 0.5 time, 0,0,1: 1 time, 0,1,0: 1.5 time, 0,1,1: 2 time
																		1,0,0: 3 time, 1,0,1: 4 time, 1,1,0: 6 time, 1,1,1: 7.5 time
084	0054																	
086	0056													1	0	1	0	Test register
:																		
096	0060																	
097	0061											GM1P[5]	GM1P[4]	GM1P[3]	GM1P[2]	GM1P[1]	GM1P[0]	adjustment V10 positive polarity
												1	0	1	0	1	1	
098	0062											GM3N[5]	GM3N[4]	GM3N[3]	GM3N[2]	GM3N[1]	GM3N[0]	adjustment V9 negative polarity
												0	1	0	1	0	0	
099	0063											GM2P[5]	GM2P[4]	GM2P[3]	GM2P[2]	GM2P[1]	GM2P[0]	adjustment V34 positive polarity
												0	1	1	1	1	1	
100	0064											GM2N[5]	GM2N[4]	GM2N[3]	GM2N[2]	GM2N[1]	GM2N[0]	adjustment V31 negative polarity
												0	1	1	1	1	1	
101	0065											GM3P[5]	GM3P[4]	GM3P[3]	GM3P[2]	GM3P[1]	GM3P[0]	adjustment V61 positive polarity
												0	1	0	1	0	0	
102	0066											GM1N[5]	GM1N[4]	GM1N[3]	GM1N[2]	GM1N[1]	GM1N[0]	adjustment V61 negative polarity
												1	0	1	0	1	1	
103	0067											SOUT_MODE1	SOUT_MODE0					Source Hi-Z period setting/display data complement
												0	1					Source Hi-Z period setting {SOUT_MODE1,SOUT_MODE0} =
																		0,0: COM voltage output, 0,1: Hi-Z, 1,0: COM voltage & Hi-Z, 1,1: Hi-Z
															0			Test register (0 fixed)
																0		Test register (0 fixed)
																	0	Test register (0 fixed)
104	0068																	
:																		
111	006F																	
112	0070																BPSEL	Back porch count method switch
												1						Test register (1 fixed)
													0					Test register (0 fixed)
																	0	
113	0071													0		0	0	Test register (0 fixed)
114	0072															0	0	Test register (0 fixed)
115	0073														0	0	0	Test register (0 fixed)
117	0075																0	Test register (0 fixed)
118	0076									0	0	0	0	0	1	0	1	Test register
119	0077		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Test register (0 fixed)
121	0079				0	0	0	0	0	0	0	0	0	0	0	0	0	Test register (0 fixed)
123	007B																0	Test register (0 fixed)
126	007E									0	0	0	0	0	0	0	0	Test register (0 fixed)
127	007F															0	0	Test register (0 fixed)
:																		
192	00C0																0	Test register (0 fixed)
:																		
65535	FFFF																	

Register mode 3, 4

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Index		Data																Description
10 HEX.	16 HEX.	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
000	0000																OSCON	
																	0	Oscillator control (0: Oscillator stop, 1: Oscillator operation)
001	0001					SCN1	SCN0	R_L	ADX	ADY	ADC							
						0	0											Panel connection setting on gate signal
								0										Gate scan direction (0: O1 to O320, 1: O320 to O1)
									0									RAM X address direction inversion (0: Normal, 1: Inversion)
										0								RAM Y address direction inversion (0: Normal, 1: Inversion)
											0							RAM write control (X direction, both R and B are switchable) (0: Y1 to Y720, 1: Y720 to Y1)
												0						Test register (0 fixed)
002	0002						GSCAN[1]	GSCAN[0]								NLINE[1]	NLINE[0]	
							0	0										Interlace display
																		{GSCAN1,GSCAN0} = 0,0: n line inversion, 0,1: Frame inversion, 1,0: Skip 1D, 1,1: Skip 2B
																0	0	Line number of line inversion
																		{NLINE1,NLINE0} = 0,0: 1-line inversion, 0,1: 2-line inversion, 1,0: 4-line inversion, 1,1: 8-line inversion
003	0003				BGR				WAS			YDIR	XDIR	INC				
					0													RGB data inversion (R and B are swichable) (0: Normal, 1: Inversion)
									0									Window access control (0: Normal access, 1: Window access)
										0								Test register (0 fixed)
												0						Y address counter control (0: Increment, 1: Decrement)
													0					X address counter control (0: Increment, 1: Decrement)
														0				RAM address counter control (0: Count to X direction, 1: Count to Y direction)
004	0004																	
005	0005																	
006	0006																CRES	
																	0	Soft reset (occur reset pulse when write to "1")
007	0007											GOE2ON	GOE1ON	DISP1	DISP0	STBY_SOFF	STBY	
						1												Test register (1 fixed)
							0											Test register (0 fixed)
								1										Test register (1 fixed)
									0									Test register (0 fixed)
												0						Gate "H" fixed function (0: Normal operation, 1: Gate all "H")
													0					Gate "L" fixed function (0: Gate all "L", 1: Normal operation)
														1				Display data all 1 output (0: Normal, 1: All 1 fixed [6'h3F])
															0			Display data all 0 output (0: Normal, 1: All 0 fixed [6'h00])
																0		Stand-by fixed state control (0: As usual, 1: Source = Hi-Z, gate = all OFF, common = VSS)
																	0	Display OFF (0: Normal operation, 1: Display OFF)
008	0008																	
009	0009				PSEL		PGR	PGG	PGB	PNFRM			GSM		GSMLN[2]	GSMLN[1]	GSMLN[0]	
					0													Partial non-display area display setting (0: Specified color, 1: RAM data 8-color display)
							0											Partial non-display area [R] specified color setting (0:6'h00, 1:6'h3F)
								0										Partial non-display area [G] specified color setting (0:6'h00, 1:6'h3F)
									0									Partial non-display area [B] specified color setting (0:6'h00, 1:6'h3F)
										0								Polarity inversion on partial non-display area (0: Line inversion, 1: Frame inversion)
													0					Gate scan on partial non-display area (0: Normal operation, 1: Stop)
															0	0	0	Gate scan in partial mode
																		{GSMLN2,1,0} = 0,0,0,: Scan stop, 0,0,1: 3-frame cycle, 0,1,0: 5-frame cycle…
																		… 1,1,0: 13-frame cycle, 1,1,1: 15-frame cycle}
010	000A																	
011	000B																GS	
																	0	GS = 0: 260-k color (64-gray scale), GS = 1: 8 color (2-gray scale)
012	000C							NWRGB	RGBS			VIMD	DISPCK					
								0										RGB interface mode (0: RGB invalid, 1: RGB valid)
									0									RGB interface mode (0: Through mode, 1: Capture mode)
												0						VSYNC interface mode (0: OSC or RGB interface display, 1: VSYNC interface display)
													0					Display clock (0: OSC, 1: DOTCLK)
013	000D								LTS	BCNT[7]	BCNT[6]	BCNT[5]	BCNT[4]	BCNT[3]	BCNT[2]	BCNT[1]	BCNT[0]	
									0									Frame frequency 1/2 (= 1-line time x 2) (0: Normal, 1: 1/2)
										0	0	0	0	0	0	0	0	Basical clock for 1 line (BASECOUNT[7:0]) number specified
014	000E																OC	
																	0	Calibration start/stop (0: Stop, 1: Start)
015	000F	VBP[3]	VBP[2]	VBP[1]	VBP[0]	HBP[3]	HBP[2]	HBP[1]	HBP[0]	BPSEL			VSEG	HSEG			DCKEG	
		0	0	0	1													Vertical back porch period
						0	0	0	1									Horizontal back porch period
										0								Back porch count method switchable
											0							Test register (0 fixed)
													0					VSYNC active direction (0: L active, 1: H active)
														0				HSYNC active direction (0: L active, 1: H active)
																	0	DOTCLK active direction (0: Rising edge, 1: Falling edge)

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016	0010								RGBST[8]	RGBST[7]	RGBST[6]	RGBST[5]	RGBST[4]	RGBST[3]	RGBST[2]	RGBST[1]	RGBST[0]	
									0	0	0	0	0	0	0	0	0	RGB interface through mode display start line
017	0011								RGBED[8]	RGBED[7]	RGBED[6]	RGBED[5]	RGBED[4]	RGBED[3]	RGBED[2]	RGBED[1]	RGBED[0]	
									0	0	0	0	0	0	0	0	0	RGBinterface through mode display end line
018	0012									CAPXMIN[7]	CAPXMIN[6]	CAPXMIN[5]	CAPXMIN[4]	CAPXMIN[3]	CAPXMIN[2]	CAPXMIN[1]	CAPXMIN[0]	
										0	0	0	0	0	0	0	0	Minimum X address in RGB interface capture mode window access
019	0013									CAPXMAX[7]	CAPXMAX[6]	CAPXMAX[5]	CAPXMAX[4]	CAPXMAX[3]	CAPXMAX[2]	CAPXMAX[1]	CAPXMAX[0]	
										1	1	1	0	1	1	1	1	Maximum X address in RGB interface capture mode window access
020	0014								CAPYMIN[8]	CAPYMIN[7]	CAPYMIN[6]	CAPYMIN[5]	CAPYMIN[4]	CAPYMIN[3]	CAPYMIN[2]	CAPYMIN[1]	CAPYMIN[0]	
									0	0	0	0	0	0	0	0	0	Minimum Y address in RGB interface capture mode window access
021	0015								CAPYMAX[8]	CAPYMAX[7]	CAPYMAX[6]	CAPYMAX[5]	CAPYMAX[4]	CAPYMAX[3]	CAPYMAX[2]	CAPYMAX[1]	CAPYMAX[0]	
									1	0	0	1	1	1	1	1	1	Maximum Y address in RGB interface capture mode window access
022	0016																	
023	0017																	
024	0018	GOED[7]	GOED[6]	GOED[5]	GOED[4]	GOED[3]	GOED[2]	GOED[1]	GOED[0]	GOST[7]	GOST[6]	GOST[5]	GOST[4]	GOST[3]	GOST[2]	GOST[1]	GOST[0]	
		0	0	0	0	0	0	0	1									GOE1 falling position setting
										0	0	0	0	0	1	0	1	GOE1 rising position setting
025	0019									VMCHG[7]	VMCHG[6]	VMCHG[5]	VMCHG[4]	VMCHG[3]	VMCHG[2]	VMCHG[1]	VMCHG[0]	
										0	0	0	0	0	0	0	1	COM(VM) polarity switch position
026	001A	SWED[7]	SWED[6]	SWED[5]	SWED[4]	SWED[3]	SWED[2]	SWED[1]	SWED[0]	SWST[7]	SWST[6]	SWST[5]	SWST[4]	SWST[3]	SWST[2]	SWST[1]	SWST[0]	
		0	0	0	0	0	0	0	0									SWON falling edge position
										0	0	0	0	0	1	0	0	SWON rising edge position
027	001B																	
028	001C																	
029	001D																	
030	001E															SOUT_MODE[1]	SOUT_MODE[0]	
																0	1	Source Hi-Z period setting {SOUT_MODE1,SOUT_MODE0} =
																		0,0: COM voltage output, 0,1: Hi-Z, 1,0: COM voltage & Hi-Z, 1,1: Hi-Z
031	001F																	
:																		
067	0043																	
068	0044														E2OPC[2]	E2OPC[1]	E2OPC[0]	
															0	0	0	E2PROM operation start
069	0045									E2EN[7]	E2EN[6]	E2EN[5]	E2EN[4]	E2EN[3]	E2EN[2]	E2EN[1]	E2EN[0]	
										0	0	0	0	0	0	0	0	E2PROM write permission enable register
																		When making it E2OPC[2:0] =0,1,0, unless it sets this register to AAH,
																		signal is not outputted to E2PROM
070	0046									E2A[7]	E2A[6]	E2A[5]	E2A[4]	E2A[3]	E2A[2]	E2A[1]	E2A[0]	
										0	0	0	0	0	0	0	0	E2PROM write address specified
071	0047	E2IR[15]	E2IR[14]	E2IR[13]	E2IR[12]	E2IR[11]	E2IR[10]	E2IR[9]	E2IR[8]	E2IR[7]	E2IR[6]	E2IR[5]	E2IR[4]	E2IR[3]	E2IR[2]	E2IR[1]	E2IR[0]	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	E2PROM write index register specified
072	0048									E2ID[23]	E2ID[22]	E2ID[21]	E2ID[20]	E2ID[19]	E2ID[18]	E2ID[17]	E2ID[16]	
										0	0	0	0	0	0	0	0	Product information register [23:16]
073	0049									E2ID[15]	E2ID[14]	E2ID[13]	E2ID[12]	E2ID[11]	E2ID[10]	E2ID[9]	E2ID[8]	
										0	0	0	0	0	0	0	0	Product information register [15:8]
074	004A									E2ID[7]	E2ID[6]	E2ID[5]	E2ID[4]	E2ID[3]	E2ID[2]	E2ID[1]	E2ID[0]	
										0	0	0	0	0	0	0	0	Product information register [7:0]
075	004B									E2SA[7]	E2SA[6]	E2SA[5]	E2SA[4]	E2SA[3]	E2SA[2]	E2SA[1]	E2SA[0]	
										0	0	0	0	0	0	0	0	E2PROM read start address specified
076	004C																	
:																		
112	0070											1	0					Test register
113	0071													0		0	0	Test register (0 fixed)
114	0072															0	0	Test register (0 fixed)
115	0073														0	0	0	Test register (0 fixed)
118	0076									0	0	0	0	0	1	0	1	Test register
119	0077			0	0	0	0	0	0	0	0	0	0	0	0	0	0	Test register (0 fixed)
121	0079				0	0	0	0	0	0	0	0	0	0	0	0	0	Test register (0 fixed)
123	007B																0	Test register (0 fixed)
126	007E									0	0	0	0	0	0	0	0	Test register (0 fixed)
127	007F															0	0	Test register (0 fixed)
:																		
192	00C0																0	Test register (0 fixed)

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:																	
256	0100												LPM				Low power mode setting
													0				Low power mode (0: Normal mode, 1: Low power mode)
257	0101				VDCION	RGONR	RGON	VCLON	VGLREF	VGLON[1]	VGLON[0]	VGHREF	VGHON[1]	VGHON[0]	VD2ON[1]	VD2ON[0]	DCON	DC/DC operation setting
					0	0	0	0	0	0	0	0	0	0	0	0	0	
258	0102									VDCISEL	VDCHZ	VRHI	VSHI	DCFRM	DC3HZ	DC2HZ	DC1HZ	DC/DC output setting
										0	0	0	0	1	0	0	0	
259	0103									LFS[3]	LFS[2]	LFS[1]	LFS[0]	FS[3]	FS[2]	FS[1]	FS[0]	DC/DC frequency setting
										0	1	0	1	0	1	0	1	
260	0104											PONM	PON	DUPF[1]	DUPF[0]	PUPT[1]	PUPT[0]	DC/DC rising setting
												1	0	0	0	1	0	
261	0105				SFVSEL	VSEL[2]	VSEL[1]	VSEL[0]	VRSEL[2]	VRSEL[1]	VRSEL[0]	VSSEL[2]	VSSEL[1]	VSSEL[0]	VC[2]	VC[1]	VC[0]	Regulator voltage setting
					1	0	0	0	0	1	1	0	1	1	1	0	1	
262	0106								REGMON	LCDMCS[1]	LCDMCS[0]	COMCS[1]	COMCS[0]	LACS[1]	LACS[0]	ACS[1]	ACS[0]	Regulator current setting
									0	0	0	0	0	0	0	1	0	
263	0107											COMP[1]	COMP[0]		COMHM		COMONM	VCOM output setting
												0	0		0		0	
264	0108											DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	VCOM amplitude setting
												0	0	0	0	0	0	
265	0109									COMINM	CDA[6]	CDA[5]	CDA[4]	CDA[3]	CDA[2]	CDA[1]	CDA[0]	VCOMM cencter setting
										0	0	0	0	0	0	0	0	
266	010A																	
:																		
512	0200									XA[7]	XA[6]	XA[5]	XA[4]	XA[3]	XA[2]	XA[1]	XA[0]	RAM X address
										0	0	0	0	0	0	0	0	
513	0201								YA[8]	YA[7]	YA[6]	YA[5]	YA[4]	YA[3]	YA[2]	YA[1]	YA[0]	RAM Y address
									0	0	0	0	0	0	0	0	0	
514	0202																	RAM write index
515	0203			WM[11]	WM[10]	WM[9]	WM[8]	WM[7]	WM[6]			WM[5]	WM[4]	WM[3]	WM[2]	WM[1]	WM[0]	RAM write mask
				0	0	0	0	0	0			0	0	0	0	0	0	
516	0204											WM[17]	WM[16]	WM[15]	WM[14]	WM[13]	WM[12]	RAM write mask
												0	0	0	0	0	0	
517	0205														0	0	0	Test register
:																		
527	020F																	
528	0210									XMN[7]	XMN[6]	XMN[5]	XMN[4]	XMN[3]	XMN[2]	XMN[1]	XMN[0]	Minimum X address in RGB interface capture mode window access
										0	0	0	0	0	0	0	0	
529	0211									XMX[7]	XMX[6]	XMX[5]	XMX[4]	XMX[3]	XMX[2]	XMX[1]	XMX[0]	Maximum X address in RGB interface capture mode window access
										1	1	1	0	1	1	1	1	
530	0212								YMN[8]	YMN[7]	YMN[6]	YMN[5]	YMN[4]	YMN[3]	YMN[2]	YMN[1]	YMN[0]	Minimum Y address in RGB interface capture mode window access
									0	0	0	0	0	0	0	0	0	
531	0213								YMX[8]	YMX[7]	YMX[6]	YMX[5]	YMX[4]	YMX[3]	YMX[2]	YMX[1]	YMX[0]	Maximum Y address in RGB interface capture mode window access
									1	0	0	1	1	1	1	1	1	
532	0214																	
:																		
535	0217																	
536	0218									LCDMN[7]	LCDMN[6]	LCDMN[5]	LCDMN[4]	LCDMN[3]	LCDMN[2]	LCDMN[1]	LCDMN[0]	[LCDSIZE] X MIN. size set
										0	0	0	0	0	0	0	0	
537	0219									LCDMX[7]	LCDMX[6]	LCDMX[5]	LCDMX[4]	LCDMX[3]	LCDMX[2]	LCDMX[1]	LCDMX[0]	[LCDSIZE] X MAX. size set
										1	1	1	0	1	1	1	1	
538	021A								LCDYMN[8]	LCDYMN[7]	LCDYMN[6]	LCDYMN[5]	LCDYMN[4]	LCDYMN[3]	LCDYMN[2]	LCDYMN[1]	LCDYMN[0]	[LCDSIZE] Y MIN. size set
									0	0	0	0	0	0	0	0	0	
539	021B								LCDYMX[8]	LCDYMX[7]	LCDYMX[6]	LCDYMX[5]	LCDYMX[4]	LCDYMX[3]	LCDYMX[2]	LCDYMX[1]	LCDYMX[0]	[LCDSIZE] Y MAX. size set
									1	0	0	1	1	1	1	1	1	
540	021C																	

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:																		
768	0300			GM3P[5]	GM3P[4]	GM3P[3]	GM3P[2]	GM3P[1]	GM3P[0]			GM1P[5]	GM1P[4]	GM1P[3]	GM1P[2]	GM1P[1]	GM1P[0]	
				0	1	0	1	0	0									adjustment V61 positive polarity
												1	0	1	0	1	1	adjustment V10 positive polarity
769	0301																	
770	0302																	
771	0303											GM2P[5]	GM2P[4]	GM2P[3]	GM2P[2]	GM2P[1]	GM2P[0]	
												0	1	1	1	1	1	adjustment V34 positive polarity
772	0304		GPL[6]	GPL[5]	GPL[4]	GPL[3]	GPL[2]	GPL[1]	GPL[0]		GPH[6]	GPH[5]	GPH[4]	GPH[3]	GPH[2]	GPH[1]	GPH[0]	
			0	0	0	0	0	0	0									amplitude setting
											1	1	1	1	1	1	1	amplitude setting
773	0305			GM3N[5]	GM3N[4]	GM3N[3]	GM3N[2]	GM3N[1]	GM3N[0]			GM1N[5]	GM1N[4]	GM1N[3]	GM1N[2]	GM1N[1]	GM1N[0]	
				0	1	0	1	0	0									adjustment V9 negative polarity
												1	0	1	0	1	1	adjustment V61 negative polarity
774	0306																	
775	0307																	
776	0308											GM2N[5]	GM2N[4]	GM2N[3]	GM2N[2]	GM2N[1]	GM2N[0]	
												0	1	1	1	1	1	adjustment V31 negative polarity
777	0309		GNL[6]	GNL[5]	GNL[4]	GNL[3]	GNL[2]	GNL[1]	GNL[0]		GNH[6]	GNH[5]	GNH[4]	GNH[3]	GNH[2]	GNH[1]	GNH[0]	
			0	0	0	0	0	0	0									amplitude setting
											1	1	1	1	1	1	1	amplitude setting
778	030A																	
779	030B																	
780	030C						GI[2]	GI[1]	GI[0]		GAP[2]	GAP[1]	GAP[0]		GAN[2]	GAN[1]	GAN[0]	
							0	0	1									amplifier bias current （set up for magnification, using a default state as 1)
																		{GI2,1,0} = 0,0,0: 0.5 time, 0,0,1: 1 time, 0,1,0: 1.5 time, 0,1,1: 2 time
																		1,0,0: 2.5 time, 1,0,1: 3 time, 1,1,0: 3.5 time, 1,1,1: 4 time
											0	0	1					Gray scale amp. 0 to 31-gray scale bias current control （set up for maginfication, using a default state as 1)
																		{GAP2 to 0} = 0,0,0: 0.5 time, 0,0,1: 1 time, 0,1,0: 1.5 time, 0,1,1: 2 time
																		1,0,0: 3 time, 1,0,1: 4 time, 1,1,0: 6 time, 1,1,1: 7.5 time
															0	0	1	Gray scale amp. 32 to 63-gray scale bias current control (set up for magnification, using a default state as 1)
																		{GAP2 to 0} = 0,0,0: 0.5 time, 0,0,1: 1 time, 0,1,0: 1.5 time, 0,1,1: 2 time
																		1,0,0: 3 time, 1,0,1: 4 time, 1,1,0: 6 time, 1,1,1: 7.5 time
781	030D												GRES			G3SW		
													0					resistance switch
																0		middle amplifier (0: OFF, 1: ON)
782	030E																	
:																		
1024	0400																DTY	
																	0	Partial display (0: Normal display, 1: Partial display)
1025	0401																DINV	
																	0	RAM write, read data inversion (0: Normal, 1: Data inversion)
1026	0402							P1SL[8]	P1SL[7]	P1SL[6]	P1SL[5]	P1SL[4]	P1SL[3]	P1SL[2]	P1SL[1]	P1SL[0]		
								0	0	0	0	0	0	0	0	0		Partial 1 display area start line
1027	0403							P1AW[8]	P1AW[7]	P1AW[6]	P1AW[5]	P1AW[4]	P1AW[3]	P1AW[2]	P1AW[1]	P1AW[0]		
								0	0	0	0	0	0	0	0	0		Partial 1 display area line number
1028	0404							P1SA[8]	P1SA[7]	P1SA[6]	P1SA[5]	P1SA[4]	P1SA[3]	P1SA[2]	P1SA[1]	P1SA[0]		
								0	0	0	0	0	0	0	0	0		Partial 1 display area start line display RAM address
1029	0405							P2SL[8]	P2SL[7]	P2SL[6]	P2SL[5]	P2SL[4]	P2SL[3]	P2SL[2]	P2SL[1]	P2SL[0]		
								0	0	0	0	0	0	0	0	0		Partial 2 display area start line
1030	0406							P2AW[8]	P2AW[7]	P2AW[6]	P2AW[5]	P2AW[4]	P2AW[3]	P2AW[2]	P2AW[1]	P2AW[0]		
								0	0	0	0	0	0	0	0	0		Partial 2 display area line number
1031	0407							P2SA[8]	P2SA[7]	P2SA[6]	P2SA[5]	P2SA[4]	P2SA[3]	P2SA[2]	P2SA[1]	P2SA[0]		
								0	0	0	0	0	0	0	0	0		Partial 2 display area start line display RAM address
1032	0408																	
:																		
65535	FFFF																	

11.2 Command Description

- **Register mode 1/register mode 2**

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Register	Bit	Symbol	Function
R0	D7	DISP1	This command performs the same output as when all data is 1, independently of the internal RAM data (white display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 1. DISP1 takes precedence over DISP0. When DISP1 = 1, DISP0 = 1 is ignored.
	D6	DISP0	This command performs the same output as when all data is 0, independently of the internal RAM data (black display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 0.
	D5	ADC	The direction of column address The direction of source driver output can be selected.
	D4	DTY	Partial function is selected. In addition, efficiency of this command is carried out after transmission from the timing which outputs the following line data. 0: Normal display mode 1: Partial display mode
	D3	STBY	This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed, the amplifiers, and oscillator at each output circuit are stopped. After executing the stand-by function using this bit, set the regulator for gate power supply IC to OFF and set the DC/DC converter to OFF. For the sequence, refer to the preliminary product information of the power supply IC etc. Note that when releasing stand-by, perform the opposite operation, after setting the DC/DC converter to ON and setting the regulators of the gate IC and power supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (Display read OFF from RAM stop, VCOM stop, display OFF = all data output as 1)
	D2	STBY_GOFF	This bit selects the gate level, source level, and VCOM level at the time of stand-by. 0: Gate level (V_{GH}), source level (V_{SS}), VCOM level (COML) 1: Gate level (V_{GL}), source level (Hi-Z), VCOM level (V_{SS})
	D1	LPM	This bit is used in case it sets to the low power mode. 0: Normal mode 1: Low power mode
	D0	GSM	Sets output of the gate scanning signal during partial display. If this bit is set to 1, the gate of the lines set in the partial non-display area is scanned every frame period set by the R52 register. 0: Normal mode 1: The gate scanning cycle of partial non-display area is determined with the setting value to R52 register.

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="4">R1</td><td>D7</td><td>ADX</td><td>Addressing of X address is inverted. For more details, refer to Figure 5–36.</td></tr>
<tr><td>D6</td><td>ADY</td><td>Addressing of Y address is inverted. For more details, refer to Figure 5–36.</td></tr>
<tr><td>D4</td><td>BGR</td><td>The order of RGB data is changed at the time of writing (The data of R and B is replaced).
0: Normal operation
<18 bits bus width: 1 pixel = 18 bits>
<table><tr><td>Date bus</td><td>D17 to D12</td><td>D11 to D6</td><td>D5 to D0</td></tr><tr><td>RAM</td><td>RAM • D17 to RAM • D12</td><td>RAM • D11 to RAM • D6</td><td>RAM • D5 to RAM • D0</td></tr></table>
<16 bits bus width: 1 pixel = 16 bits>
<table><tr><td>Data bus</td><td>D15 to D11</td><td>D10 to D5</td><td>D4 to D0</td></tr><tr><td>RAM</td><td>RAM • D17 to RAM • D13
(D12: Supplemental transaction)</td><td>RAM • D11 to RAM • D6</td><td>RAM • D5 to RAM • D1
(D0: Supplemental transaction)</td></tr></table>
1: Write in by replacing R and B data.
<18 bits bus width: 1 pixel = 18 bits>
<table><tr><td>Data bus</td><td>D17 to D12</td><td>D11 to D6</td><td>D5 to D0</td></tr><tr><td>RAM</td><td>RAM • D5 to RAM • D0</td><td>RAM • D11 to RAM • D6</td><td>RAM • D17 to RAM • D12</td></tr></table>
<16 bits bus width: 1 pixel = 16 bits>
<table><tr><td>Data bus</td><td>D15 to D11</td><td>D10 to D5</td><td>D4 to D0</td></tr><tr><td>RAM</td><td>RAM • D5 to RAM • D1
(D0: Supplemental transaction)</td><td>RAM • D11 to RAM • D6</td><td>RAM • D17 to RAM • D13
(D12: Supplemental transaction)</td></tr></table></td></tr>
<tr><td>D1</td><td>LTS</td><td>The setting time of calibration is selected.
The calibration function adjusts frame frequency by setting up the time of one line. The setting time of one line can be selected from the following setup by this command.
0: 1 line time = t_{cal}
1: 1 line time = t_{cal} x 2
(t_{cal}: calibration setting time = 1 ÷ frame frequency ÷ display line number)</td></tr>
</table>

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<R>

Register	Bit	Symbol	Function
R2	D6	DCKEG	The active level of DOTCLK is selected. 0: Data latch by rising edge 1: Data latch by falling edge
	D5	VSEG	The active level of VSYNC is selected. 0: Low active 1: High active
	D4	HSEG	The active level of HSYNC is selected. 0: Low active 1: High active
	D3	VIMD	VSYNC interface mode is selected. If VSYNC is inputted when VSYNC interface mode is selected, scan for one frame will be performed. 0: Normal mode 1: VSYNC interface mode
	D2	NWRGB	The input of RGB interface becomes invalid. 0: The input of RGB interface becomes invalid. 1: The input of RGB interface becomes valid.
	D1	RGBS	The mode of RGB interface is selected. 0: Through mode 1: Capture mode
	D0	DISPCK	The timing clock for display output at the time of RGB interface is selected. 0: Internal oscillation clock 1: HSYNC/VSYNC/DOTCLK
R3	D0	CRES	This bit is command reset function. Be sure to perform after power supply injection. Command reset clears this bit automatically after execution (CRES = 1). Therefore, there is no necessity (normal operation is selected) of setting up 0 more nearly again soft. Moreover, after command reset execution, since this bit of time to change to 1 → 0 is very short, by the time it sets up the following command, it is not necessary to vacate time after command reset setup. 0: Normal operation 1: Command reset

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Register	Bit	Symbol	Function
R4	D0	GS	This bit selects color numbers. GS = 0: 262,144-color GS = 1: 8-color
R5	D4	WAS	Window access mode setting When the window access mode is set, the address is increment/decrement only in the range set by the MIN. ·X address setting register (R8), MAX. ·X address setting register (R9), MIN. ·Y address setting register (R10), and MAX. ·Y address setting register (R11). 0: Normal operation 1: Window access mode
	D3	DINV	RAM write date inversion 0: Normal mode 1: Inversion mode
	D2	INC	This bit selects the direction in which the address is to be increment. 0: Increments X address 1: Increments Y address
R6	D7 to D0	XAn	This register sets the X address of the display RAM. Set 00H to EFH.
R7	D8 to D0	YAn	This register sets the Y address of the display RAM. Set 000H to 13FH.
R8	D7 to D0	XMINn	The minimum value of X address at the time of window access mode is set up. After carrying out the increment of the X address to X address maximum set up by the MAX. X address register (R9), they are the next increments and are initialized by the address value set up by this command. Set up 00H to EFH.
R9	D7 to D0	XMXn	The maximum of X address at the time of window access mode is set up. After carrying out the increment of the X address to the address value set up by this command, they are the next increments and are initialized by X address minimum value set up by the MIN. X address register (R8). Set up 00H to EFH.
R10	D8 to D0	YMINn	The minimum value of Y address at the time of window access mode is set up. After carrying out the increment of the Y address to Y address maximum set up by the MAX. Y address register (R11), they are the next increments and are initialized by the address value set up by this command. Set up to 000H to 13FH.
R11	D8 to D0	YMXn	The maximum of Y address at the time of window access mode is set up. After carrying out the increment of the Y address to the address value set up by this command, it is the next increment and is initialized by Y address minimum value set up by the MIN. Y address register (R10). Set up to 000H to 13FH.

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Register	Bit	Symbol	Function
R16	D0	PSEL	Partial OFF area color register 1 Selects whether the data specified in R17 register as color data, using MSB of a display data RAM is used as color data. 0: Use the data specified to be R17 register 1: Use MSB of display data RAM, making it into color data.
R17	D2, D1, D0	PGR, PGG, PGB	Partial OFF area color register 2 Sets the color of the screen other than the partial display area during partial display (R0: DTY = 1). One of eight colors can be selected (RGB: 1 bit each) as the OFF color. The relationship between each color data and the bits of this register is as follows. This relationship is not dependent upon the value of ADC. PGR: R OFF = 0, ON = 1 PGG: G OFF = 0, ON = 1 PGB: B OFF = 0, ON = 1
R18	D8 to D0	P1SLn	This is partial 1 display area start line register (000H to 13FH). From the line set up by this command to the line set up by the partial 1 display area end line register (R20) becomes partial 1 display area at the time of partial display (R0: DTY = 1).
R19	D8 to D0	P2SLn	This is partial 2 display area start line register (000H to 13FH). From the line set up by this command to the line set up by the partial 2 display area end line register (R21) becomes partial 2 display area at the time of partial display (R0: DTY = 1).
R20	D8 to D0	P1AWn	This is partial 1 display area line count register (000H to 13FH). An area starting from the line set by the partial 1 display area start register (R18) and ending as set by this command is the partial 1 display area. If this register is 0, the values of the partial 2 display area start line register (R19) and the partial 2 display area line count register (R21) are not valid.
R21	D8 to D0	P2AWn	This is partial 2 display area line count register (000H to 13FH) An area starting from the line set by the partial 2 display area start register (R19) and ending as set by this command is the partial 2 display area. If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R19) and partial 2 display area line count register (R21) are not valid.
R22	D8 to D0	P1SAn	This is partial 1 display area start line display RAM address.
R23	D8 to D0	P2SAn	This is partial 2 display area start line display RAM address.

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Register	Bit	Symbol	Function
R24	D12	VDCION	ON/OFF of V_{DCI} regulator is controlled. 0: V_{DCI} regulator OFF 1: V_{DCI} regulator ON
	D11	RGONR	ON/OFF of V_R regulator is controlled. 0: V_R regulator OFF 1: V_R regulator ON
	D10	RGON	ON/OFF of V_S regulator is controlled. 0: V_S regulator OFF 1: V_S regulator ON
	D9	VCLON	ON/OFF of V_{CL} boost is controlled. 0: V_{CL} boost OFF 1: V_{CL} boost ON (V_{DCI} x –1)
	D8	VGLREF	V_{GL} boost mode is switched 0: $V_{GL} = V_R$ x (–2 or –3) + V_{SS} 1: $V_{GL} = V_R$ x (–2 or –3) + V_{CL}
	D7, D6	VGLON1 VGLON0	ON/OFF of V_{GL} boost is controlled. <VGLON1, VGLON0 = 0, 0> V_{GL} boost OFF <VGLON1, VGLON0 = 0, 1> $V_{GL} = V_R$ x –2 + (V_{SS} or V_{CL}) <VGLON1, VGLON0 = 1, X> $V_{GL} = V_R$ x –3 + (V_{SS} or V_{CL})
	D5	VGHREF	V_{GH} boost mode is switched. 0: $V_{GH} = V_R$ x (2 or 3) + V_R 1: $V_{GH} = V_R$ x (2 or 3) + V_{DCI}
	D4, D3	VGHON1 VGHON0	ON/OFF of V_{GH} boost is controlled. <VGHON1, VGHON0 = 0, 0> V_{GH} boost OFF <VGHON1, VGHON0 = 0, 1> $V_{GH} = V_R$ x 2 + (V_R or V_{DCI}) <VGHON1, VGHON0 = 1, X> $V_{GH} = V_R$ x 3 + (V_R or V_{DCI})
	D2, D1	VD2ON1 VD2ON0	ON/OFF of V_{DD2} boost is controlled. <VD2ON1, VD2ON0 = 0, 0> V_{DD2} boost OFF (V_{DCI} or Hi-Z) <VD2ON1, VD2ON0 = 0, 1> $V_{DD2} = V_{DCI}$ x 2 boost ON <VD2ON1, VD2ON0 = 1, X> $V_{DD2} = V_{DCI}$ x 3 boost ON
	D0	DCON	ON/OFF of DC/DC converter is controlled. 0: DC/DC converter OFF 1: DC/DC converter ON

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<R>

Register	Bit	Symbol	Function
R25	D7	VDCISEL	When V_{DCI} regulator OFF (VDCION [R24] = 0) and V_{DCI} output is not set into Hi-Z (VDCIHZ [R25] = 0), the output state of V_{DCI} regulator is controlled. <VDCISEL = 0> $V_{DCI} = V_{DC}$ <VDCISEL = 1> $V_{DCI} = V_{SS}$
	D6	VDCIHZ	Output state of V_{DCI} pin is defined when V_{DCI} regulator is OFF (VDCION [R24] = 0). <VDCIHZ = 0> $V_{DCI} = V_{DC}$ or V_{SS} (setting by VDCISEL) <VDCIHZ = 1> V_{DCI} =Hi-Z
	D5	VRHI	Output of V_R regulator is selected. <VRHI = 0> V_R regulator = ON <VRHI = 1> V_R regulator = Hi-Z
	D4	VSHI	Output of V_S regulator is selected. <VSHI = 0> V_S regulator = ON <VSHI = 1> V_S regulator = Hi-Z
	D3	DCFRM	This bit selects whether DC/DC operation is synchronized with frame signal. <DCFRM = 0> DC/DC operation = frame asynchronous <DCFRM = 1> DC/DC operation = frame synchronization
	D2	DC3HZ	The output state of V_{CL} at the time of V_{CL} boost OFF is controlled. <DC3HZ = 0> $V_{CL} = V_{SS}$ <DC3HZ = 1> V_{CL} = Hi-Z
	D1	DC2HZ	The output state of V_{GH} and V_{GL} at the time of V_{GH} and V_{GL} boost OFF is controlled. <DC2HZ = 0> $V_{GH} = V_{DD2}$, $V_{GL} = V_{SS}$ <DC2HZ = 1> V_{GH} = Hi-Z, V_{GL} = Hi-Z
	D0	DC1HZ	The output state of V_{DD2} at the time of V_{DD2} boost OFF is controlled. <DC1HZ = 0> $V_{DD2} = V_{DCI}$ <DC1HZ = 1> V_{DD2} = Hi-Z

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Register	Bit	Symbol	Function		
R26	D7, D6	LFS3, LFS2	When low power mode (LPM [R0] = 1), V_{GH}, V_{GL} boost frequency are selected.		
			LFS3	LFS2	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D5, D4	LFS1, LFS0	When low power mode (LPM [R0] = 1), V_{DD2}, V_{CL} boost frequency are selected.		
			LFS1	LFS0	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D3, D2	FS3, FS2	When normal drive (LPM [R0] = 0), V_{GH}, V_{GL} boost frequency are selected.		
			FS3	FS2	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D1, D0	FS1, FS0	When normal drive (LPM [R0] = 0), V_{DD2}, V_{CL} boost frequency are selected.		
			FS1	FS0	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
R27	D5	PONM	The internal sequence of DC/DC rising operation and an external sequence are selected. 0: External sequence 1: Internal sequence		
	D4	PON	The frequency of operation at the time of the rising of V_{GH}, V_{DD2}, V_{GL} and V_{CL} when DC/DC rising is selected. It becomes valid only at the time of PONM = 0. 0: Normal operation 1: Rising operation		
	D3, D2	DUPF1, DUPF0	The frequency of operation of whole DC/DC converter circuit when DC/DC rising is selected.		
			DUPF1	DUPF0	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D1, D0	PUPT1, PUPT0	The ON time at the time of the rising of V_{GH}, V_{DD2}, V_{GL}, V_{CL} RGON, RGONR when DC/DC rising is selected. It becomes valid only at the time of PONM = 1.		

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Register	Bit	Symbol	Function
R28	D12	SFVSEL	Output voltage of RV_{DD} regulator is selected. <SFVSEL = 0> RV_{DD} = 2.1 V (for test) <SFVSEL = 1> RV_{DD} = 2.3 V
	D11 to D9	VSEL2 to VSEL0	Output voltage of V_{GM} regulator is selected. <VC2 = 1, VC1 = 0, VC0 = 1> At V_{REFR} = 2.0 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.40 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.50 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.60 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.70 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.80 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.90 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 5.00 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 5.10 V
	D8 to D6	VRSEL2 to VRSEL0	Output voltage of V_R regulator is selected. <VC2 = 1, VC1 =0, VC0 = 1> At V_{REFR} = 2.0 V <VRSEL2 = 0, VRSEL1 = 0, VRSEL0 = 0> V_R = 4.50 V <VRSEL2 = 0, VRSEL1 = 0, VRSEL0 = 1> V_R = 4.80 V <VRSEL2 = 0, VRSEL1 = 1, VRSEL0 = 0> V_R = 4.90 V <VRSEL2 = 0, VRSEL1 = 1, VRSEL0 = 1> V_R = 5.00 V <VRSEL2 = 1, VRSEL1 = 0, VRSEL0 = 0> V_R = 5.05 V <VRSEL2 = 1, VRSEL1 = 0, VRSEL0 = 1> V_R = 5.10 V <VRSEL2 = 1, VRSEL1 = 1, VRSEL0 = 0> V_R = 5.20 V <VRSEL2 = 1, VRSEL1 = 1, VRSEL0 = 1> V_R = 5.40 V
	D5 to D3	VSSEL2 to VSSEL0	Output voltage of V_S regulator is selected. <VC2 = 1, VC1 =0, VC0 = 1> At V_{REFR} = 2.0 V <VSSEL2 = 0, VSSEL1 = 0, VSSEL0 = 0> V_S = 4.85 V <VSSEL2 = 0, VSSEL1 = 0, VSSEL0 = 1> V_S = 4.90 V <VSSEL2 = 0, VSSEL1 = 1, VSSEL0 = 0> V_S = 4.95 V <VSSEL2 = 0, VSSEL1 = 1, VSSEL0 = 1> V_S = 5.00 V <VSSEL2 = 1, VSSEL1 = 0, VSSEL0 = 0> V_S = 5.05 V <VSSEL2 = 1, VSSEL1 = 0, VSSEL0 = 1> V_S = 5.10 V <VSSEL2 = 1, VSSEL1 = 1, VSSEL0 = 0> V_S = 5.15 V <VSSEL2 = 1, VSSEL1 = 1, VSSEL0 = 1> V_S = 5.20 V
	D2 to D0	VC2 to VC0	Output voltage of REFR regulator is selected. <VC2 = 0, VC1 = 0, VC0 = 0> V_{REFR} = 1.50 V <VC2 = 0, VC1 = 0, VC0 = 1> V_{REFR} = 1.60 V <VC2 = 0, VC1 = 1, VC0 = 0> V_{REFR} = 1.70 V <VC2 = 0, VC1 = 1, VC0 = 1> V_{REFR} = 1.80 V <VC2 = 1, VC1 = 0, VC0 = 0> V_{REFR} = 1.90 V <VC2 = 1, VC1 = 0, VC0 = 1> V_{REFR} = 2.00 V <VC2 = 1, VC1 = 1, VC0 = 0> V_{REFR} = 2.05 V <VC2 = 1, VC1 = 1, VC0 = 1> V_{REFR} = 2.10 V

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Register	Bit	Symbol	Function
R29	D8	REGMONI	Output state of TVREFR is selected. 0: TVREFR = Hi-Z 1: TVREFR = Output setup voltage in VC2 to VC0
	D7, D6	LCOMCS1 LCOMCS0	When low power mode, COMH/COML amplitude current is selected. <LCOMCS1, LCOMCS0 = 0, 0> Amp. current = x 0.25 mode <LCOMCS1, LCOMCS0 = 0, 1> Amp. current = x 0.5 mode <LCOMCS1, LCOMCS0 = 1, 0> Amp. current = x 1.0 mode <LCOMCS1, LCOMCS0 = 1, 1> Amp. current = x 1.5 mode
	D5, D4	COMCS1, COMCS0	COMH/COML amplitude current is selected. <COMCS1, COMCS0 = 0, 0> Amp. current = x 1 mode <COMCS1, COMCS0 = 0, 1> Amp. current = x 2 mode <COMCS1, COMCS0 = 1, 0> Amp. current = x 3 mode <COMCS1, COMCS0 = 1, 1> Amp. current = x 7 mode
	D3, D2	LACS1, LACS0	When low power mode (LPM [R0] = 1), V_R and V_S regulator amplitude current is selected. <LACS1, LACS0 = 0, 0> Amp. current = x 0.25 mode <LACS1, LACS0 = 0, 1> Amp. current = x 0.5 mode <LACS1, LACS0 = 1, 0> Amp. current = x 1.0 mode <LACS1, LACS0 = 1, 1> Amp. current = x 1.5 mode
	D1 D0	ACS1, ACS0	When normal drive (LPM [R0] = 0), V_R and V_S regulator amplitude current is selected. <ACS1, ACS0 = 0, 0> Amp. current = x 1 mode <ACS1, ACS0 = 0, 1> Amp. current = x 2 mode <ACS1, ACS0 = 1, 0> Amp. current = x 3 mode <ACS1, ACS0 = 1, 1> Amp. current = x 6 mode

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Register	Bit	Symbol	Function
R30	D5, D4	COMP1, COMP0	VCOMM ability at VCOMM output is selected. <COMP1, COMP0 = 0, 0> x 1 mode <COMP1, COMP0 = 0, 1> x 1.5 mode <COMP1, COMP0 = 1, 0> x 2 mode <COMP1, COMP0 = 1, 1> x 2.5 mode
	D2	COMHIM	Output state of VCOMM is controlled. 0: VCOMHM/VCOMLM 1: Hi-Z
	D0	COMONM	ON/OFF control of the common drive output VCOMM is carried out. 0: OFF (VCOMHM and VCOMLM amplifier-OFF) 1: ON (VCOMHM and VCOMLM amplifier-ON)
R31	D5 to D0	DAn	The amplitude of VCOMM output is controlled by 6-bit D/A.
R32	D7	COMINM	The center voltage input of VCOMM is selected. 0: Internal D/A becomes valid 1: Center level voltage of VCOMINM input becomes valid
	D6 to D0	CDAn	The center level of VCOMM output is controlled by 7-bit D/A.
R36	D6 to D0	GPHn	Sets the positive polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
R37	D6 to D0	GNHn	Sets the negative polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
R38	D6 to D0	GPLn	Sets the positive polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
R39	D6 to D0	GNLn	Sets the negative polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
R41	D7 to D0	LCDXMINn	The minimum value of X addresses of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the X addresses to X address maximum set up by the LCDMAX X address register (R43), they are the next increments and are initialized by the address value set up by this command. In addition, the source output pin which is not specified by LCDXMIN (R41) and LCDXMX (R43) does not output. Set up 00H to EFH. Moreover, specify a surely bigger area than the window area in window access mode.
R42	D8 to D0	LCDYMINn	The minimum value of Y address of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the Y address to Y address maximum set up by the LCDMAX Y address register (R44), it is the next increment and is initialized by the address value set up by this command. Set up 000H to 13FH. Moreover, specify a surely bigger area than the window area in window access mode.
R43	D7 to D0	LCDXMXn	The maximum of X addresses of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the X addresses to the address value set up by this command, they are the next increments and are initialized by X address minimum value set up by the LCDMIN X address register (R41). In addition, the source output pin which is not specified by LCDXMIN (R41) and LCDXMX (R43) does not output. Set up 00H to EFH. Moreover, specify a surely bigger area than the window area in window access mode.

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Register	Bit	Symbol	Function
R44	D8 to D0	LCDYMXn	The maximum of Y address of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the Y address to the address value set up by this command, it is the next increment and is initialized by Y address minimum value set up by the LCDMIN Y address register (R42). Set up 000H to 13FH. Moreover, specify a surely bigger area than the window area in window access mode.
R45	D0	OC	This bit is used for calibration. The time from calibration start command execution until calibration stop command execution becomes the time for 1 line. 0: Calibration stop 1: Calibration start
R46	D7 to D0	BCNTn	It specifies a part for what clock of a basic clock (an internal oscillation clock or DOTCLK) 1 horizontal period becomes. Moreover, 1 horizontal period determined by the calibration function is able to get to know a part for what clock of a basic clock it is by reading and adding this register.
R50	D2	R_L	Scan direction of gate driver is selected. 0: Scan to G320 from G0 1: Scan to G0 from G320
	D1	SCN1	Gate scan mode is selected. {SCN1, SCN0} = 0, 0: MODE1 0, 1: MODE2 1, 0: MODE3 1, 1: Setting prohibited
	D0	SCN0	
R51	D1, D0	NLINE1, NLINE0	The number of lines of n line inversion is set up.

NLINE1	NLINE0	Number of Lines of n Line Inversion
0	0	n = 1
0	1	n = 2
1	0	n = 4
1	1	n = 8

R52	D2, D1, D0	GSMLN2, GSMLN1, GSMLN0	Gate scan operation of partial non-displaying area is selected. GSMLN2 to GSMLIN0 = 0, 0, 0: Gate scan stop GSMLN2 to GSMLIN0 = 0, 0, 1: 3 frame cycle GSMLN2 to GSMLIN0 = 0, 1, 0: 5 frame cycle : GSMLN2 to GSMLIN0 = 1, 1, 0: 13 frame cycle GSMLN2 to GSMLIN0 = 1, 1, 1: 15 frame cycle
R53	D0	PNFRM	Only partial non-displaying area carries out frame inversion operation. This bit becomes valid only when a partial display area is line inversion. 0: Partial non-displaying area is line inversion. 1: Partial non-displaying area is frame inversion.
R55	D1, D0	GSCAN1, GSCAN0	Skip inversion mode is selected.

GSCAN1	GSCAN0	Scan Operation
0	0	n line inversion
0	1	Frame inversion
1	0	Skip inversion 1D
1	1	Skip inversion 2B

R58	D0	OSCON	Internal oscillator is controlled. 0: Oscillator stop 1: Oscillator operate

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Register	Bit	Symbol	Function
R59	D1	GOE2ON	GOE2 output is controlled. 0: Normal operation 1: GOE2 output Low fixation (All gate ON).
	D0	GOE1ON	Gate scan ON/OFF is selected by GOE1 output. 0: Gate scan OFF (GOE1 = Low fixation) 1: Normal operation
R60	D8 to D0	RGBSTn	These bits set the start line of the display area to be displayed by in RGB interface through mode. (000H ≤ R60 ≤ 13FH) Be sure to observe the relationship “Set value of R60 register < Set value of R61 register“.
R61	D8 to D0	RGBEDn	These bits set the end line of the display area to be displayed by in RGB interface through mode. (000H ≤ R61 ≤ 13FH) Be sure to observe the relationship “Set value of R60 register < Set value of R61 register“.
<R> R62	D7 to D4	HBPn	These bits set the horizontal back porch period of the RGB interface. 18/16-bit mode: Horizontal back porch period = This register setting value x DOTCLK unit 6-bit mode: Horizontal back porch period = This register setting value x 3 x DOTCLK unit
	D3 to D0	VBPn	These bits set the vertical back porch period of the RGB interface. Vertical back porch period = This register setting value x HSYNC unit.
R63	D7 to D0	CAPXMINn	The minimum value of X addresses of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the X addresses to X address maximum set up by the MAX X address register (R64), they are the next increments and are initialized by the address value set up by this command. Set up 00H to EFH.
R64	D7 to D0	CAPXMXn	The maximum of X addresses of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the X addresses to the address value set up by this command, they are the next increments and are initialized by X address minimum value set up by the MIN X address register (R63). Set up 00H to EFH.
R65	D8 to D0	CAPYMINn	The minimum value of Y address of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the Y address to Y address maximum set up by the MAX Y address register (R66), it is the next increment and is initialized by the address value set up by this command. Set up 000H to 13FH.
R66	D8 to D0	CAPYMXn	The maximum of Y address of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the Y address to the address value set up by this command, it is the next increment and is initialized by Y address minimum value set up by the MIN Y address register (R65). Set up 000H to 13FH.
R68	D2, D1, D0	E2OPC2 E2OPC1 E2OPC0	E^2PROM interface is controlled.

E2OPC2	E2OPC1	E2OPC0	E^2PROM Control
0	0	0	Setting prohibited
0	0	1	EPSAVE: Writing execution to E^2PROM
0	1	0	MASKON: Writing/elimination permission to E^2PROM
0	1	1	MASKOF: Writing/elimination prohibit to E^2PROM
1	0	0	EPCLR: All area elimination of E^2PROM
1	0	1	EPWALL: It is the writing of FFFFH to all the area of E^2PROM
1	1	0	EPREAD: Reading execution of E^2PROM
1	1	1	Setting prohibited

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Register	Bit	Symbol	Function			
R69	D7 to D0	E2ENn	This is writing permission to E^2PROM enable register.			
R70	D7 to D0	E2An	The writing address to E^2PROM is specified.			
R71	D15 to D0	E2Irn	The index of a register which writes in to E^2PROM is specified. The index and data of the register specified to be this register are written in the address of E^2PROM specified by R70.			
R72	D7 to D0	E2Idn	The product information register for E^2PROM [23:16]	The setting of this register is not the register that affects driver operation but the temporary register which saves data.		
R73	D7 to D0	E2Idn	The product information register for E^2PROM [15:8]			
R74	D7 to D0	E2Idn	The product information register for E^2PROM [7:0]			
R75	D7 to D0	E2SAn	The reading start address of E^2PROM is specified.			
<R> R77	D15 to D8	GOEDn	GOE1 falling position is setup. For more detail, refer to **5.4.1 Horizontal period**.			
	D7 to D0	GOSTn	GOE1 rising position is setup. For more detail, refer to **5.4.1 Horizontal period**.			
<R> R78	D7 to D0	VMCHGn	Polarity changing position of COM is setup. For more detail, refer to **5.4.1 Horizontal period**. Also, set up over 1.			
<R> R79	D15 to D8	SWEDn	The drive end timing in horizontal period is set up. For more detail, refer to **5.4.1 Horizontal period**.			
	D7 to D0	SWSTn	The drive start timing in horizontal period is set up.			
R82	D7 to D5	GIn	The bias current of γ-amplifier is adjusted.			
			GI2	GI1	GI0	Current Value (Magnification)
			0	0	0	0.5
			0	0	1	1.0 (default)
			0	1	0	1.5
			0	1	1	2
			1	0	0	2.5
			1	0	1	3
			1	1	0	3.5
			1	1	1	4
	D2	GRES	The γ-resistance is switched. For more detail, refer to **5.5 γ-Curve Correction Circuit**.			
	D0	G3SW	γ-center Amp. is controlled. 0: γ-center Amp. OFF 1: γ-center Amp. ON			

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th colspan="4">Function</th></tr>
<tr><td rowspan="11">R83</td><td rowspan="10">D6 to D4</td><td rowspan="10">GAPn</td><td colspan="4">The bias current of positive polarity side γ-gray scale amplifier is adjusted.</td></tr>
<tr><td>GAP2</td><td>GAP1</td><td>GAP0</td><td>Current Value (Magnification)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.0 (default)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1.5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7.5</td></tr>
<tr><td rowspan="10">D2 to D0</td><td rowspan="10">GANn</td><td colspan="4">The bias current of negative polarity side γ-gray scale amplifier is adjusted.</td></tr>
<tr><td>GAN2</td><td>GAN1</td><td>GAN0</td><td>Current Value (Magnification)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.0 (default)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1.5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7.5</td></tr>
<tr><td>R97</td><td>D5 to D0</td><td>GM1Pn</td><td colspan="4">Positive polarity side γ-adjustment register</td></tr>
<tr><td>R98</td><td>D5 to D0</td><td>GM3Nn</td><td colspan="4">Negative polarity side γ-adjustment register</td></tr>
<tr><td>R99</td><td>D5 to D0</td><td>GM2Pn</td><td colspan="4">Positive polarity side γ-adjustment register</td></tr>
<tr><td>R100</td><td>D5 to D0</td><td>GM2Nn</td><td colspan="4">Negative polarity side γ-adjustment register</td></tr>
<tr><td>R101</td><td>D5 to D0</td><td>GM3Pn</td><td colspan="4">Positive polarity side γ-adjustment register</td></tr>
<tr><td>R102</td><td>D5 to D0</td><td>GM1Nn</td><td colspan="4">Negative polarity side γ-adjustment register</td></tr>
<tr><td>R103</td><td>D5,
D4</td><td>SOUT_MODE1,
SOUT_MODE0</td><td colspan="4">Source output in dummy period is selected.

SOUT_MODE1 | SOUT_MODE0 | Source Output in Dummy Period
0 | 0 | Reverse phase for COM and V_S or V_{SS}
0 | 1 | Hi-Z
1 | 0 | (Reverse phase for COM and V_S or V_{SS}) and Hi-Z
1 | 1 | Hi-Z</td></tr>
</table>

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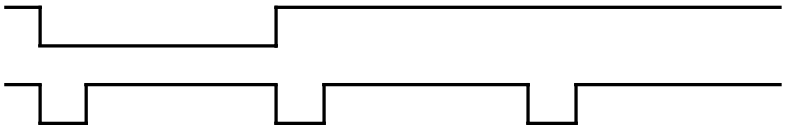
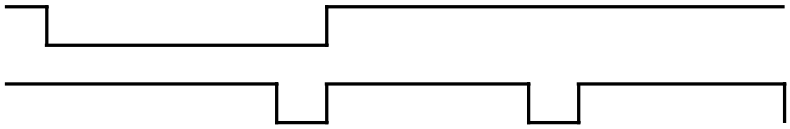
Register	Bit	Symbol	Function
R112	D0	BPSEL	Count method of back porch is selected. 20H: It becomes as it is shown in the following figures (VSYNC is recognized in the rising edge of HSYNC).  Vertical back porch = 1 Vertical back porch = 2 21H: It becomes as it is shown in the following figures (VSYNC is recognized in the falling edge of HSYNC).  Vertical back porch = 1 Vertical back porch = 2

• **Register mode 3/register mode 4**

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Register	Bit	Symbol	Function		
R0 (R0H)	D0	OSCON	Internal oscillator is controlled. 0: Oscillator stop 1: Oscillator operate		
R1 (R1H)	D11, D10	SCN1, SCN0	Gate scan mode is selected.		
			SCN1	SCN0	Gate Scan Mode
			0	0	MODE1
			0	1	MODE2
			1	0	MODE3
			1	1	Setting prohibited
	D9	R_L	Scan direction of gate driver is selected. 0: Scan to G320 from G0 1: Scan to G0 from G320		
	D8	ADX	Addressing of X address is inverted. For more details, refer to **Figure 5–36**.		
	D7	ADY	Addressing of Y address is inverted. For more details, refer to **Figure 5–36**.		
	D6	ADC	Column address direction Source driver output direction is selected.		
R2 (R2H)	D10, D9	GSCAN1, GSCAN0	Skip inversion mode is selected.		
			GSCAN1	GSCAN0	Scan Operation
			0	0	n line inversion
			0	1	Frame inversion
			1	0	Skip inversion 1D
			1	1	Skip inversion 2B
	D1, D0	NLINE1, NLINE0	Line number of n line inversion is selected.		
			NLINE1	NLINE0	Line Number of n Line Inversion
			0	0	n = 1
			0	1	n = 2
			1	0	n = 4
			1	1	n = 8

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Register	Bit	Symbol	Function
R3 (35H)	D12	BGR	In case it writes in display data RAM, this bit changes into BGR the data written in as RGB. 0: RGB 1: BGR
	D8	WAS	Window access mode setting When the window access mode is set, the address is increment/decrement only in the range set by the MIN. ·X address setting register (R528), MAX. ·X address setting register (R529), MIN. ·Y address setting register (R530), and MAX. ·Y address setting register (R531). 0: Normal operation 1: Window access mode
	D5	YDIR	Y address counter control 0: Y address increment 1: Y address decrement
	D4	XDIR	X address counter control 0: X address increment 1: X address decrement
	D3	INC	Address increment direction is selected. 0: X address increment 1: Y address increment
R6 (R6H)	D0	CRES	This bit is command reset function. Be sure to perform after power supply injection. Command reset clears this bit automatically after execution (CRES = 1). Therefore, there is no necessity (normal operation is selected) of setting up 0 more nearly again soft. Moreover, after command reset execution, since this bit of time to change to 1 → 0 is very short, by the time it sets up the following command, it is not necessary to vacate time after command reset setup. 0: Normal operation 1: Command reset
R7 (R7H)	D5	GOE2ON	GOE2 output is controlled. 0: Normal operation 1: GOE2 output Low fixed (gate all ON)
	D4	GOE1ON	ON/OFF of gate scan is selected by GOE1 output. 0: OFF (GOE1 = L fixed) 1: Normal operation
	D3	DISP1	This command performs the same output as when all data is 1, independently of the internal RAM data (white display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 1. DISP1 takes precedence over DISP0. When DISP1 = 1, DISP0 = 1 is ignored.
	D2	DISP0	This command performs the same output as when all data is 0, independently of the internal RAM data (black display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 0.

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Register	Bit	Symbol	Function
R7 (R7H)	D1	STBY_GOFF	This bit selects the gate level, source level, and VCOM level at the time of stand-by. 0: Gate level (V_{GH}), source level (V_{SS}), VCOM level (COML) 1: Gate level (V_{GL}), source level (Hi-Z), VCOM level (V_{SS})
	D0	STBY	This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed, the amplifiers at each output circuit are stopped. After executing the stand-by function using this bit, set the regulator for gate power supply IC to OFF and set the DC/DC converter to OFF. For the sequence, refer to the preliminary product information of the power supply IC etc. Note that when releasing stand-by, perform the opposite operation, after setting the DC/DC converter to ON and setting the regulators of the gate IC and power supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (Display read OFF from RAM stop, VCOM stop, display OFF = all data output as 1)
R9 (R9H)	D12	PSEL	Partial OFF area color register 1 Selects whether the data specified in PGR/PGB/PGG registers as color data, using MSB of a display data RAM is used as color data. 0: Use the data specified to be PGR/PGB/PGG register 1: Use MSB of display data RAM, making it into color data.
	D10, D9, D8	PGR, PGB, PGG	Partial OFF area color register 2 Sets the color of the screen other than the partial display area during partial display (R1024: DTY = 1). One of eight colors can be selected (RGB: 1 bit each) as the OFF color. The relationship between each color data and the bits of this register is as follows. This relationship is not dependent upon the value of ADC. PGR: R OFF = 0, ON = 1 PGG: G OFF = 0, ON = 1 PGB: B OFF = 0, ON = 1
	D7	PNFRM	Only partial non-displaying area carries out frame inversion operation. This bit becomes valid only when a partial display area is line inversion. 0: Partial non-displaying area is line inversion. 1: Partial non-displaying area is frame inversion.
	D4	GSM	
	D2 to D0	GSMLN2 to GSMLN0	Gate scan operation of partial non-displaying area is selected. GSMLN2 to GSMLIN0 = 0, 0, 0: Gate scan stop GSMLN2 to GSMLIN0 = 0, 0, 1: 3 frame cycle GSMLN2 to GSMLIN0 = 0, 1, 0: 5 frame cycle : GSMLN2 to GSMLIN0 = 1, 1, 0: 13 frame cycle GSMLN2 to GSMLIN0 = 1, 1, 1: 15 frame cycle
R11 (RBH)	D0	GS	Color number is selected. GS = 0: 262,144-color GS = 1: 8-color
R12 (RCH)	D9	NWRGB	The input of RGB interface becomes invalid. 0: The input of RGB interface becomes invalid. 1: The input of RGB interface becomes valid.
	D8	RGBS	RGB interface mode is selected. 0: Through mode 1: Capture mode

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Register	Bit	Symbol	Function
R12 (RCH)	D5	VIMD	VSYNC interface mode is selected. If VSYNC is inputted when VSYNC interface mode is selected, scan for one frame will be performed. 0: Normal mode 1: VSYNC interface mode
	D4	DISPCK	The timing clock for display output at the time of RGB interface is selected. 0: Internal oscillation clock 1: HSYNC/VSYNC/DOTCLK
R13 (RDH)	D8	LTS	The setting time of calibration is selected. The calibration function adjusts frame frequency by setting up the time of one line. The setting time of one line can be selected from the following setup by this command. 0: 1 line time = t_{cal} 1: 1 line time = t_{cal} x 2 (t_{cal}: calibration setting time = 1 ÷ frame frequency ÷ display line number)
	D7 to D0	BCNTn	It specifies a part for what clock of a basic clock (an internal oscillation clock or DOTCLK) 1 horizontal period becomes. Moreover, 1 horizontal period determined by the calibration function is able to get to know a part for what clock of a basic clock it is by reading and adding this register.
R14 (REH)	D0	OC	This bit is used for calibration. The time from calibration start command execution until calibration stop command execution becomes the time for 1 line. 0: Calibration stop 1: Calibration start
<R> R15 (RFH)	D15 to D12	VBPn	These bits set the vertical back porch period of the RGB interface. Vertical back porch period = This setting value x HSYNC unit.
	D11 to D8	HBPn	These bits set the horizontal back porch period of the RGB interface. 18/16-bit mode: Horizontal back porch period = This setting value x DOTCLK unit 6-bit mode: Horizontal back porch period = This setting value x 3 x DOTCLK unit
	D7	BPSEL	Count method of back porch is selected.
	D4	VSEG	The active level of VSYNC is selected. 0: Low active 1: High active
	D3	HSEG	The active level of HSYNC is selected. 0: Low active 1: High active
	D0	DCKEG	The active level of DOTCLK is selected. 0: Data latch by rising edge 1: Data latch by falling edge
R16 (R10H)	D8 to D0	RGBSTn	These bits set the start line of the display area to be displayed by in RGB interface through mode. (000H ≤ R16 ≤ 13FH) Be sure to observe the relationship “Set value of R16 register < Set value of R17 register“.
R17 (R11H)	D8 to D0	RGBETn	These bits set the end line of the display area to be displayed by in RGB interface through mode. (000H ≤ R17 ≤ 13FH) Be sure to observe the relationship “Set value of R16 register < Set value of R17 register“.
R18 (R12H)	D7 to D0	CAPXMINn	The minimum value of X addresses of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the X addresses to X address maximum set up by the MAX X address register (R19), they are the next increments and are initialized by the address value set up by this command. Set up 00H to EFH.
R19 (R13H)	D7 to D0	CAPXMAXn	The maximum of X addresses of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the X addresses to the address value set up by this command, they are the next increments and are initialized by X address minimum value set up by the MIN X address register (R18). Set up 00H to EFH.

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Register	Bit	Symbol	Function
R20 (R14H)	D8 to D0	CAPYMINn	The minimum value of Y address of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the Y address to Y address maximum set up by the MAX Y address register (R21), it is the next increment and is initialized by the address value set up by this command. Set up 000H to 13FH.
R21 (R15H)	D8 to D0	CAPYMAXn	The maximum of Y address of window access at the time of RGB interface capture mode is set up. After carrying out the increment of the Y address to the address value set up by this command, it is the next increment and is initialized by Y address minimum value set up by the MIN Y address register (R20). Set up 000H to 13FH.
R24 (R18H)	D15 to D8	GOEDn	GOE1 falling position is setup. For more detail, refer to **5.4.1 Horizontal period**.
	D7 to D0	GOSTn	GOE1 rising position is setup. For more detail, refer to **5.4.1 Horizontal period**.
<R> R25 (R19H)	D7 to D0	VMCHGn	The COM polarity change position is set up. For more detail, refer to **5.4.1 Horizontal period**. Also, set up over 1.
R26 (R1AH)	D15 to D8	SWEDn	The drive end timing in horizontal period is set up. For more detail, refer to **5.4.1 Horizontal period**.
	D7 to D0	SWSTn	The drive start timing in horizontal period is set up. For more detail, refer to **5.4.1 Horizontal period**.
R30 (R1EH)	D1, D0	SOUT_MODE1, SOUT_MODE0	Source output in dummy period is selected.

SOUT_MODE1	SOUT_MODE0	Source Output in Dummy Period
0	0	Reverse phase for COM and V_S or V_{SS}
0	1	Hi-Z
1	0	(Reverse phase for COM and V_S or V_{SS}) and Hi-Z
1	1	Hi-Z

R68 (R44H)	D2 to D0	E2OPC2 to E2OPC0	E^2PROM interface is controlled.

E2OPC2	E2OPC1	E2OPC0	E^2PROM Control
0	0	0	Setting prohibited
0	0	1	EPSAVE: Writing execution to E^2PROM
0	1	0	MASKON: Writing/elimination permission to E^2PROM
0	1	1	MASKOF: Writing/elimination prohibit to E^2PROM
1	0	0	EPCLR: All area elimination of E^2PROM
1	0	1	EPWALL: It is the writing of FFFFH to all the area of E^2PROM
1	1	0	EPREAD: Reading execution of E^2PROM
1	1	1	Setting prohibited

R69 (R45H)	D7 to D0	E2ENn	This is writing permission to E^2PROM enable register.	
R70 (R46h)	D7 to D0	E2An	The writing address to E^2PROM is specified.	
R71 (R47H)	D15 to D0	E2IRn	The index of a register which writes in to E^2PROM is specified.	
R72 (R48H)	D7 to D0	E2IDn	Products information register [23:16]	The setting of this register is not the register that affects driver operation but the temporary register which saves data.
R73 (R49H)	D7 to D0	E2IDn	Products information register [15:8]	
R74 (R4AH)	D7 to D0	E2IDn	Products information register [7:0]	
R75 (R4BH)	D7 to D0	E2SAn	The reading start address of E^2PROM is specified.	
R256 (R100H)	D3	LPM	This bit is used in case it sets to the low power mode. 0: Normal mode 1: Low power mode	

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Register	Bit	Symbol	Function
R257 (R101H)	D12	VDCION	ON/OFF of V_{DCI} regulator is controlled. 0: V_{DCI} regulator OFF 1: V_{DCI} regulator ON
	D11	RGONR	ON/OFF of V_R regulator is controlled. 0: V_R regulator OFF 1: V_R regulator ON
	D10	RGON	ON/OFF of V_S regulator is controlled. 0: V_S regulator OFF 1: V_S regulator ON
	D9	VCLON	ON/OFF of V_{CL} boost is controlled. 0: V_{CL} boost OFF 1: V_{CL} boost ON (V_{DCI} x –1)
	D8	VGLREF	V_{GL} boost mode is switched 0: $V_{GL} = V_R$ x (–2 or –3) + V_{SS} 1: $V_{GL} = V_R$ x (–2 or –3) + V_{CL}
	D7, D6	VGLON1, VGLON0	ON/OFF of V_{GL} boost is controlled. <VGLON1, VGLON0 = 0, 0> V_{GL} boost OFF <VGLON1, VGLON0 = 0, 1> $V_{GL} = V_R$ x –2 + (V_{SS} or V_{CL}) <VGLON1, VGLON0 = 1, X> $V_{GL} = V_R$ x –3 + (V_{SS} or V_{CL})
	D5	VGHREF	V_{GH} boost mode is switched. 0: $V_{GH} = V_R$ x (2 or 3) + V_R 1: $V_{GH} = V_R$ x (2 or 3) + V_{DCI}
	D4, D3	VGHON1, VGHON0	ON/OFF of V_{GH} boost is controlled. <VGHON1, VGHON0 = 0, 0> V_{GH} boost OFF <VGHON1, VGHON0 = 0, 1> $V_{GH} = V_R$ x 2 + (V_R or V_{DCI}) <VGHON1, VGHON0 = 1, X> $V_{GH} = V_R$ x 3 + (V_R or V_{DCI})
	D2, D1	VD2ON1, VD2ON0	ON/OFF of V_{DD2} boost is controlled. <VD2ON1, VD2ON0 = 0, 0> V_{DD2} boost OFF (V_{DCI} or Hi-Z) <VD2ON1, VD2ON0 = 0, 1> $V_{DD2} = V_{DCI}$ x 2 boost ON <VD2ON1, VD2ON0 = 1, X> $V_{DD2} = V_{DCI}$ x 3 boost ON
	D0	DCON	ON/OFF of DC/DC converter is controlled. 0: DC/DC converter OFF 1: DC/DC converter ON

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Register	Bit	Symbol	Function
<R> R258 (R102H)	D7	VDCISEL	When V_{DCI} regulator OFF (VDCION [R257] = 0) and V_{DCI} output is not set into Hi-Z (VDCIHZ [R25] = 0), the output state of V_{DCI} regulator is controlled. <VDCISEL = 0> $V_{DCI} = V_{DC}$ <VDCISEL = 1> $V_{DCI} = V_{SS}$
	D6	VDCIHZ	Output state of V_{DCI} pin is defined when V_{DCI} regulator is OFF (VDCION [R257] = 0). <VDCIHZ = 0> $V_{DCI} = V_{DC}$ or V_{SS} (setting by VDCISEL) <VDCIHZ = 1> V_{DCI} =Hi-Z
	D5	VRHI	Output of V_R regulator is selected. <VRHI = 0> V_R regulator = ON <VRHI = 1> V_R regulator = Hi-Z
	D4	VSHI	Output of V_S regulator is selected. <VSHI = 0> V_S regulator = ON <VSHI = 1> V_S regulator = Hi-Z
	D3	DCFRM	This bit selects whether DC/DC operation is synchronized with frame signal. <DCFRM = 0> DC/DC operation = frame asynchronous <DCFRM = 1> DC/DC operation = frame synchronization
	D2	DC3HZ	The output state of V_{CL} at the time of V_{CL} boost OFF is controlled. <DC3HZ = 0> $V_{CL} = V_{SS}$ <DC3HZ = 1> V_{CL} = Hi-Z
	D1	DC2HZ	The output state of V_{GH} and V_{GL} at the time of V_{GH} and V_{GL} boost OFF is controlled. <DC2HZ = 0> $V_{GH} = V_{DD2}$, $V_{GL} = V_{SS}$ <DC2HZ = 1> V_{GH} = Hi-Z, V_{GL} = Hi-Z
	D0	DC1HZ	The output state of V_{DD2} at the time of V_{DD2} boost OFF is controlled. <DC1HZ = 0> $V_{DD2} = V_{DCI}$ <DC1HZ = 1> V_{DD2} = Hi-Z

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Register	Bit	Symbol	Function		
R259 (R103H)	D7, D6	LFS3, LFS2	When low power mode (LPM [R256] = 1), V_{GH}, V_{GL} boost frequency are selected.		
			LFS3	LFS2	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D5, D4	LFS1, LFS0	When low power mode (LPM [R256] = 1), V_{DD2}, V_{CL} boost frequency are selected.		
			LFS1	LFS0	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D3, D2	FS3, FS2	When normal drive (LPM [R256] = 0), V_{GH}, V_{GL} boost frequency are selected.		
			FS3	FS2	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D1, D0	FS1, FS0	When normal drive (LPM [R256] = 0), V_{DD2}, V_{CL} boost frequency are selected.		
			FS1	FS0	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
R260 (R104H)	D5	PONM	The internal sequence of DC/DC rising operation and an external sequence are selected. 0: External sequence 1: Internal sequence		
	D4	PON	The frequency of operation at the time of the rising of V_{GH}, V_{DD2}, V_{GL} and V_{CL} when DC/DC rising is selected. It becomes valid only at the time of PONM = 0. 0: Normal operation 1: Rising operation		
	D3, D2	DUPF1, DUPF0	The frequency of operation of whole DC/DC converter circuit when DC/DC rising is selected.		
			DUPF1	DUPF0	Boost Frequency
			0	0	$f_{DCCLK}/1$
			0	1	$f_{DCCLK}/2$
			1	0	$f_{DCCLK}/4$
			1	1	$f_{DCCLK}/8$
	D1, D0	PUPT1, PUPT0	The ON time at the time of the rising of V_{GH}, V_{DD2}, V_{GL}, V_{CL} RGON, RGONR when DC/DC rising is selected. It becomes valid only at the time of PONM = 1.		

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Register	Bit	Symbol	Function
R261 (R105H)	D12	SFVSEL	Output voltage of RV_{DD} regulator is selected. <SFVSEL = 0> RV_{DD} = 2.1 V (for test) <SFVSEL = 1> RV_{DD} = 2.3 V
	D11 to D9	VSEL2 to VSEL0	Output voltage of V_{GM} regulator is selected. <VC2 = 1, VC1 = 0, VC0 = 1> At V_{REFR} = 2.0 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.40 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.50 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.60 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.70 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.80 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 4.90 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 5.00 V <VSEL2 = 0, VSEL1 = 0, VSEL0 = 0> V_{GM} = 5.10 V
	D8 to D6	VRSEL2 to VRSEL0	Output voltage of V_R regulator is selected. <VC2 = 1, VC1 =0, VC0 = 1> At V_{REFR} = 2.0 V <VRSEL2 = 0, VRSEL1 = 0, VRSEL0 = 0> V_R = 4.50 V <VRSEL2 = 0, VRSEL1 = 0, VRSEL0 = 1> V_R = 4.80 V <VRSEL2 = 0, VRSEL1 = 1, VRSEL0 = 0> V_R = 4.90 V <VRSEL2 = 0, VRSEL1 = 1, VRSEL0 = 1> V_R = 5.00 V <VRSEL2 = 1, VRSEL1 = 0, VRSEL0 = 0> V_R = 5.05 V <VRSEL2 = 1, VRSEL1 = 0, VRSEL0 = 1> V_R = 5.10 V <VRSEL2 = 1, VRSEL1 = 1, VRSEL0 = 0> V_R = 5.20 V <VRSEL2 = 1, VRSEL1 = 1, VRSEL0 = 1> V_R = 5.40 V
	D5 to D3	VSSEL2 to VSSEL0	Output voltage of V_S regulator is selected. <VC2 = 1, VC1 =0, VC0 = 1> At V_{REFR} = 2.0 V <VSSEL2 = 0, VSSEL1 = 0, VSSEL0 = 0> V_S = 4.85 V <VSSEL2 = 0, VSSEL1 = 0, VSSEL0 = 1> V_S = 4.90 V <VSSEL2 = 0, VSSEL1 = 1, VSSEL0 = 0> V_S = 4.95 V <VSSEL2 = 0, VSSEL1 = 1, VSSEL0 = 1> V_S = 5.00 V <VSSEL2 = 1, VSSEL1 = 0, VSSEL0 = 0> V_S = 5.05 V <VSSEL2 = 1, VSSEL1 = 0, VSSEL0 = 1> V_S = 5.10 V <VSSEL2 = 1, VSSEL1 = 1, VSSEL0 = 0> V_S = 5.15 V <VSSEL2 = 1, VSSEL1 = 1, VSSEL0 = 1> V_S = 5.20 V
	D2 to D0	VC2 to VC0	Output voltage of REFR regulator is selected. <VC2 = 0, VC1 = 0, VC0 = 0> V_{REFR} = 1.50 V <VC2 = 0, VC1 = 0, VC0 = 1> V_{REFR} = 1.60 V <VC2 = 0, VC1 = 1, VC0 = 0> V_{REFR} = 1.70 V <VC2 = 0, VC1 = 1, VC0 = 1> V_{REFR} = 1.80 V <VC2 = 1, VC1 = 0, VC0 = 0> V_{REFR} = 1.90 V <VC2 = 1, VC1 = 0, VC0 = 1> V_{REFR} = 2.00 V <VC2 = 1, VC1 = 1, VC0 = 0> V_{REFR} = 2.05 V <VC2 = 1, VC1 = 1, VC0 = 1> V_{REFR} = 2.10 V

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Register	Bit	Symbol	Function
R262 (R106H)	D8	REGMONI	Output state of TVREFR is selected. 0: TVREFR = Hi-Z 1: TVREFR = Output setup voltage in VC2 to VC0
	D7, D6	LCOMCS1, LCOMCS0	When low power mode, COMH/COML amplitude current is selected. <LCOMCS1, LCOMCS0 = 0, 0> Amp. current = x 0.25 mode <LCOMCS1, LCOMCS0 = 0, 1> Amp. current = x 0.5 mode <LCOMCS1, LCOMCS0 = 1, 0> Amp. current = x 1.0 mode <LCOMCS1, LCOMCS0 = 1, 1> Amp. current = x 1.5 mode
	D5, D4	COMCS1 COMCS0	COMH/COML amplitude current is selected. <COMCS1, COMCS0 = 0, 0> Amp. current = x 1 mode <COMCS1, COMCS0 = 0, 1> Amp. current = x 2 mode <COMCS1, COMCS0 = 1, 0> Amp. current = x 3 mode <COMCS1, COMCS0 = 1, 1> Amp. current = x 7 mode
	D3, D2	LACS1. LACS0	When low power mode (LPM [R256] = 1), V_R and V_S regulator amplitude current is selected. Although drive capability is improved so that there is much current passed in amplifier, power consumption increases. This value recommends what it opts for after evaluating enough by the real panel. <LACS1, LACS0 = 0, 0> Amp. current = x 0.25 mode <LACS1, LACS0 = 0, 1> Amp. current = x 0.5 mode <LACS1, LACS0 = 1, 0> Amp. current = x 1.0 mode <LACS1, LACS0 = 1, 1> Amp. current = x 1.5 mode
	D1, D0	ACS1, ACS0	When normal drive (LPM [R256] = 0), V_R and V_S regulator amplitude current is selected. <ACS1, ACS0 = 0, 0> Amp. current = x 1 mode <ACS1, ACS0 = 0, 1> Amp. current = x 2 mode <ACS1, ACS0 = 1, 0> Amp. current = x 3 mode <ACS1, ACS0 = 1, 1> Amp. current = x 6 mode
R263 (R107H)	D5, D4	COMP1 COMP0	VCOMM ability at VCOMM output is selected. <COMP1, COMP0 = 0, 0> x 1 mode <COMP1, COMP0 = 0, 1> x 1.5 mode <COMP1, COMP0 = 1, 0> x 2 mode <COMP1, COMP0 = 1, 1> x 2.5 mode
	D2	COHIM	Output state of VCOMM is controlled. 0: VCOMHM/VCOMLM 1: Hi-Z
	D0	COMONM	ON/OFF control of the common drive output VCOMM is carried out. 0: OFF (VCOMHM and VCOMLM amplifier-OFF) 1: ON (VCOMHM and VCOMLM amplifier-ON)
R264 (R108H)	D5 to D0	DAn	The amplitude of VCOMM/VCOMS output is controlled by 6-bit D/A.
R265 (R109H)	D7	COMINM	The center voltage input of VCOMM is selected. 0: Internal D/A becomes valid 1: Center level voltage of VCOMINM input becomes valid
	D6 to D0	MCDA	The center level of VCOMM output is controlled by 7-bit D/A.

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Register	Bit	Symbol	Function
R512 (R200H)	D7 to D0	XAn	This register sets the X address of the display RAM. Set 00H to EFH.
R513 (R201H)	D8 to D0	YAn	This register sets the Y address of the display RAM. Set 000H to 13FH.
R515 (R203h)	D13 to D8	WMn	Display data write mask setup (D [11:6] support)
	D5 to D0	WMn	Display data write mask setup (D [5:0] support)
R516 (R204H)	D5 to D0	WMn	Display data write mask setup (D [17:12] support)
R528 (R210H)	D7 to D0	XMNn	The minimum value of X address at the time of window access mode is set up. After carrying out the increment of the X address to X address maximum set up by the MAX. X address register (R529), they are the next increments and are initialized by the address value set up by this command. Set up 00H to EFH.
R529 (R211H)	D7 to D0	XMXn	The maximum of X address at the time of window access mode is set up. After carrying out the increment of the X address to the address value set up by this command, they are the next increments and are initialized by X address minimum value set up by the MIN. X address register (R528). Set up 00H to EFH.
R530 (R212H)	D8 to D0	YMNn	The minimum value of Y address at the time of window access mode is set up. After carrying out the increment of the Y address to Y address maximum set up by the MAX. Y address register (R531), they are the next increments and are initialized by the address value set up by this command. Set up to 000H to 13FH.
R531 (R213H)	D8 to D0	YMXn	The maximum of Y address at the time of window access mode is set up. After carrying out the increment of the Y address to the address value set up by this command, it is the next increment and is initialized by Y address minimum value set up by the MIN. Y address register (R530). Set up to 000H to 13FH.
R536 (R218H)	D7 to D0	LCDXMNn	The minimum value of X addresses of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the X addresses to X address maximum set up by the LCDMAX X address register (R537), they are the next increments and are initialized by the address value set up by this command. In addition, the source output pin which is not specified by LCDXMIN (R536) and LCDXMX (R537) does not output. Set up 00H to EFH. Moreover, specify a surely bigger area than the window area in window access mode.
R537 (R219H)	D7 to D0	LCDXMXn	The maximum of X addresses of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the X addresses to the address value set up by this command, they are the next increments and are initialized by X address minimum value set up by the LCDMIN X address register (R536). In addition, the source output pin which is not specified by LCDXMIN (R536) and LCDXMX (R537) does not output. Set up 00H to EFH. Moreover, specify a surely bigger area than the window area in window access mode.
R538 (R21AH)	D8 to D0	LCDYMNn	The minimum value of Y address of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the Y address to Y address maximum set up by the LCDMAX Y address register (R539), it is the next increment and is initialized by the address value set up by this command. Set up 000H to 13FH. Moreover, specify a surely bigger area than the window area in window access mode.

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Register	Bit	Symbol	Function
R539 (R21BH)	D8 to D0	LCDYMXn	The maximum of Y address of a liquid crystal display area is set up. When window access mode is not being used, after carrying out the increment of the Y address to the address value set up by this command, it is the next increment and is initialized by Y address minimum value set up by the LCDMIN Y address register (R538). Set up 000H to 13FH. Moreover, specify a surely bigger area than the window area in window access mode.
R768 (R300H)	D13 to D8	GM3Pn	Positive polarity side γ-adjustment register
	D5 to D0	GM1Pn	Positive polarity side γ-adjustment register
R771 (R303H)	D5 to D0	GM2Pn	Positive polarity side γ-adjustment register
R772 (R304H)	D14 to D8	GPLn	Sets the positive polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
	D6 to D0	GPHn	Sets the positive polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
R773 (R305H)	D13 to D8	GM3n	Negative polarity side γ-adjustment register
	D5 to D0	GM1n	Negative polarity side γ-adjustment register
R776 (R308H)	D5 to D0	GM2n	Negative polarity side γ-adjustment register
R777 (R309H)	D14 to D8	GNLn	Sets the negative polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
	D6 to D0	GNHn	Sets the negative polarity γ-amplitude adjustment. For more detail, refer to **5.5 γ-Curve Correction Circuit**.
R780 (R30CH)	D10 to D8	GIn	The bias current of γ-amplifier is adjusted.

GI2	GI1	GI0	Current value (magnification)
0	0	0	0.5
0	0	1	1.0 (default)
0	1	0	1.5
0	1	1	2
1	0	0	2.5
1	0	1	3
1	1	0	3.5
1	1	1	4

	D6 to D4	GAPn	The bias current of positive polarity side γ-gray scale amplifier is adjusted.

GAP2	GAP1	GAP0	Current value (magnification)
0	0	0	0.5
0	0	1	1.0 (default)
0	1	0	1.5
0	1	1	2
1	0	0	3
1	0	1	4
1	1	0	6
1	1	1	7.5

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th colspan="4">Function</th></tr>
<tr><td rowspan="10">R780
(R30CH)</td><td rowspan="10">D2 to D0</td><td rowspan="10">GANn</td><td colspan="4">The bias current of negative polarity side γ-gray scale amplifier is adjusted.</td></tr>
<tr><td>GAN2</td><td>GAN1</td><td>GAN0</td><td>Current value (magnification)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.0 (default)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1.5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7.5</td></tr>
<tr><td rowspan="2">R781
(R30DH)</td><td>D4</td><td>GRES</td><td colspan="4">The γ-resistance is switched.
For more detail, refer to 5.5 γ-Curve Correction Circuit.</td></tr>
<tr><td>D1</td><td>G3SW</td><td colspan="4">γ-center Amp. is controlled.
0: γ-center Amp. OFF
1: γ-center Amp. ON</td></tr>
<tr><td>R1024
(R400H)</td><td>D0</td><td>DTY</td><td colspan="4">Partial function is selected.
In addition, efficiency of this command is carried out after transmission from the timing which outputs the following line data.
0: Normal display mode
1: Partial display mode</td></tr>
<tr><td>R1025
(R401H)</td><td>D0</td><td>DINV</td><td colspan="4">RAM write data is inverted.
(0: Normal mode 1: Inversion mode)</td></tr>
<tr><td>R1026
(R402H)</td><td>D8 to D0</td><td>P1SLn</td><td colspan="4">This is partial 1 display area start line register (000H to 13FH).
From the line set up by this command to the line set up by the partial 1 display area end line register (R1027) becomes partial 1 display area at the time of partial display (R1024: DTY = 1).</td></tr>
<tr><td>R1027
(R403H)</td><td>D8 to D0</td><td>P1AWn</td><td colspan="4">This is partial 1 display area line count register (000H to 13FH).
An area starting from the line set by the partial 1 display area start register (R1026) and ending as set by this command is the partial 1 display area.
If this register is 0, the values of the partial 2 display area start line register (R1029) and the partial 2 display area line count register (R1030) are not valid.</td></tr>
<tr><td>R1028
(R404H)</td><td>D8 to D0</td><td>P1SAn</td><td colspan="4">This is partial 1 display area start line display RAM address.</td></tr>
<tr><td>R1029
(R405H)</td><td>D8 to D0</td><td>P2SLn</td><td colspan="4">This is partial 2 display area start line register (000H to 13FH).
From the line set up by this command to the line set up by the partial 2 display area end line register (R1030) becomes partial 2 display area at the time of partial display (R1024: DTY = 1).</td></tr>
<tr><td>R1030
(R406H)</td><td>D8 to D0</td><td>P2AWn</td><td colspan="4">This is partial 2 display area line count register (000H to 13FH)
An area starting from the line set by the partial 2 display area start register (R1029) and ending as set by this command is the partial 2 display area.
If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R1029) and partial 2 display area line count register (R1030) are not valid.</td></tr>
<tr><td>R1031
(R407H)</td><td>D8 to D0</td><td>P2SAn</td><td colspan="4">This is partial 2 display area start line display RAM address.</td></tr>
</table>

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	–0.3 to +3.0	V
Power supply voltage	V_{CCIO}	–0.3 to +6.0	V
Power supply voltage	V_{DC}	–0.3 to +4.2	V
Power supply voltage	V_{GM}, V_S	–0.3 to +6.0	V
Power supply voltage	V_R	–0.3 to +7.0	V
Power supply voltage	V_{DD2}	–0.3 to +7.0	V
Power supply voltage	V_{CL}	–4.2 to +0.3	V
Power supply voltage	V_{GH}–V_{GL}	–0.3 to +40.0	V
Power supply voltage	V_{DCI}–V_{CL}	–0.3 to +7.0	V
Input voltage	V_I Note 1	–0.3 to V_{CCIO} + 0.3	V
Input voltage	V_I Note 2	–0.3 to V_{DC} + 0.3	V
Input current	I_I	±10	mA
Output current	I_{O1} Note 3	±10	mA
Output current	I_{O2} Note 4	±100	mA
Output current	I_{O3} Note 5	0 to 50	mA
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Notes 1. Power supply system of V_{CCIO} pin

2. Power supply system of V_{DC} pin

3. D0 to D17, CSTB, ECS, ESK, EDO, Y_1 to Y_{720}, G_1 to G_{240}

4. VCOMM

5. RV_{DD}

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	2.1	2.3	2.5	V
Power supply voltage	V_{CCIO}	1.65	2.8	3.3	V
Power supply voltage	V_{DC}	2.5	2.8	3.3	V
Power supply voltage	V_{GM}	3.0	5.0	5.5	V
Power supply voltage	V_S	3.4	5.0	5.5	V
Power supply voltage	V_R	3.0	5.0	6.5	V
Power supply voltage	V_{DD2}	4.6	5.6	6.5	V
Power supply voltage	V_{CL}	–3.3	–2.8	–1.9	V
Power supply voltage	V_{GH}–V_{GL}	8.3	25.0	35.0	V
Input voltage	V_{I1} Note1	0		V_{CCIO}	V
Input voltage	V_{I2} Note2	0		V_{DC}	V

Notes 1. Power supply system of V_{CCIO} pin

2. Power supply system of V_{DC} pin

Power supply series (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD} = 2.1 to 2.5 V, V_{CCIO} = 1.65 to 3.3 V, V_{DC} = 2.5 to 3.3 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions	MIN.	TYP. Note1	MAX.	Unit
V_S output voltage	V_S	VC[2:0] = 101, VSSEL[2:0] = 011, Is = 1 mA, V_{DD2} = 5.5 to 6.5 V	4.6	5.0	5.4	V
V_S output resistance	RV_S	Is = 0→1 mA variable, V_S measurement conditions		10	30	Ω
V_R output voltage	V_R	VC[2:0] = 101, VRSEL[2:0] = 011, I_R = 1 mA, V_{DD2} = 5.5 to 6.5 V	4.6	5.0	5.4	V
V_R output resistance	RV_R	I_R = 0→1 mA variable, V_R measurement conditions		10	30	Ω
V_{GM} output voltage	V_{GM}	VC[2:0] = 101, VSEL[2:0] = 000, I_{GM} = 100 μA, VSSEL[2:0] = 011	4.05	4.4	4.75	V
V_{GM} output resistance	RV_{GM}	I_{GM} = 0→100 μA variable, V_{GM} measurement conditions		30	60	Ω
V_{DD2} boost voltage efficient 1	V_{DD21}	V_{DCI} x 2 boost, I_{DD2} = 4 mA Note2	92		100	%
V_{DD2} boost voltage efficient 2	V_{DD22}	V_{DCI} x 3 boost, I_{DD2} = 4 mA Note2	75		100	%
V_{CL} boost voltage efficient	V_{CL}	V_{DCI} x –1 boost, I_{CL} = –2 mA Note2	79		100	%
V_{GH} boost voltage efficient 1	V_{GH1}	V_R x 2 + V_R boost, I_{GH} = 300 μA Note2	85		100	%
V_{GH} boost voltage efficient 2	V_{GH2}	V_R x 3 + V_R boost, I_{GH} = 300 μA Note2	85		100	%
V_{GH} boost voltage efficient 3	V_{GH3}	V_R x 2 + V_{DCI} boost, I_{GH} = 300 μA Note2	82		100	%
V_{GH} boost voltage efficient 4	V_{GH4}	V_R x 3 + V_{DCI} boost, I_{GH} = 300 μA Note2	82		100	%
V_{GL} boost voltage efficient 1	V_{GL1}	V_R x –2 + V_{SS} boost, I_{GL} = –300 μA Note2	82		100	%
V_{GL} boost voltage efficient 2	V_{GL2}	V_R x –3 + V_{SS} boost, I_{GL} = –300 μA Note2	82		100	%
V_{GL} boost voltage efficient 3	V_{GL3}	V_R x –2 + V_{CL} boost, I_{GL} = –300 μA Note2	85		100	%
V_{GL} boost voltage efficient 4	V_{GL4}	V_R x –3 + V_{CL} boost, I_{GL} = –300 μA Note2	85		100	%
V_{DD2} output resistance 1	RV_{DD21}	V_{DC} x 2 boost, I_{DD2} = 0→4 mA variable Note2		65	100	Ω
V_{DD2} output resistance 2	RV_{DD22}	V_{DC} x 3 boost, I_{DD2} = 0→4 mA variable Note2		210	330	Ω
V_{CL} output resistance	RV_{CL}	V_{DCI} x –1 boost, I_{CL}= 0→–2 mA variable Note2		200	300	Ω
V_{GH} output resistance 1	RV_{GH1}	V_R x 2 + V_R boost, I_{GH} = 0→300 μA variable Note2		4.2	7.0	kΩ
V_{GH} output resistance 2	RV_{GH2}	V_R x 3 + V_R boost, I_{GH} = 0→300 μA variable Note2		5.2	9.0	kΩ
V_{GH} output resistance 3	RV_{GH3}	V_R x 2 + V_{DCI} boost, I_{GH} = 0→300 μA variable Note2		4.2	7.0	kΩ
V_{GH} output resistance 4	RV_{GH4}	V_R x 3 + V_{DCI} boost, I_{GH} = 0→300 μA variable Note2		5.5	10.0	kΩ

Notes 1. TYP. values are reference values when V_{DD} = 2.3 V, V_{CCIO} = 2.8 V, V_{DC} = 2.8 V, T_A = 25°C.

<R> **2.** External capacitance: V_{GH}, V_{GL}, C21 to C23 = 0.47 μF, V_{DD2}, VCL, C11, C12, C31 = 1 μF, DC/DC boost frequency setup: FS<3:0> = 0101

Power supply series (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD} = 2.1 to 2.5 V, V_{CCIO} = 1.65 to 3.3 V, V_{DC} = 2.5 to 3.3 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions	MIN.	TYP. Note1	MAX.	Unit
V_{GL} output resistance 1	RV_{GL1}	V_R x –2 + V_{SS} boost, I_{GL} = 0→ –300 μA variable Note2		3.3	5.5	kΩ
V_{GL} output resistance 2	RV_{GL2}	V_R x –3 + V_{SS} boost, I_{GL} = 0→ –300 μA variable Note2		4.2	7.5	kΩ
V_{GL} output resistance 3	RV_{GL3}	V_R x –2 + V_{CL} boost, I_{GL} = 0→ –300 μA variable Note2		3.5	6.0	kΩ
V_{GL} output resistance 4	RV_{GL4}	V_R x –3 + V_{CL} boost, I_{GL} = 0→ –300 μA variable Note2		4.4	8.0	kΩ
RV_{DD} output voltage	VRV_{DD}	SFVSEL = 1, IRVDD = 10 mA	2.1	2.3	2.5	V
RV_{DD} output resistance	RRV_{DD}	SFVSEL = 1, IRVDD = 0→10 mA variable		1	5	Ω
V_{DCI} output voltage 1	V_{DCI1}	VD2ON1 = 1, IVDCI = 10 mA, V_{DC} = 3.3 V	2.9	3.2	3.3	V
V_{DCI} output voltage 2	V_{DCI2}	VD2ON1 = 0, IVDCI = 10 mA	1.9	2.1	2.3	V
V_{DCI} output resistance 1	RV_{DCI1}	VD2ON1 = 0, IVDCI = 0→10 mA variable, V_{DC} = 3.3 V		7	14	Ω
V_{DCI} output resistance 2	RV_{DCI2}	VD2ON1 = 0, IVDCI = 0→10 mA variable		1	14	Ω
Consumption current	I_{CCIO}	V_{CCIO} pin (CPU non-access) Note3		0.1	10	μA
	I_{DC}	V_{DC} pin (CPU non-access) Note3		2.7	4.5	mA
	I_{STBY1}	V_{CCIO} pin (stand-by mode) Note4		0.1	3	μA
	I_{STBY2}	V_{DC} pin (stand-by mode) Note4		1.6	10	

Notes 1. TYP. values are reference values when V_{DD} = 2.3 V, V_{CCIO} = 2.8 V, V_{DC} = 2.8 V, T_A = 25°C.

<R> **2.** External capacitance: V_{GH}, V_{GL}, C21, C22, C23 = 0.47 μF, V_{DD2}, VCL, C11, C12, C31 = 1 μF, DC/DC boost frequency setup: FS<3:0> = 0101

3. V_{CCIO} = 2.8 V, V_{DC} = 2.8 V, V_{DD}: RV_{DD} connection (VSTBY = L), at SFVSEL = 1, white display, line inversion, frame frequency: 60 Hz, V_{DD2} = V_{DC} x 2 boost, 262,144-color mode, γ-middle AMP_ON, V_S = 5 V, COMCS<1:0> = 11, ACS<1:0> = 11, no load

4. V_{CCIO} = 3.3 V, V_{DC} = 3.3 V, V_{DD}: RV_{DD} connection (VSTBY = L), at SFVSEL = 1

Logic series (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD} = 2.1 to 2.5 V, V_{CCIO} = 1.65 to 3.3 V, V_{DC} = 2.3 to 3.3 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}	V_{CCIO} series	0.8 V_{CCIO}			V
Low level input voltage	V_{IL}	V_{CCIO} series			0.2 V_{CCIO}	V
High level output voltage 1	V_{OH1}	V_{CCIO} series, I_{OUT} = –100 μA	0.8 V_{CCIO}			V
Low level output voltage 1	V_{OL1}	V_{CCIO} series, I_{OUT} = 100 μA			0.2V_{CCIO}	V
High level output voltage 2	V_{OH2}	V_{DC} series, I_{OUT} = –100 μA	0.8 V_{DC}			V
Low level output voltage 2	V_{OL2}	V_{DC} series, I_{OUT} = 100 μA			0.2V_{DC}	V
High level input current	I_{IH1}	V_{CCIO} series			1	μA
	I_{IH2}	V_{DC} series			1	μA
Low level input current	I_{IL1}	V_{CCIO} series	–1			μA
	I_{IL2}	V_{DC} series	–1			μA

Driver series (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = 2.1 to 2.5 V, V_{CCIO} = 1.65 to 3.3 V, V_{DC} = 2.5 to 3.3 V, V_S = 3.4 to 5.5 V, V_{SS} = 0 V, V_{GH} = 15 V, V_{GL} = –15 V)

Parameter	Symbol	Condition		MIN.	TYP. Note1	MAX.	Unit
Source driver output voltage range	V_{P-P}			V_{SS} + 0.1		V_S – 0.1	V
Source driver output deviation	ΔV_O			–10		+10	mV
Source driver output delay time	t_{PHLS1}	R_L = 40 kΩ, C_L = 20 pF Note2	1-output select		2.5	5	μs
	t_{PHLS2}		720-output simultaneous selection		5.0	10	μs
	t_{PLHS1}	R_L = 40 kΩ, C_L = 20 pF Note2	1-output select		2.5	5	μs
	t_{PLHS2}		720-output simultaneous selection		5.0	10	μs
Gate driver output through rate time	t_{THLG1}	C_L = 35 pF Note2	1-output order driving		0.50	1.0	μs
	t_{THLG2}		320-output simultaneous driving		0.50	1.0	μs
	t_{TLHG1}	C_L = 35 pF Note2	1-output order driving		0.75	1.5	μs
	t_{TLHG2}		320-output simultaneous driving		0.75	1.5	μs
VCOMM output voltage range				V_{CL} + 0.1		V_S – 0.1	V
VCOMHM output voltage	V_{COMHM}	I_{COMHM} = 1 mA Note3		2.25	2.50	2.75	V
VCOMLM output voltage	V_{COMLM}	I_{COMLM} = 1 mA Note3		–0.70	–0.50	–0.30	V
VCOMHM output resistance	R_{VCOMHM}	I_{COMHM} = 0→1 mA variable Note3			15	30	Ω
VCOMLM output resistance	R_{VCOMLM}	I_{COMLM} = 0→1 mA variable Note3			20	40	Ω
VCOMM high level output voltage	V_{COMMH}	I_{VCOMM} = 1 mA, COMP<1:0> = 00 Note3		2.20	2.50	2.75	V
VCOMM low level output voltage	V_{COMML}	I_{VCOMM} = 1 mA, COMP<1:0> = 00 Note3		–0.70	–0.50	–0.25	V
VCOMM high level output resistance	R_{VCOMMH}	I_{VCOMM} = 0→1 mA variable, V_{COMMH} condition Note3			50	100	Ω
VCOMM low level output resistance	R_{VCOMML}	I_{VCOMM} = 0→1 mA variable, V_{COMML} condition Note3			50	100	Ω

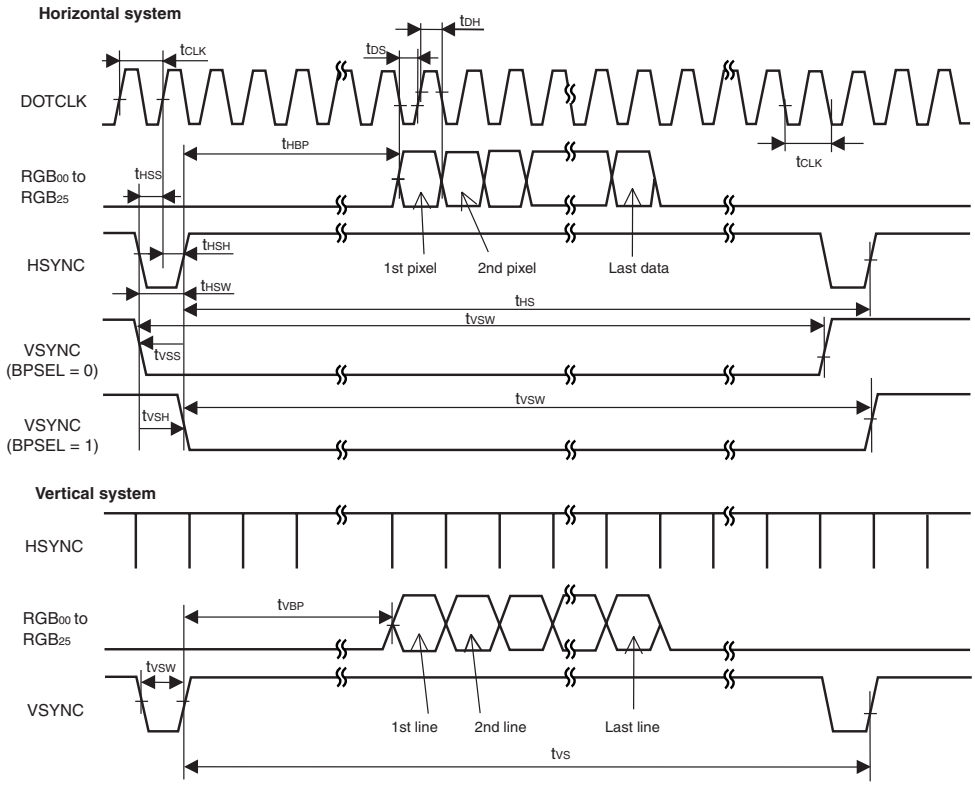
Notes 1. The TYP. Values are reference values at V_S = 5.0 V, V_{GH} = 15 V, V_{GL} = –15 V, T_A = 25°C.

2. Load is thing per one output.

3. VCOMM amplitude setup: DA<5:0> = 00H, VCOMM center setup: MCDA<6:0> = 00H, VC<2:0> = 101, VSEL<2:0> = 110 (V_{GM} = 5 V output setup)

AC specification (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD} = 2.1 to 2.5 V, V_{CCIO} = 1.65 to 3.3 V)

<R> **(a) 16-bit /18-bit RGB interface**



	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
<R>	Dot clock cycle time	t_{CLK}		120			ns
	Dot clock high level pulse width	t_{CLKH}		60			ns
	Dot clock low level pulse width	t_{CLKL}		60			ns
	Data set-up time	t_{DS}		50			ns
<R>	Data hold time	t_{DH}		50			ns
	HSYNC pulse width	t_{HSW}		1			DOTCLK
<R>	HSYNC set-up time	t_{HSS}		50			ns
<R>	HSYNC hold time	t_{HSH}		50			ns
	Horizontal period back porch time	t_{HBP}		1			DOTCLK
	VSYNC pulse width	t_{VSW}		1			H
<R>	VSYNC set-up time	t_{VSS}	BPSEL = 0	t_{HSW}			DOTCLK
<R>	VSYNC hold time	t_{VSH}	BPSEL = 1	t_{HSW}			DOTCLK
	Vertical period back porch time	t_{VBP}		1			H

Remarks 1. The rise and fall times (t_r, t_f) of an input signal are 15 ns or less.

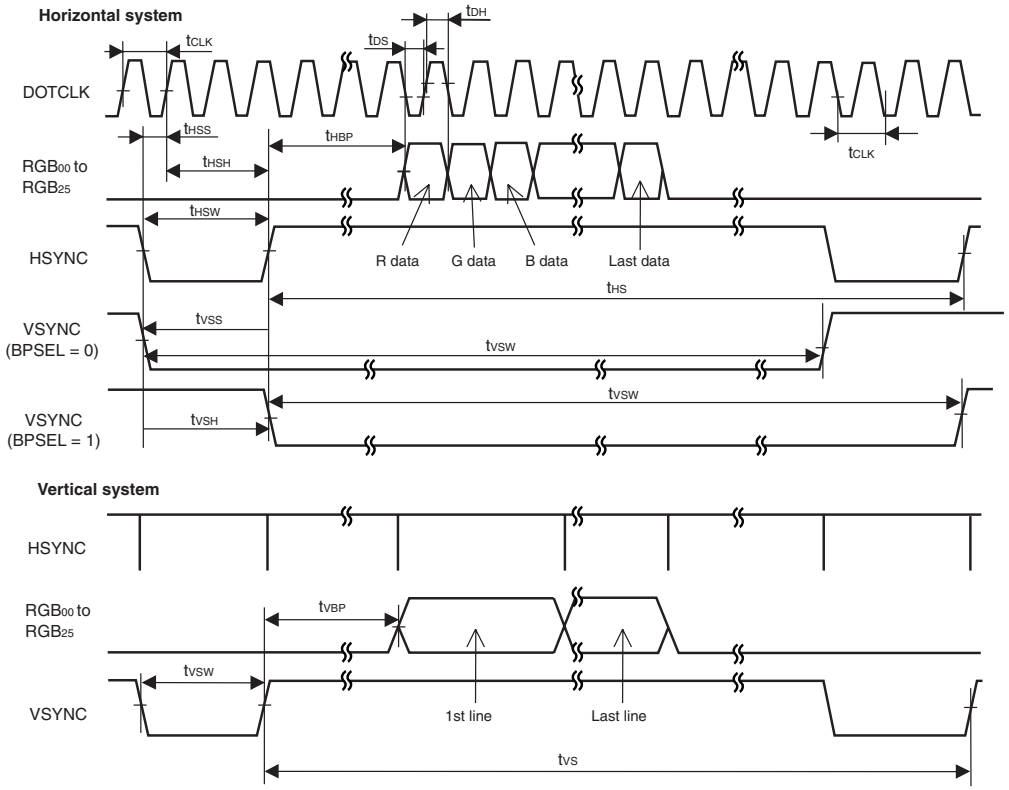
2. All timing data is specified at 20 to 80% of V_{CCIO}.

3. The DOTCLK number which should be inputted also at the lowest in 1 level period is as follows.
1 horizontal period DOTCLK number ≥ [DOTCLK number of HSYNC "L" in mode] + [Horizontal back porch period] + [Pixel display time 240 times] = 242

4. The HSYNC number which should be inputted also at the lowest in 1 level period is as follows.
1 frame period HSYNC number ≥ [HSYNC number of VSYNC "L" period mode] + [Vertical back porch period] + [Pixel display time 320 line] = 322

5. When use it by IF_SHARE = H in parallel I/F (PSX = L), use /CS, /RD (E) and /WR (R,/W) in non-active state.

<R> **(b) 6-bit RGB interface**



	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Dot clock cycle time	t_{CLK}		47			ns
	Dot clock high level pulse width	t_{CLKH}		24			ns
	Dot clock low level pulse width	t_{CLKL}		24			ns
	Data set-up time	t_{DS}		30			ns
	Data hold time	t_{DH}		10			ns
	HSYNC pulse width	t_{HSW}		3			DOTCLK
	HSYNC set-up time	t_{HSS}		20			ns
	HSYNC hold time	t_{HSH}		20			ns
	Horizontal period back porch time	t_{HBP}		3			DOTCLK
	VSYNC pulse width	t_{VSW}		1			H
<R>	VSYNC set-up time	t_{VSS}	BPSEL = 0	t_{HSW}			DOTCLK
<R>	VSYNC hold time	t_{VSH}	BPSEL = 1	t_{HSW}			DOTCLK
	Vertical period back porch time	t_{VBP}		1			H

Remarks 1. The rise and fall times (t_r, t_f) of an input signal are 15 ns or less.

2. All timing data is specified at 20 to 80% of V_{CCIO}.

3. The DOTCLK number which should be inputted also at the lowest in 1 level period is as follows.

1 horizontal period DOTCLK number ≥ [DOTCLK number of HSYNC "L" in mode] **Note1** + [DOTCLK number of horizontal back porch period] **Note2** + [Pixel display time 240 times x 3] +3 = 726

Notes 1. [DOTCLK number of HSYNC "L" in mode] = 3 multiple (3, 6, 9…)

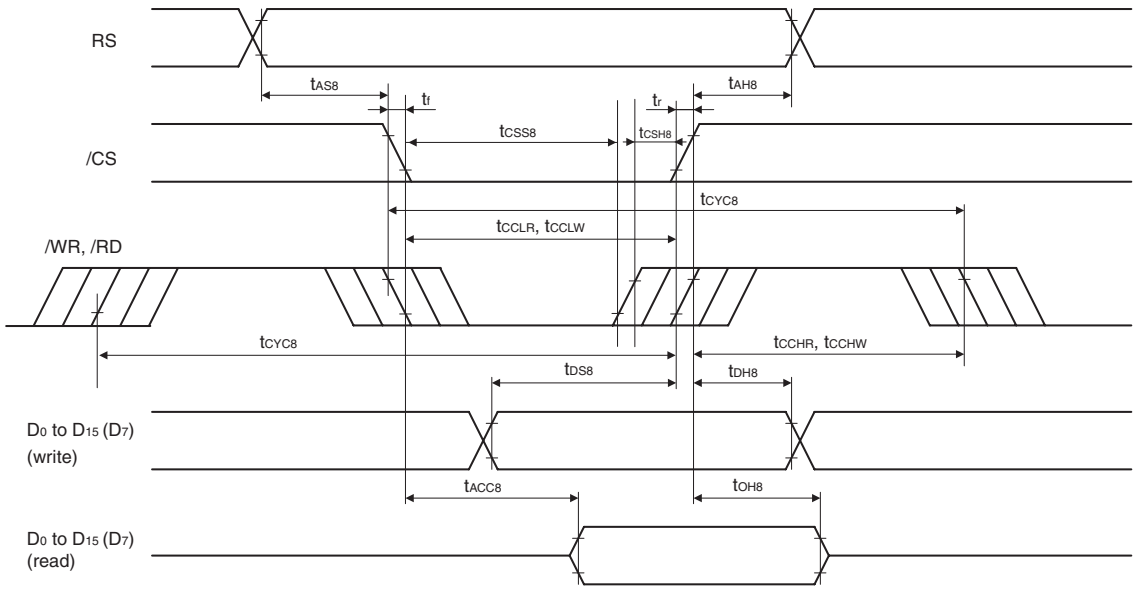
2. [DOTCLK number of horizontal back porch period] = 3 multiple (3, 6, 9…)

4. The HSYNC number which should be inputted also at the lowest in 1 level period is as follows.

1 frame period HSYNC number ≥ [HSYNC number of VSYNC "L" period mode] + [Vertical back porch period] + [Pixel display time 320 line] = 322

5. When use it by IF_SHARE = H in parallel I/F (PSX = L), use /CS, /RD (E) and /WR (R,/W) in non-active state.

(c) i80 CPU interface



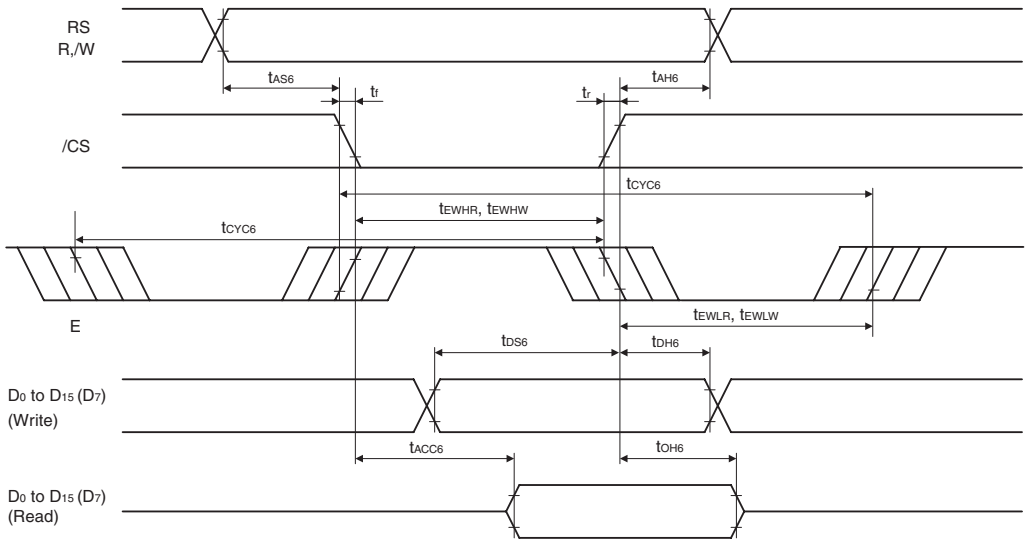
V_{DD} = 2.1 to 2.5 V (SFVSEL = 1), V_{CCIO} = 1.65 to 3.3 V

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Address hold time	t_{AH8}	RS		20			ns
Address set-up time	t_{AS8}	RS		0			ns
System cycle time	t_{CYC8}	Read		400			ns
		Write Horizontal writing (INC = 0)		60			ns
		Write Vertical writing (INC = 1)		100			ns
Control low level pulse width (/WR)	t_{CCLW}	/WR		25			ns
Control low level pulse width (/RD)	t_{CCLR}	/RD		200			ns
Control high level pulse width (/WR)	t_{CCHW}	/WR		25			ns
Control high level pulse width (/RD)	t_{CCHR}	/RD		80			ns
Data set-up time	t_{DS8}	D0 to D17		40			ns
Data hold time	t_{DH8}	D_0 to D_{17}		0			ns
CS set-up time	t_{CSS8}	CS	$V_{CCIO} \geq 2.55$ V	35			ns
			$V_{CCIO} < 2.55$ V	75			ns
CS hold time	t_{CSH8}	CS		0			ns
/RD access time	t_{ACC8}	D0 to D17, C_L = 100 pF				200	ns
Output disable time	t_{OH8}	D0 to D17				100	ns

<R> **Remarks 1.** The rise and fall times (t_r, t_f) of an input signal are 15 ns or less. It is prescribed by ($t_r + t_f$) < (t_{CYC8}–t_{CCLR}–t_{CCHR}) or ($t_r + t_f$) < (t_{CYC8}–t_{CCLW}–t_{CCHW}) the case where system cycle time is used at high speed.

2. All timing data is specified at 20 to 80% of V_{CCIO}.

(d) M68 CPU interface



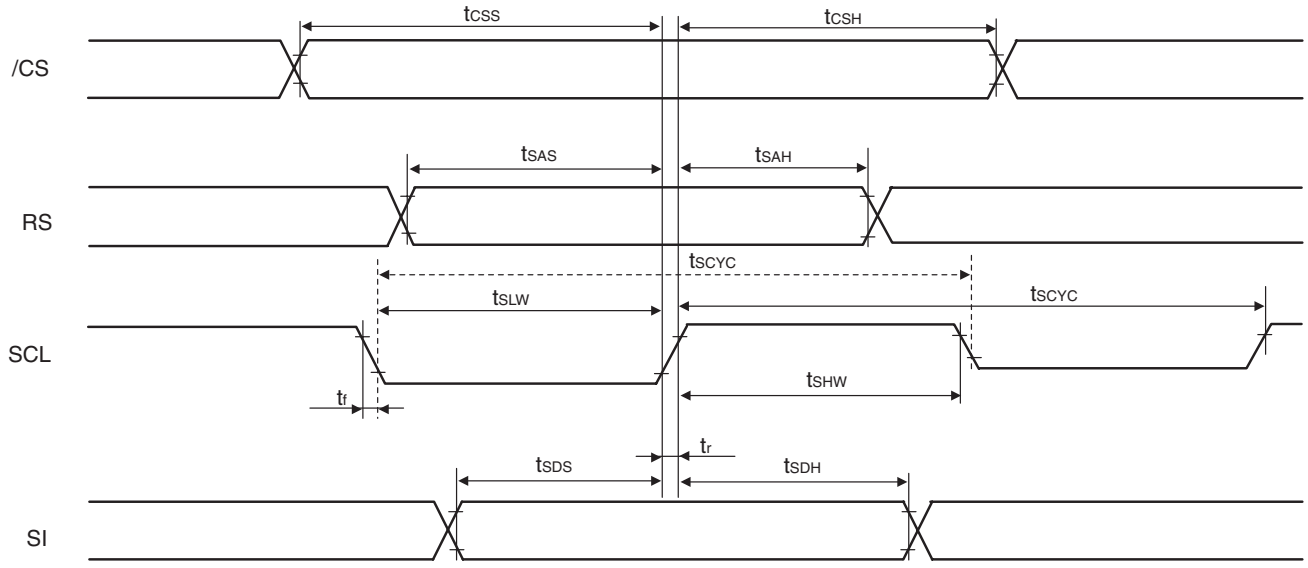
V_{DD} = 2.1 to 2.5 V (SFVSEL = 1), V_{CCIO} = 1.65 to 3.3 V (Normal write mode)

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit
Address hold time		t_{AH6}	RS		20			ns
Address set-up time		t_{AS6}	RS		0			ns
System cycle time		t_{CYC6}	Read		400			ns
			Write (V_{DD} > 2.0 V) Horizontal writing (INC = 0)		60			ns
			Write (V_{DD} > 2.0 V) Vertical writing (INC = 1)		100			ns
Data set-up time		t_{DS6}	D0 to D17		40			ns
Data hold time		t_{DH6}	D0 to D17		0			ns
CS set-up time		t_{CSS6}	CS	$V_{DDIO} \geq 2.55$ V	40			ns
				V_{DDIO} < 2.55 V	75			ns
CS hold time		t_{CSH6}	CS		0			ns
Access time		t_{ACC6}	D0 to D17, C_L = 100 pF				200	ns
Output disable time		t_{OH6}	D0 to D17				100	ns
Enable high level pulse width	Read	t_{EWHR}	E		200			ns
	Write	t_{EWHW}	E		25			ns
Enable low level pulse width	Read	t_{EWLR}	E		80			ns
	Write	t_{EWLW}	E		25			ns

Remarks 1. The rise and fall times (t_r, t_f) of an input signal are 15 ns or less. It is prescribed by ($t_r + t_f$) < (t_{CYC6}–t_{EWLR}–t_{EWHR}) or ($t_r + t_f$) < (t_{CYC6}–t_{EWLW}–t_{EWHW}) the case where system cycle time is used at high speed.

2. All timing data is specified at 20 to 80% of V_{CCIO}.

(e) Serial interface (between CPU and μPD161704A)



V_{DD} = 2.1 to 2.5 V, V_{CCIO} = 1.65 to 3.3 V

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	66			ns
SCL high level pulse width	t_{SHW}	SCL	20			ns
SCL low level pulse width	t_{SLW}	SCL	20			ns
Address hold time	t_{SAH}	RS	20			ns
Address set-up time	t_{SAS}	RS	10			ns
Data set-up time	t_{SDS}	SI	10			ns
Data hold time	t_{SDH}	SI	20			ns
CS – SCL time	t_{ACCS}	/CS	20			ns
	t_{OHS}	/CS	20			ns

Remarks 1. The rise and fall times (t_r, t_f) of an input signal are 15 ns or less.

2. All timing data is specified at 20 to 80% of V_{CCIO}.

(f) Common

Parameter	Symbol	Condition	MIN.	TYP. Note1	MAX.	Unit
Calibration setting time (frame frequency)	t_{CAL1} (f_{FRAME0})	**Note2,** f_{FRAME} = 60 Hz		51.60 (60)		μs (Hz)
Frame frequency	f_{FRAME1}	Before calibrate, OSCSEL = L (use of internal oscillation)	35	60	96	Hz
		Before calibrate, OSCSEL = H (use of external oscillation), R = 24 kΩ	47	60	67	Hz
	f_{FRAME2}	Calibrated Note3 T_A = –40 to +85°C, OSCSEL = L	40	60	80	Hz
		Calibrated Note3 T_A = –40 to +85°C OSCSEL = H, R = 24 kΩ	51	60	67	Hz
	f_{FRAME3}	Calibrated Note4 T_A = 25 ± 5°C, OSCSEL = L	55	60	65	Hz
		Calibrated Note4 T_A = 25 ± 5°C OSCSEL = H, R = 24 kΩ	57	60	63	Hz
Oscillation frequency	f_{OSC1}	OSCSEL = L	0.69	1.16	1.86	MHz
	f_{OSC2}	OSCSEL = H, R = 24 kΩ Note5	0.92	1.16	1.28	MHz
Reset pulse width	t_{RW}		10			μs
Reset un-reacted pulse width	t_{ET}				2	μs

Notes 1. TYP. values are reference values when V_{DD} = 2.3 V, V_{CCIO} = 2.8 V, V_{DC} = 2.8 V, T_A = 25°C.

2. The relationship between the frame frequency (f_{FRAME}) and the calibration setting time is as follows.

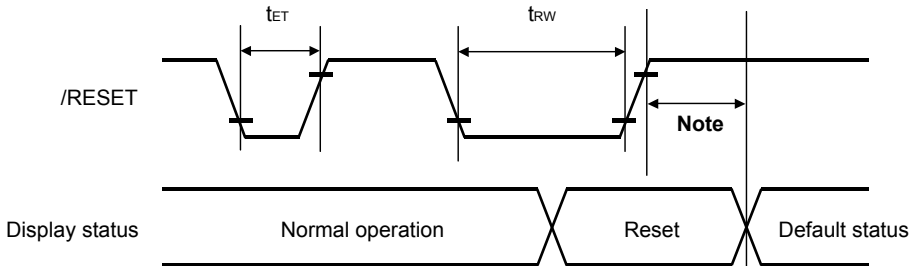
$$t_{cal} = 1 / (f_{FRAME} \times (320 + 3))$$

3. Measured at T_A = –40 to +85°C, after calibration at frame frequency = 60 Hz, T_A = 25°C exactly.

4. Measured at ±5°C, after calibration at frame frequency = 60 Hz exactly.

<R> **5.** Frequency changes by the parasitism capacity to which it is connected with OSCIN pin at the time of external resistance mode. (R = 24 kΩ) is obtained as a reference value, in case use it, sufficient evaluation is carried out, and please determine the resistance to be used. The recommendation resistance value which uses general module is 36 kΩ.

Figure 12–1. /RESET Specification



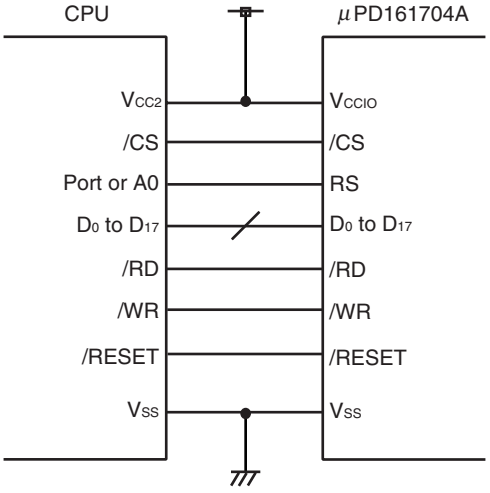
Note Secure recovery time more than 10 μs after reset release.

13. EXAMPLE OF μPD161704A AND CPU CONNECTION

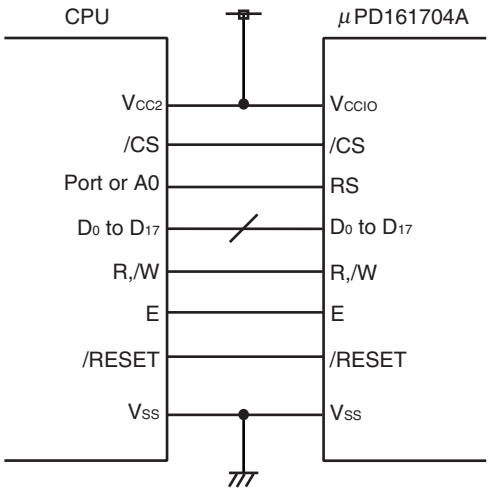
Examples of μPD161704A and CPU connection are shown below.

In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

(1) i80 series format



(2) M68 series format



14. REVISION HISTORY

Edition/ Date	Page		Description	
	Previous edition	This edition	Type of revision	Location
1.0 edition/ May, '05			New	From the μPD161704 preliminary product information 2.7 version change product name.
1.1 edition/ June, '05	p.45	p.45	Added	The figure about a back porch is added.
	p.157, 158	p.157, 158	Added	Spec. item addition
1.2 edition/ June, '05	p.107	p.107	Corrected	V_{GH}: 0.47 to 1 F are corrected to 0.47 to 1.
	p.133	p.133	Corrected	D7 to D0 of R44 is corrected to D8 to D0.
	p.136	p.136	Corrected	"5.8 γ-curve Correction Circuit" is corrected to 5.5.
	p.150	p.150	Corrected	"5.8 γ-curve Correction Circuit" is corrected to 5.5.
PPI → DS 1.0 edition/ September, '05	p.24	p.24	Added	Notes 2 is added.
	p.118	p.118	Corrected	Explanation of R103 is corrected.
	p.120	p.120	Corrected	Explanation of R30 is corrected.
	p.137	p.137	Corrected	Explanation of R103 is corrected.
	p.142	p.142	Corrected	Explanation of R30 is corrected.
	p.154	p.154	Corrected	The MIN. value of the VCOMM output voltage range is corrected.
	p.155, 156	p.155, 156	Added	Remarks 3 is added.
	p.157	p.157	Corrected	t_{CYC8} (write, inc = 0) and t_{CCLR} are corrected.
	p.158	p.158	Corrected	t_{CYC6} (write, inc = 0) and t_{EWHR} are corrected.
	p.159	p.159	Corrected	t_{SAH} and t_{SDH} are corrected to 10 ns → 20 ns.
	p.160	p.160	Added	Notes 5 is added.
1.1 edition/ October, '05	p.65	p.65	Corrected	Description is corrected
	p.66	p.66	Corrected, added	Add and correct figure of γ-curve correction circuit
	p.82	p.83	Corrected	N line inversion in figure is corrected.
	p.105	p.106	Corrected	Formula on VCOMLM and example of $VCOM_{p-p}$
	p.115 to 121	p.116 to 124	Corrected	Test register, DINV to register mode 1, 2, and other modifications
	p.125	p.128	Added	DINV bit
	All	All	Corrected	Misspelling and so
2.0 edition/ March, '06	p.18, 92	p.18, 92	Corrected	ESK in description
	p.20	p.20	Corrected	3.4 Test or Other Pins
	p.26	p.26	Corrected	Table 5–3
	p.44	p.44	Added	Figure 5–24
	p.50	p.50	Added	VSYNC interface mode
	p.93	p.93	Corrected	Register number in 6.2 Each Operation
	–	p.106	Added	7.8.7 VGM Regulator selection output
	–	p.120	Added	10. POWER SUPPLY INJECTION/INTERCEPTION ORDER
	p.122 to 128	p.122 to 128	Corrected	11.1 Command List (Register mode 1 to 4)
	p.134, 141, 148	p.135, 142, 149	Corrected	Command description
	p.140, 147	p.141, 148	Added	HBPn, VBPn setting method
	p.162	p.163	Corrected	(a) 16-bit/18-bit RGB interface table and figure
	p.163	p.164	Corrected	(b) 6-bit RGB interface
	p.167	p.168	Corrected	Part of notes 5 is corrected

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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  The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)
(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).