

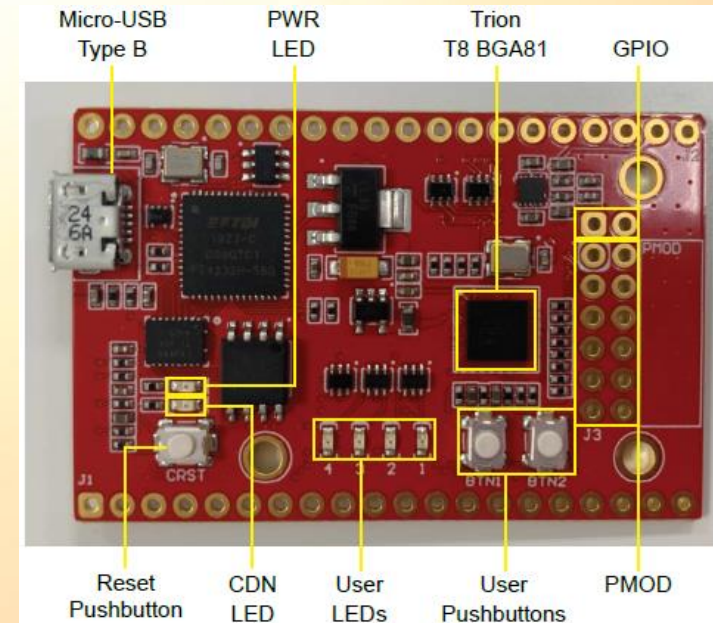


Accelerating Your Innovation

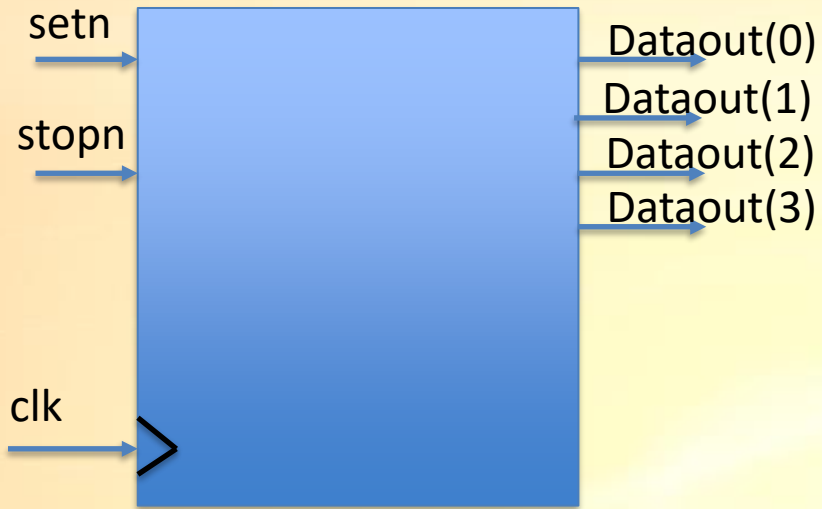
Trion Xyloni T8 LAB

By Harald Werner

Version: 1.0.0

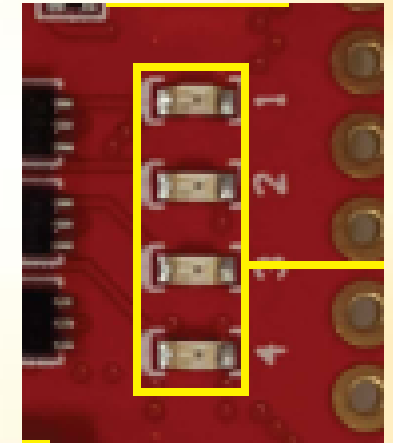
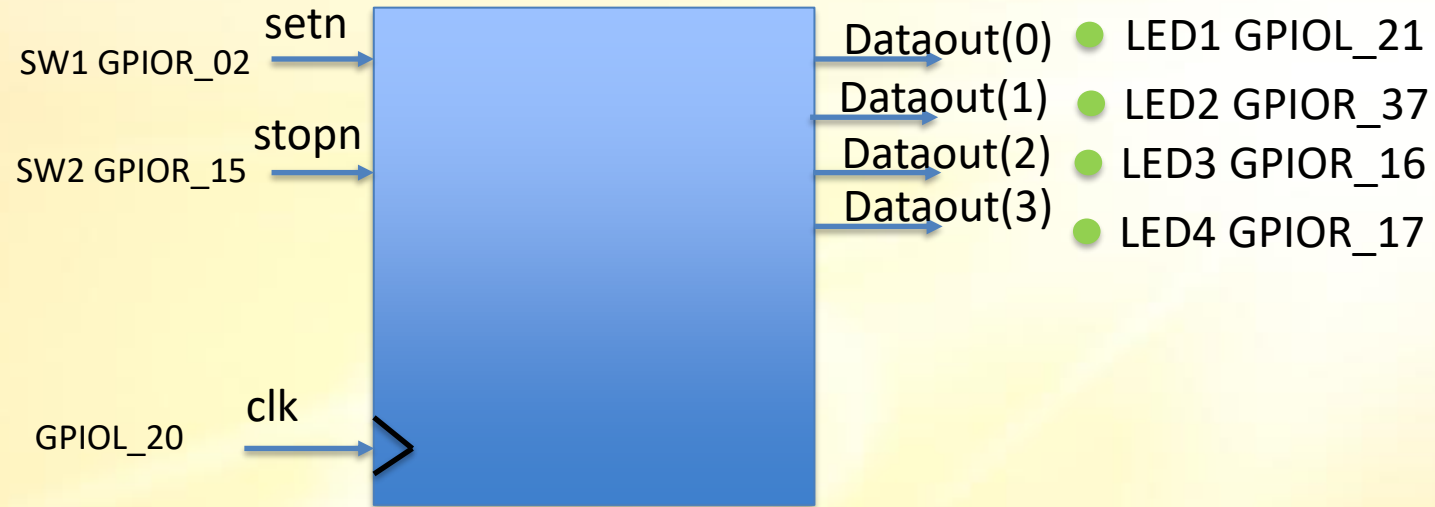


Design (simple up counter with set and stop)

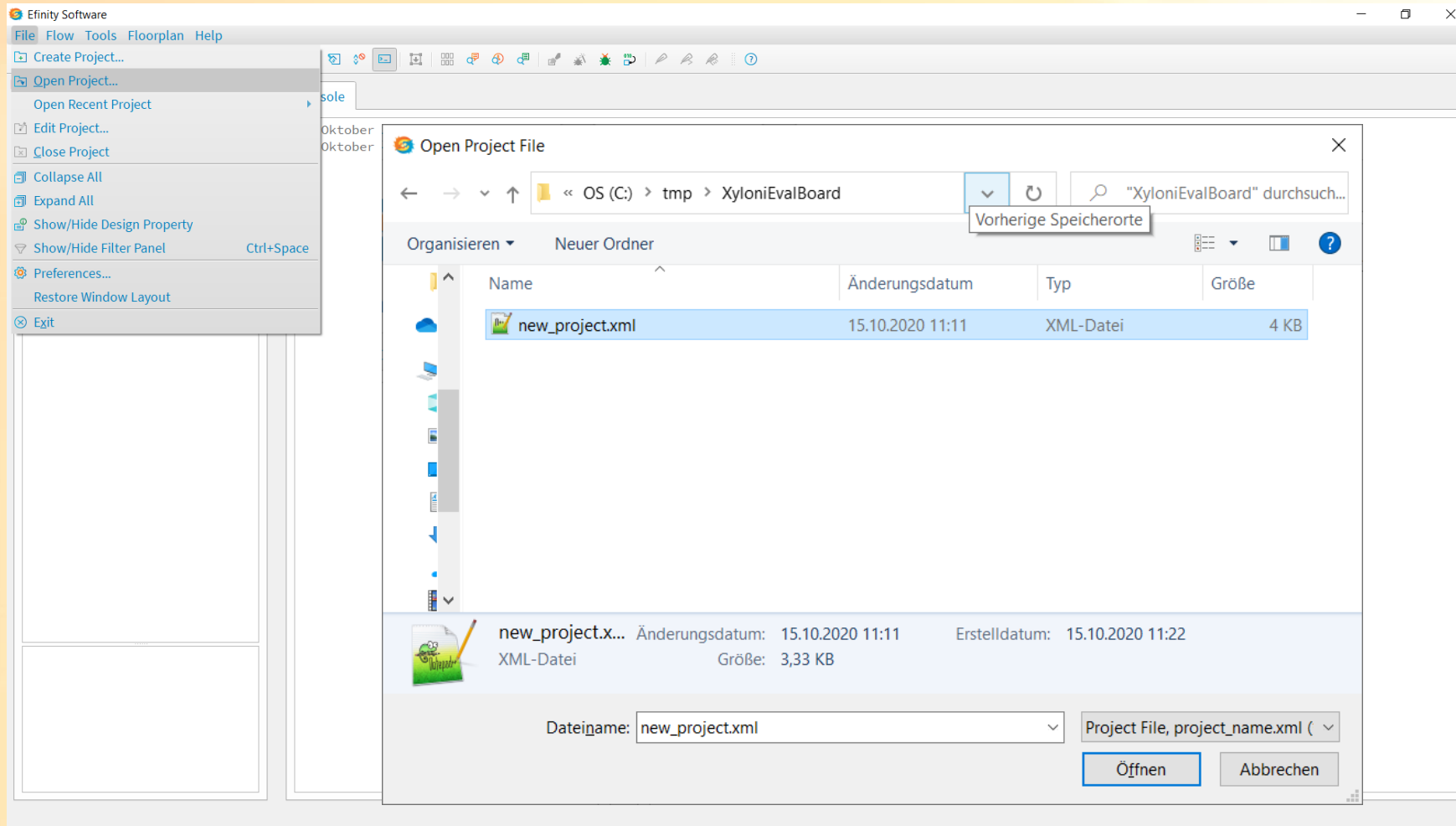


```
Code Editor
counter.vhd x
1 -- smal example design for the Xyloni Efinix Eval Board
2 -- By Harald Werner
3 -- 15.10.2020
4 library ieee;
5 use ieee.std_logic_1164.all;
6 use ieee.std_logic_unsigned.all;
7
8 entity counter is
9 port ( clk      : in std_logic;           -- clock input. Could be from internal osc (T8) or from the external 33.3MHz clock use GPIOL_20
10       setn     : in std_logic;           -- Set signal, low active; sett all outputs to '1' (LED are high active, means all LEDs msut be ON) GPIOR_02
11       stopn    : in std_logic;           -- Stop signal, low active Stop counting GPIOR_15
12       Dataout   : out std_logic_vector(3 downto 0)); -- Output data connected to the LEDs (low high); GPIOR_17,GPIOR_16,GPIOLR37,GPIOL_21
13 end counter;
14
15 architecture vers1 of counter is
16 signal cnt: std_logic_vector ( 29 downto 0) := (others => '0');
17 begin
18 cnt_proc : process(clk, setn)
19 begin
20     if setn = '0' then
21         cnt <= (others => '1');
22         dataout <= (others => '1');
23     elsif clk'event and clk = '1' then
24         if stopn = '0' then
25             cnt <= cnt;
26         else
27             cnt <= cnt +1;
28         end if;
29         Dataout <= cnt(17 downto 14); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
30         Dataout <= cnt(29 downto 26); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
31     end if;
32 end process;
```

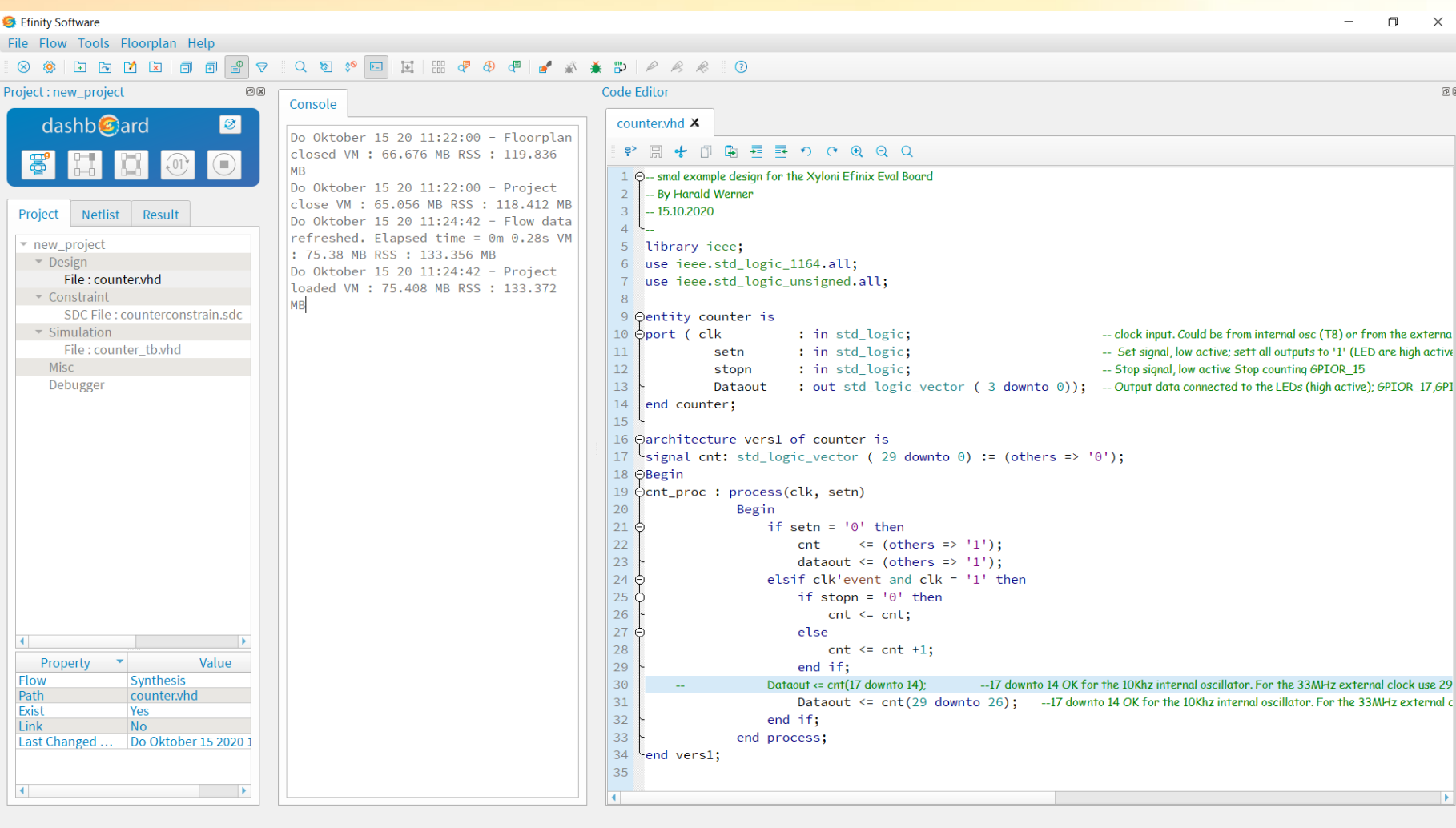
Design / Board connection



1. Open Efinity new_project.xml

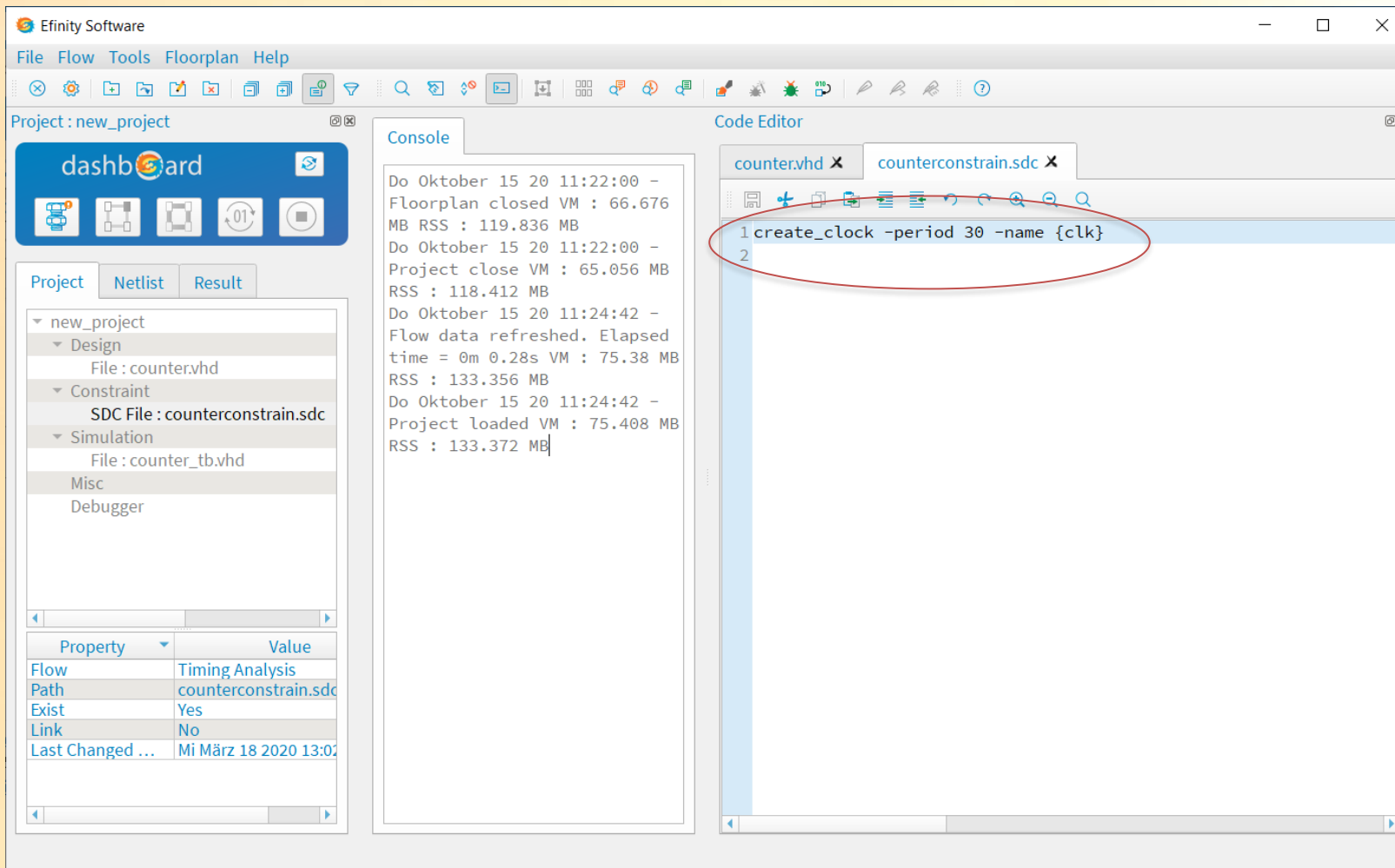


Double click on counter.vhd



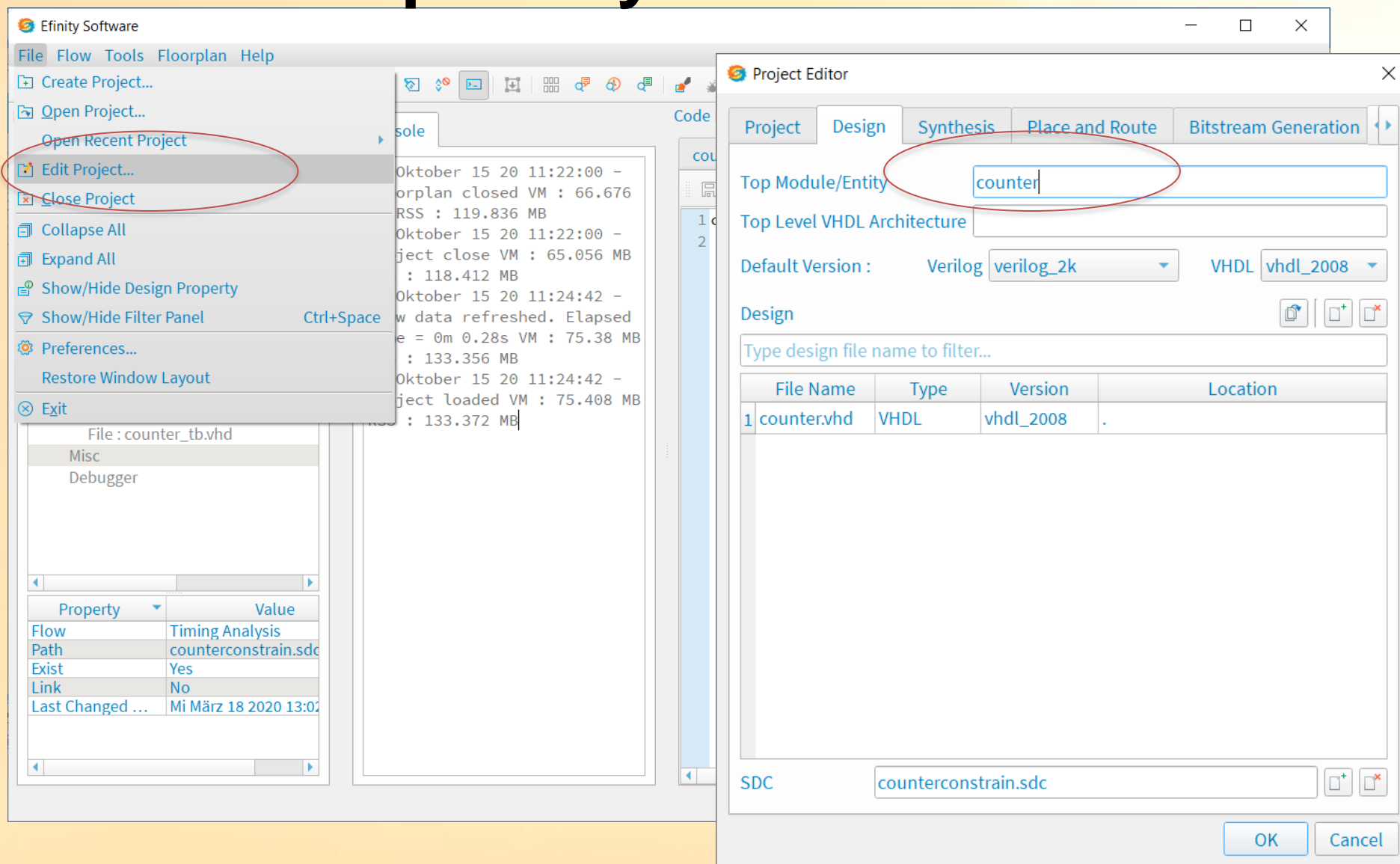
- The counter.vhd will show up in the Code Editor

Double click on the timing constrain counterconstrain.sdc



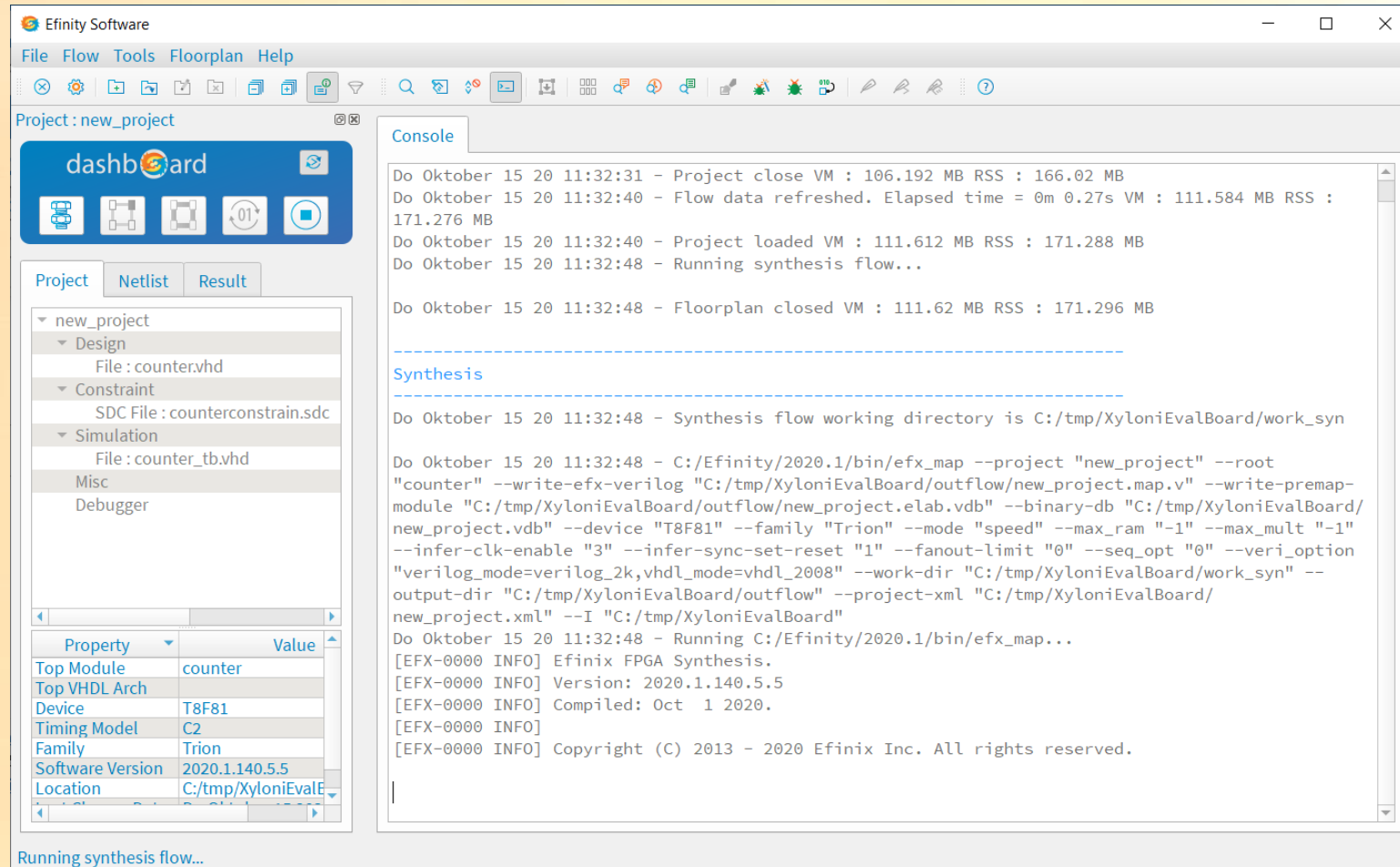
The counterconstrain.sdc will show up and you can see the 30ns period constrain for the 33MHz clock



Set the top entity name




Enter counter
to top
Module/Entity
and click OK

Run the whole flow or just Synthesis



- If the Automated flow button is grayed out  click on the button to activate the automated flow. 

- Click on the synthesis icon and the flow will run automatically 

Assign the top level Signals to Pins.

1. Open Interface Designer

The screenshot displays the Efinity Software interface. The top menu bar includes 'File', 'Flow', 'Tools', 'Floorplan', and 'Help'. Below the menu is a toolbar with various icons. The main workspace is divided into three panels: 'Project: new_project' on the left, 'Console' in the center, and 'Code Editor' on the right.

The 'Project: new_project' panel shows a 'dashboard' with icons for 'Interface', 'Simulation', 'Synthesis', 'Placement', 'Routing', 'Bitstream', and 'Debugger'. The 'Synthesis' tab is selected, showing a list of synthesis steps: 'Interface', 'Simulation', 'Synthesis', 'Placement', 'Routing', 'Bitstream', and 'Debugger'.

The 'Console' panel displays the following output:

```
processing end (Real time : 0s)
INFO: ***** Beginning VDB Netlist Checker ... *****
INFO: VDB Netlist Checker took 0.0198807 seconds.
INFO: VDB Netlist Checker took 0.02 seconds (approximately) in total CPU time.
INFO: VDB Netlist Checker virtual memory usage: begin = 38.3 MB, end = 38.3 MB, delta = 0 MB
INFO: VDB Netlist Checker peak virtual memory usage = 103.848 MB
INFO: VDB Netlist Checker resident set memory usage: begin = 45.068 MB, end = 45.1 MB, delta = 0.032 MB
INFO: VDB Netlist Checker peak resident set memory usage = 64.852 MB
INFO: ***** Ending VDB Netlist Checker ... *****
-- Writing netlist 'counter' to Verilog file 'C:/tmp/XyloniEvalBoard/outflow/new_project.map.v' (VDB-1030)
[EFX-0000 INFO] Resource Summary
[EFX-0000 INFO] =====
[EFX-0000 INFO] EFX_ADD      :      29
[EFX-0000 INFO] EFX_FF       :      34
[EFX-0000 INFO] EFX_GBUFCE   :       1
[EFX-0000 INFO] =====
Do Oktober 15 20 11:31:42 - C:/Efinity/2020.1/bin/efx_map finished. Exit code = 0 Exit status : Normal
Running synthesis flow done.
Do Oktober 15 20 11:31:42 - Flow data refreshed. Elapsed time = 0m 0.30s VM : 114.004 MB RSS : 171.044 MB
Do Oktober 15 20 11:31:42 - Running synthesis flow done. Duration = 0m 3.249s
```

The 'Code Editor' panel is currently empty.

At the bottom of the interface, a status bar indicates: 'Running synthesis flow done. Duration = 0m 3.249s'.

Show GPIO Resource Assigner

The screenshot displays the Efinity Interface Designer software interface. The main window is titled "Efinity Interface Designer - new_project". The "Resource Assigner" panel is active, showing a table with columns: Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, Clock Region, and Package. A tooltip "Show/Hide GPIO Resource Assigner" is visible over the Resource Assigner icon. The "Design Explorer" panel on the left shows a tree view with "Design : T8F81" expanded, showing "Device Setting" and "I/O Banks (5)". The "Design Summary" panel on the right shows a table with properties and values.

Property	Value
1 Name	new_project
2 Device	T8F81
3 Package	81-ball FBGA
4 Timing Model	C2
5 Location	C:\tmp\XyloniEvalBoard
6 Version	2020.1.140.5.5
7 Last Change Date	Thu Oct 15 11:33:18 2020
8 Database Version	20201999

Select GPIO, RMB, Create Bus

The screenshot displays the Efinity Interface Designer software interface for a new project. The main window is titled "Efinity Interface Designer - new_project". The top menu bar includes "File", "Design", "Report", and "Help". Below the menu is a toolbar with various icons for file operations and design actions.

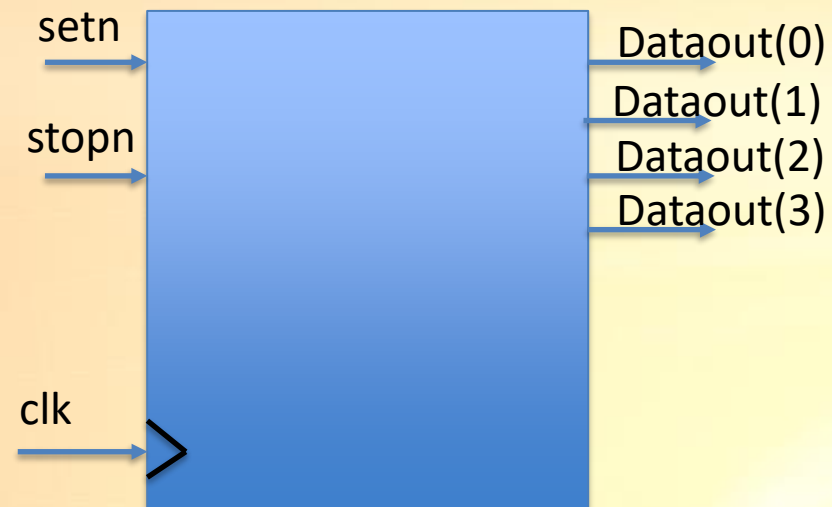
The interface is divided into several panels:

- Resource Assigner:** This panel is currently showing the "GPIO : Instance View". It contains a table with columns: Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, Clock Region, and Pad. The table is currently empty.
- Design Explorer:** This panel on the left shows a tree view of the project structure. Under "Design : T8F81", there is a "Device Setting" folder which contains "I/O Banks (5)". A right-click context menu is open over "GPIO (0)", with options: "Create Block", "Create Bus" (highlighted), "Expand All", and "Collapse All".
- Block Summary:** This panel shows a table of properties and values for the selected block. It has two rows:

Property	Value
1 Global Unused Setting	
2 State	input with weak pullup
- Block Editor:** This panel on the right shows the configuration for the selected block. It has a section titled "Unused State" with a dropdown menu currently set to "input with weak pullup".

At the bottom left, there is a button labeled "Add bus instance".

Create a Output BUS Dataout(3 downto 0)



A screenshot of a software dialog box titled 'Add New Bus'. The dialog has a title bar with a question mark and a close button. Inside, there is a back arrow and a pencil icon. The fields are as follows:
Name: A text box containing 'Dataout'.
MSB: A text box containing '3'.
LSB: A text box containing '0'.
Mode: A dropdown menu with 'input', 'output' (highlighted in blue), and 'inout' options.
I/O Stand: A dropdown menu with 'input' and 'inout' options.
At the bottom right, there are 'Next' and 'Cancel' buttons.

Name: Dataout

MSB: 3

LSB: 0

Mode: output

Click Next

Set drive strength to 3; click Next

?

×

← Add New Bus

Output

Pin Name

Dataout

Register Option

none

Drive Strength (1-weakest, 4-strongest)

1

2

3


4

Next

Cancel

Click Finish

? ×

←  Add New Bus

A new bus will be created with these properties

	Property	Value
1	Bus Name	Dataout
2	MSB	3
3	LSB	0
4	Mode	output
5	I/O Standard	3.3V LVTTTL / LVCMOS
6	Output	
7	Pin Name	Dataout
8	Constant Output	none
9	Drive Strength	3
10	Enable Slew Rate	false
11	Register Option	none

Finish Cancel

Adding the additional Pins clk, stopn, setn

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[0]							
Dataout[1]							
Dataout[2]							

Design Explorer

Type and press Enter to search...

Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (4)**
 - Dataout [3:0]**
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Create Block
Create Bus
Expand All
Collapse All

Block Summary

Property	Value
1 Global Unused Setting	
2 State	input with weak pullup

Block Editor

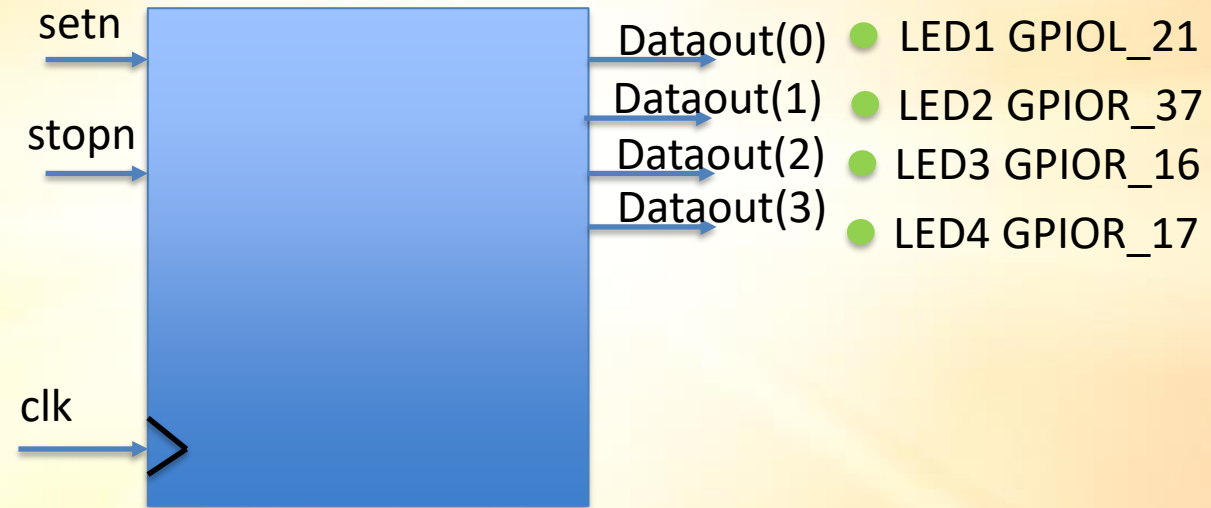
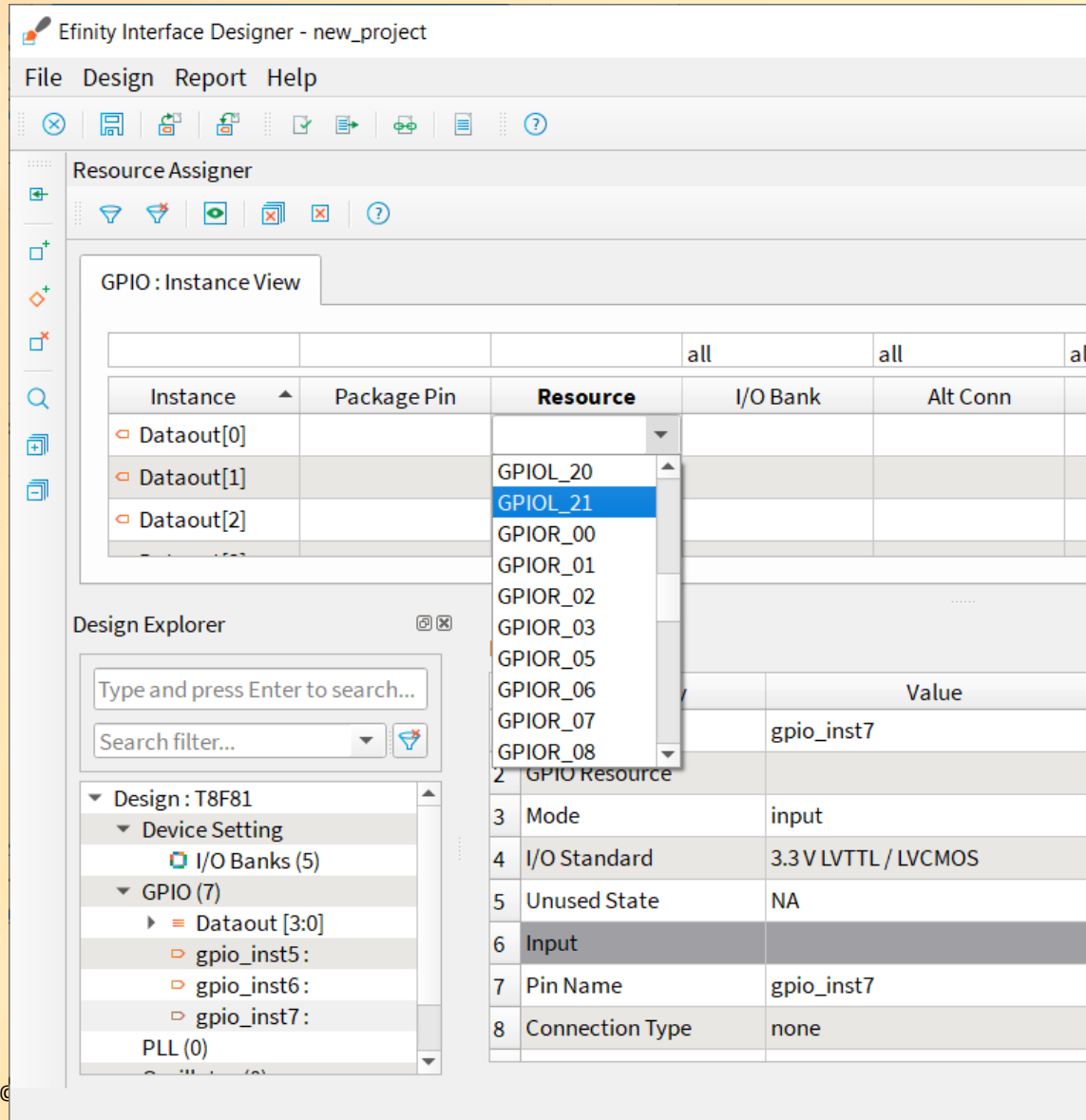
Unused State

input with weak pullup

Add periphery block instance

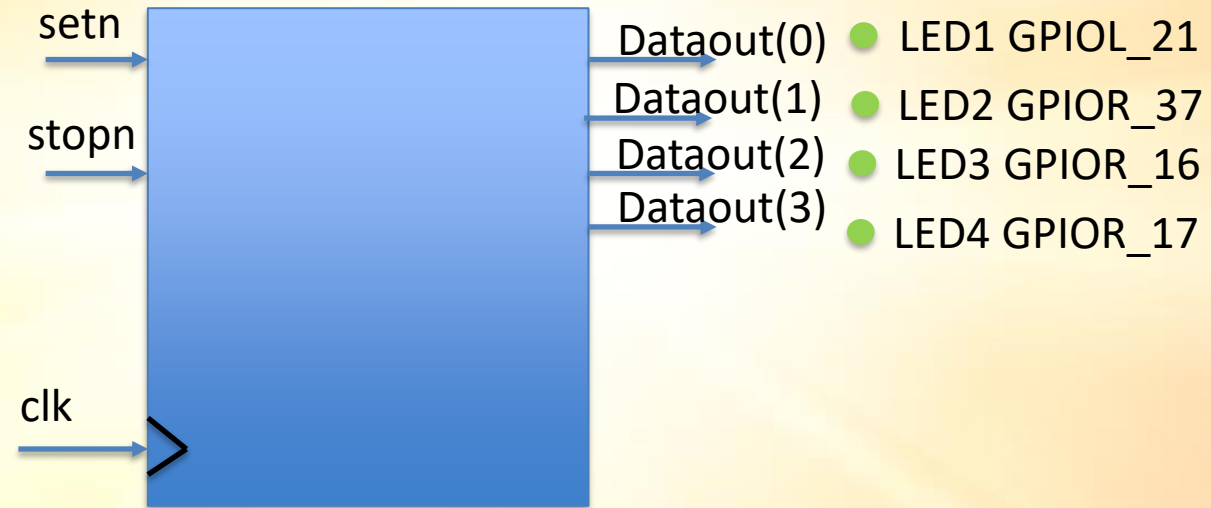
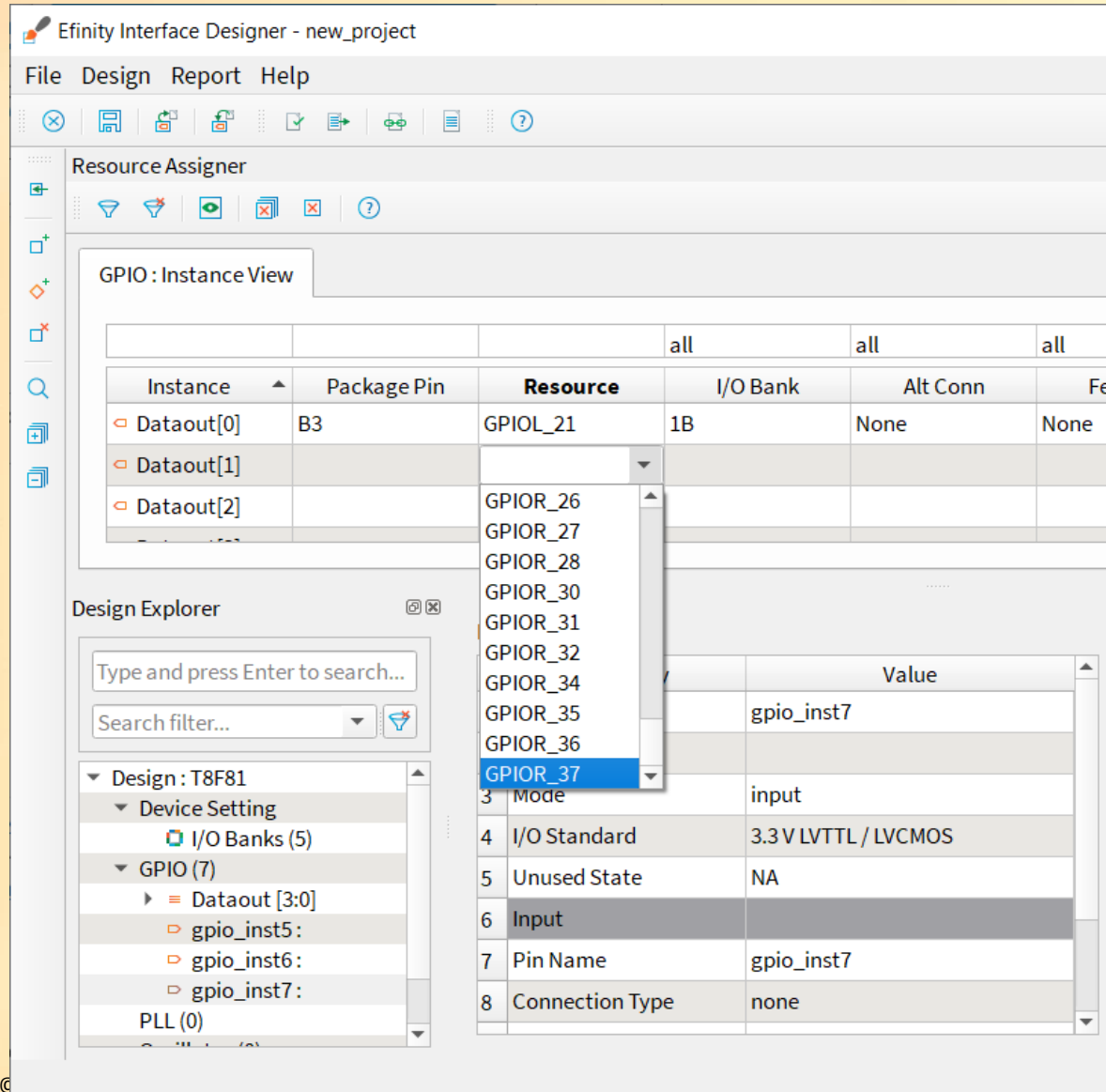
Select GPIO
Create Block
Select GPIO
Create Block
Select GPIO
Create Block

Select GPIO: Instance View Dataout[0]->Resource



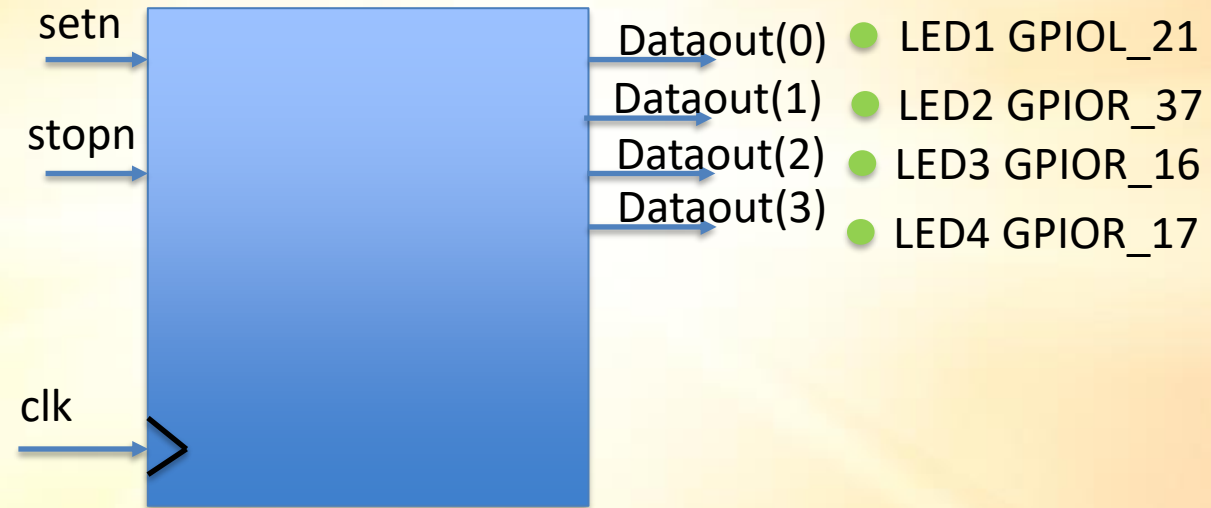
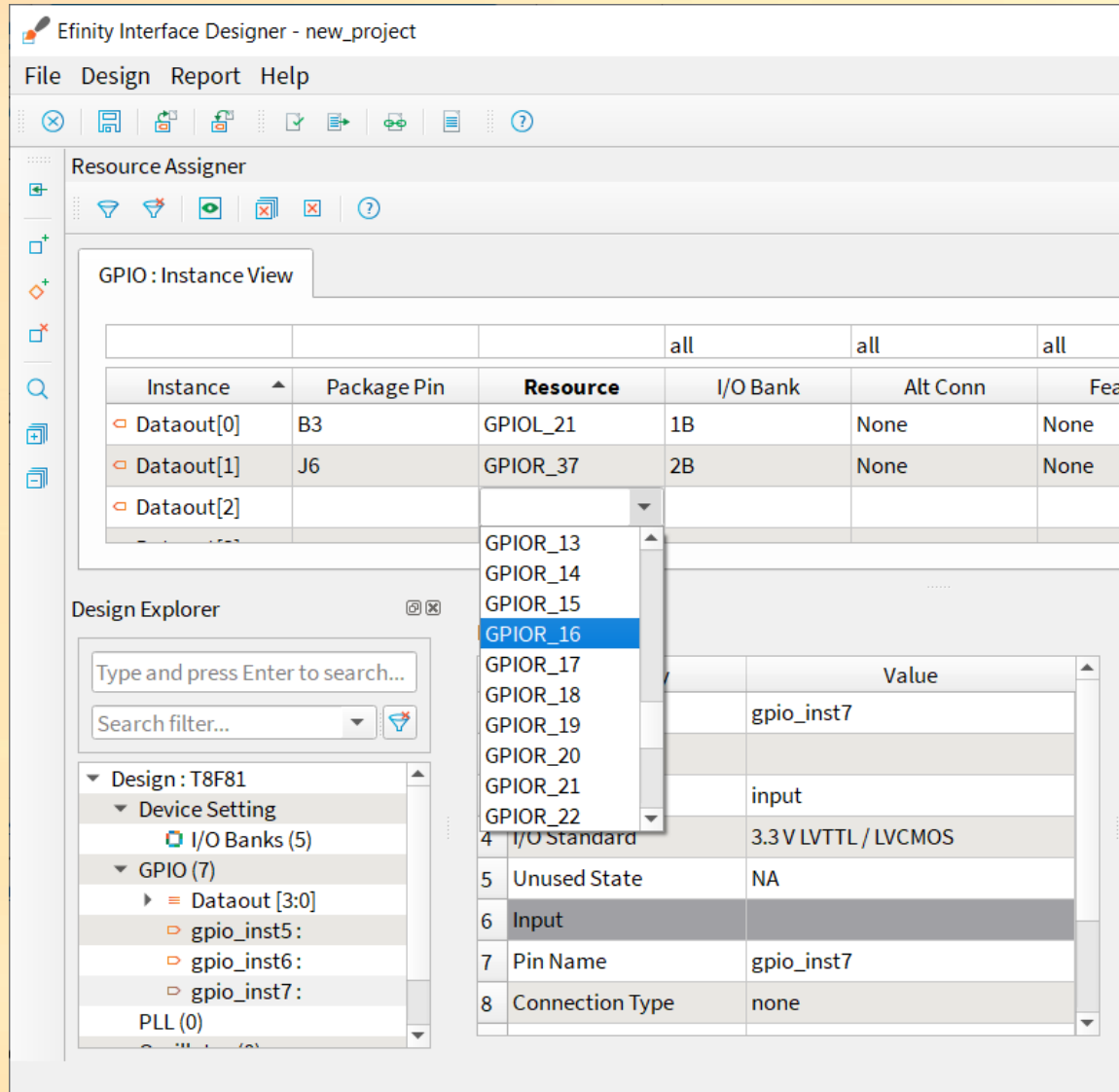
Dataout[0] ->GPIO_L_21

Select GPIO: Instance View Dataout[1]->Resource



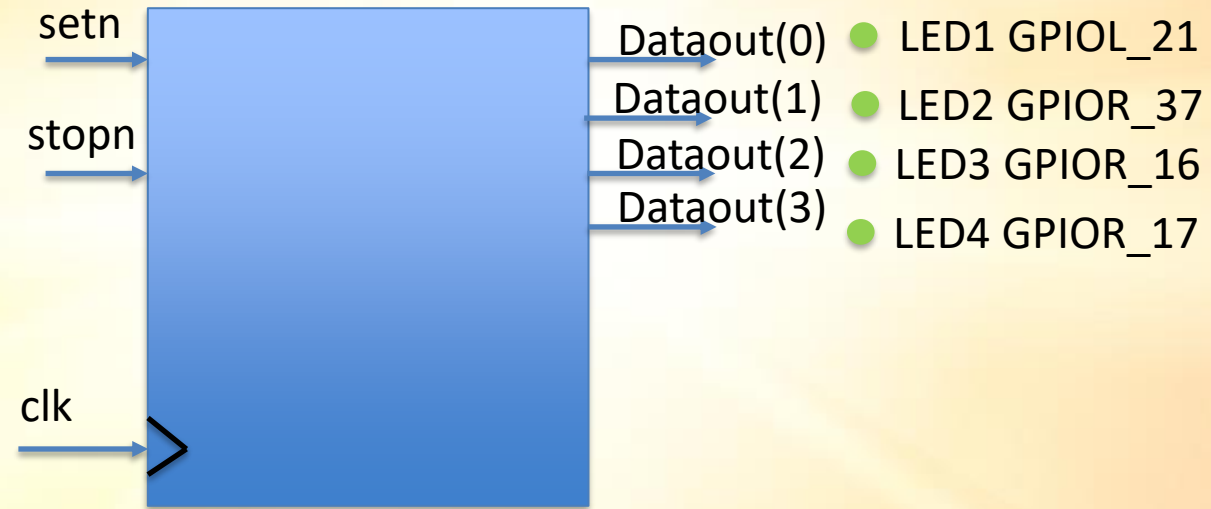
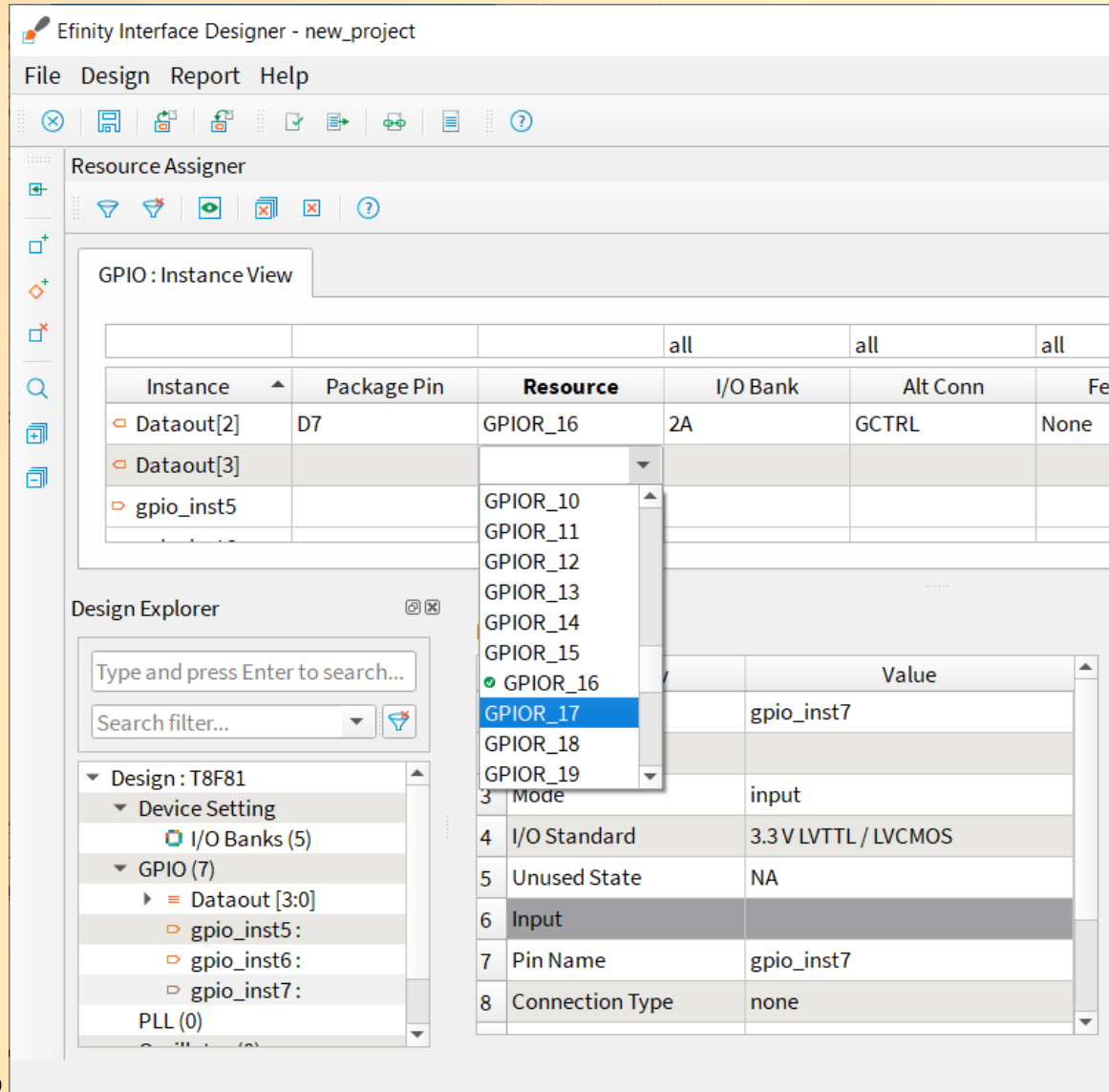
Dataout[1] ->GPIOR_37

Select GPIO: Instance View Dataout[2]->Resource



Dataout[2] ->GPIOR_16

Select GPIO: Instance View Dataout[3]->Resource



Dataout[3] -> GPIOR_17

Change the name from the remaining Inputs: clk

Select gpio_inst5
Enter name in the
Block Editor clk
and press enter !

The screenshot shows the Efinity Interface Designer interface with the following components:

- Resource Assigner (GPIO : Instance View):** A table listing GPIO instances. The instance `gpio_inst5` is highlighted.
- Design Explorer:** A tree view on the left showing the project structure. The `gpio_inst5` instance is highlighted under the `GPIO (7)` folder.
- Block Summary:** A table showing properties for the selected instance. The `Instance Name` property is highlighted with a red circle.
- Block Editor:** A panel on the right showing the configuration for the selected instance. The `Instance Name` field is highlighted with a red circle and contains the text `clk`.

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[2]	D7	GPIOR_16	2A	GCTRL	None	R1	GPIOR_16_CTRL7_CBUS1
Dataout[3]	D8	GPIOR_17	2A	GCTRL	None	R1	GPIOR_17_CTRL6_CBUS2
gpio_inst5							

Property	Value
1 Instance Name	gpio_inst5
2 GPIO Resource	
3 Mode	input
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	gpio_inst5
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false

Property	Value
Instance Name	clk
Mode	gpio_inst5
I/O Standard	3.3 V LVTTTL / LVCMOS
Input	
Pin Name	gpio_inst5
Connection Type	none

setn

The screenshot shows the Efinity Interface Designer interface with the following components:

- Resource Assigner (GPIO : Instance View):** A table showing GPIO instances and their resource assignments.
- Design Explorer:** A tree view showing the project structure, with `gpio_inst6` highlighted.
- Block Summary:** A table listing properties for the selected block.
- Block Editor:** A form for configuring the block's properties.

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[3]	D8	GPIOR_17	2A	GCTRL	None	R1	GPIOR_17_CTRL6_CBUS2
clk							
gpio_inst6							

Property	Value
1 Instance Name	gpio_inst6
2 GPIO Resource	
3 Mode	input
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	gpio_inst6
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false

Instance Name	setn
Mode	input
I/O Standard	3.3 V LVTTTL / LVCMOS
Input	
Pin Name	gpio_inst6
Connection Type	none

Select gpio_inst6
Enter name in the
Block Editor setn
and press enter !

stopn

The screenshot shows the Efinity Interface Designer interface. The **Resource Assigner** panel at the top displays the **GPIO : Instance View** table:

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[3]	D8	GPIOR_17	2A	GCTRL	None	R1	GPIOR_17_CTRL6_CBUS2
clk							
gpio_inst7							

The **Design Explorer** panel on the left shows the project hierarchy for **Design : T8F81**. The **GPIO (7)** folder is expanded, and **gpio_inst7 :** is circled in red.

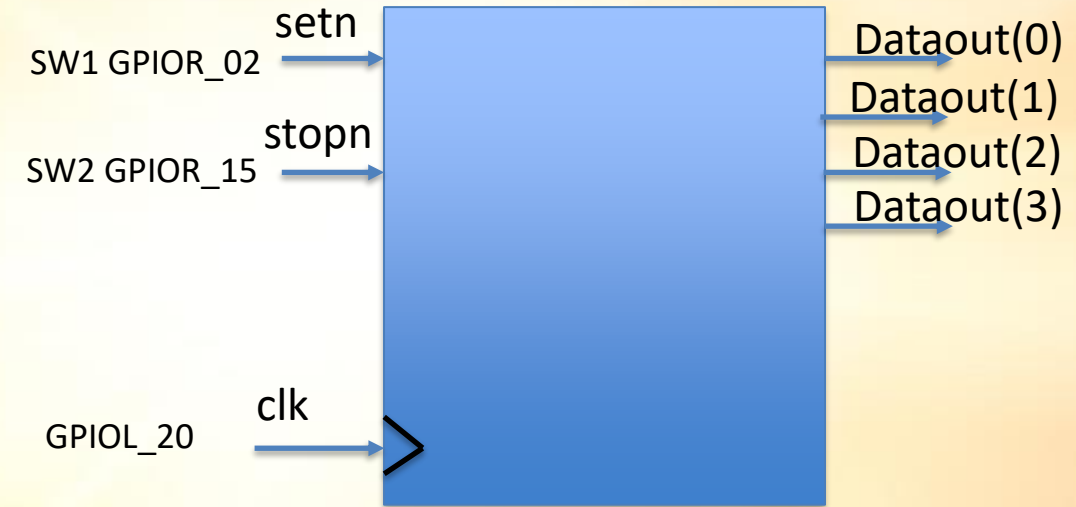
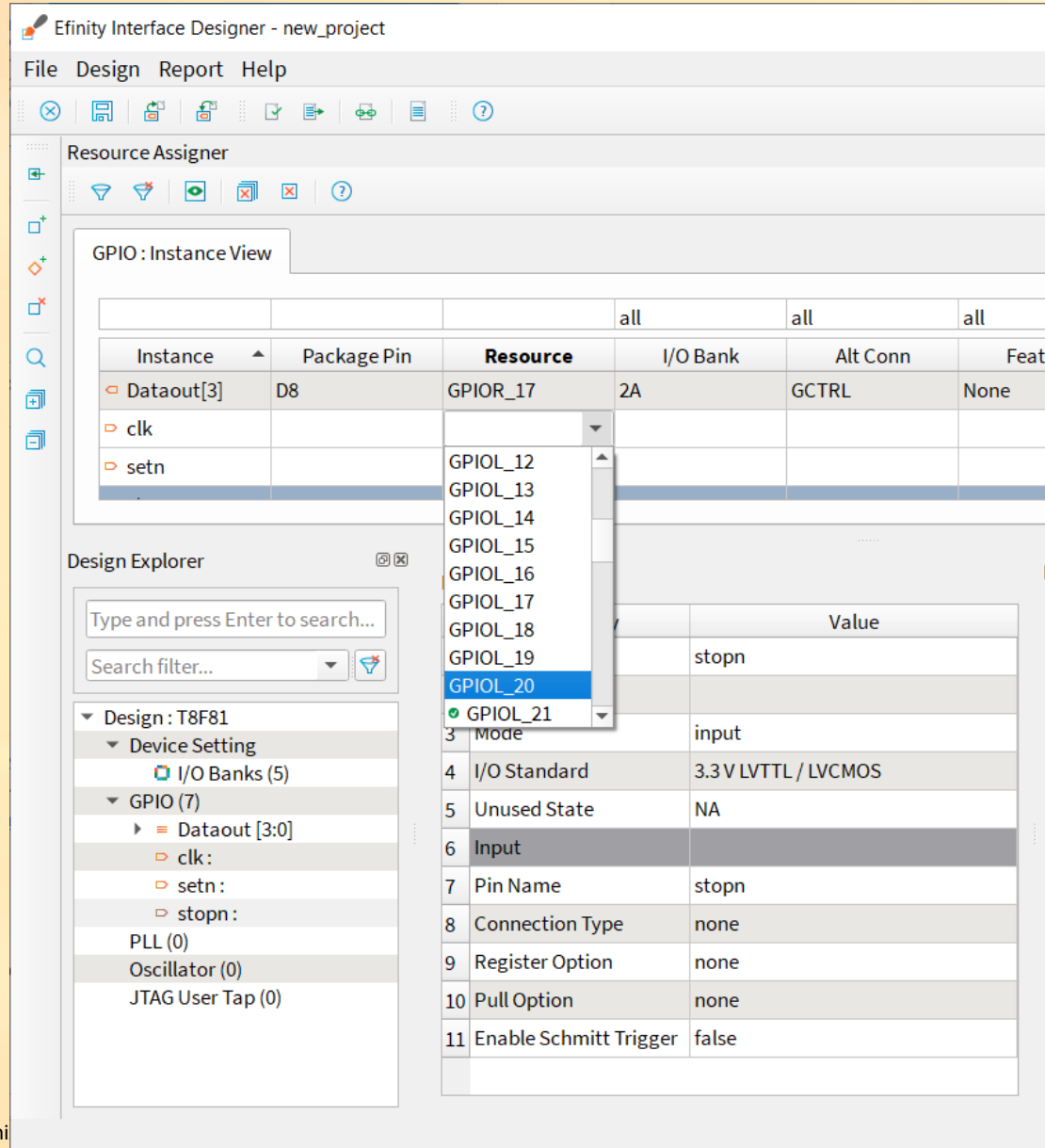
The **Block Summary** panel in the center shows the properties for the selected block:

Property	Value
1 Instance Name	gpio_inst7
2 GPIO Resource	
3 Mode	input
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	gpio_inst7
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false

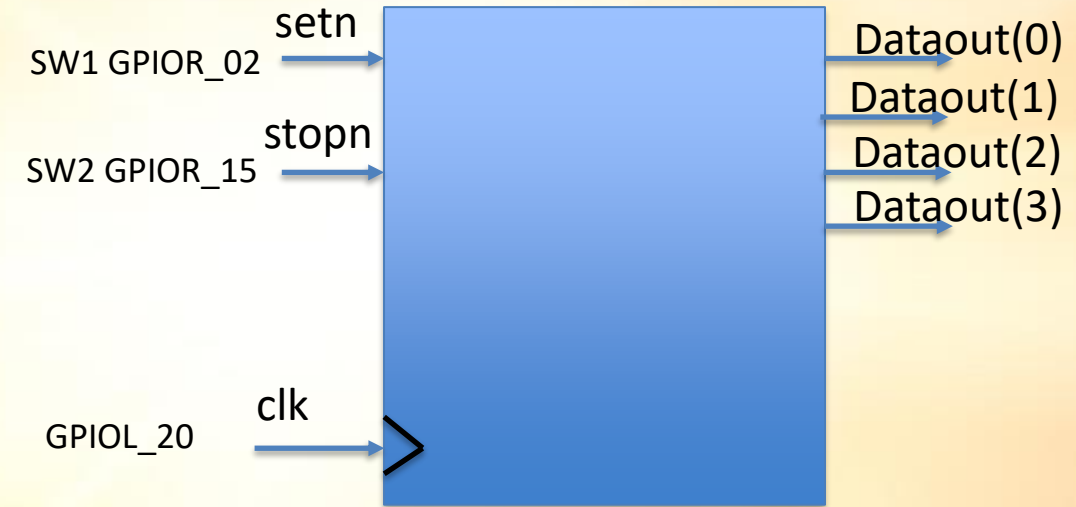
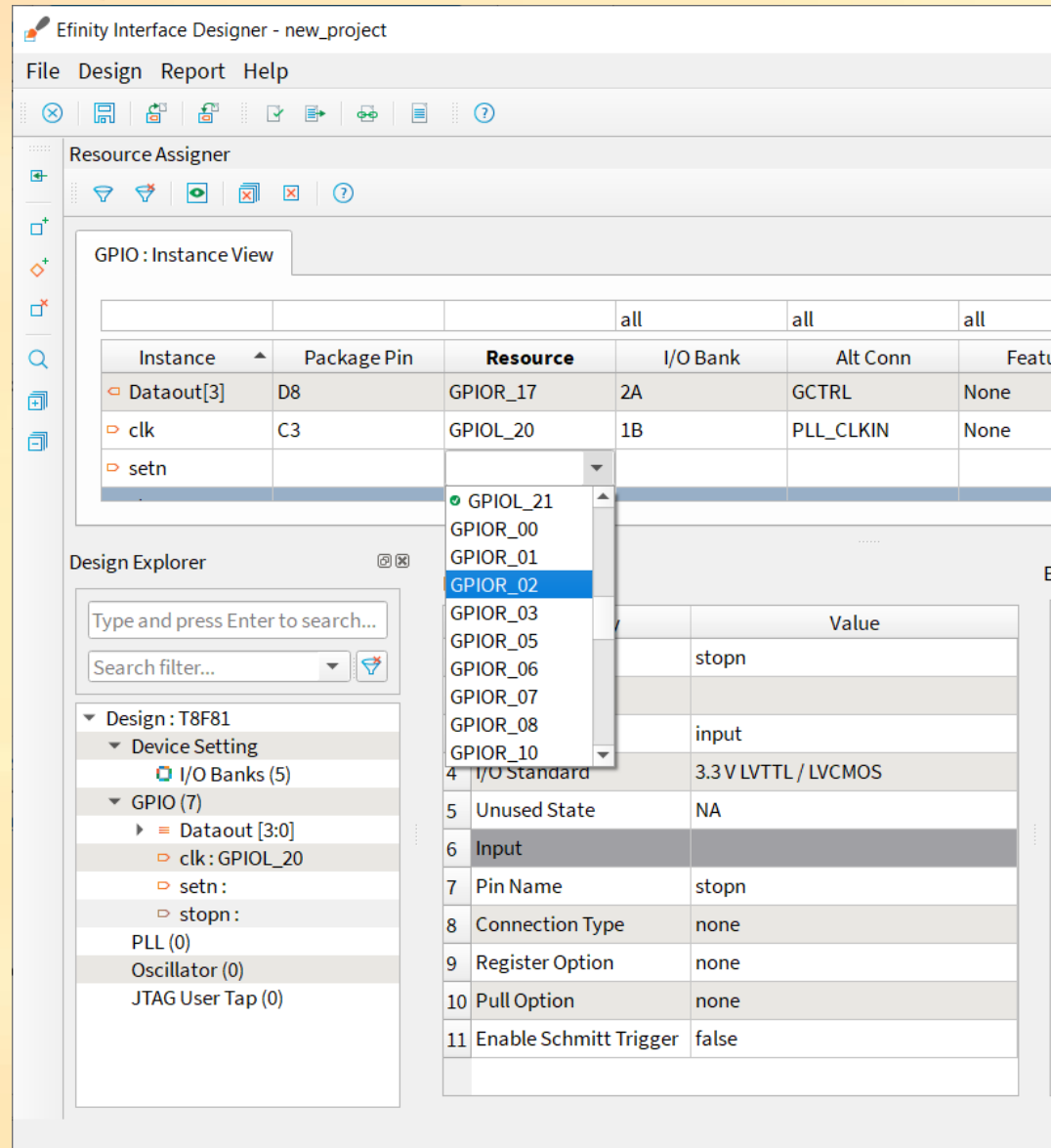
The **Block Editor** panel on the right shows the configuration for the selected block. The **Instance Name** field is circled in red and contains the text **stopn**.

Select gpio_inst8
Enter name in the
Block Editor stopn
and press enter !

Assign the Resource CLK=>GPIOL_20



Assign the Resource setn=>GPIOR_02



Assign the Resource stopn=>GPIOR_15

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Feat
clk	C3	GPIOL_20	1B	PLL_CLKIN	None
setn	C5	GPIOR_02	2A	None	None
stopn					

Design Explorer

Type and press Enter to search...

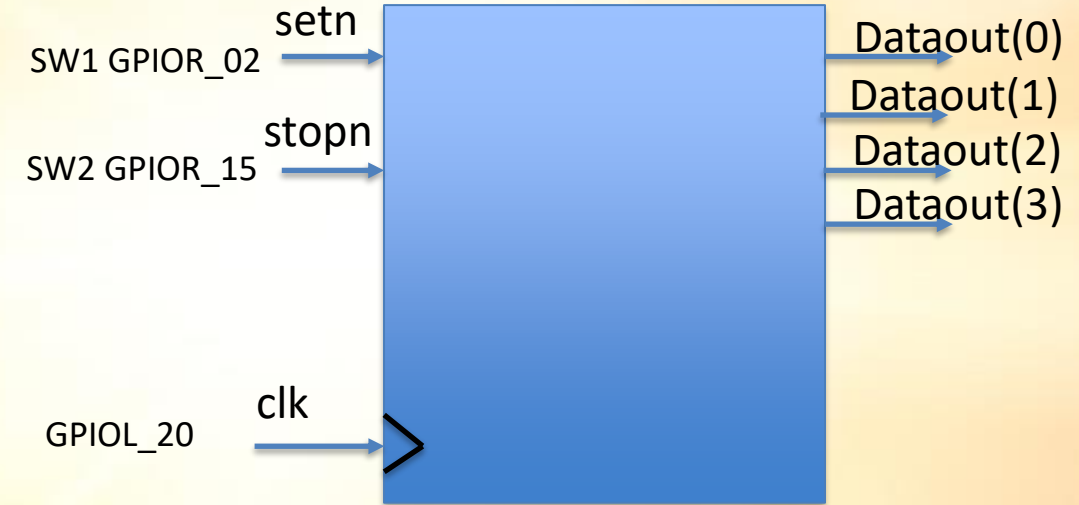
Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (7)
 - Dataout [3:0]
 - clk : GPIOL_20
 - setn : GPIOR_02
 - stopn :
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Value

GPIOR_10	
GPIOR_11	
GPIOR_12	
GPIOR_13	
GPIOR_14	
GPIOR_15	stopn
GPIOR_16	
GPIOR_17	
GPIOR_18	input
GPIOR_19	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	stopn
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false



Check the design and close the interface designer

The screenshot shows the Efinity Interface Designer window with the title 'Efinity Interface Designer - new_project'. The menu bar includes 'File', 'Design', 'Report', and 'Help'. The toolbar contains various icons, with the 'Check Design' icon (a green checkmark) circled in red. Below the toolbar is the 'Resource Assigner' section, which includes a 'GPIO : Instance View' table. The table has columns for Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, Clock Region, and Pad. It lists three instances: 'clk' (GPIO_L_20), 'setn' (GPIOR_02), and 'stopn' (GPIOR_15). Below the table is the 'Design Explorer' section, which shows a tree view of the design hierarchy. The 'Block Summary' section displays a table of properties and values for the selected 'stopn' instance. The 'Block Editor' section shows the configuration for the 'stopn' instance, including its name, mode, I/O standard, and input settings.

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
clk	C3	GPIO_L_20	1B	PLL_CLKIN	None	L1	GPIO_L_20_PLLIN
setn	C5	GPIOR_02	2A	None	None	R1	GPIOR_02_RESERVED_OUT
stopn	C9	GPIOR_15	2A	None	None	R1	GPIOR_15_CBUS0

Design Explorer

Type and press Enter to search...

Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (7)
 - Dataout [3:0]
 - clk : GPIO_L_20
 - setn : GPIOR_02
 - stopn : GPIOR_15
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Block Summary

Property	Value
1 Instance Name	stopn
2 GPIO Resource	GPIOR_15
3 Mode	input
4 I/O Standard	3.3V LVTTTL / LVCMOS
5 Unused State	NA
6 Alternate Connection	None
7 Features	None
8 Clock Region	R1
9 I/O Bank	2A
10 Pad	GPIOR_15_CBUS0
11 Package Pin	C9
12 Input	

Block Editor

Instance Name

stopn

Mode

input

I/O Standard

3.3V LVTTTL / LVCMOS

Input

Pin Name

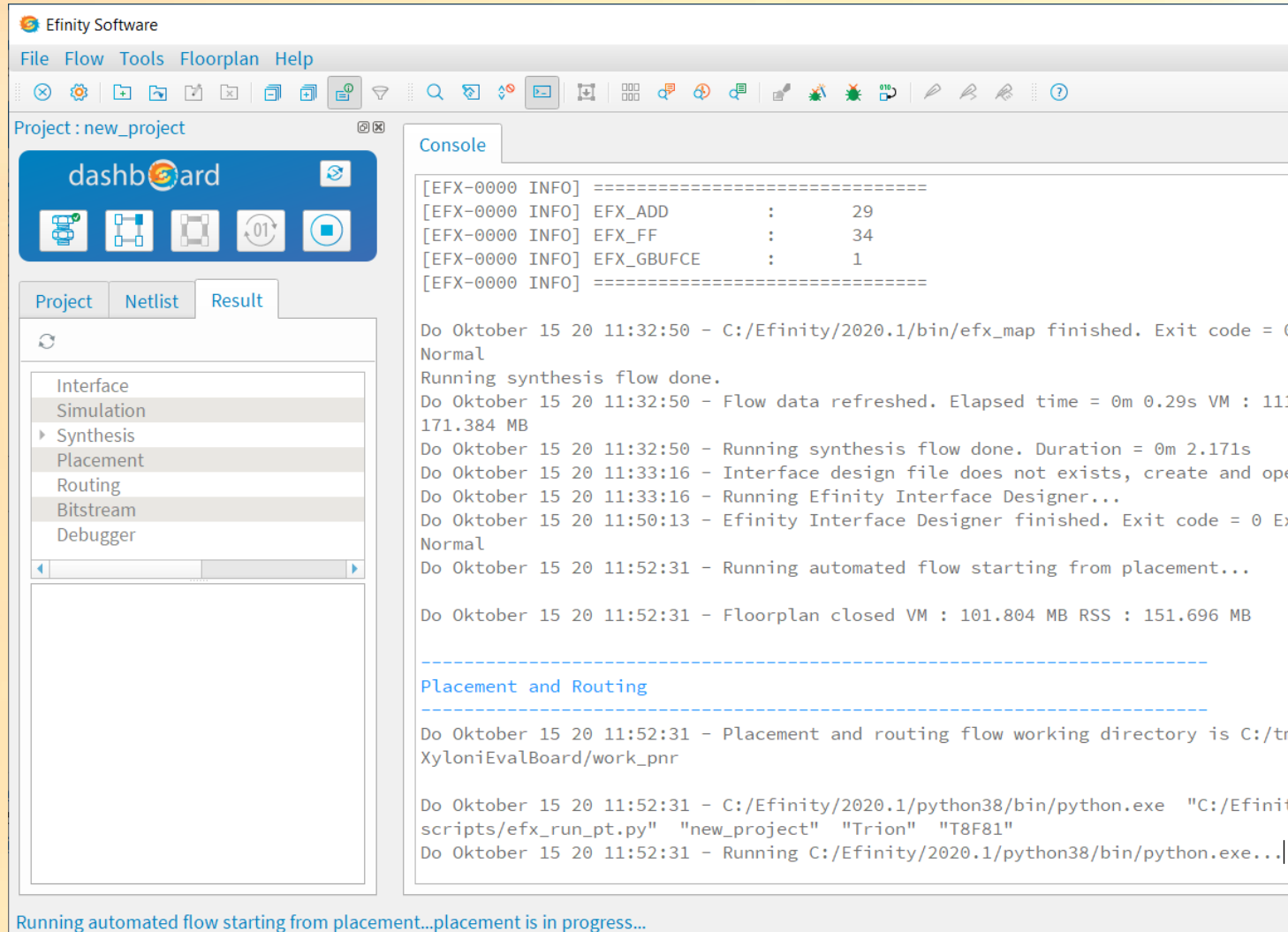
stopn



Connection Type

none

Check design...done. 0 issue.

Run the whole flow with clicking on placement



- If the Automated flow button is grayed out click on the button to activate the automated flow. 
- Click on the Place icon and the flow will run automatically 



If you have an unassigned pin, check the Placement report, go back to interface designer and fix the name and rerun the flow

The screenshot displays the Efinity Software interface with the following components:

- Project : new_project** (top left)
- dashbord** (top left, blue header)
- Project | Netlist | Result** (tabs)
- Placement** (selected in the left sidebar)
- Outputs** table:

Outputs	5 / 113
Clocks	1 / 16
Logic Elements	37 / 7384
Memory Blocks	0 / 24
Multipliers	0 / 8
Interface	
Missing Interface Pins	1
Unassigned Core Pins	1
Timing	
Least Slack	23.349 ns
clk	103.613 MHz
Debugger	
- Console** (middle left):

```
efinixprojects/T8EvalBoard/outflow/new_project.interface.csv'. Successfully processed interface constraints file "D:/user/efinixprojects/T8EvalBoard/outflow/new_project.interface.csv". SDC file 'D:/user/efinixprojects/T8EvalBoard/counterconstrain.sdc' parsed successfully. 1 clocks (including virtual clocks), 0 inputs and 0 outputs were constrained. Maximum possible analyzed clocks frequency Clock Name Period (ns) Frequency (MHz) Edge clk 9.651 103.613 (R-R) Geomean max period: 9.651 Launch Clock Capture Clock Constraint (ns) Slack (ns) Edge clk clk 33.000 23.349 (R-R) Mi März 18 20 11:36:00 - Flow data refreshed. Elapsed time = 0m 3.156s VM : 220.104 MB RSS : 253.856 MB Mi März 18 20 11:36:00 - Running automated flow starting from synthesis done. Total duration = 0m 12.308s
```
- Code Editor** (right):
 - new_project.place.rpt** (selected):

```
11 ----- Resource Summary (begin) -----
12
13 Inputs: 3 / 96 (3.12%)
14 Outputs: 5 / 113 (4.42%)
15 Clocks: 1 / 16 (6.25%)
16 Logic Elements: 37 / 7384 (0.50%)
17 LE: LUTs/Adders: 31 / 7384 (0.42%)
18 LE: Registers: 35 / 5280 (0.66%)
19 Memory Blocks: 0 / 24 (0.00%)
20 Multipliers: 0 / 8 (0.00%)
21 ----- Resource Summary (end) -----
22
23 Elapsed time for packing: 0 hours 0 minutes 0 seconds
24
25 ----- IO Interface Summary (begin) -----
26
27 +-----+
28 | Missing Interface Pins | Input/Output |
29 +-----+
30 | stop | Input |
31 +-----+
32
33 ----- IO Interface Summary (end) -----
34
35 ----- IO Placement Summary (begin) -----
36
37 +-----+
38 | Unassigned Core Pins | Input/Output |
39 +-----+
40 | stopn | Input |
41 +-----+
42
43 ----- IO Placement Summary (end) -----
44
45 Elapsed time for placement: 0 hours 0 minutes 1 seconds
46
47
```

Typo in Interface designer: **stop** instead of **stopn**

Check static timing

The screenshot displays the Efinity Software interface with the following components:

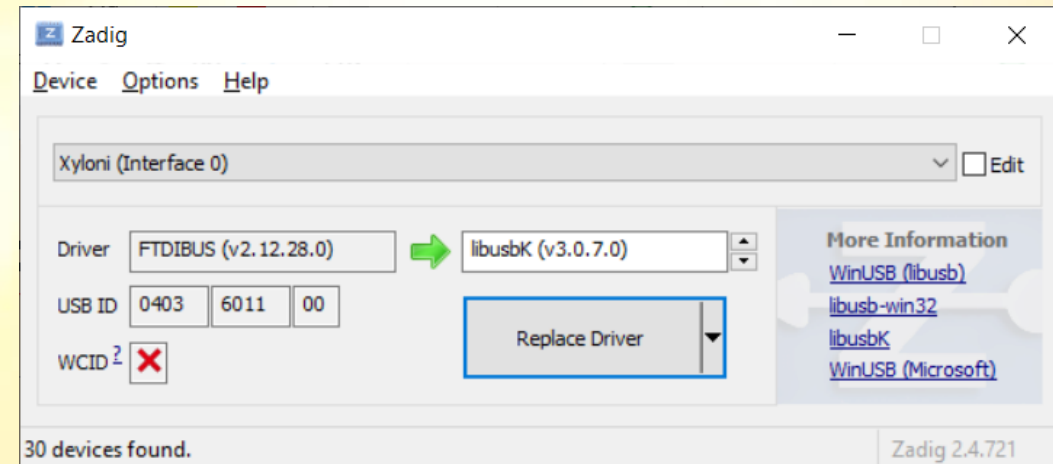
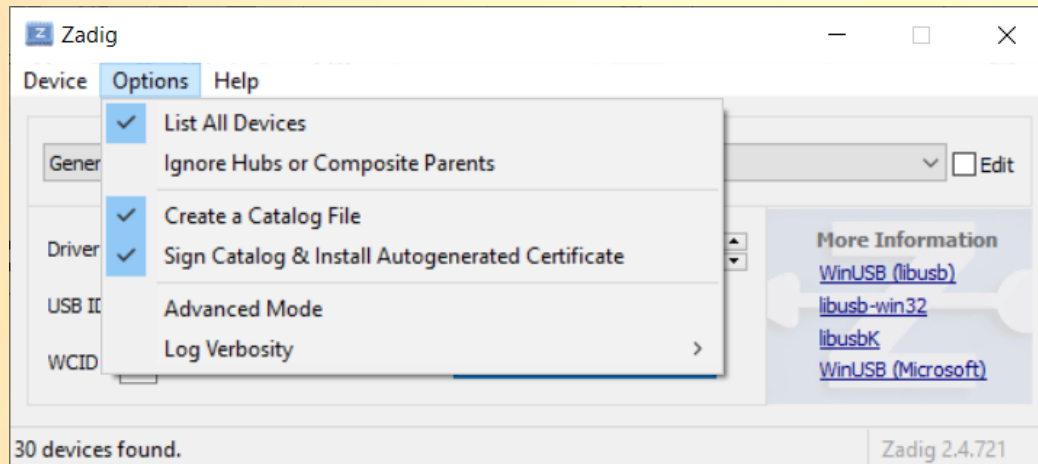
- Project:** new_project
- Console:** Shows the completion of parsing the switch_block file and the generation of 393829 RR nodes and 1460307 RR edges. It also indicates that the design has 0 global control net(s).
- Code Editor:** Displays the file new_project.timing.rpt. The file content includes:
 - temperature : 0C to 85C
 - voltage : 1.1V +/-50mV
 - speedgrade : 2
 - technology : s40ll
 - status : final
 - Table of Contents (begin)
 - 1. Clock Frequency Summary
 - 2. Clock Relationship Summary
 - 3. Path Details for Max Critical Paths
 - 4. Path Details for Min Critical Paths
 - Table of Contents (end)
 - 1. Clock Frequency Summary (begin)
 - User target constrained clocks
 - Table with 5 columns: Clock Name, Period (ns), Frequency (MHz), Waveform, Source.
 - Table with 1 row: clk, 30.000, 33.333, {0.000 15.000}
 - Maximum possible analyzed clocks frequency
 - Table with 4 columns: Clock Name, Period (ns), Frequency (MHz), Edge (R-R).
 - Table with 1 row: clk, 9.934, 100.666, (R-R)
 - Geomean max period: 9.934
 - Clock Frequency Summary (end)

To check the static timing select routing_new_project.timing.rpt.

Here you will find the constrains from the constrain file (clk :30ns) and the result

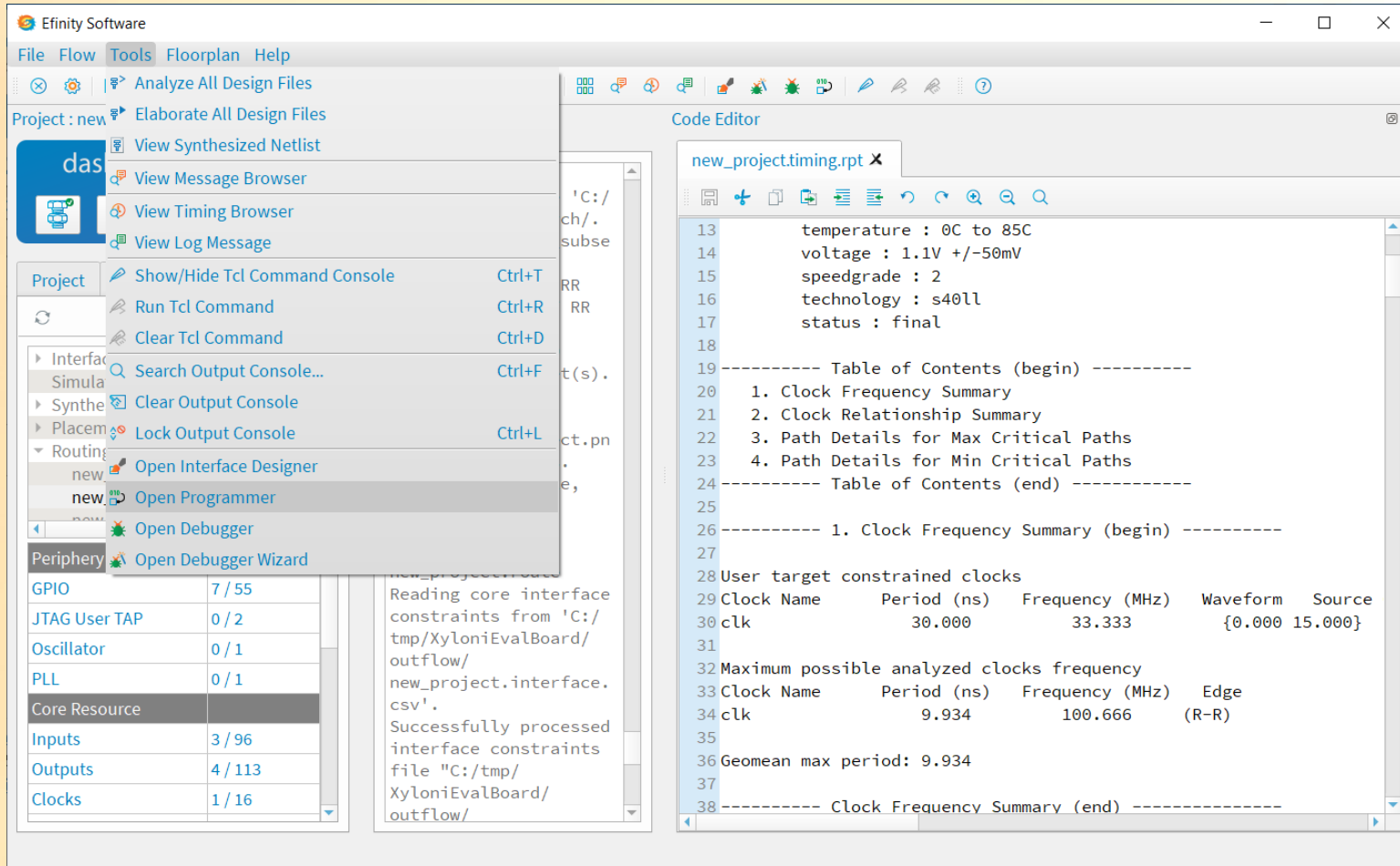
Program the Device

- To program the Device you have to install the USB driver first !
- Select Xyloni (Interface 0) for SPI programming.
- This is for Software Efinity 2020.1. Efinity 2020.2 will be different !

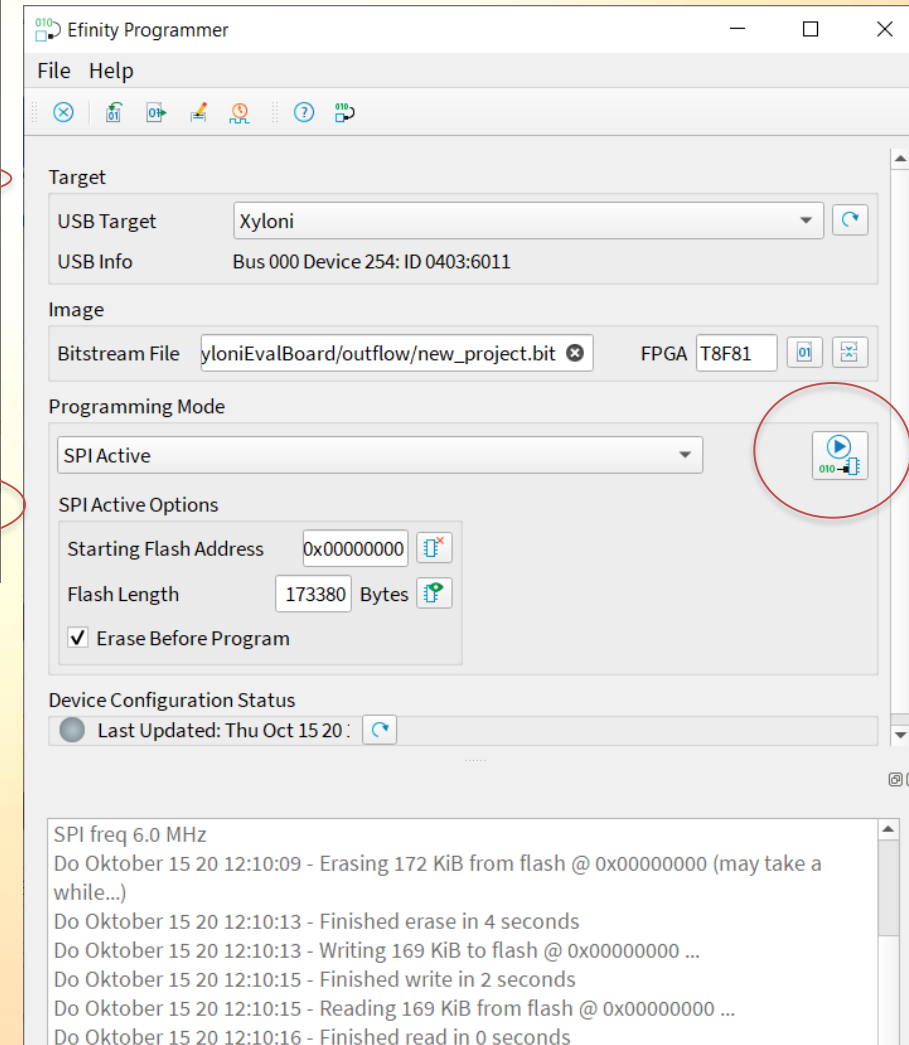
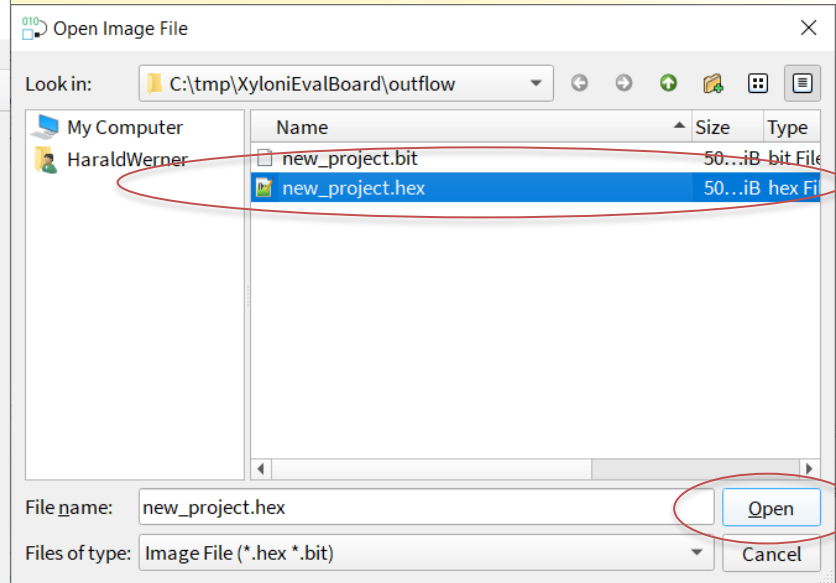
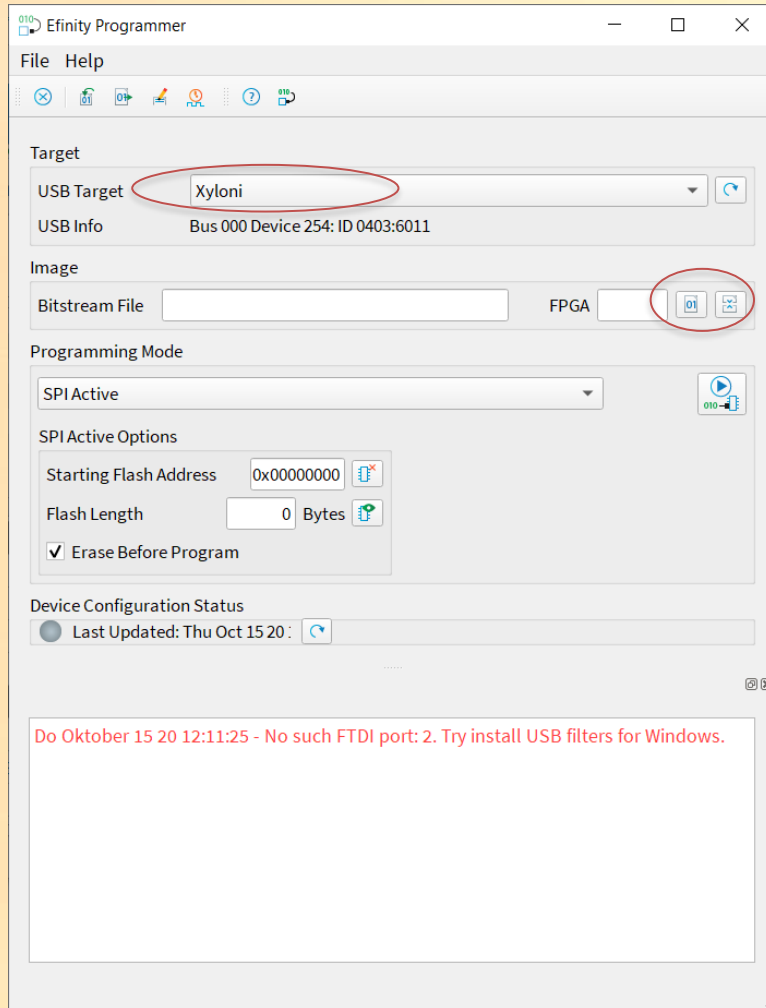


Program the Device

Open Programmer
Tools->OpenProgrammer



Select Image File, Start Program (Check USB Target: Xyloni)

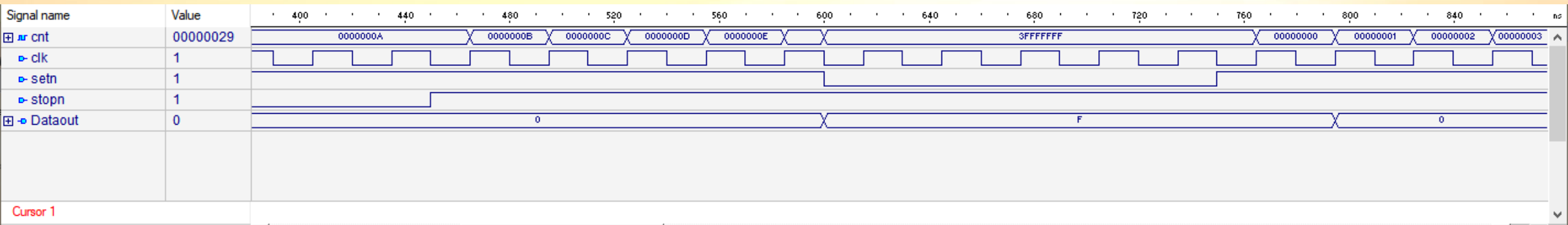


Problem solving

- All LED ON: Check VHDL if you have the correct setting for the frequency ! (29 downto 26) vs (17 downto 14)
- If you can not see the Xyloni, check if you installed the correct USB driver with zadig

Simulation

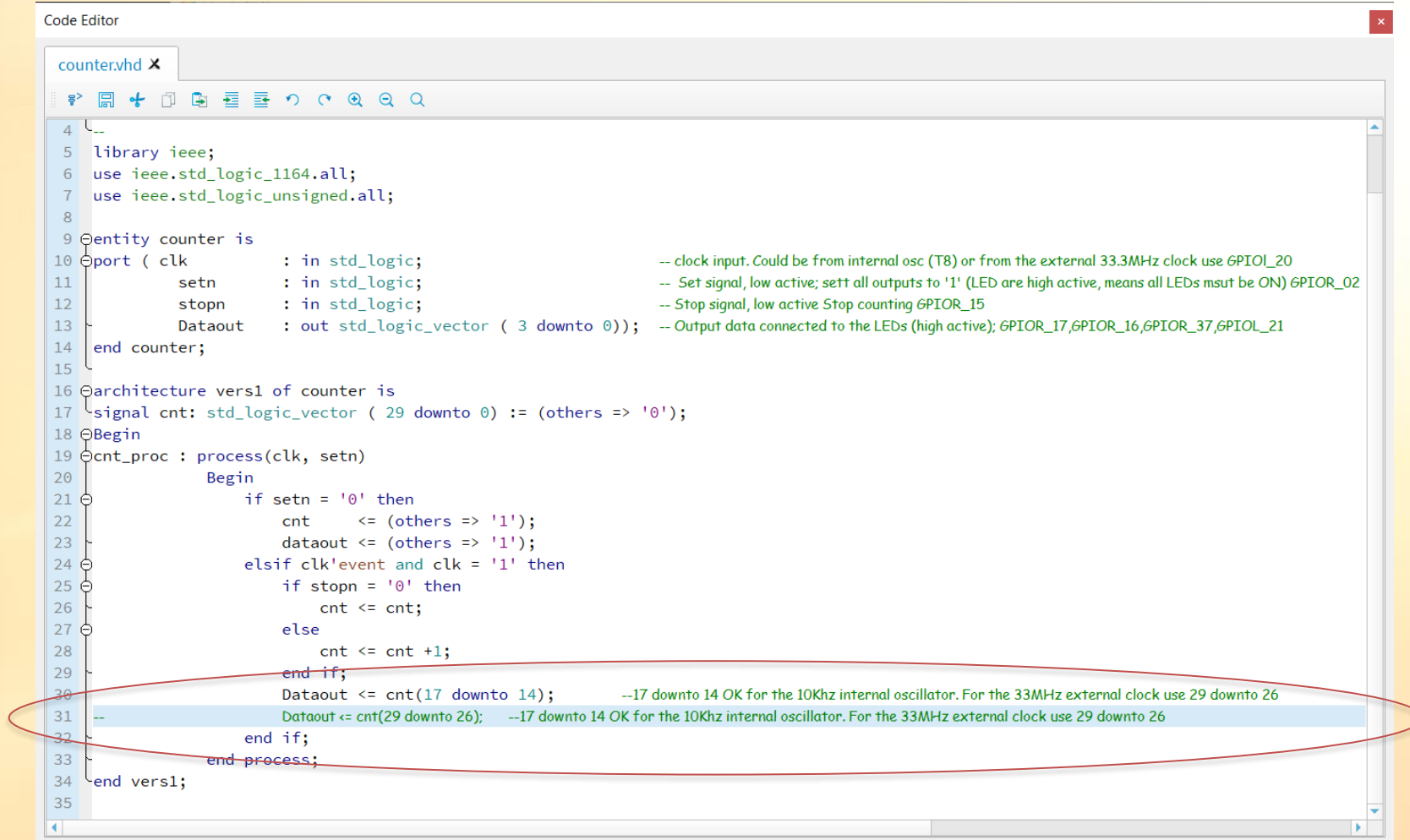
- For HDL simulation you can use any VHDL simulator. The testbench is included in the design.
- Here a wave form the design with testbench with an ALDEC HDL simulator.



- If you would like to simulate the synthesized netlist, include the new_project.dbg.map.v below the outflow folder and include the simulation libraries <installation path>\Efinity\2020.1\sim_models\verilog folder instead of the RTL Design

Design with OSC

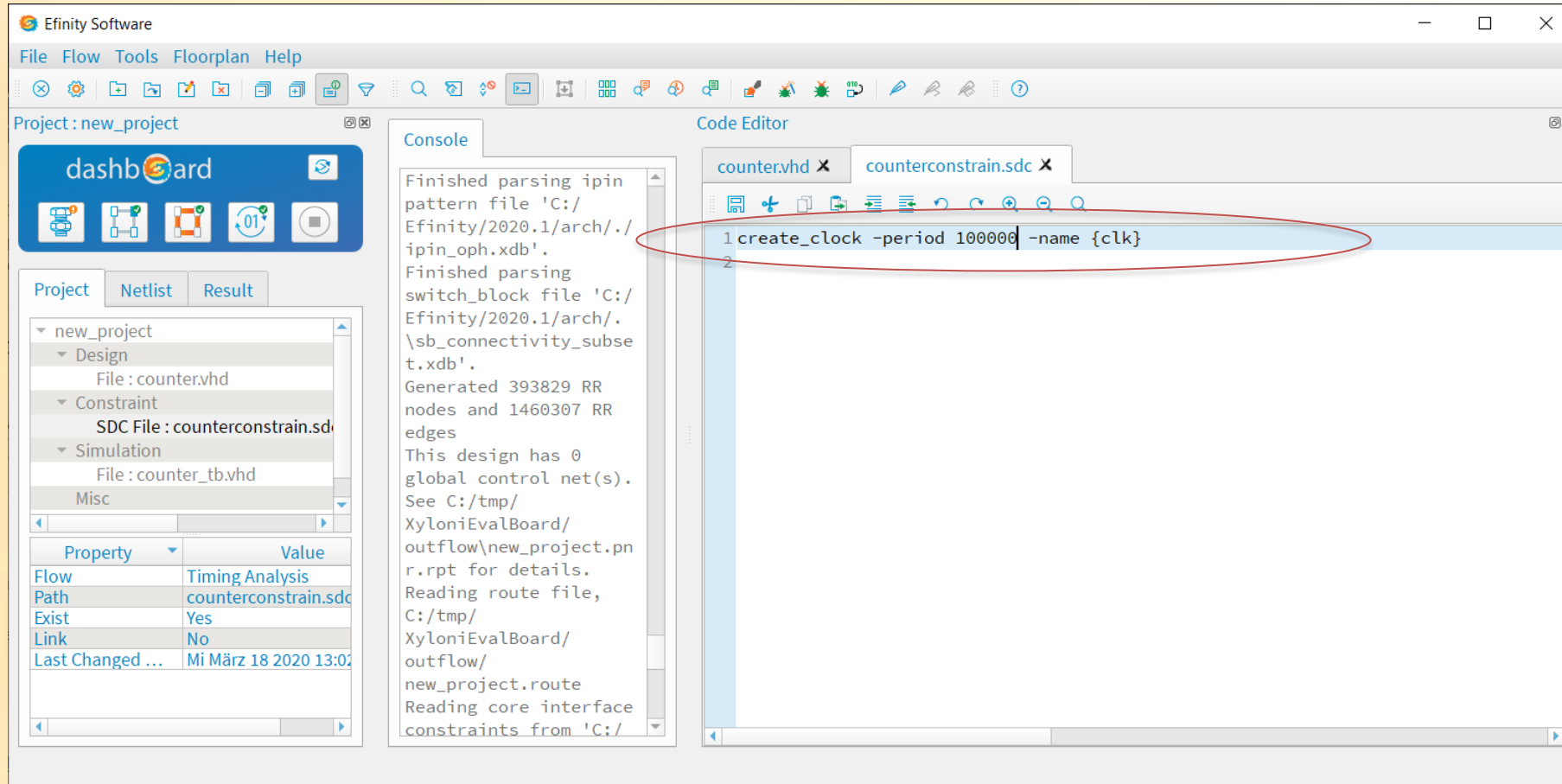
1. change VHDL file



```
4  --
5  library ieee;
6  use ieee.std_logic_1164.all;
7  use ieee.std_logic_unsigned.all;
8
9  entity counter is
10 port ( clk      : in std_logic;           -- clock input. Could be from internal osc (T8) or from the external 33.3MHz clock use GPIOL_20
11        setn     : in std_logic;         -- Set signal, low active; sett all outputs to '1' (LED are high active, means all LEDs msut be ON) GPIOR_02
12        stopn    : in std_logic;         -- Stop signal, low active Stop counting GPIOR_15
13        Dataout   : out std_logic_vector ( 3 downto 0)); -- Output data connected to the LEDs (high active); GPIOR_17,GPIOR_16,GPIOR_37,GPIOL_21
14 end counter;
15
16 architecture vers1 of counter is
17 signal cnt: std_logic_vector ( 29 downto 0) := (others => '0');
18 begin
19 cnt_proc : process(clk, setn)
20 begin
21     if setn = '0' then
22         cnt    <= (others => '1');
23         dataout <= (others => '1');
24     elsif clk'event and clk = '1' then
25         if stopn = '0' then
26             cnt <= cnt;
27         else
28             cnt <= cnt +1;
29         end if;
30         Dataout <= cnt(17 downto 14); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
31         -- Dataout <= cnt(29 downto 26); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
32     end if;
33 end process;
34 end vers1;
35
```

Design with OSC

2. change constrain file



Change Interface designer

- 3. Delete clk GPIO; Seelct clk->RMB->Delete

The screenshot displays the Efinix IDE interface with three main panels:

- Design Explorer:** Shows the project hierarchy. Under 'Design : T8F81', 'Device Setting' is expanded, showing 'I/O Banks (5)' and 'GPIO (7)'. The 'clk: GPIOL_20' instance is selected, and a right-click context menu is open with 'Delete' highlighted.
- Block Summary:** A table showing properties for the selected instance.
- Block Editor:** Shows the configuration for the 'clk' pin.

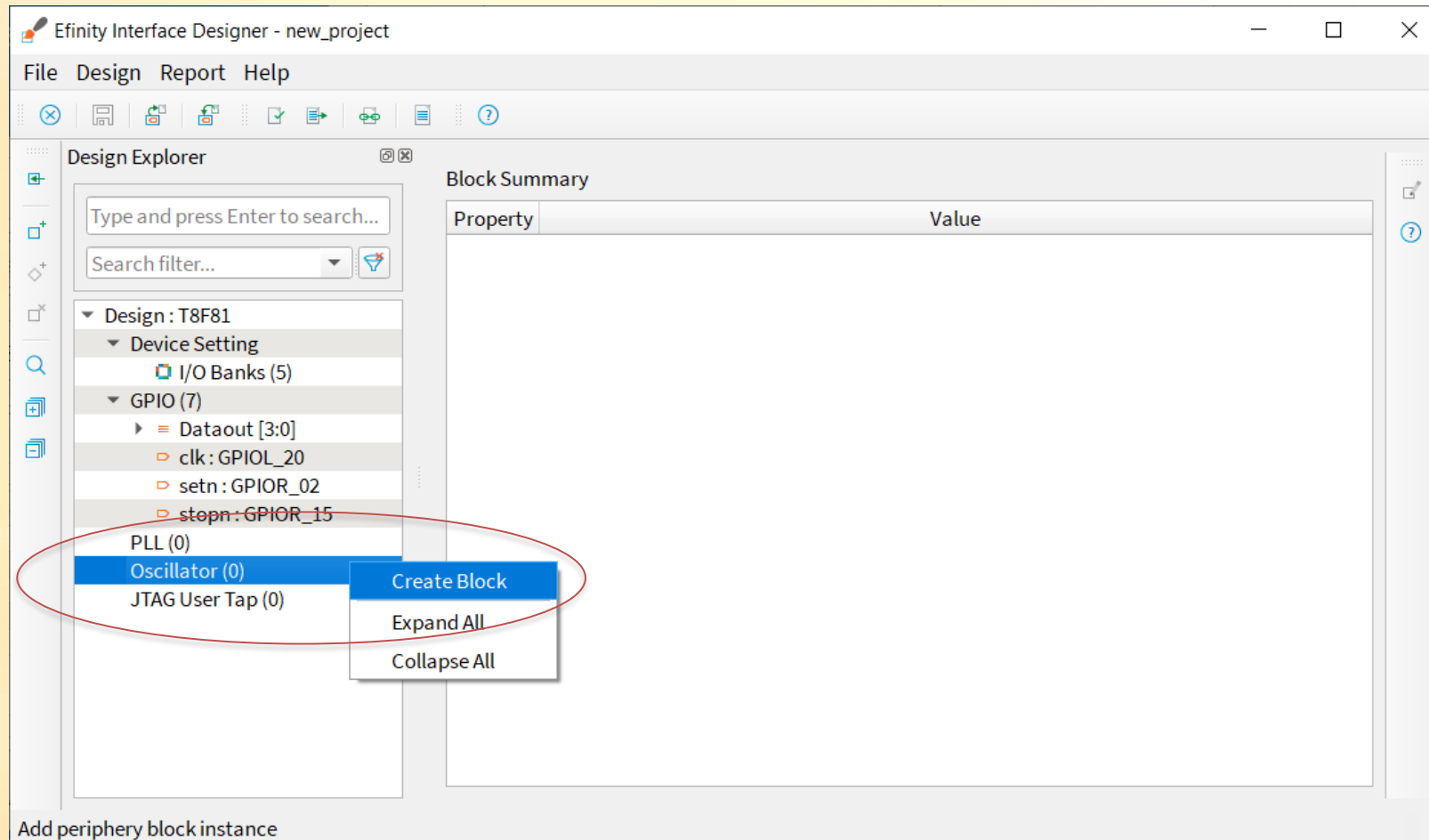
Property	
1	Instance Name
2	GPIO Resource
3	Mode
4	I/O Standard
5	Unused State
6	Alternate Connection
7	Features
8	Clock Region
9	I/O Bank
10	Pad
11	Package Pin
12	Input
13	Pin Name
14	Connection Type

Block Editor configuration for 'clk':

- Mode: input
- I/O Standard: 3.3 V LVTTTL / LVCMOS
- Input:
 - Pin Name: clk
 - Connection Type: none
 - Register Option: none
- Clock: (empty)

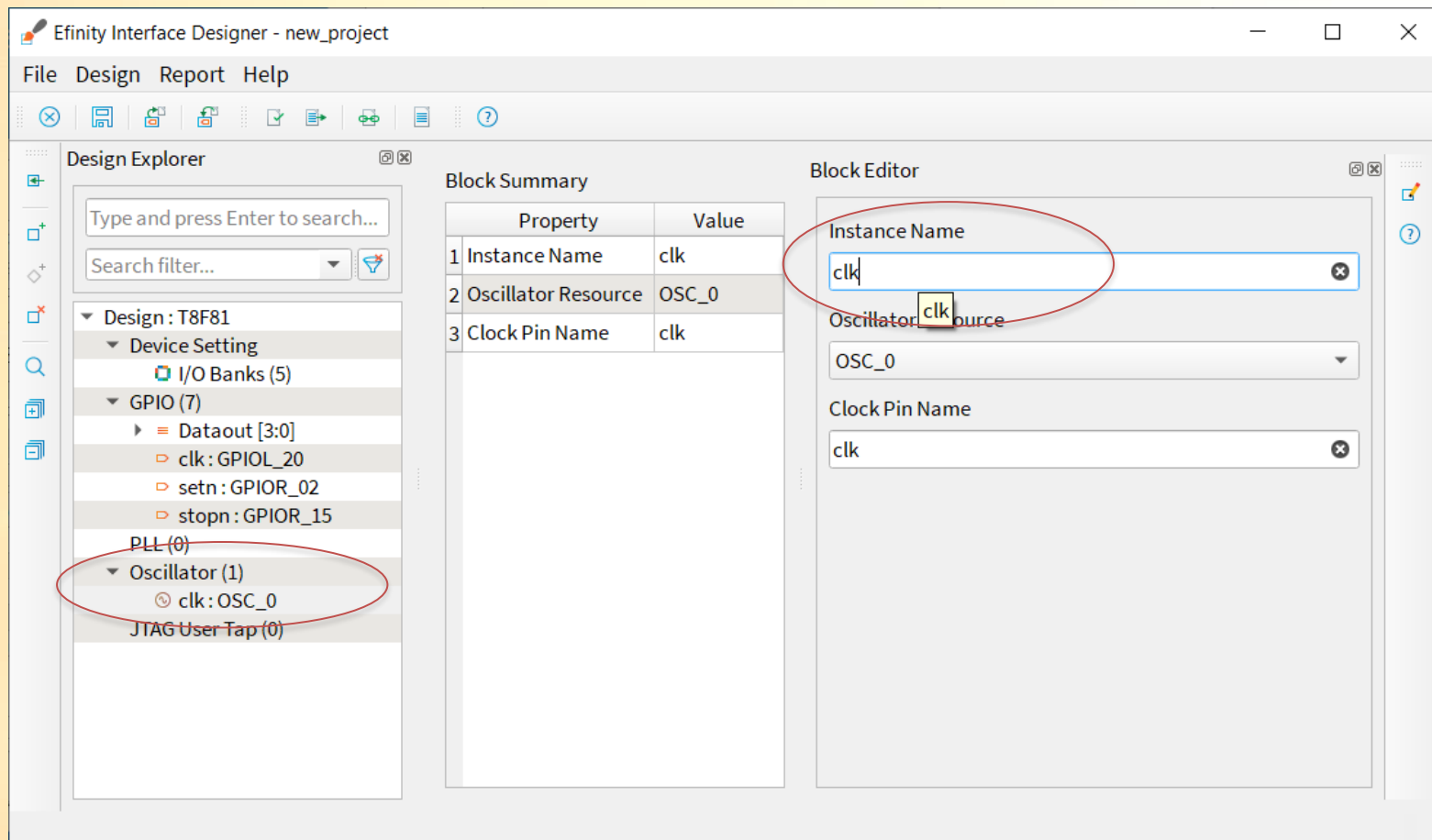
Change Interface designer

4. Add OSC; select Oscillator; RMB; Create Block

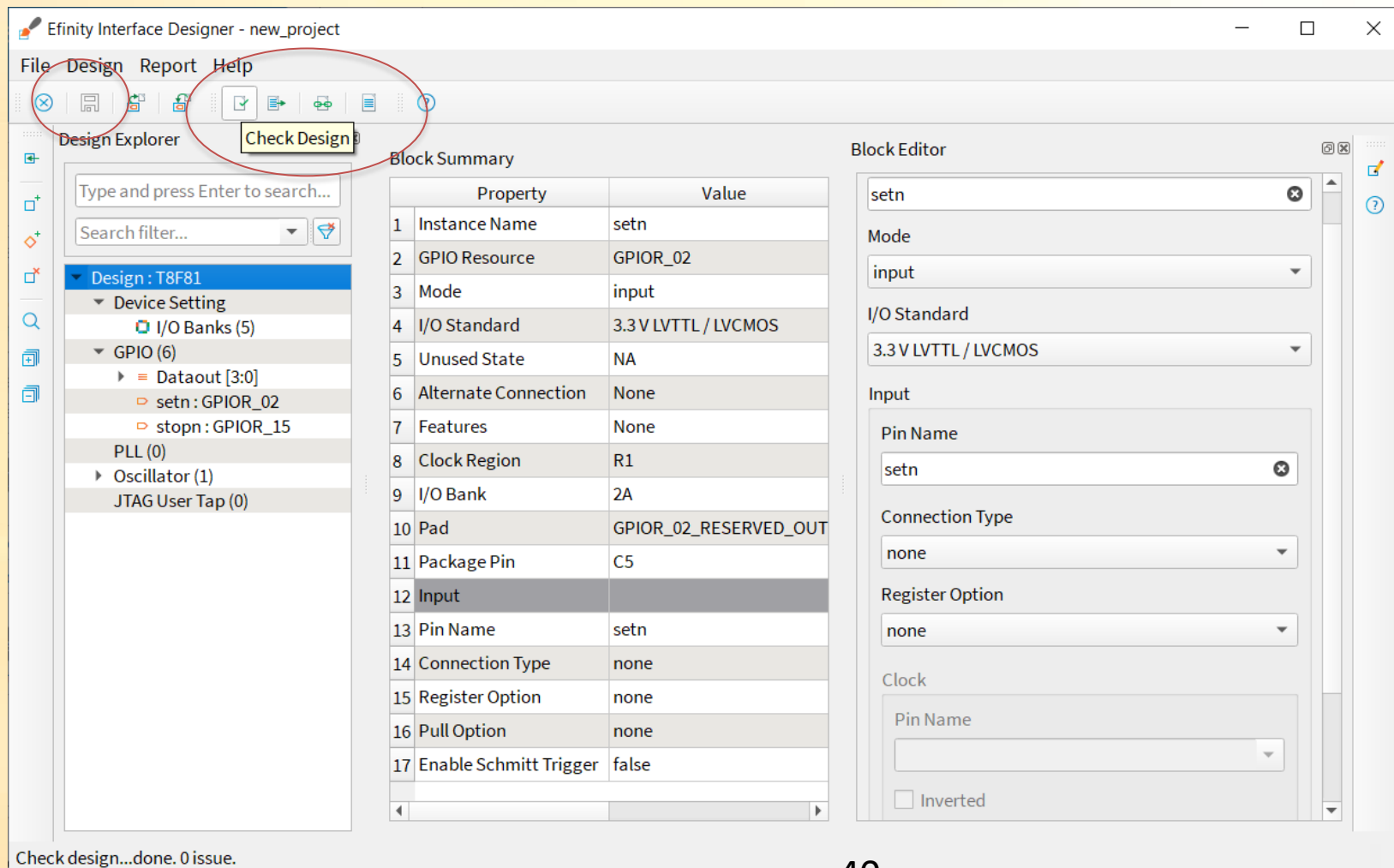


Change Interface designer

5. Assign clk to OSC Instance Name, **press ENTER !**



Check Design and save



Run the whole flow with pressing Synthesis



Efinity Software

File Flow Tools Floorplan Help

Project : new_project

dashboard

Project Netlist Result

new_project

- Design
 - File : counter.vhd
- Constraint
 - SDC File : counterconstrain.sdc
- Simulation
 - File : counter_tb.vhd
- Misc

Property	Value
Flow	Timing Analysis
Path	counterconstrain.sdc
Exist	Yes
Link	No
Last Changed ...	Mi März 18 2020 13:02

Console

```
INFO: Reading Mapping Library peak resident set memory usage = 37.312 MB
INFO: ***** Ending Reading Mapping Library ... *****
[EFX-0000 INFO] ... Pre-synthesis checks begin
[EFX-0000 INFO] ... Pre-synthesis checks end (Real time : 0s)
[EFX-0000 INFO] ... NameSpace init begin
[EFX-0000 INFO] ... NameSpace init end (Real time : 0s)
[EFX-0000 INFO] ... Mapping design "counter"
[EFX-0000 INFO] ... Hierarchical pre-synthesis "counter" begin

[EFX-0000 INFO] ... Hierarchical pre-synthesis "counter" end (Real time : 0s)
[EFX-0000 INFO] ... Flat optimizations begin
[EFX-0000 INFO] ... Flat optimizations end (Real time : 0s)
[EFX-0000 INFO] ... Flat synthesis begin
[EFX-0000 INFO] ... Flat synthesis end (Real time : 0s)
[EFX-0000 INFO] ... Flat optimizations begin
[EFX-0000 INFO] ... Flat optimizations end (Real time : 0s)
[EFX-0000 INFO] ... Check and break combinational loops begin
[EFX-0000 INFO] ... Check and break combinational loops end (Real time : 0s)
[EFX-0000 INFO] ... Top level netlist RUSHC IOs pre-synthesis begin
[EFX-0000 INFO] ... SOP modeling begin

[EFX-0000 INFO] ... SOP modeling end (Real time : 0s)
[EFX-0000 INFO] ... LUT mapping begin
```

Code Editor

counterconstrain.sdc

```
1 create_clock -peri
2
```

Running automated flow starting from synthesis...synthesis is in progress...

Check static timing

To check the static timing select routing_new_project.timing.rpt.

Here you will find the constrains from the constrain file (clk :100000ns) and the result

The screenshot displays the Efinity Software interface with the following components:

- Project:** new_project
- dashb@rd:** Includes icons for Project, Netlist, and Result.
- Project Tree:** Shows a hierarchy with folders for Interface, Simulation, Synthesis, Placement, and Routing. Under Routing, the files new_project.route.rpt and new_project.timing.rpt are listed.
- Periphery Resource Table:**

Periphery Resource	Count
GPIO	6 / 55
JTAG User TAP	0 / 2
Oscillator	1 / 1
PLL	0 / 1
Core Resource	
Inputs	3 / 96
Outputs	4 / 113
Clocks	1 / 16
Logic Elements	24 / 7384
- Console:** Displays the output of the static timing analysis, including messages like "Pass 0: Swept away 0 nets with no fanout." and "Netlist pre-processing took 0.0202929 seconds."
- Code Editor:** Shows the content of new_project.timing.rpt. A red circle highlights the "1. Clock Frequency Summary" section, which includes a table of constrained clocks and the maximum possible analyzed clocks frequency.

1. Clock Frequency Summary (begin)

Clock Name	Period (ns)	Frequency (MHz)	Waveform	Source	Clock Name
clk	100000.000	0.010	{0.000 50000.000}		virtu

Maximum possible analyzed clocks frequency

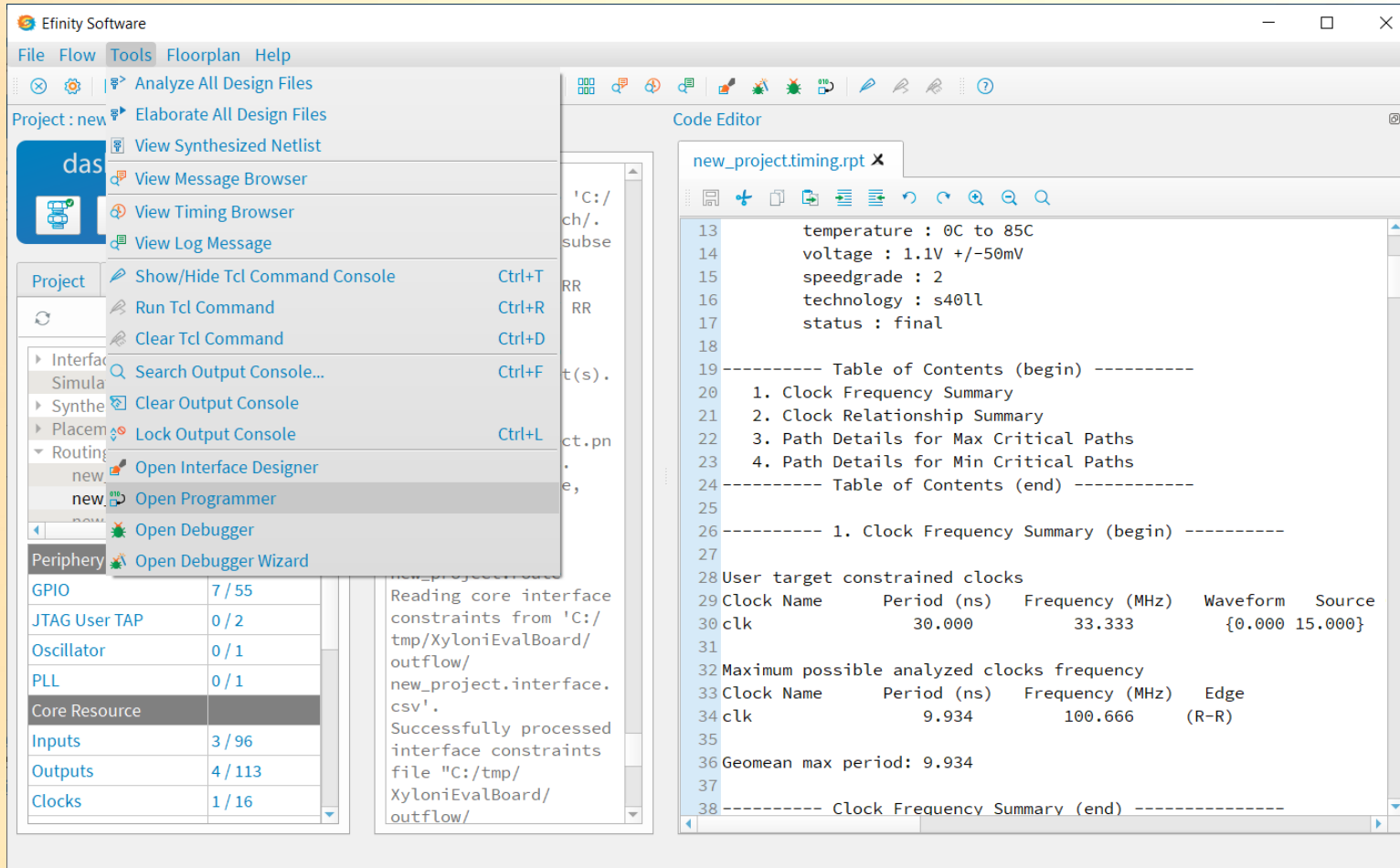
Clock Name	Period (ns)	Frequency (MHz)	Edge
clk	8.242	121.327	(R-R)

Geomean max period: 8.242

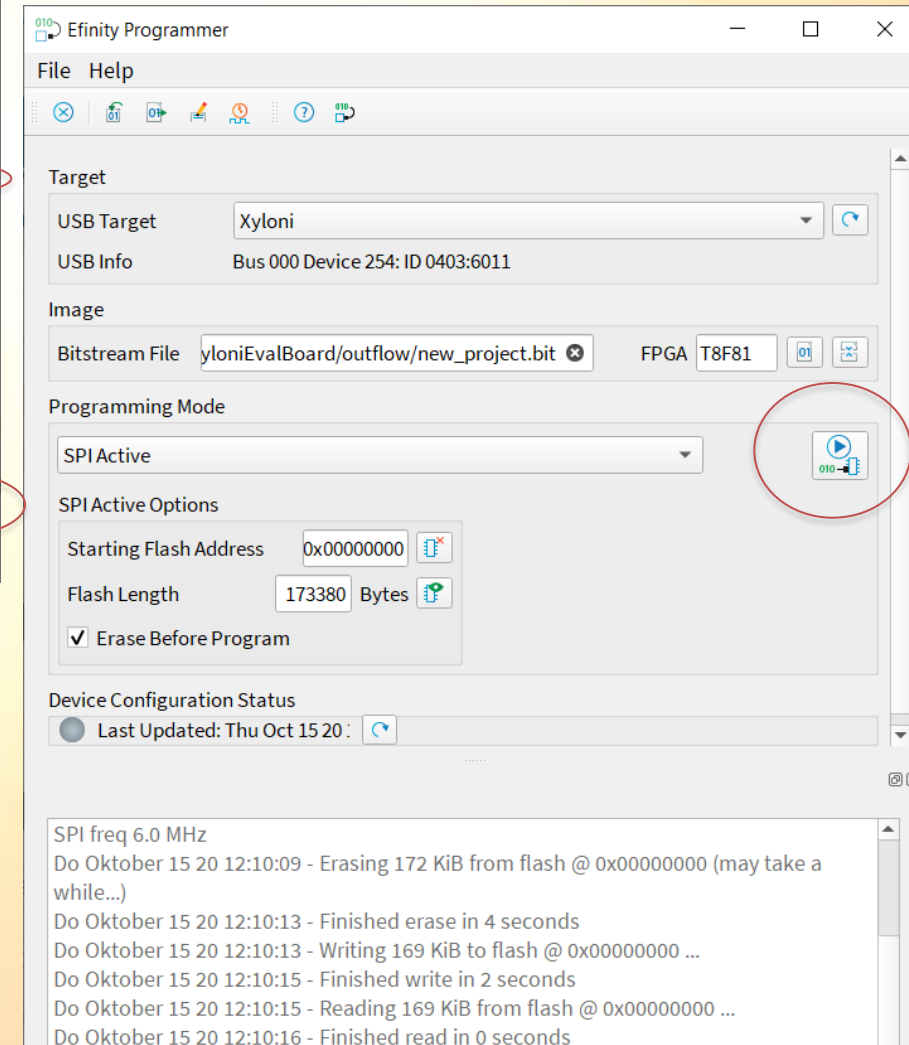
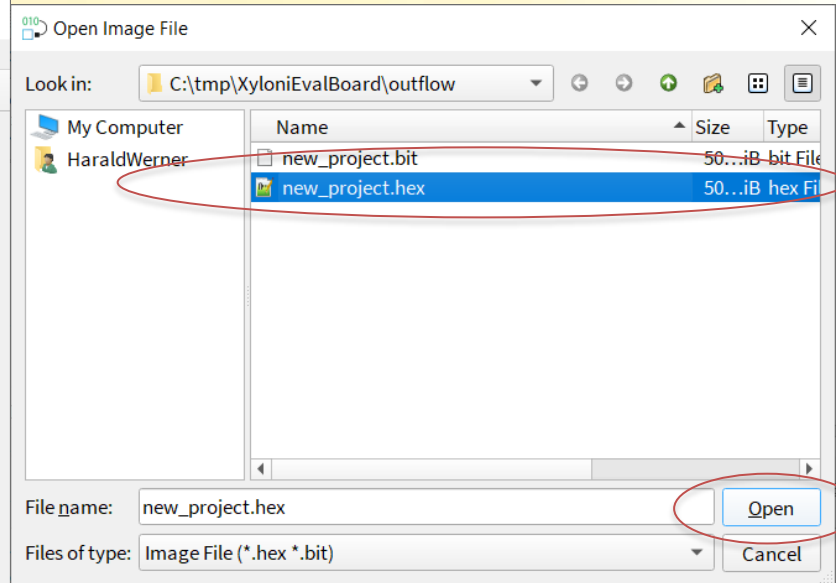
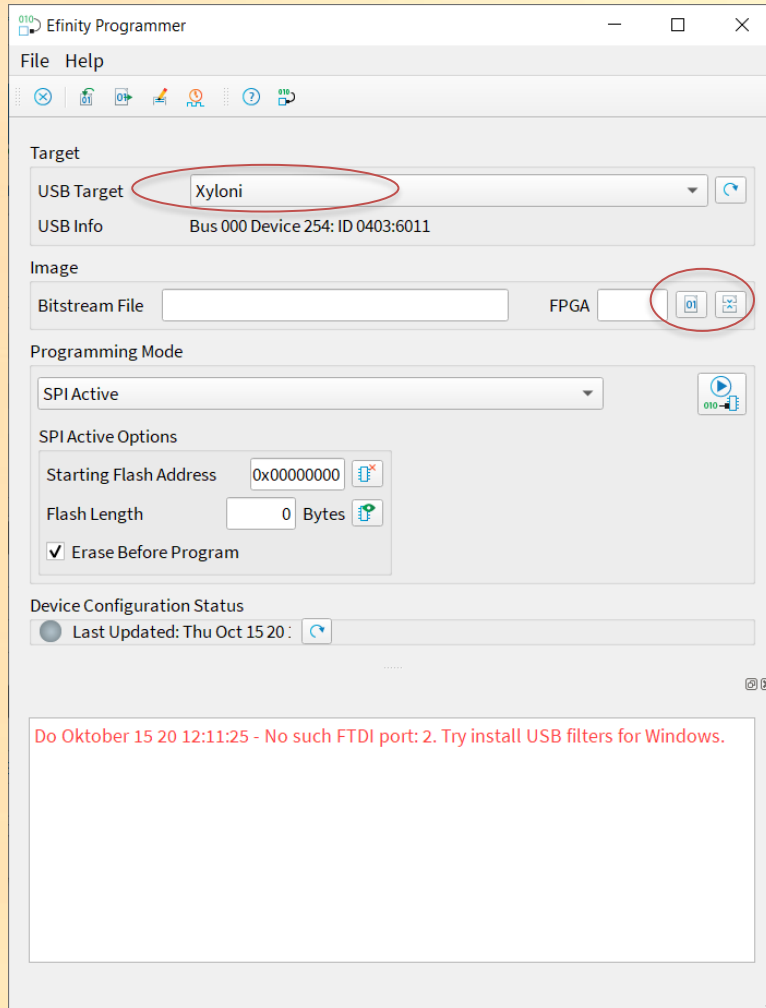
1. Clock Frequency Summary (end)

Program the Device

Open Programmer
Tools->OpenProgrammer



Select Image File, Start Program (Check USB Target: Xyloni)



Information

- If you need the complete Project, extract the XyloniEvalBoardSolution.zip file. Here you will find the project with the I/O pin assignments.