



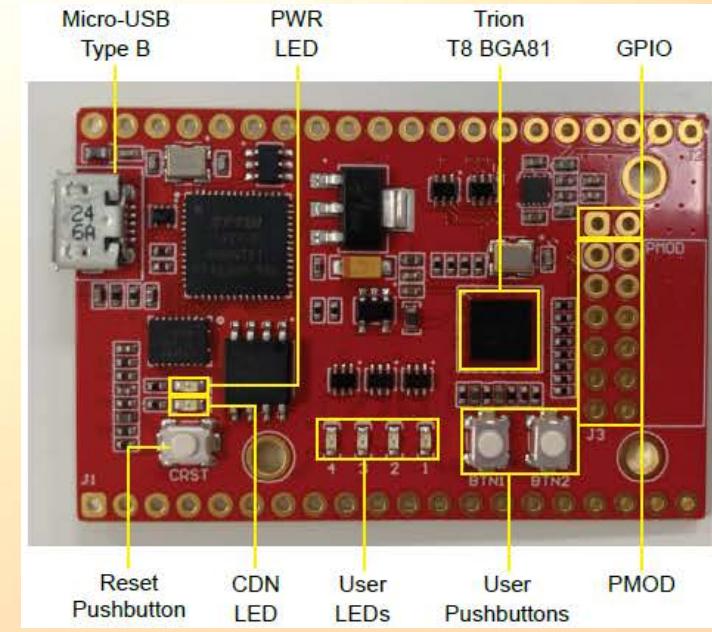
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***Accelerating Your Innovation***

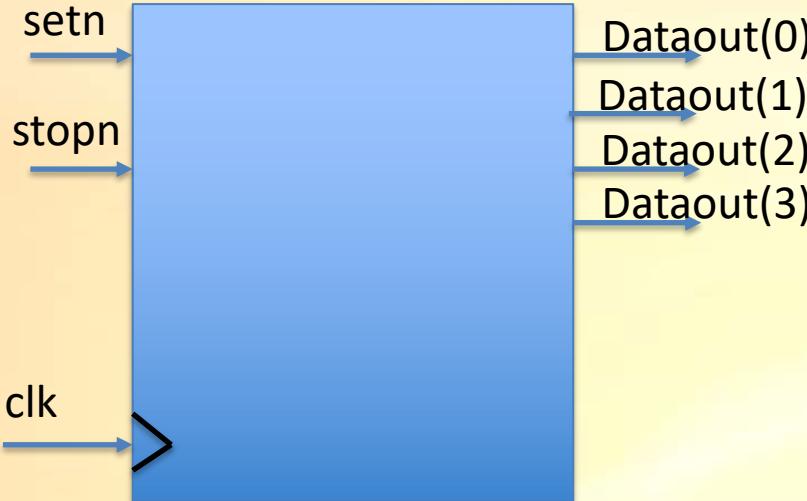
**Trion Xyloni T8 Lab**

**By Harald Werner**

**Version: 1.0.3**



# Design: Simple Up Counter with Set and Stop

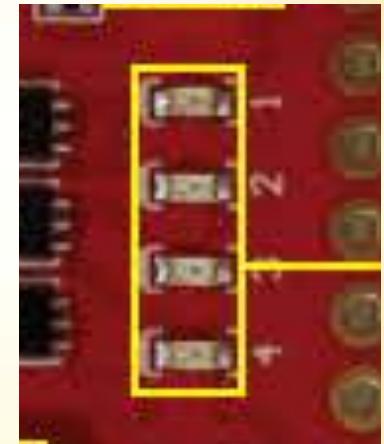
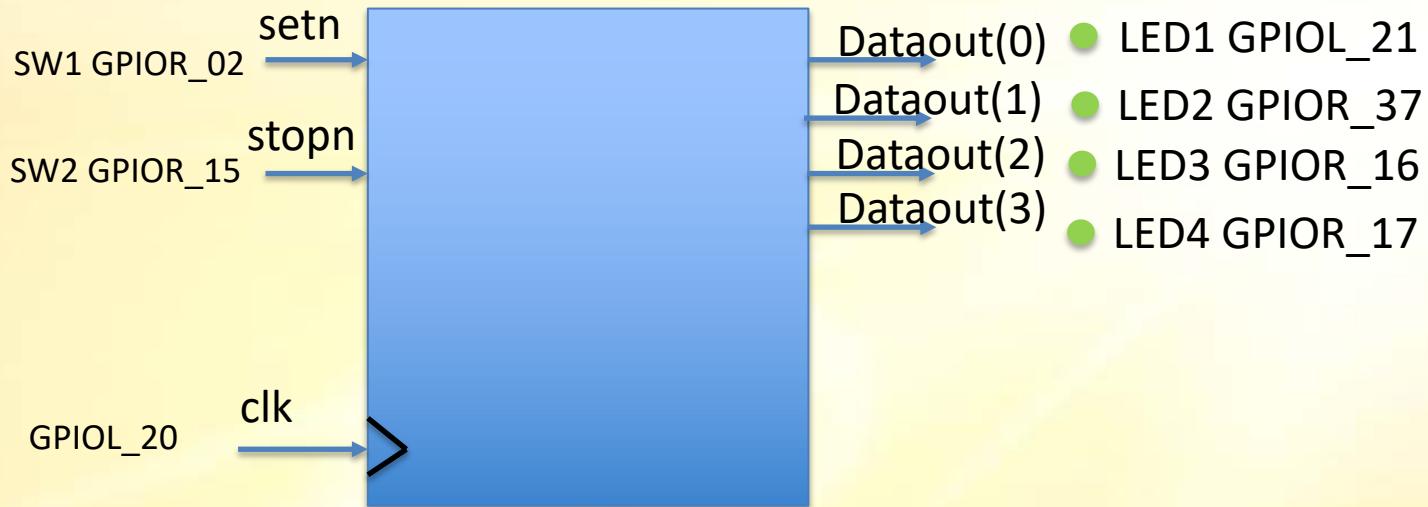
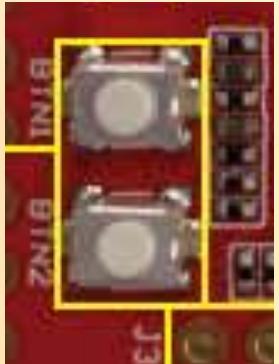


Code Editor

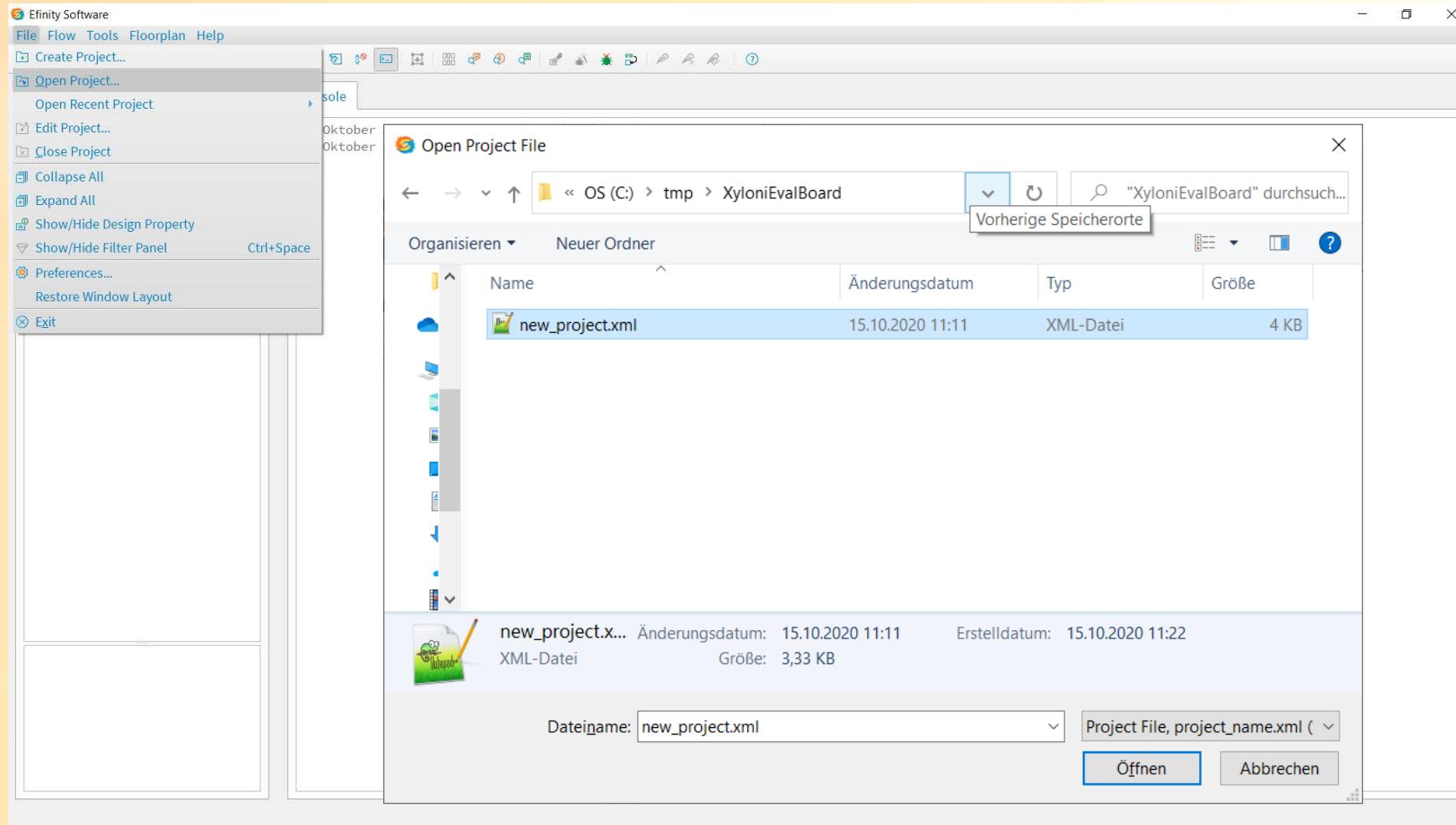
counter.vhd x

```
1 -- small example design for the Xylon Efinix Eval Board
2 -- By Harald Werner
3 -- 15.10.2020
4 library ieee;
5 use ieee.std_logic_1164.all;
6 use ieee.std_logic_unsigned.all;
7
8 entity counter is
9   port ( clk      : in std_logic;
10        setn    : in std_logic;
11        stopn   : in std_logic;
12        Dataout : out std_logic_vector(3 downto 0));
13 end counter;
14
15 architecture vers1 of counter is
16   signal cnt: std_logic_vector ( 29 downto 0 ) := (others => '0');
17 begin
18   cnt_proc : process(clk, setn)
19   begin
20     if setn = '0' then
21       cnt    <= (others => '1');
22       dataout <= (others => '1');
23     elsif clk'event and clk = '1' then
24       if stopn = '0' then
25         cnt <= cnt;
26       else
27         cnt <= cnt +1;
28       end if;
29     end if;
30     Dataout <= cnt(17 downto 14);           --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
31     Dataout <= cnt(29 downto 26);          --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
32   end process;
```

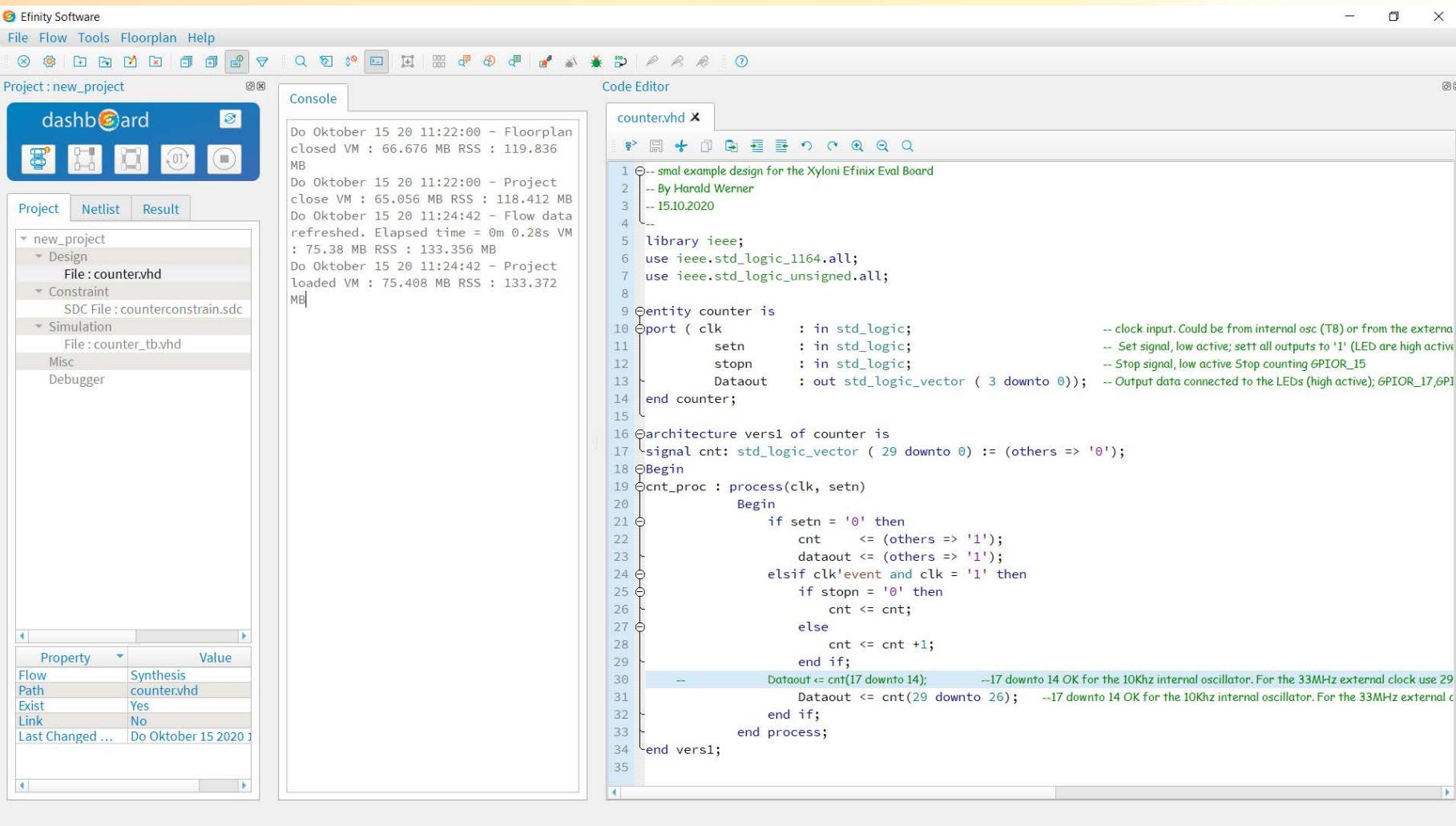
# Design / Board Connection



# Open Efinity new\_project.xml



# Double-Click on counter.vhd

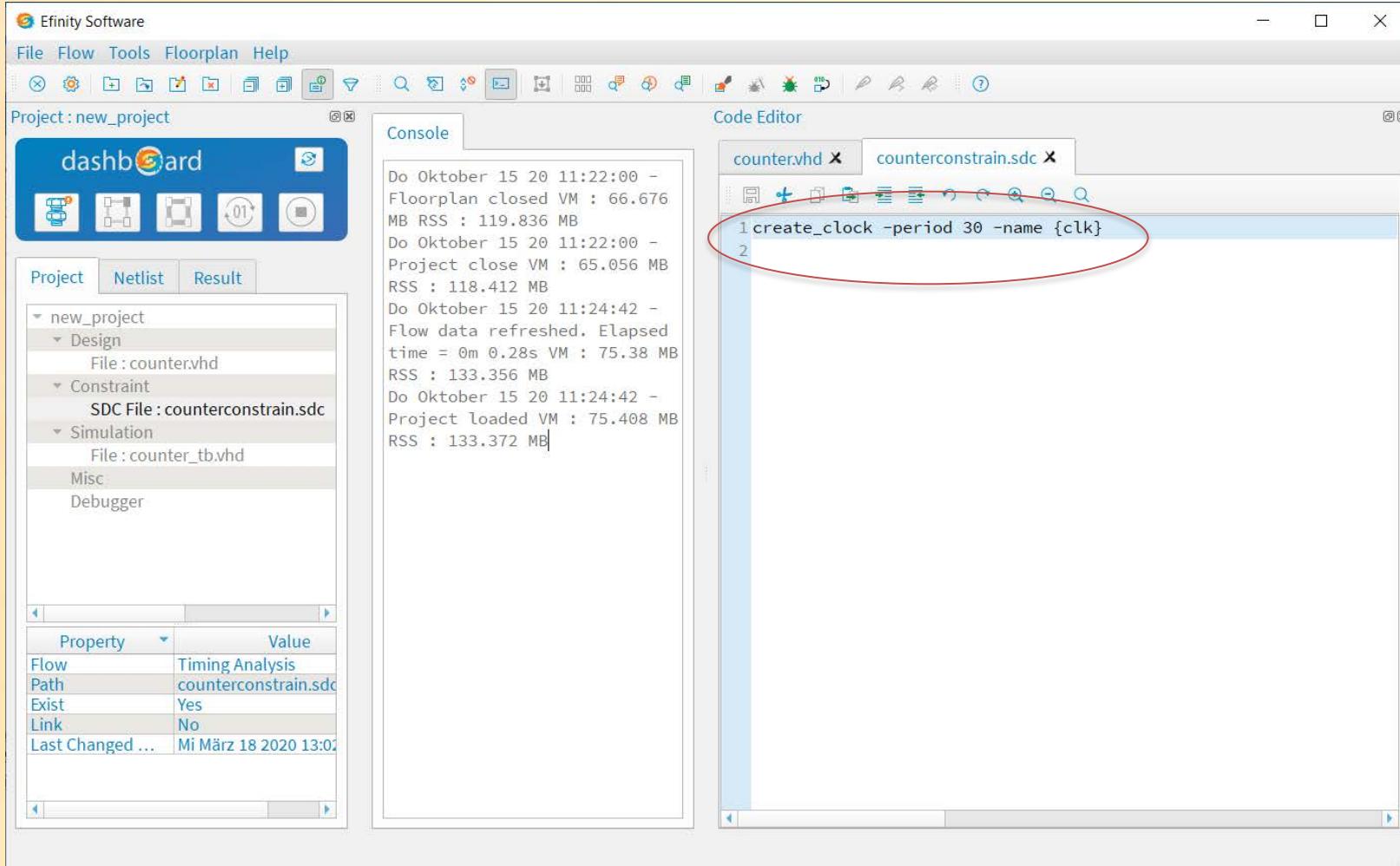


The screenshot shows the Efinix Software interface. The top menu bar includes File, Flow, Tools, Floorplan, and Help. The left sidebar displays a project named 'new\_project' with sub-sections Design (File: counter.vhd), Constraint (SDC File: counterconstrain.sdc), Simulation (File: counter\_tb.vhd), Misc, and Debugger. The main area features a 'Console' window showing build logs and a 'Code Editor' window displaying the VHDL code for 'counter.vhd'. The code defines a counter entity with four ports: clk, setn, stopn, and Dataout. It includes an architecture 'vers1' with a process that updates the counter based on setn and stopn signals, and outputs data to Dataout.

```
1 -- small example design for the Xylonix Efinix Eval Board
2 -- By Harald Werner
3 -- 15.10.2020
4 --
5 library ieee;
6 use ieee.std_logic_1164.all;
7 use ieee.std_logic_unsigned.all;
8
9 entity counter is
10    port ( clk      : in std_logic;
11           setn     : in std_logic;
12           stopn    : in std_logic;
13           Dataout  : out std_logic_vector ( 3 downto 0));
14 end counter;
15
16 architecture vers1 of counter is
17   signal cnt: std_logic_vector ( 29 downto 0) := (others => '0');
18 begin
19   cnt_proc : process(clk, setn)
20   begin
21     if setn = '0' then
22       cnt    <= (others => '1');
23       dataout <= (others => '1');
24     elsif clk'event and clk = '1' then
25       if stopn = '0' then
26         cnt <= cnt;
27       else
28         cnt <= cnt +1;
29       end if;
30     -- Dataout <= cnt(17 downto 14); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29
31     -- Dataout <= cnt(29 downto 26); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external c
32     end if;
33   end process;
34 end vers1;
```

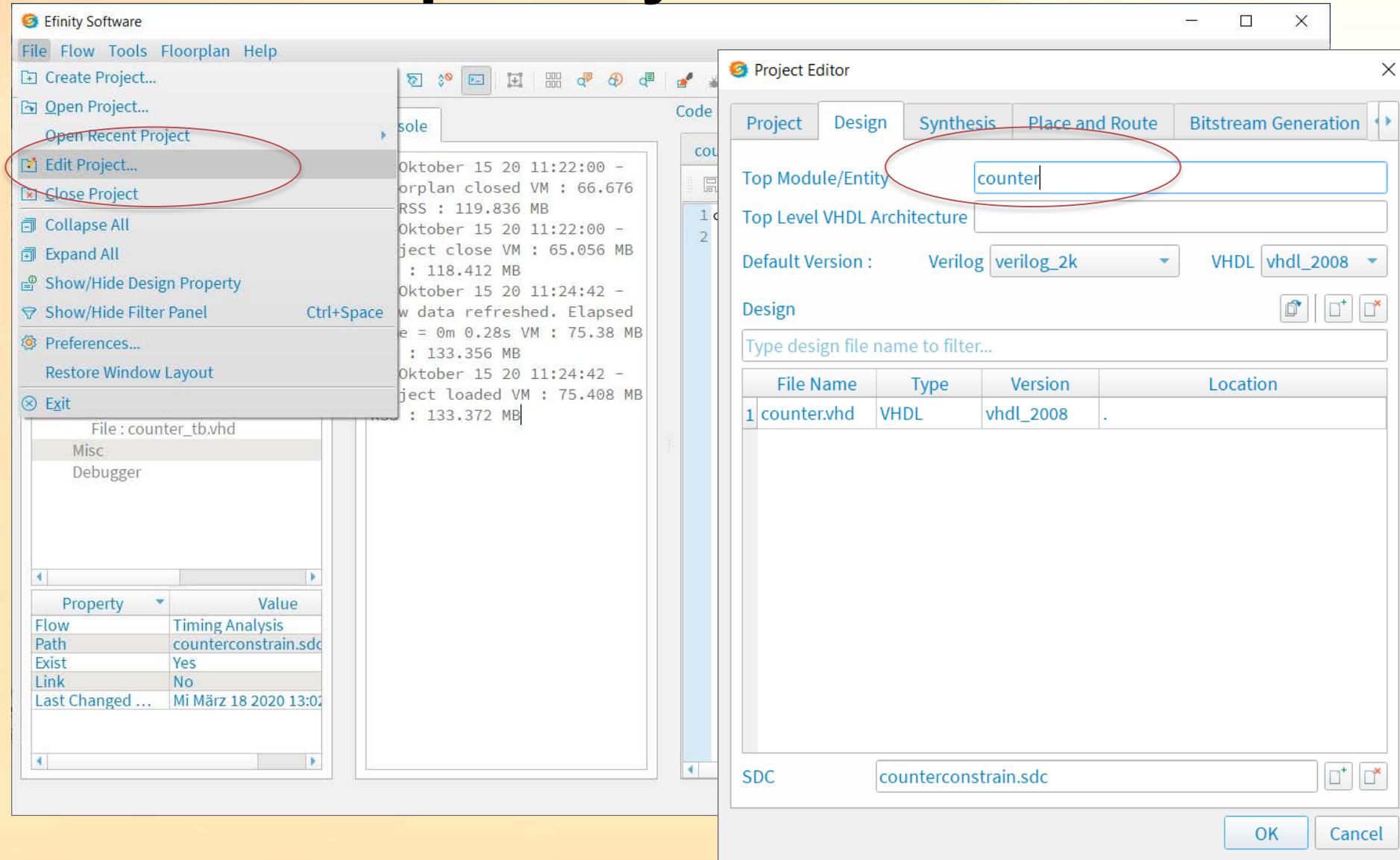
counter.vhd opens  
in the Code Editor

# Double-Click on the Timing Constraint File counterconstrain.sdc



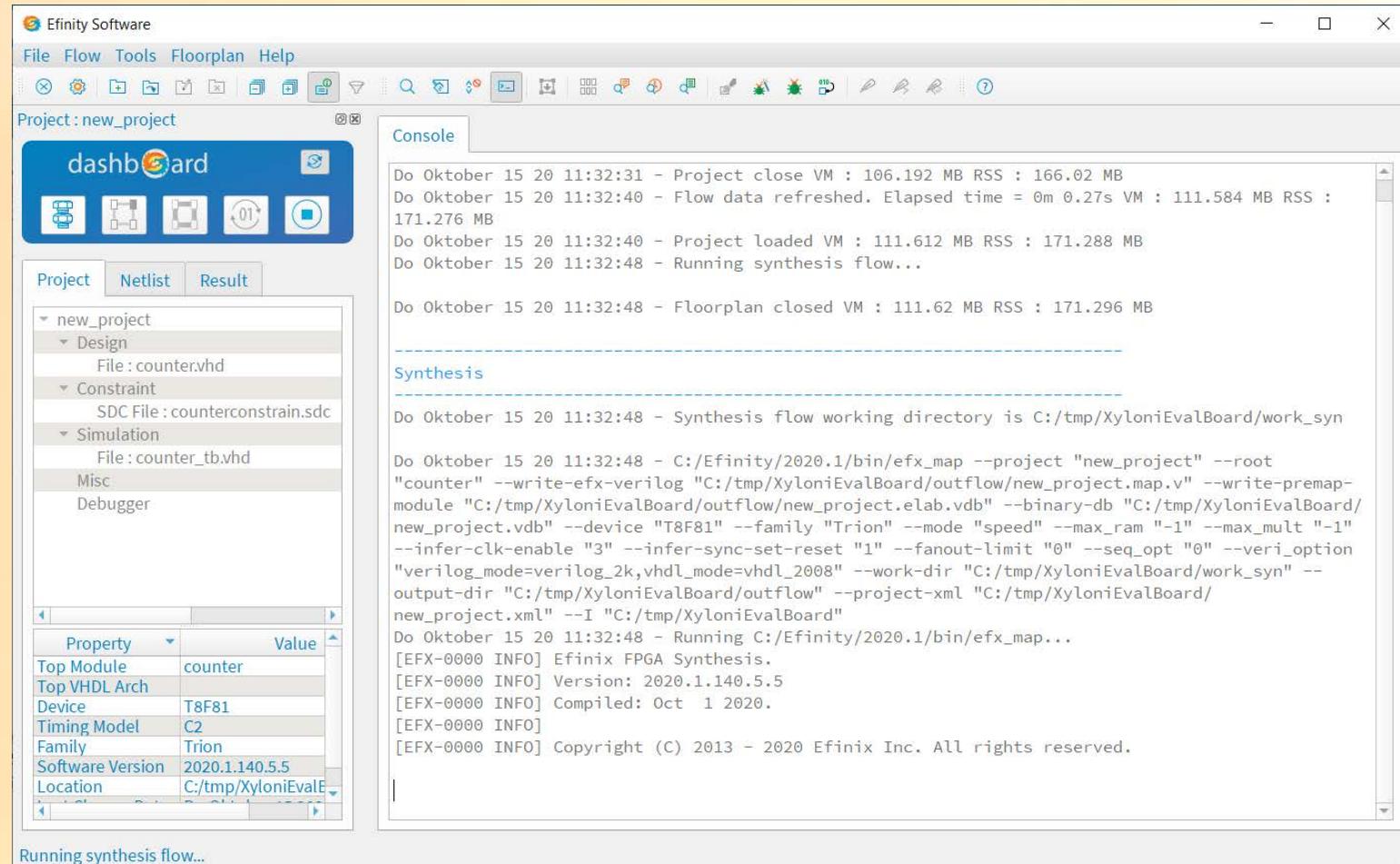
counterconstrain.sdc  
opens and you can  
see the 30 ns period  
constraint for the 33  
MHz clock

# Set the Top Entity Name



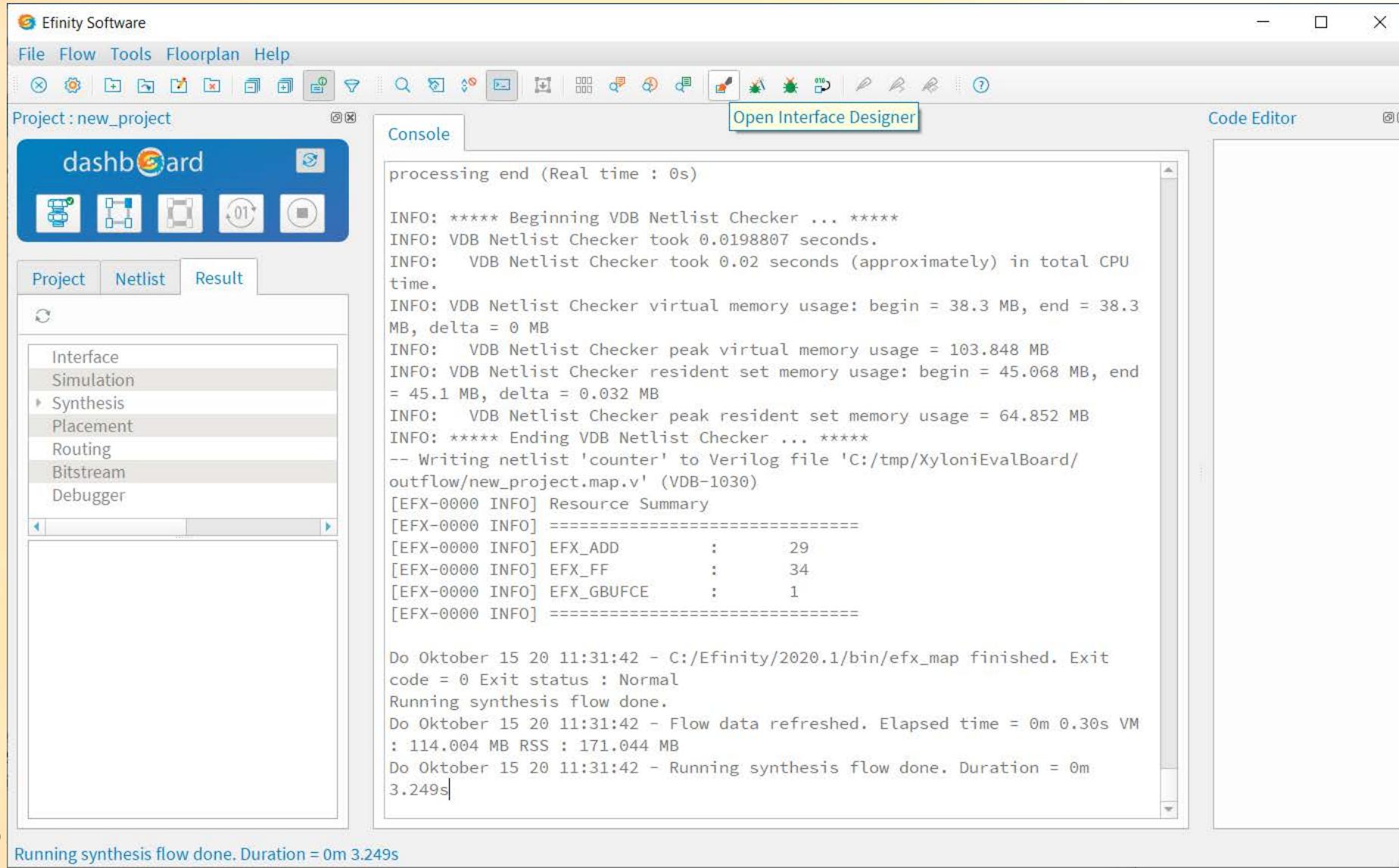
Enter counter  
as the Top  
Module/Entity  
and click OK

# Run the Whole Flow or Just Synthesis



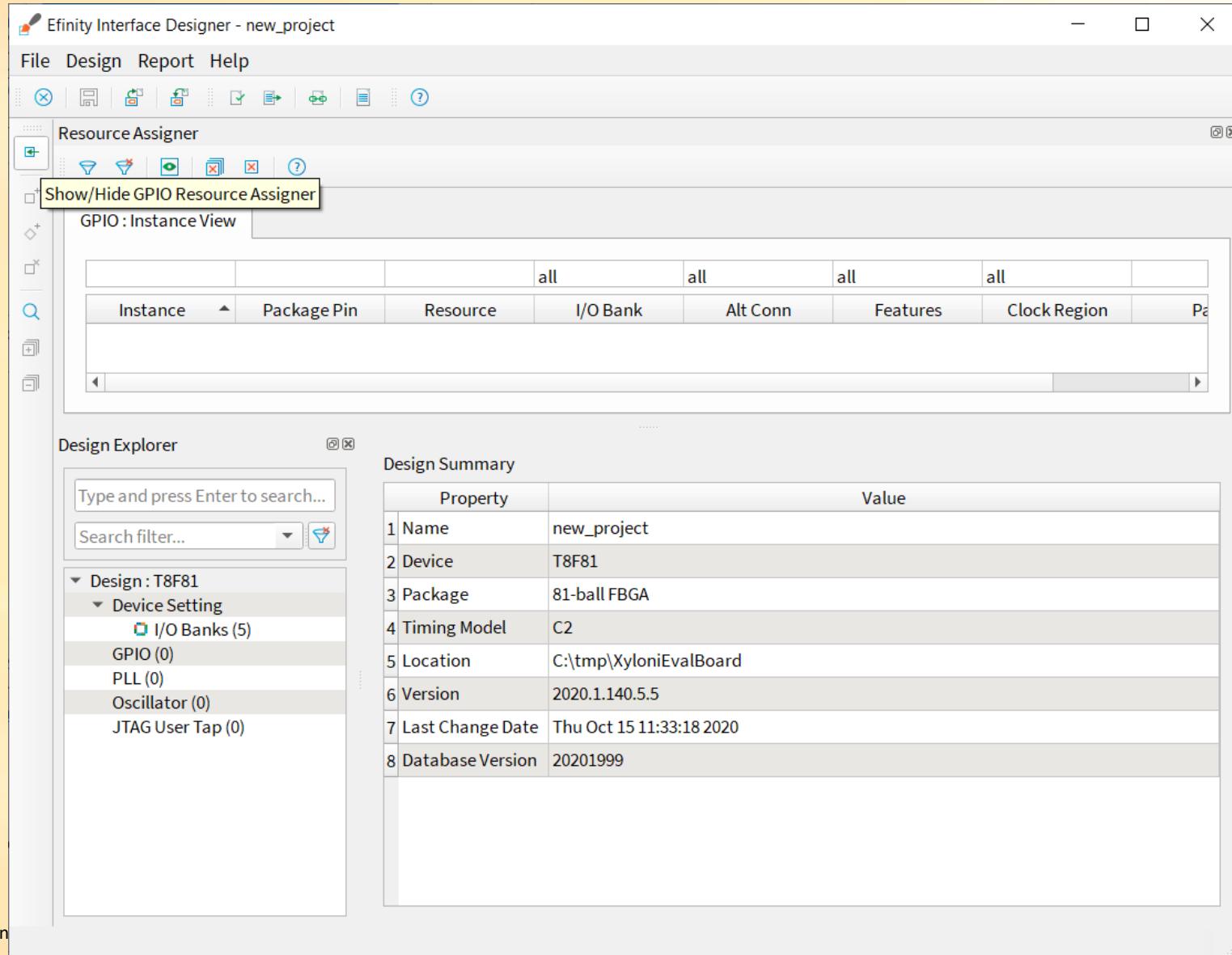
- If the Automated flow button is grayed out, click the button to activate the automated flow.
- Click the synthesis icon and the flow runs automatically

# Assign the Top-Level Signals to Pins



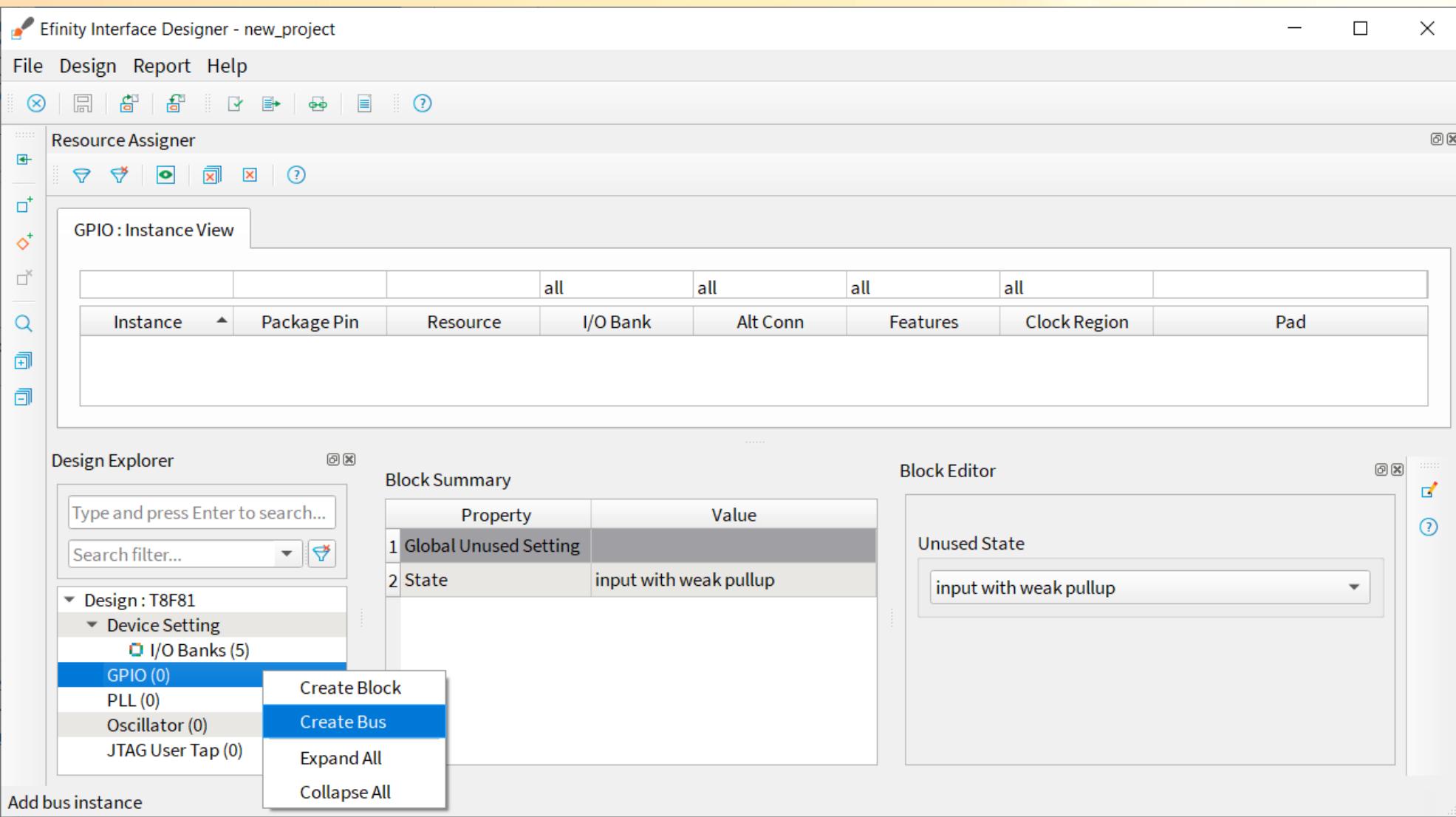
Open the Interface Designer by clicking the toolbar icon

# Show GPIO Resource Assigner



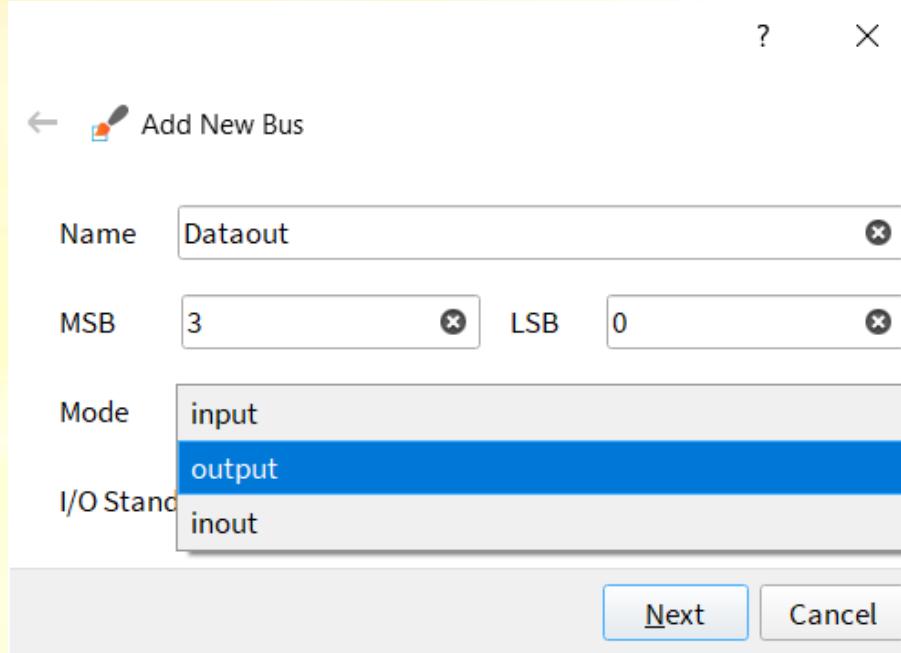
Click the first icon in the side toolbar

# Select GPIO, RMB, Create Bus



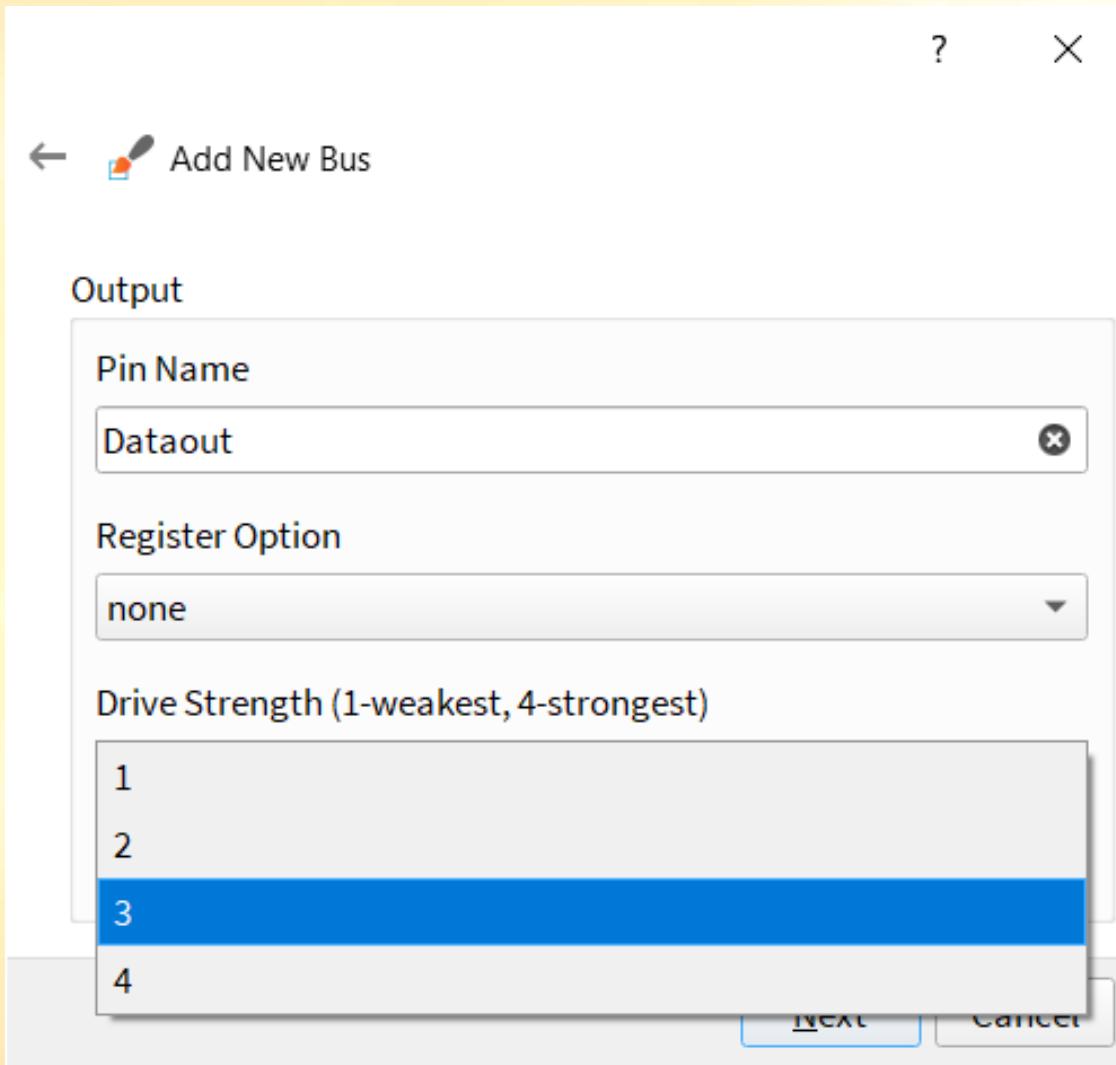
Right-click the GPIO heading and choose Create Bus

# Create Output Bus Dataout(3 downto 0)

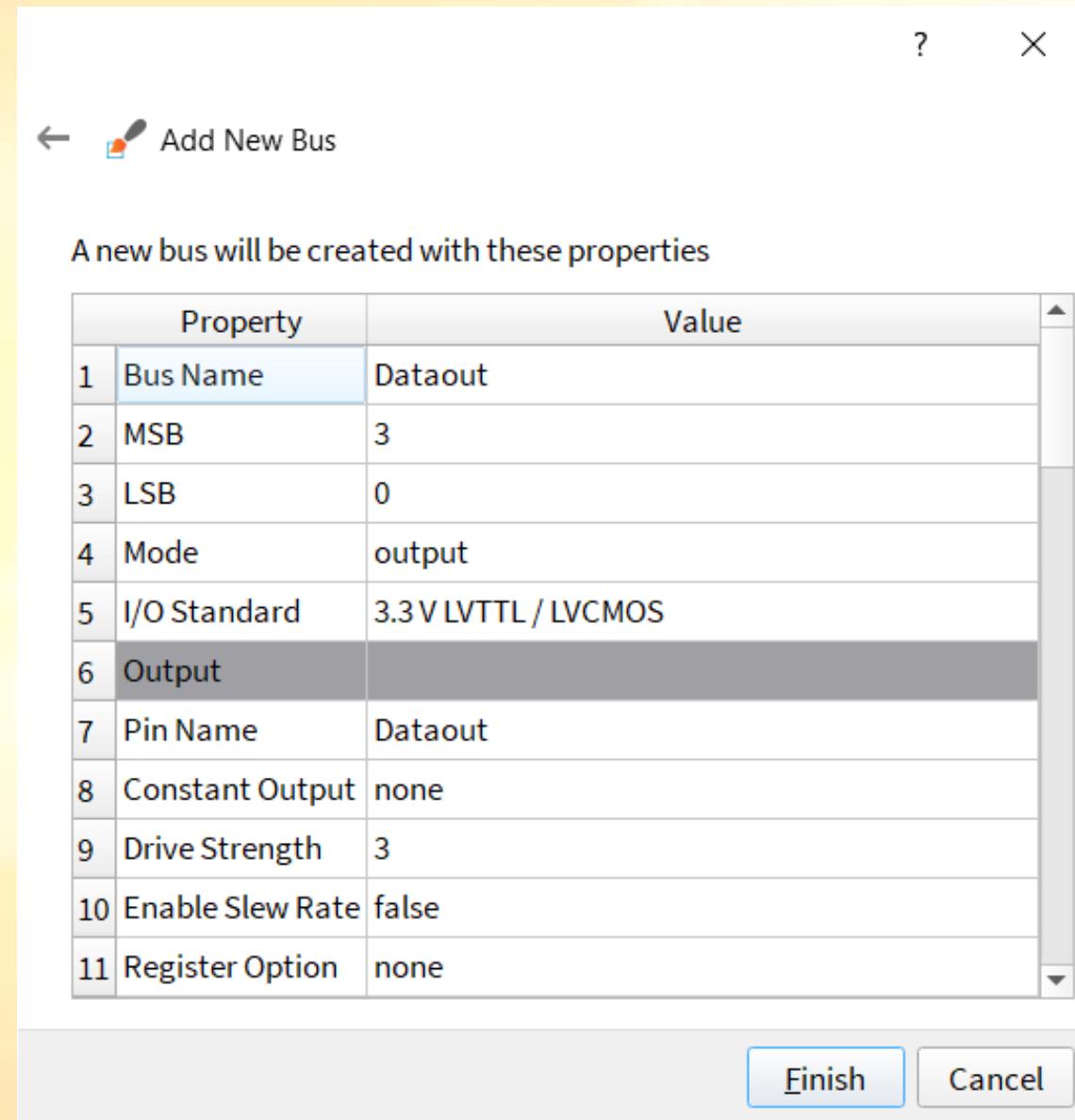


Name: Dataout  
MSB: 3  
LSB: 0  
Mode: output  
Click Next

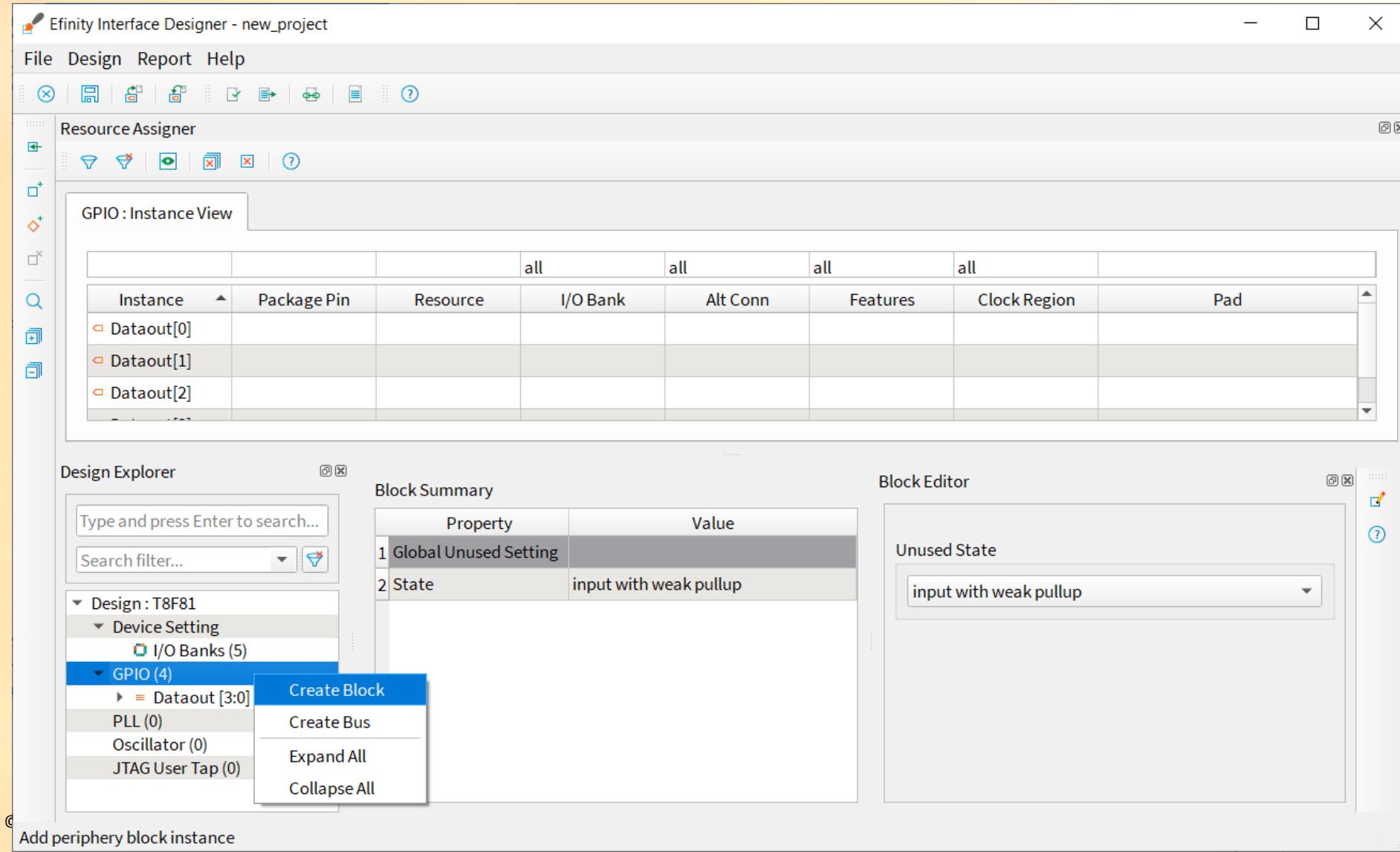
# Set Drive Strength to 3; Click Next



# Click Finish

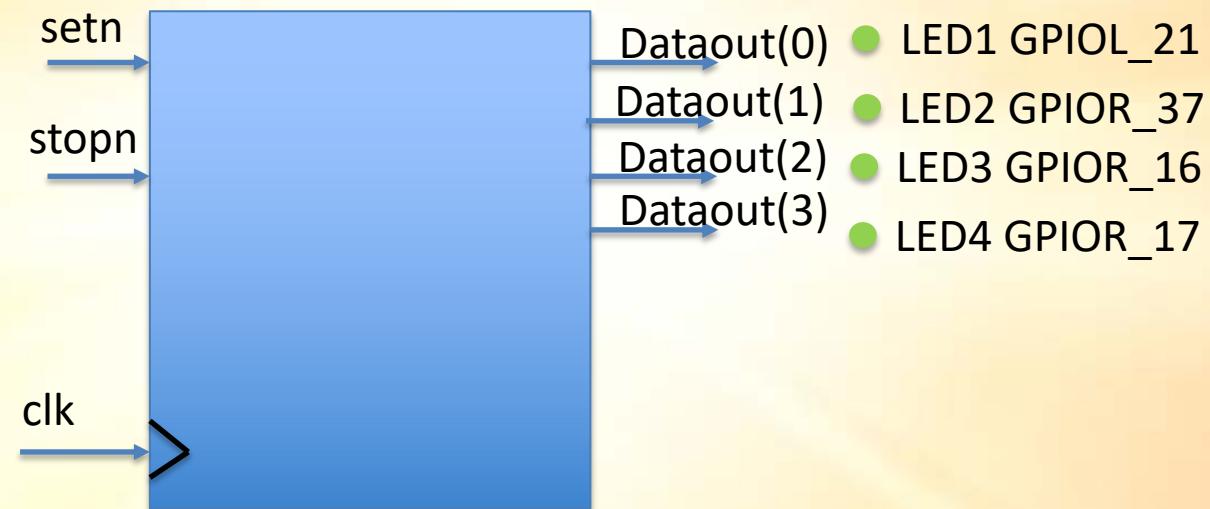
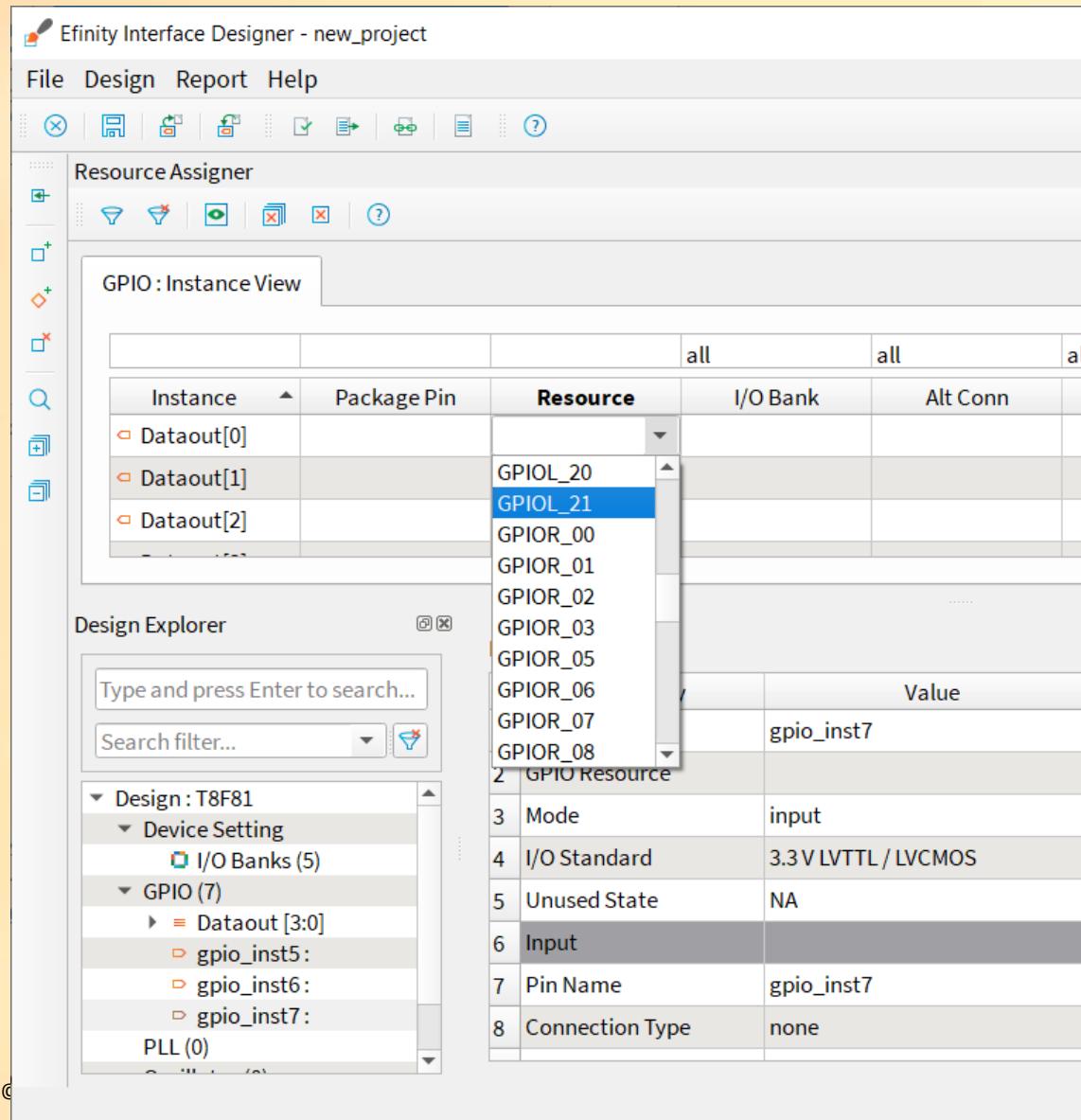


# Adding the Additional Pins clk, stopn, setn



Right-click  
GPIO > Create  
Block for each  
pin

# Select GPIO: Instance View Dataout[0]->Resource



Dataout[0] ->GPIO\_21

# Select GPIO: Instance View Dataout[1]->Resource

Efinix Interface Designer - new\_project

File Design Report Help

Resource Assigner

GPIO : Instance View

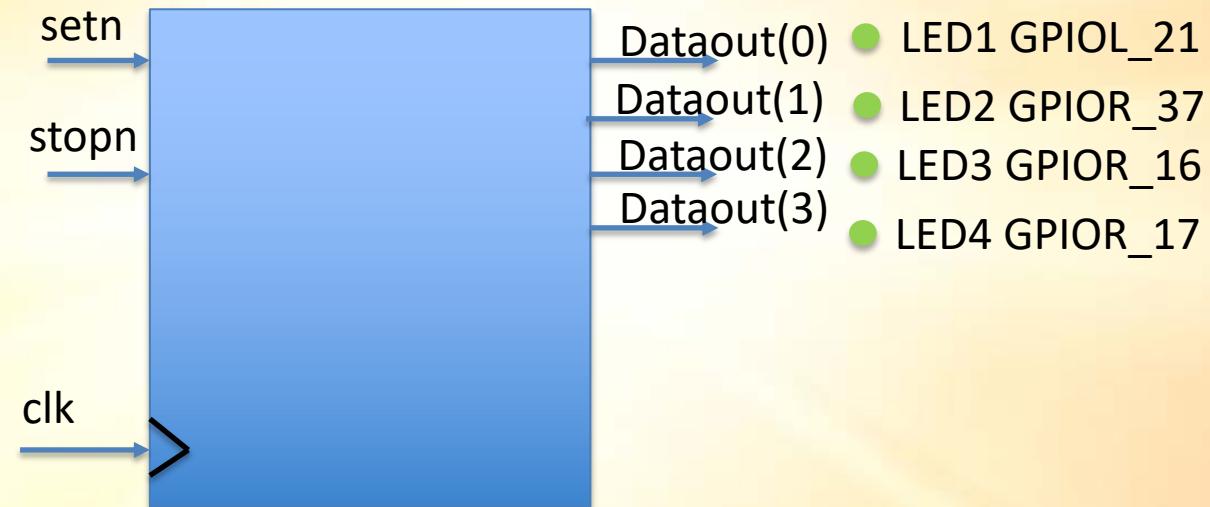
Instance	Package Pin	Resource	I/O Bank	Alt Conn	Fe
Dataout[0]	B3	GPIO_21	1B	None	None
Dataout[1]		GPIO_26			
Dataout[2]		GPIO_27			
		GPIO_28			
		GPIO_30			
		GPIO_31			
		GPIO_32			
		GPIO_34			
		GPIO_35			
		GPIO_36			
		GPIO_37			

Design Explorer

Type and press Enter to search...

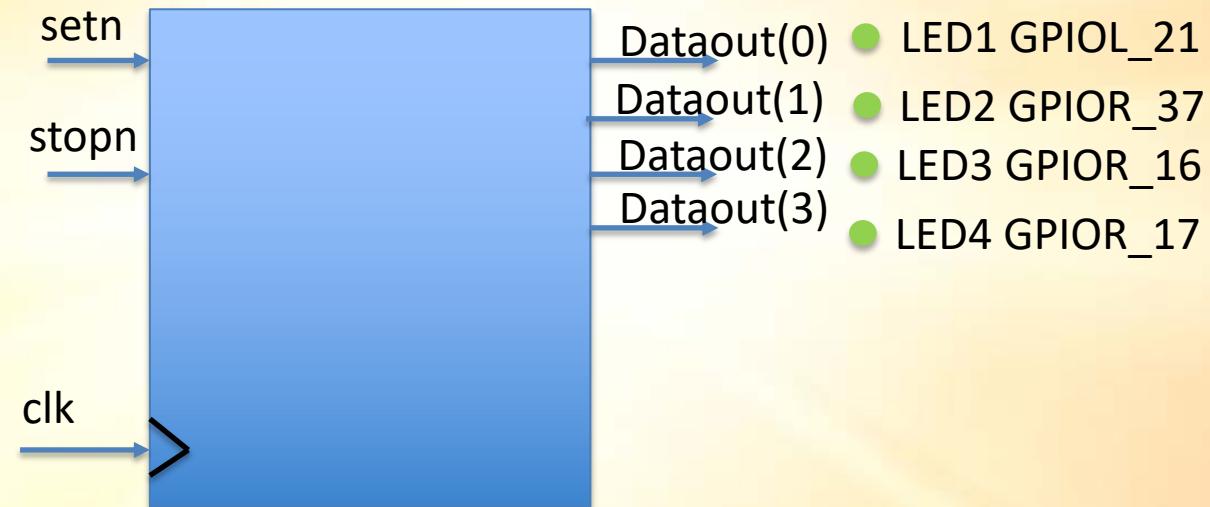
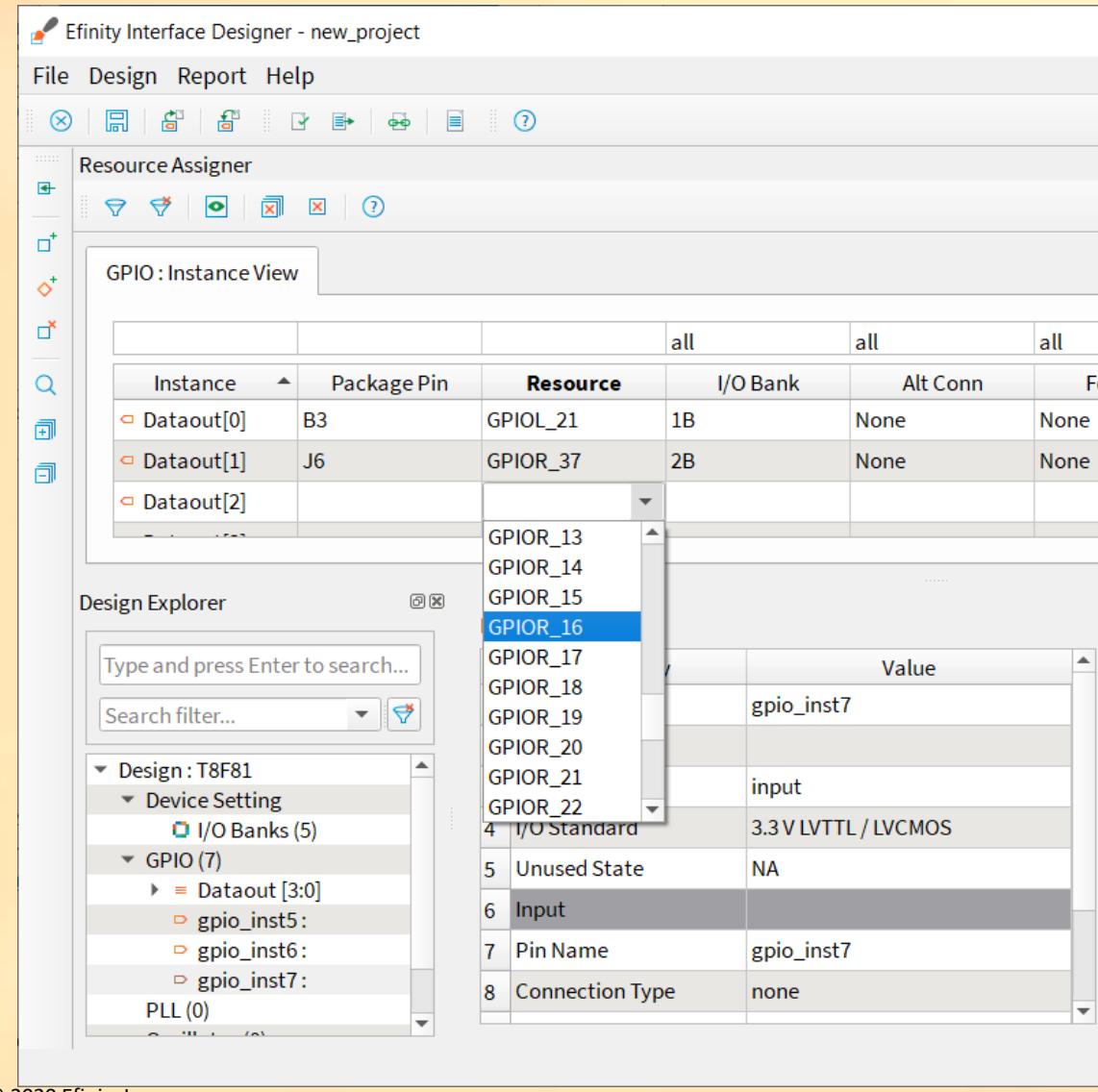
Search filter...

Design : T8F81  
Device Setting  
I/O Banks (5)  
GPIO (7)  
Dataout [3:0]  
gpio\_inst5:  
gpio\_inst6:  
gpio\_inst7:  
PLL (0)



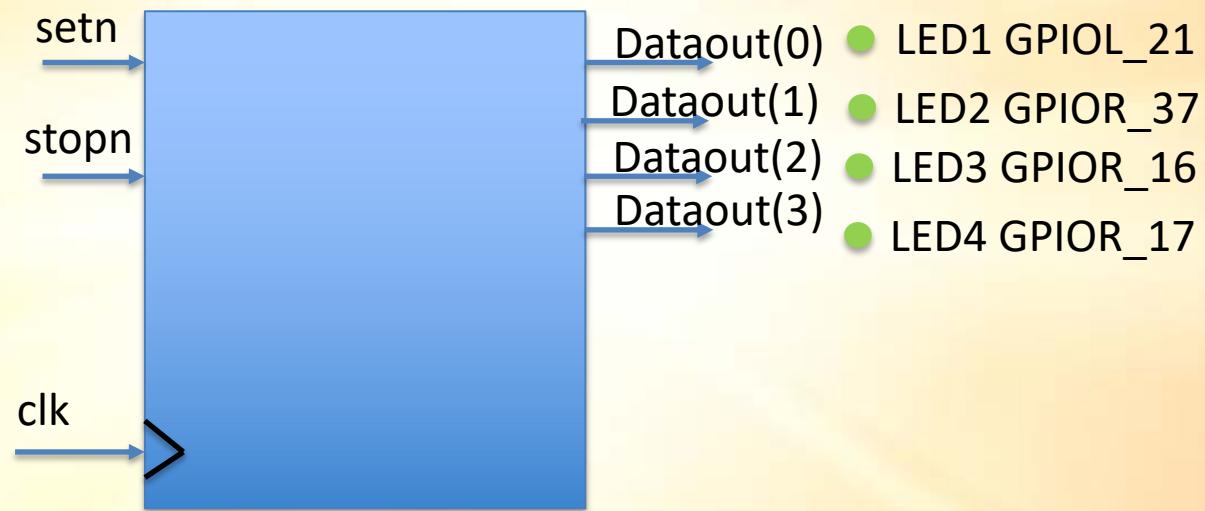
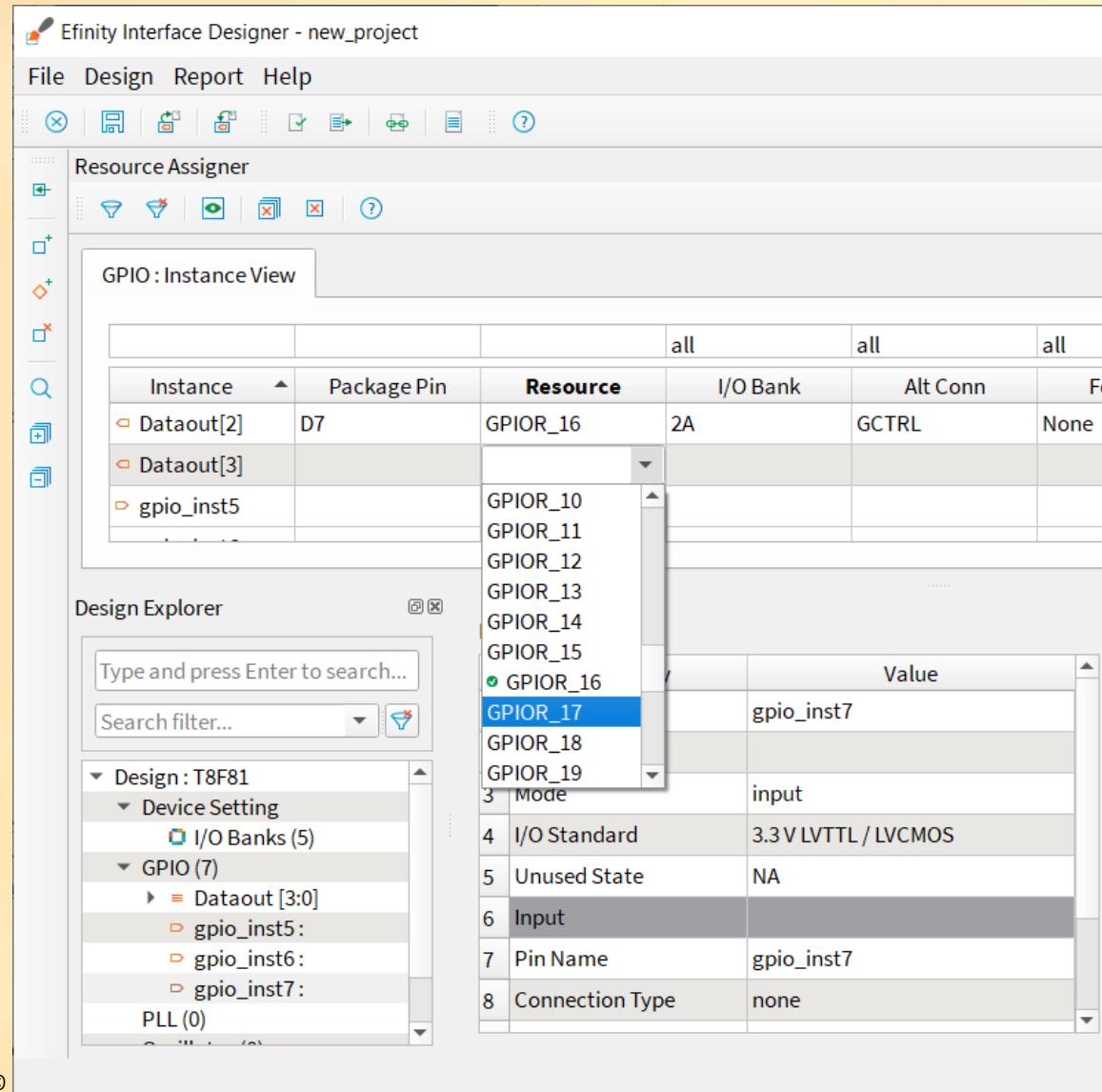
Dataout[1] ->GPIOR\_37

# Select GPIO: Instance View Dataout[2]->Resource



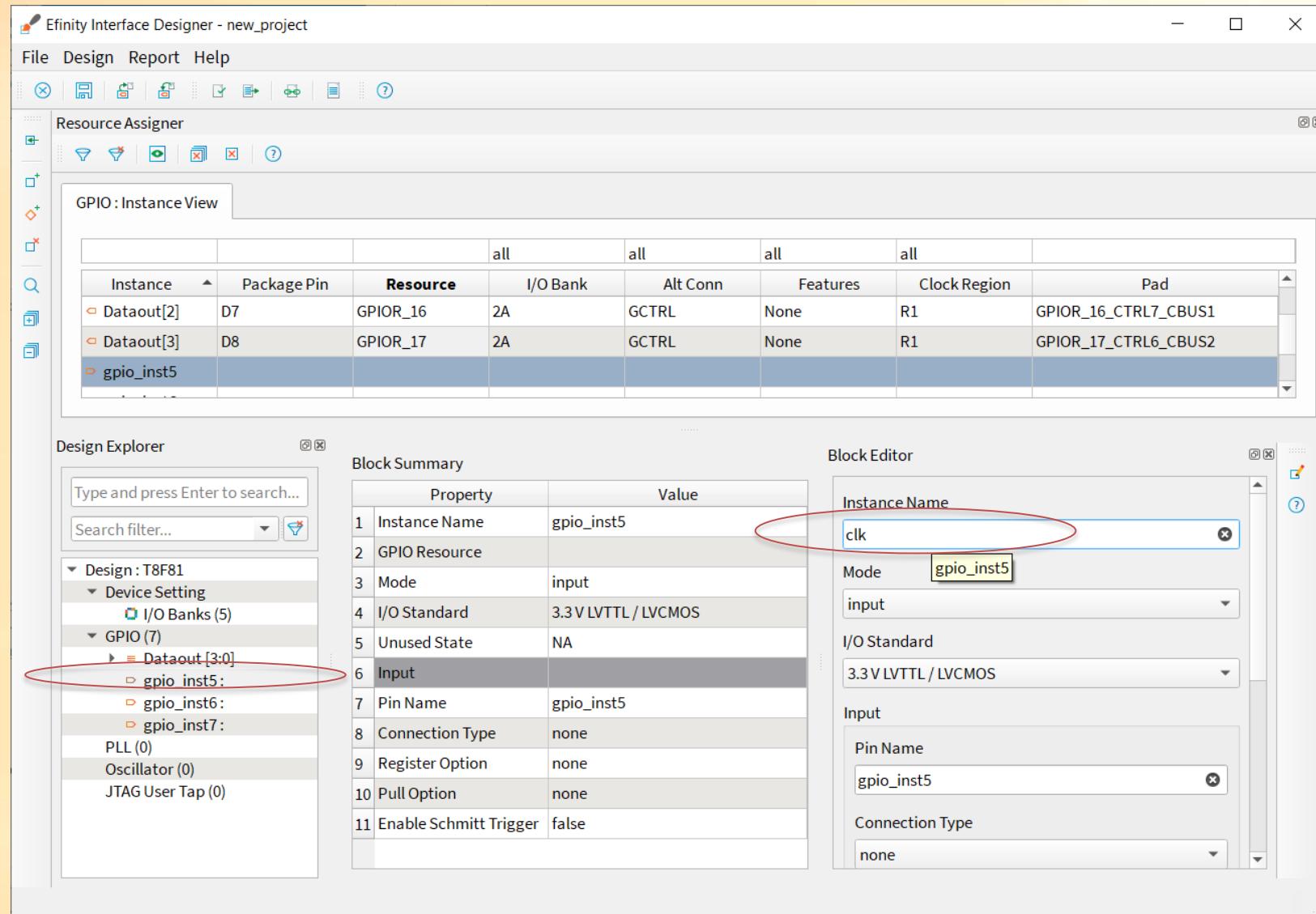
Dataout[2] ->GPIOR\_16

# Select GPIO: Instance View Dataout[3]->Resource



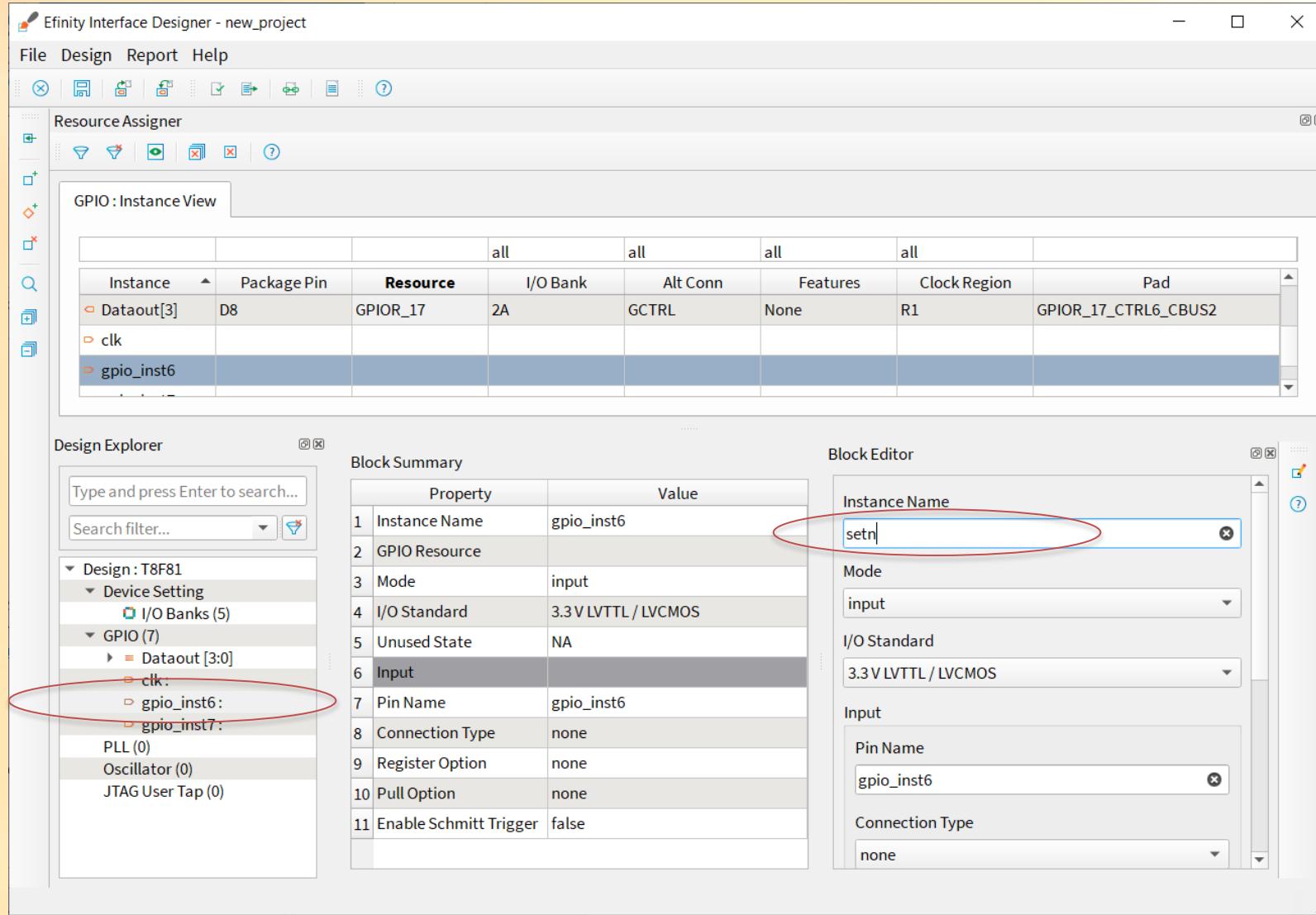
Dataout[3] ->GPIO\_R\_17

# Rename clk Input



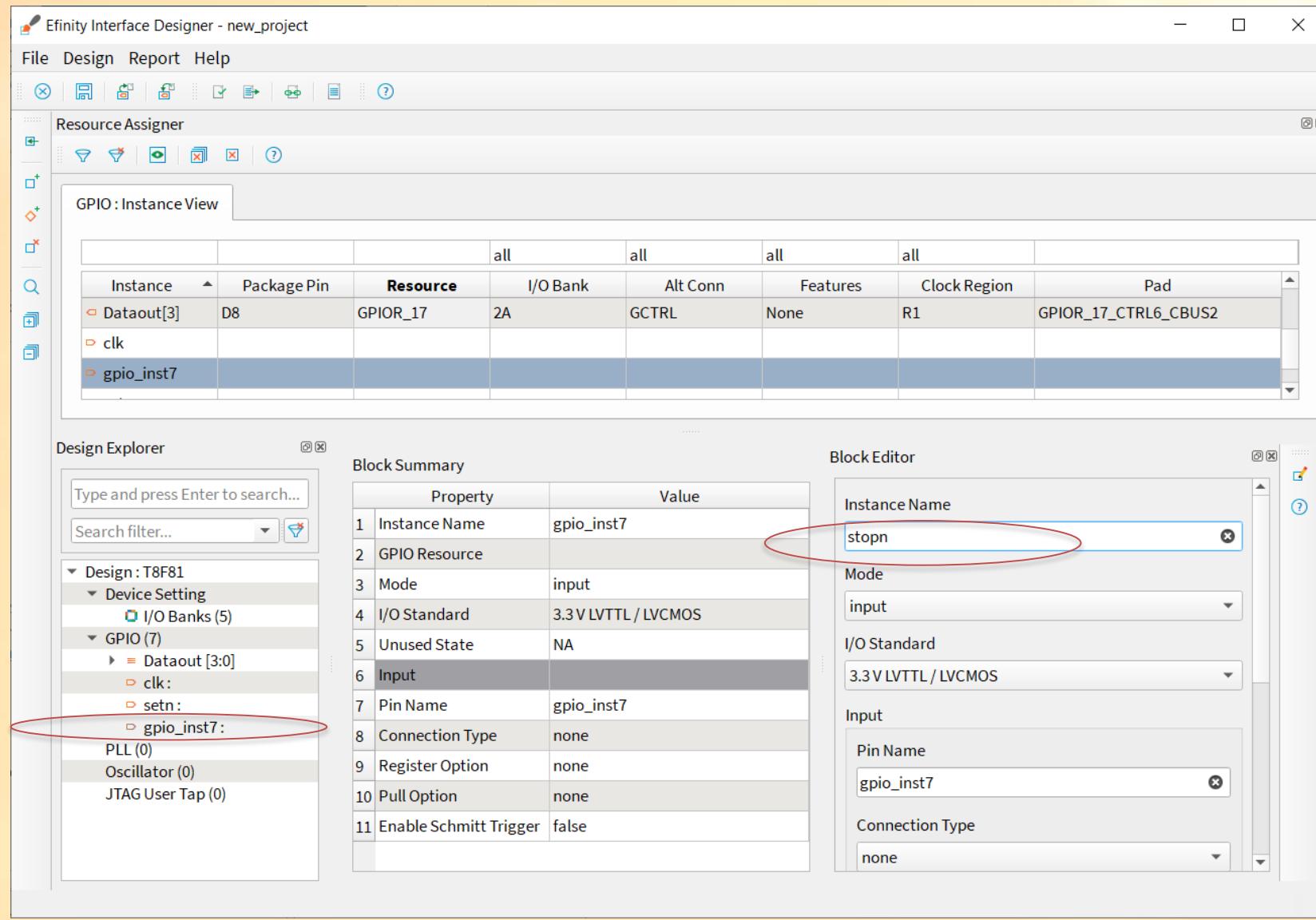
1. Select gpio\_inst5.
2. In the Block Editor, type clk as the Instance Name.
3. Press Enter!  
(Otherwise, the setting is not saved)

# Rename setn Input



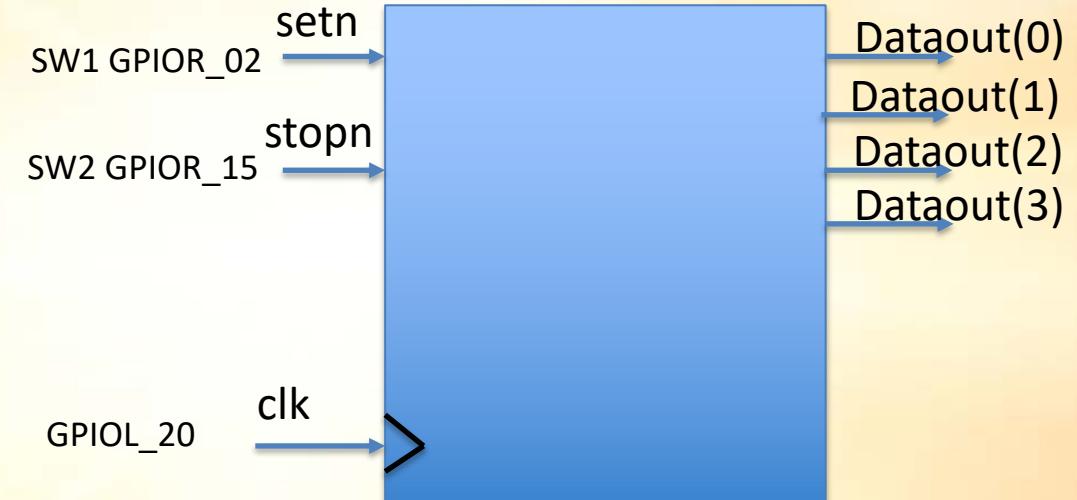
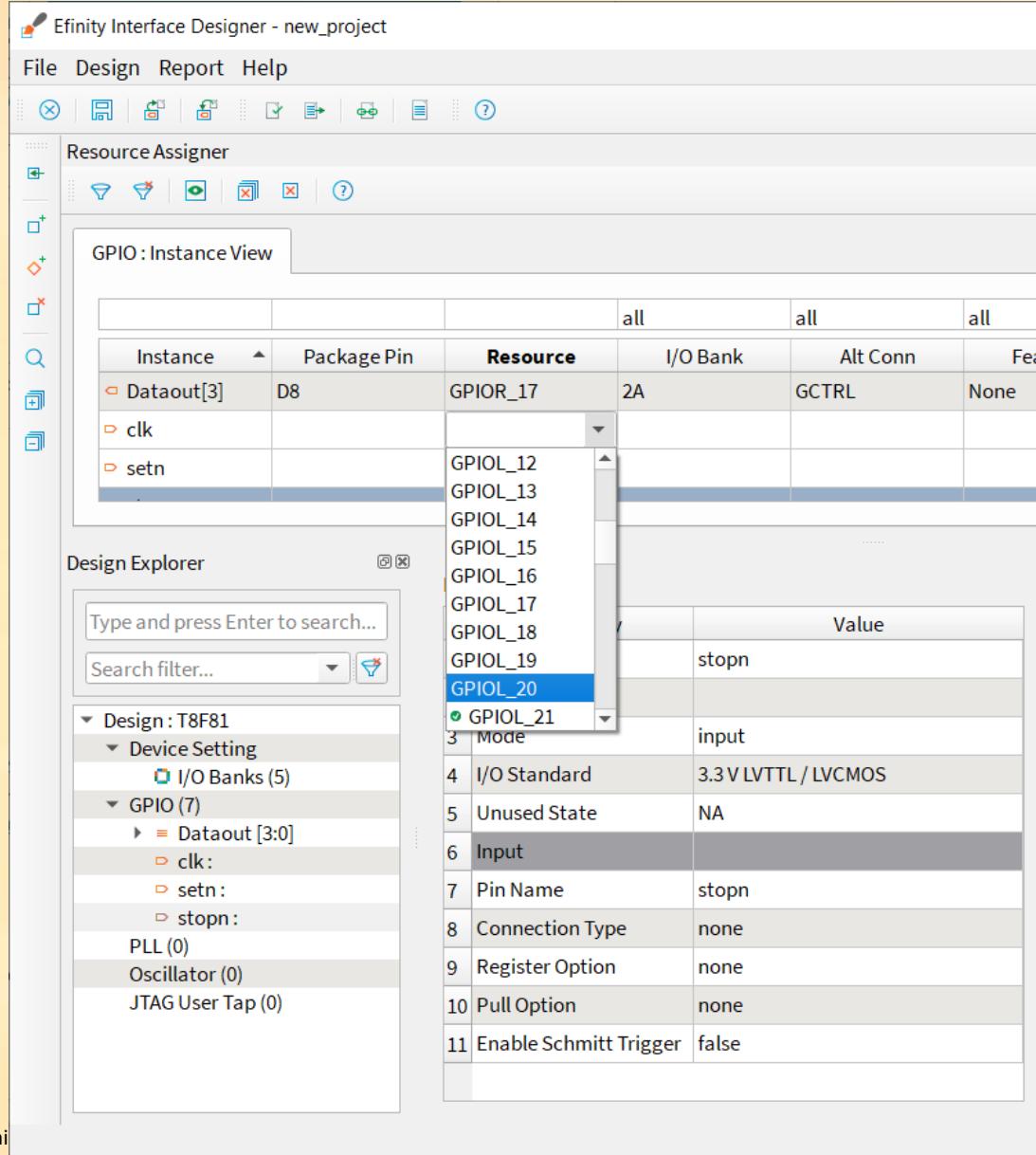
1. Select gpio\_inst6.
2. In the Block Editor, type setn as the Instance Name.
3. Press Enter!

# Rename stopn Input

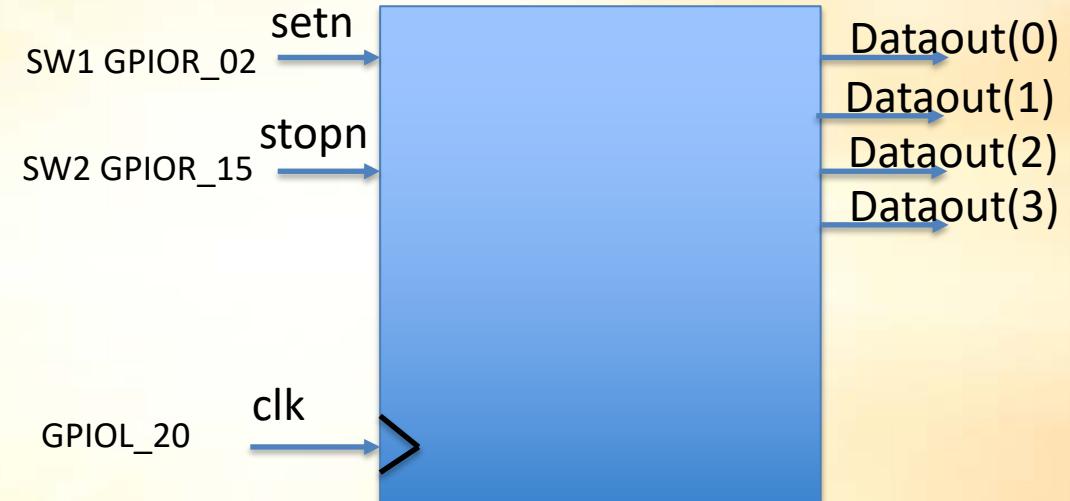
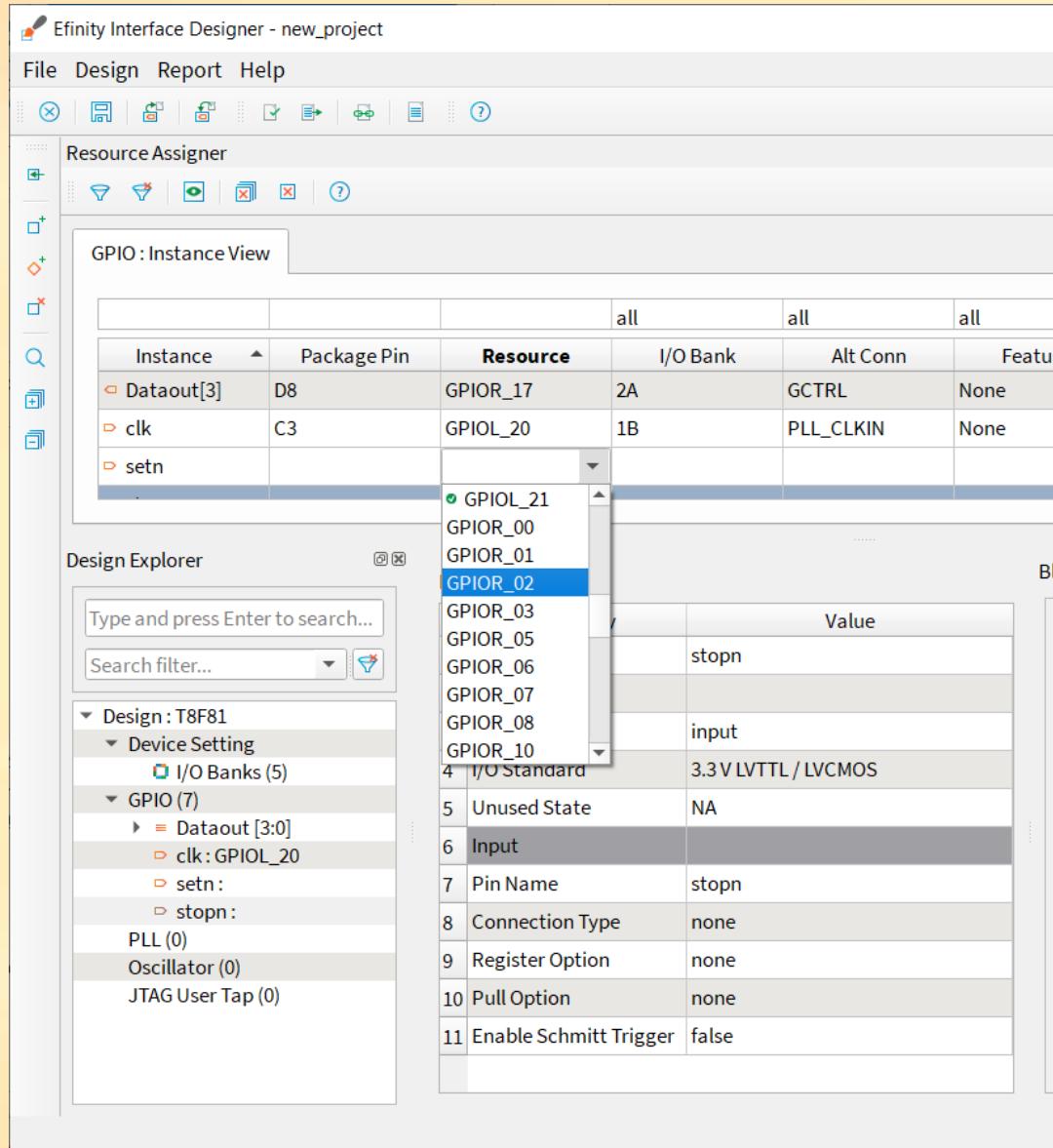


1. Select gpio\_inst7.
2. In the Block Editor, type stopn as the Instance Name.
3. Press Enter!

# Assign the Resource CLK=>GPIO\_L\_20



# Assign the Resource setn=>GPIO\_02



# Assign the Resource stopn=>GPIO\_15

Efinity Interface Designer - new\_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Feature
clk	C3	GPIOL_20	1B	PLL_CLKIN	None
setn	C5	GPIOR_02	2A	None	None
stopn					

Design Explorer

Type and press Enter to search...

Search filter...

Design : T8F81

Device Setting

I/O Banks (5)

GPIO (7)

- Dataout [3:0]
- clk : GPIOL\_20
- setn : GPIOR\_02
- stopn :

PLL (0)

Oscillator (0)

JTAG User Tap (0)

GPIOL\_20

GPIOR\_02

GPIOR\_15

GPIOR\_16

GPIOR\_17

GPIOR\_18

GPIOR\_19

stopn

Value

input

3.3 V LVTTL / LVCMOS

Unused State

NA

Input

stopn

Connection Type

none

Register Option

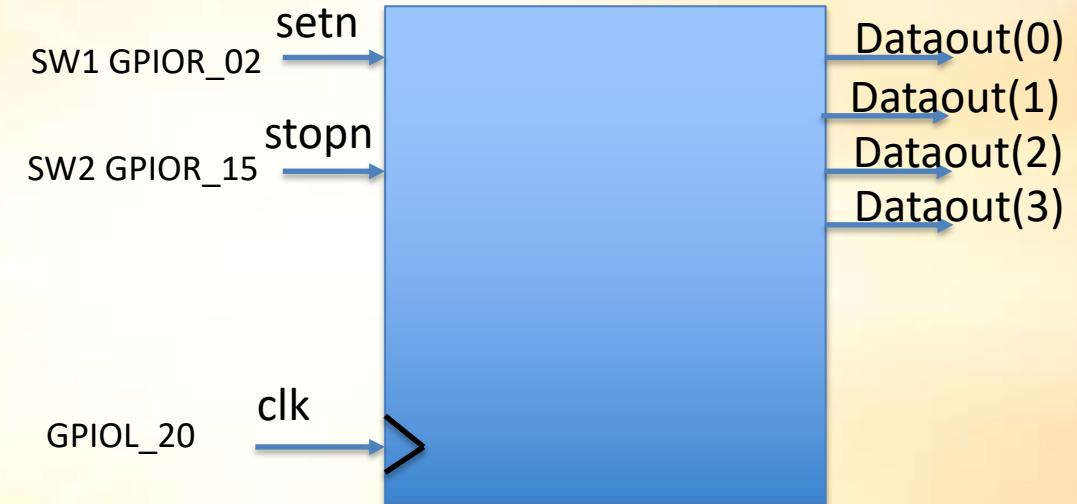
none

Pull Option

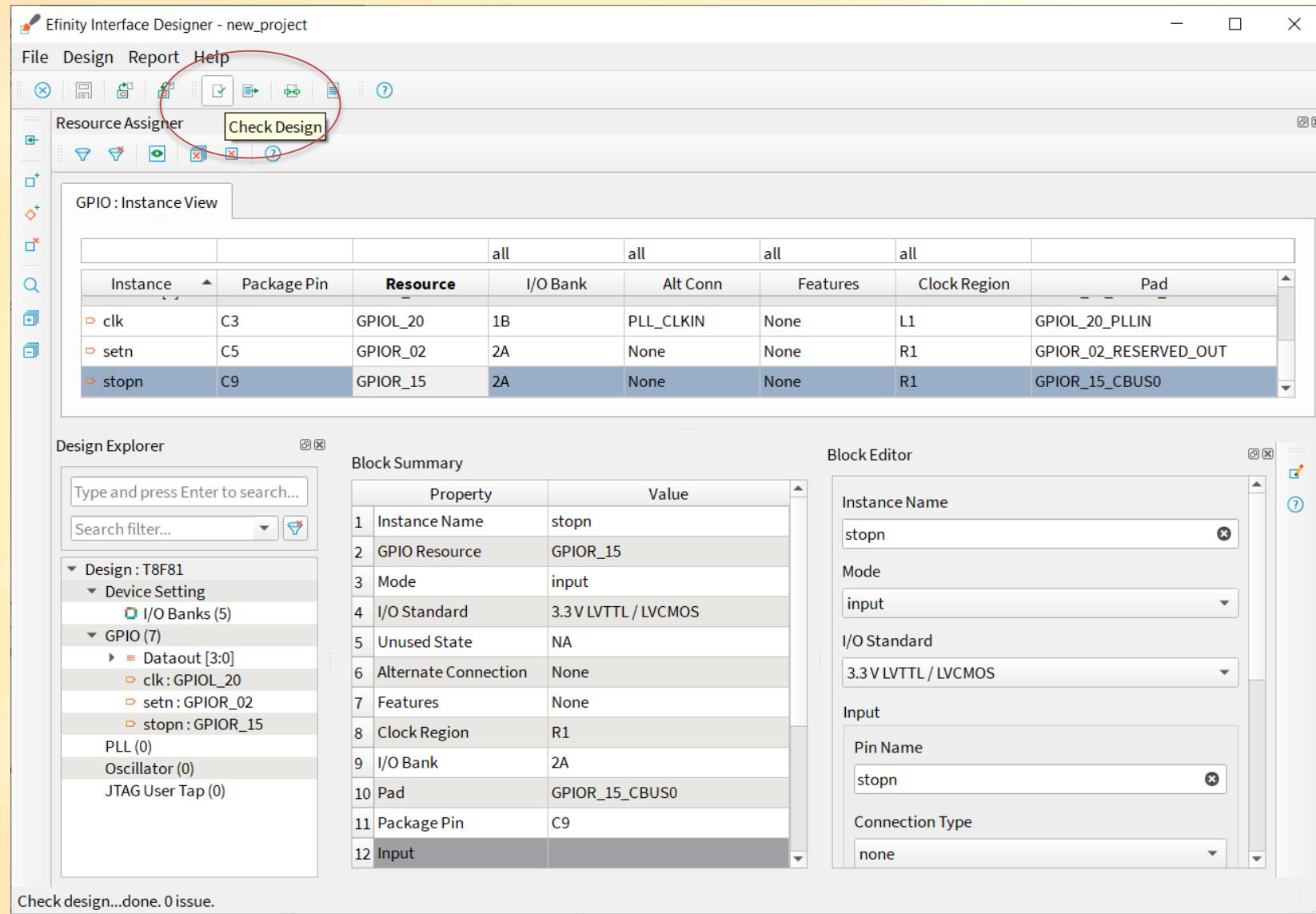
none

Enable Schmitt Trigger

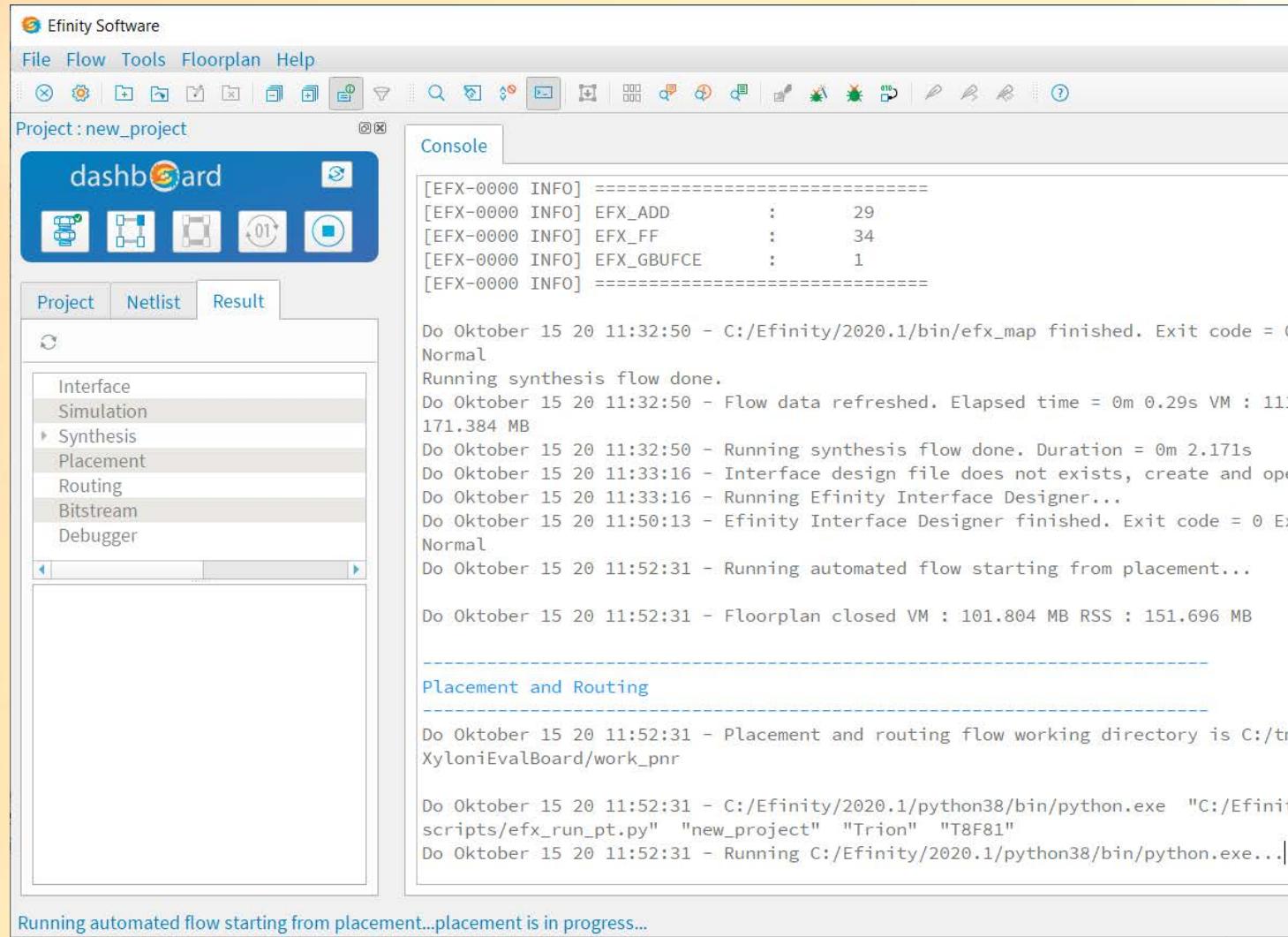
false



# Check the Design and Close the Interface Designer

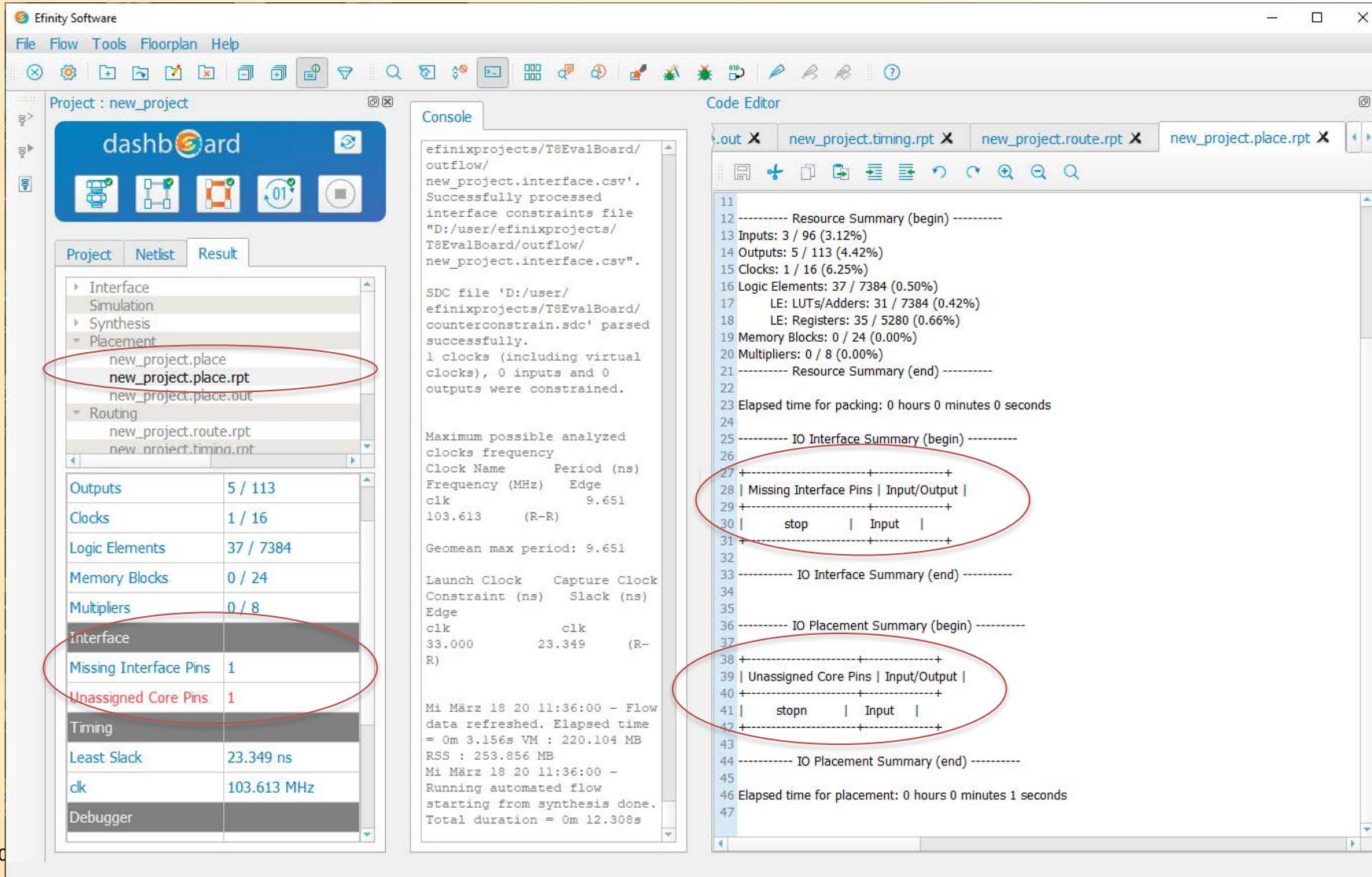


# Run the Flow by Clicking on Placement



- If the Automated flow button is grayed out, click the button to activate the automated flow 
- Click on the Place icon and the flow runs automatically 

# Fix Errors and Re-Run Flow



If you have an unassigned pin, the software reports it in the Placement report. Go back to Interface Designer, fix the name, and rerun the flow.

Typo in Interface Designer: **stop** instead of **stopn**

# Check Static Timing

The screenshot shows the Efinix Software interface. The dashboard on the left displays project statistics: Interface (0), Simulation (0), Synthesis (0), Placement (0), Routing (0), and Periphery Resource counts for GPIO (7/55), JTAG User TAP (0/2), Oscillator (0/1), and PLL (0/1). The Project tree on the right shows nodes like new\_project.route.rpt, new\_project.timing.rpt, and new\_project.route.out. The Code Editor window on the right displays the contents of 'new\_project.timing.rpt'. The report includes environmental constraints (temperature: 0C to 85C, voltage: 1.1V +/-50mV, speedgrade: 2, technology: s40ll, status: final), a table of contents, and a detailed clock frequency summary. A red oval highlights the clock frequency summary section, which lists user target constrained clocks (clk period 30.000 ns, frequency 33.333 MHz) and maximum possible analyzed clocks (clk period 9.934 ns, frequency 100.666 MHz).

```
temperature : 0C to 85C
voltage : 1.1V +/-50mV
speedgrade : 2
technology : s40ll
status : final

----- Table of Contents (begin) -----
1. Clock Frequency Summary
2. Clock Relationship Summary
3. Path Details for Max Critical Paths
4. Path Details for Min Critical Paths
----- Table of Contents (end) -----

----- 1. Clock Frequency Summary (begin) -----
28 User target constrained clocks
29 Clock Name      Period (ns)   Frequency (MHz)   Waveform   Source
30 clk            30.000        33.333          {0.000 15.000}
31
32 Maximum possible analyzed clocks frequency
33 Clock Name      Period (ns)   Frequency (MHz)   Edge
34 clk            9.934         100.666        (R-R)
35
36 Geomean max period: 9.934
----- Clock Frequency Summary (end) -----
```

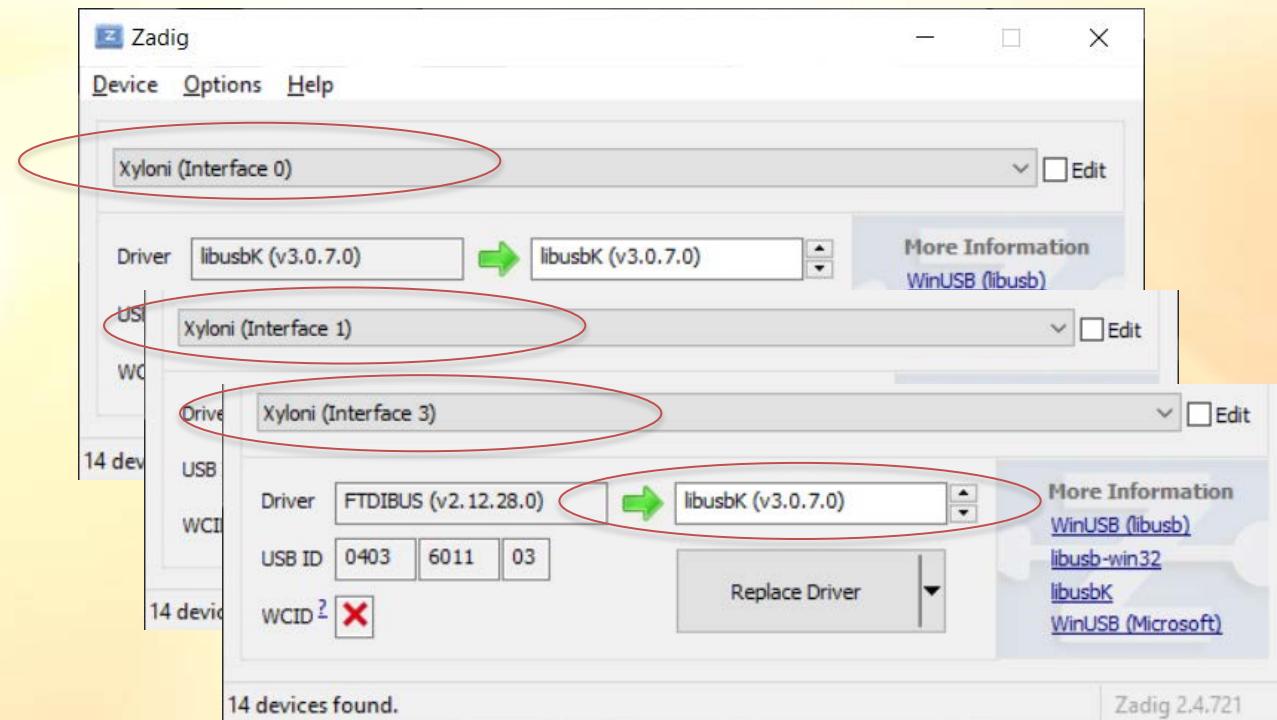
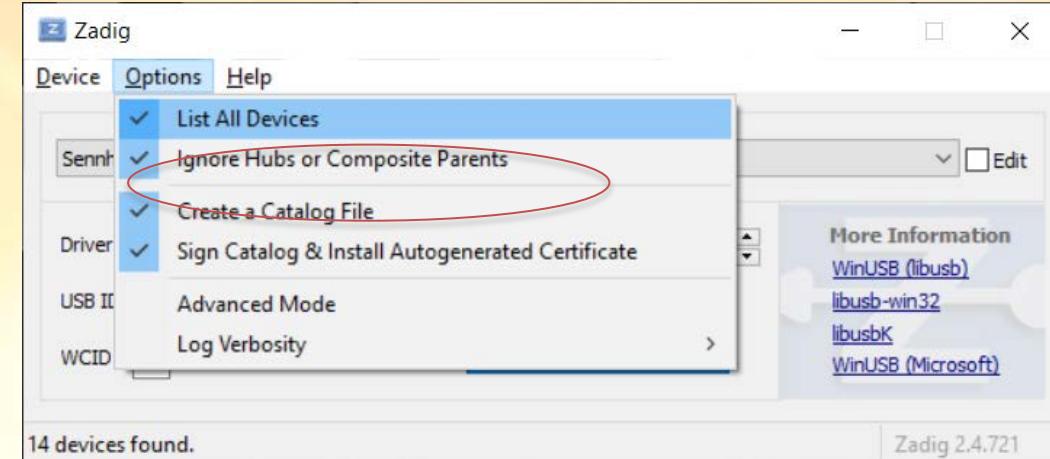
To check the static timing open the file `routing_new_project.timing.rpt`.

Here you will find the constraints from the constraint file (clk :30ns) and the result

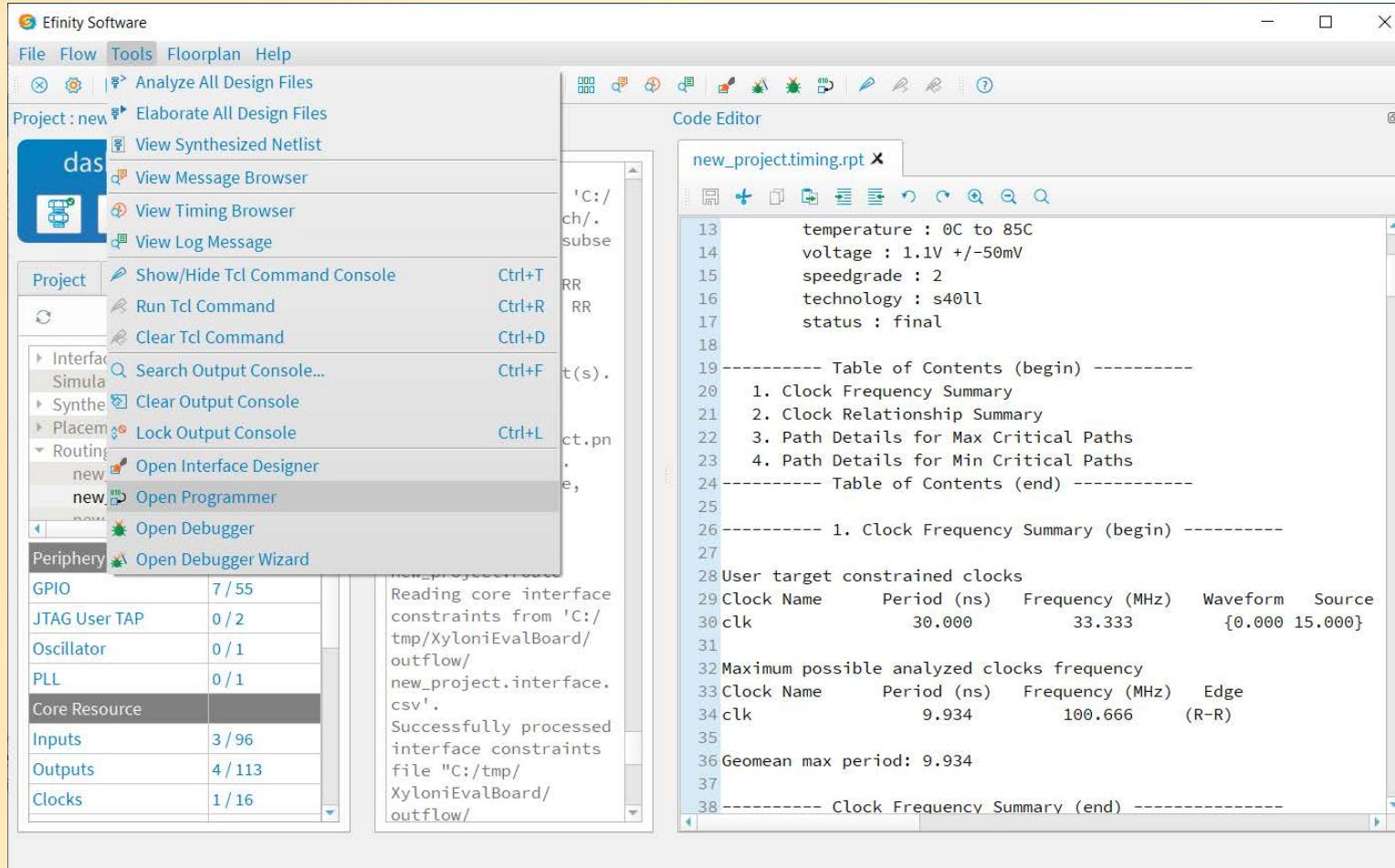
# Program the Device

- To program the device on Windows, you have to install the USB driver first !
- Select Options->List All Devices
- Change the driver for Xyloni (Interface 0,1,3) to libusbK.
- Please do not choose WinUSB or select interface 2 !

*Read Xyloni user guide for details*

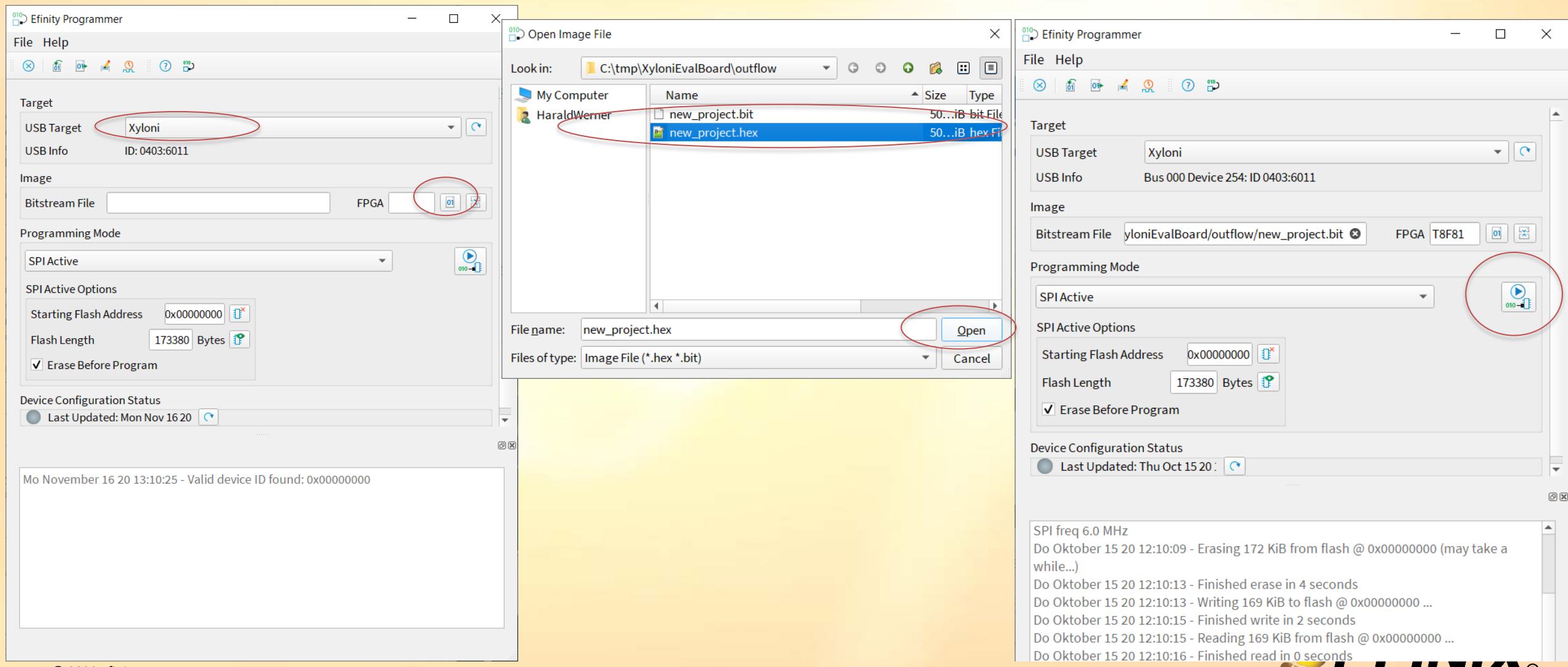


# Program the Device



Open Programmer  
Tools->Open  
Programmer  
Or click  
Programmer icon

# Select Image File, Start Program (Check USB Target: Xyloni)

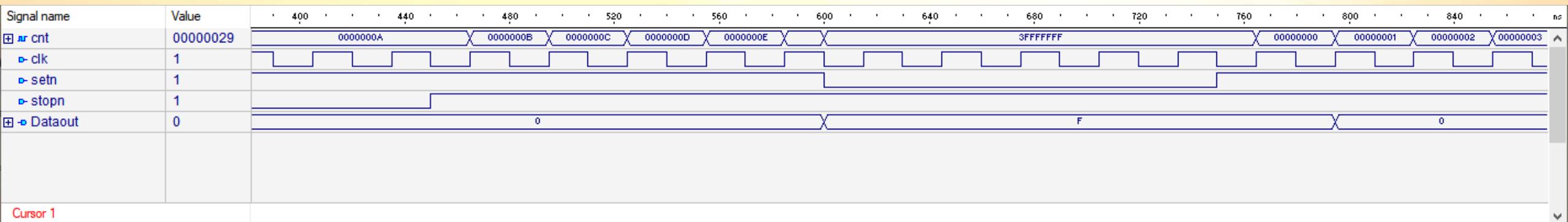


# Problem solving

- All LEDs ON: Check the VHDL code to make sure you have the correct setting for the frequency (29 downto 26) vs (17 downto 14)
- If you can not see the Xyloni board in the Programmer, check that you installed the correct USB driver with the Zadig software

# Simulation

- For HDL simulation you can use any VHDL simulator. The testbench is included in the design.
- This waveform shows simulation results with the testbench an the ALDEC HDL simulator.



- To simulate the synthesized netlist, include the new\_project.dbg.map.v below the outflow folder and include the simulation libraries <installation path>\Efinix\<version>\sim\_models\verilog folder instead of the RTL Design

# Using the Internal Oscillator

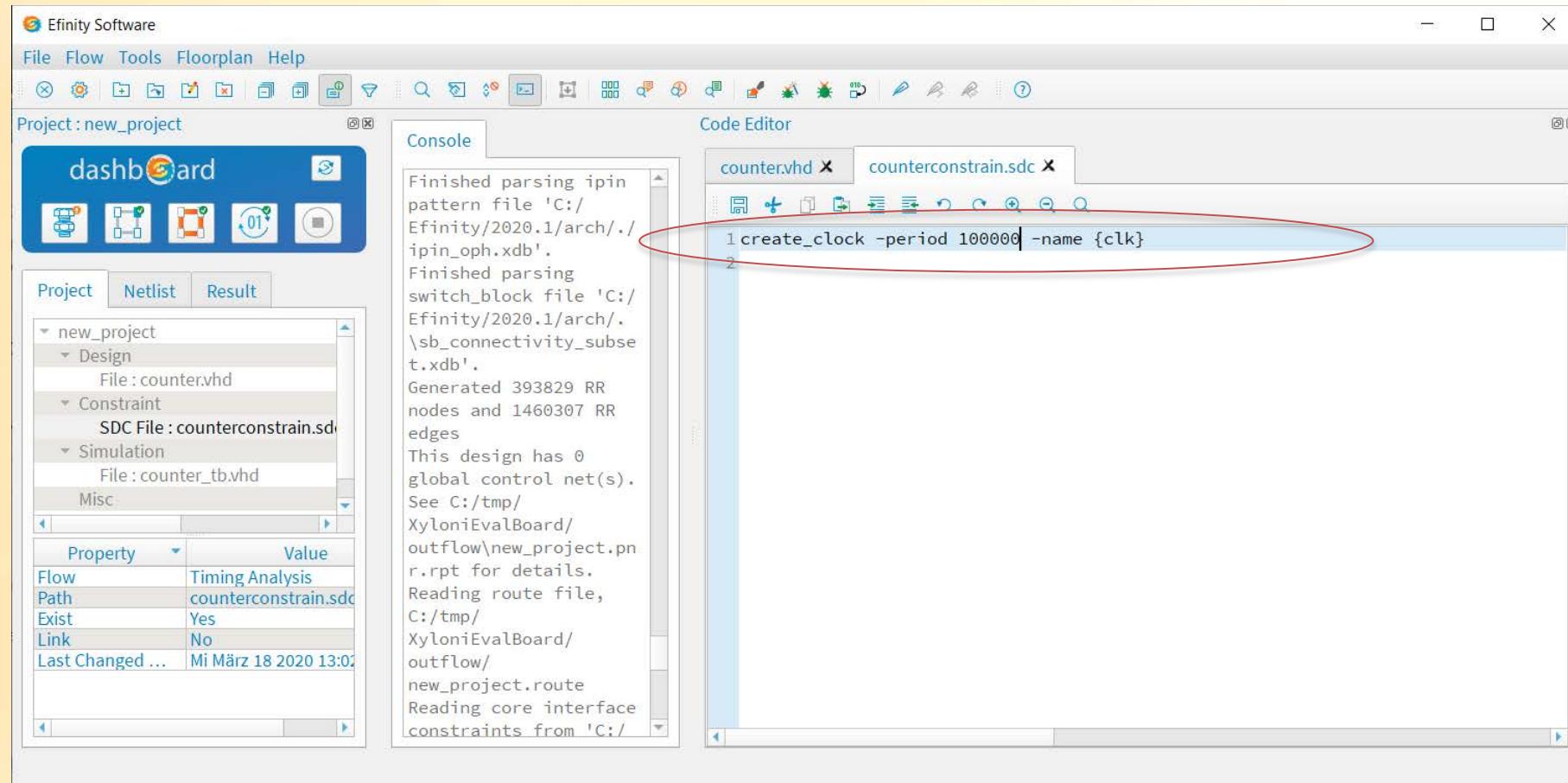
Code Editor

counter.vhd x

```
4 --  
5 library ieee;  
6 use ieee.std_logic_1164.all;  
7 use ieee.std_logic_unsigned.all;  
8  
9 entity counter is  
10 port ( clk      : in std_logic;          -- clock input. Could be from internal osc (T8) or from the external 33.3MHz clock use GPIOI_20  
11       setn     : in std_logic;          -- Set signal, low active; sett all outputs to '1' (LED are high active, means all LEDs must be ON) GPIOI_02  
12       stopn    : in std_logic;          -- Stop signal, low active Stop counting GPIOI_15  
13       Dataout   : out std_logic_vector ( 3 downto 0);  -- Output data connected to the LEDs (high active); GPIOI_17,GPIOI_16,GPIOI_37,GPIOI_21  
14 end counter;  
15  
16 architecture vers1 of counter is  
17 signal cnt: std_logic_vector ( 29 downto 0 ) := (others => '0');  
18 begin  
19   cnt_proc : process(clk, setn)  
20   begin  
21     if setn = '0' then  
22       cnt  <= (others => '1');  
23       dataout <= (others => '1');  
24     elsif clk'event and clk = '1' then  
25       if stopn = '0' then  
26         cnt <= cnt;  
27       else  
28         cnt <= cnt +1;  
29       end if;  
30       Dataout <= cnt(17 downto 14);          --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26  
31       Dataout <= cnt(29 downto 26);        --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26  
32     end if;  
33   end process;  
34 end vers1;  
35
```

First, change the VHDL file.

# Change the Constraint File



# Change the Interface Designer

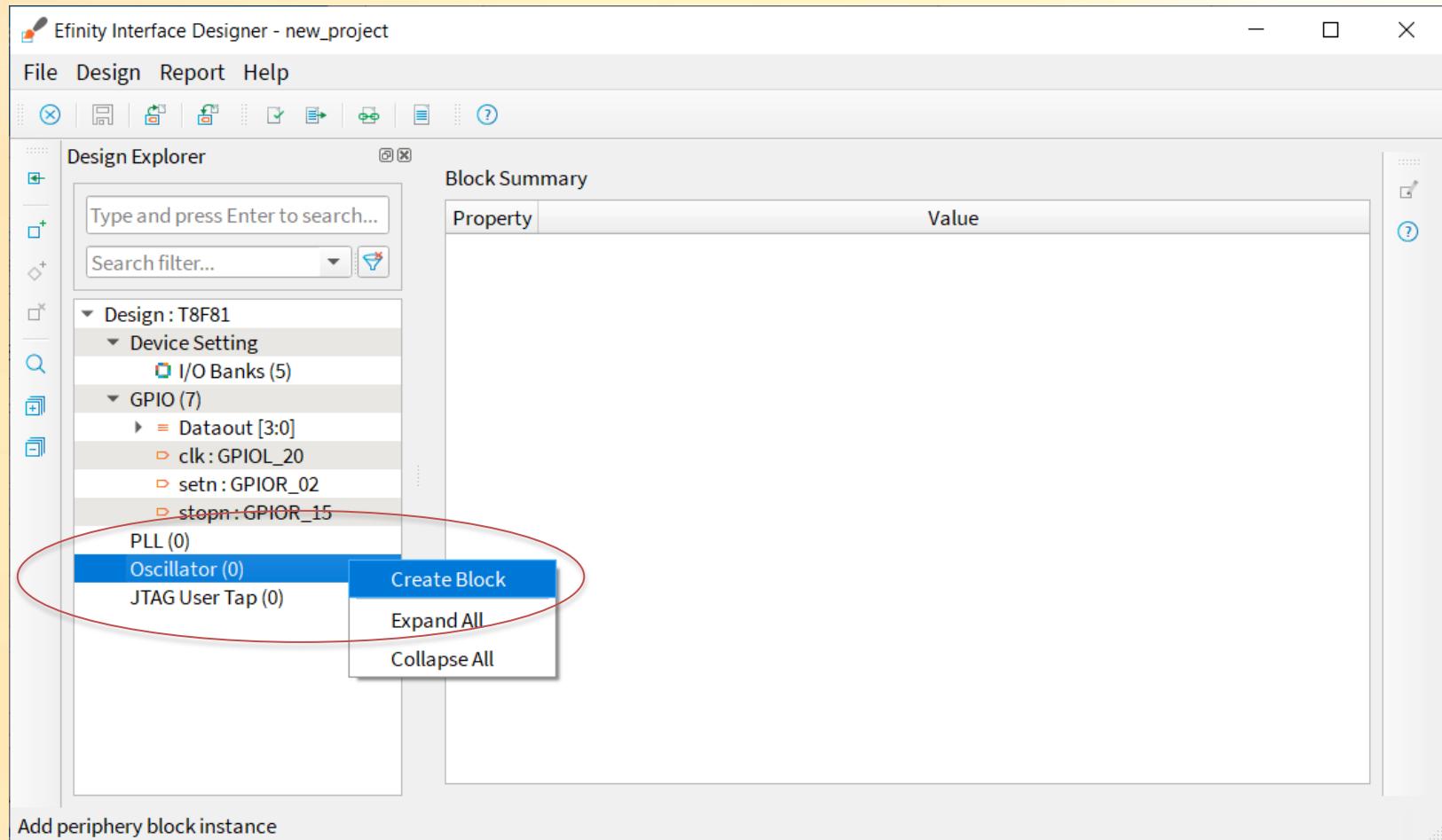
The screenshot shows the Efinix Interface Designer interface. On the left is the Design Explorer panel, which includes a search bar, a search filter dropdown, and a tree view of the design. The tree view shows a 'Design : T8F81' node with 'Device Setting' and 'GPIO (7)' children. Under 'GPIO (7)', there is a 'Dataout [3:0]' node with four items: 'clk : GPIOL\_20', 'setn : GPIOR\_02', 'stopn : GPIOR\_15', and a 'Delete' option highlighted with a blue oval. In the center is the Block Summary panel, which displays a table of properties for the selected block. The table rows are numbered 1 to 14 and include columns for Property, Instance Name, GPIO Resource, Mode, I/O Standard, Unused State, Alternate Connection, Features, Clock Region, I/O Bank, Pad, Package Pin, Input, Pin Name, and Connection Type. The 'clk' row is currently selected. On the right is the Block Editor panel, which contains fields for 'Mode' (set to 'input'), 'I/O Standard' (set to '3.3 V LVTTL / LVC MOS'), and an 'Input' section with 'Pin Name' set to 'clk'. A red oval highlights the 'clk' entry in the 'Pin Name' field.

Property	Value
1 Instance Name	clk
2 GPIO Resource	GPIO_L
3 Mode	input
4 I/O Standard	3.3 V LV
5 Unused State	NA
6 Alternate Connection	PLL_CI
7 Features	None
8 Clock Region	L1
9 I/O Bank	1B
10 Pad	GPIO_L
11 Package Pin	C3
12 Input	
13 Pin Name	clk
14 Connection Type	none

Delete the clk GPIO.

Right-click on the clk GPIO and choose Delete.

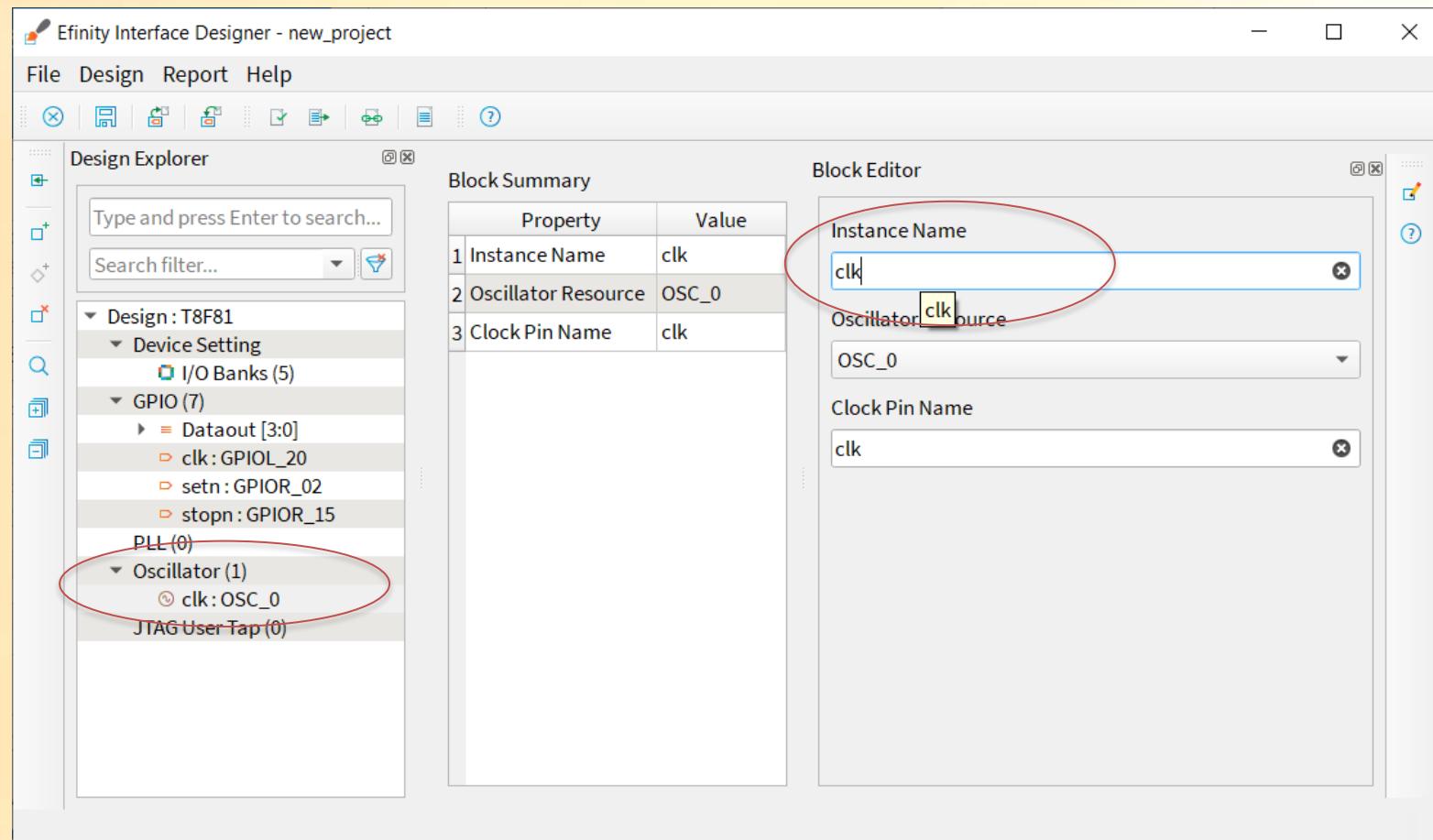
# Add the OSC Block



Select Oscillator.

Right-click and choose Create Block.

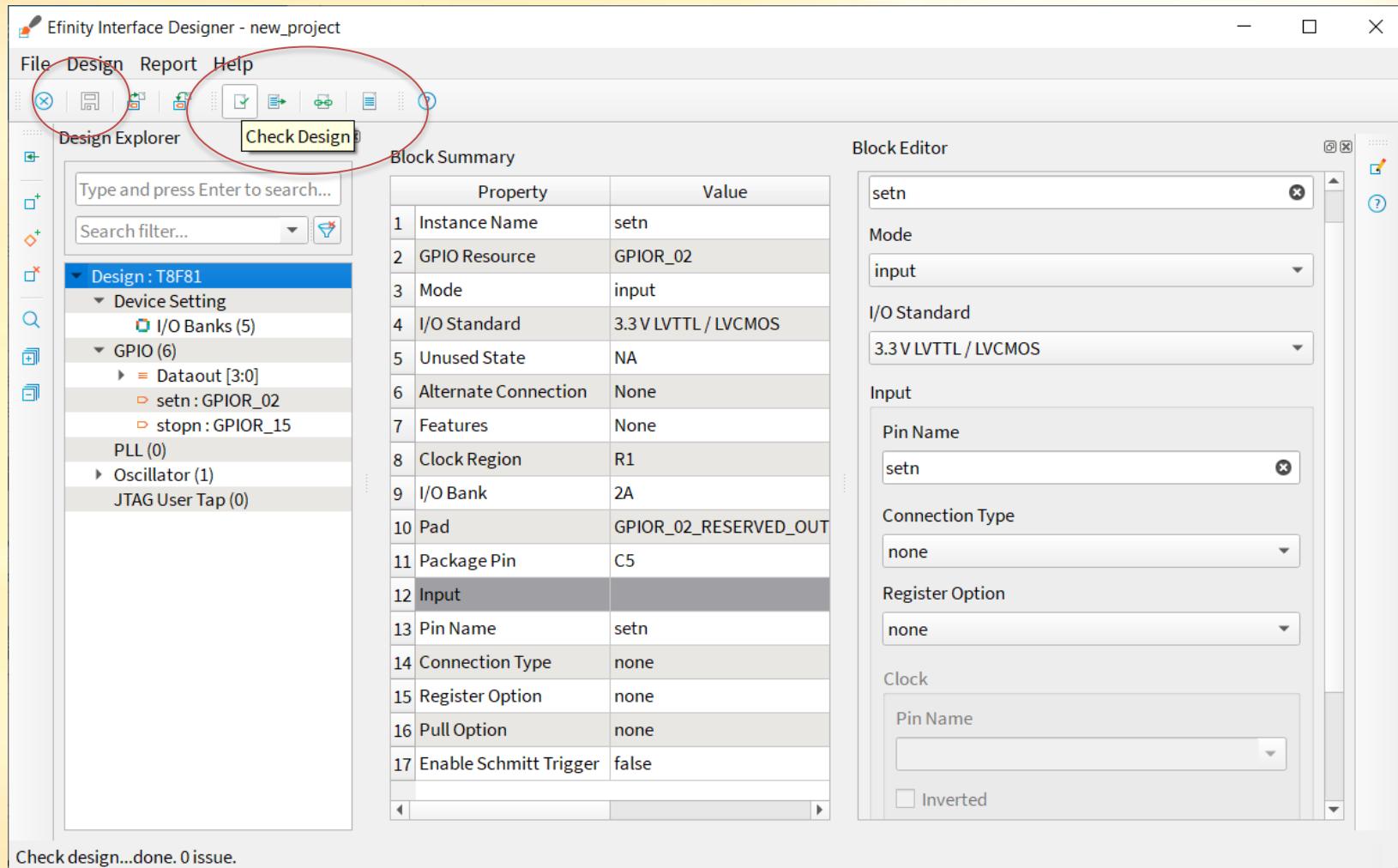
# Change Instance Name



Change the OSC  
Instance Name to  
clk.

**Press Enter !**

# Check Design and Save



# Run the Whole Flow, Press Synthesis



Efinix Software

File Flow Tools Floorplan Help

Project : new\_project

ashboard

Project Netlist Result

new\_project

Design

File : counter.vhd

Constraint

SDC File : counterconstrain.sdc

Simulation

File : counter\_tb.vhd

Misc

Property Value

Flow Timing Analysis

Path counterconstrain.sdc

Exist Yes

Link No

Last Changed ... Mi März 18 2020 13:02

Console

```
INFO: Reading Mapping Library peak resident set memory usage = 37.312 MB
INFO: ***** Ending Reading Mapping Library ... *****
[EFX-0000 INFO] ... Pre-synthesis checks begin
[EFX-0000 INFO] ... Pre-synthesis checks end (Real time : 0s)
[EFX-0000 INFO] ... NameSpace init begin
[EFX-0000 INFO] ... NameSpace init end (Real time : 0s)
[EFX-0000 INFO] ... Mapping design "counter"
[EFX-0000 INFO] ... Hierarchical pre-synthesis "counter" begin

[EFX-0000 INFO] ... Hierarchical pre-synthesis "counter" end (Real time : 0s)
[EFX-0000 INFO] ... Flat optimizations begin
[EFX-0000 INFO] ... Flat optimizations end (Real time : 0s)
[EFX-0000 INFO] ... Flat synthesis begin
[EFX-0000 INFO] ... Flat synthesis end (Real time : 0s)
[EFX-0000 INFO] ... Flat optimizations begin
[EFX-0000 INFO] ... Flat optimizations end (Real time : 0s)
[EFX-0000 INFO] ... Check and break combinational loops begin
[EFX-0000 INFO] ... Check and break combinational loops end (Real time : 0s)
[EFX-0000 INFO] ... Top level netlist RUSHC IOs pre-synthesis begin
[EFX-0000 INFO] ... SOP modeling begin

[EFX-0000 INFO] ... SOP modeling end (Real time : 0s)
[EFX-0000 INFO] ... LUT mapping begin
```

Code Editor

unterconstrain.sdc

```
1 create_clock -peri
```

Running automated flow starting from synthesis...synthesis is in progress...

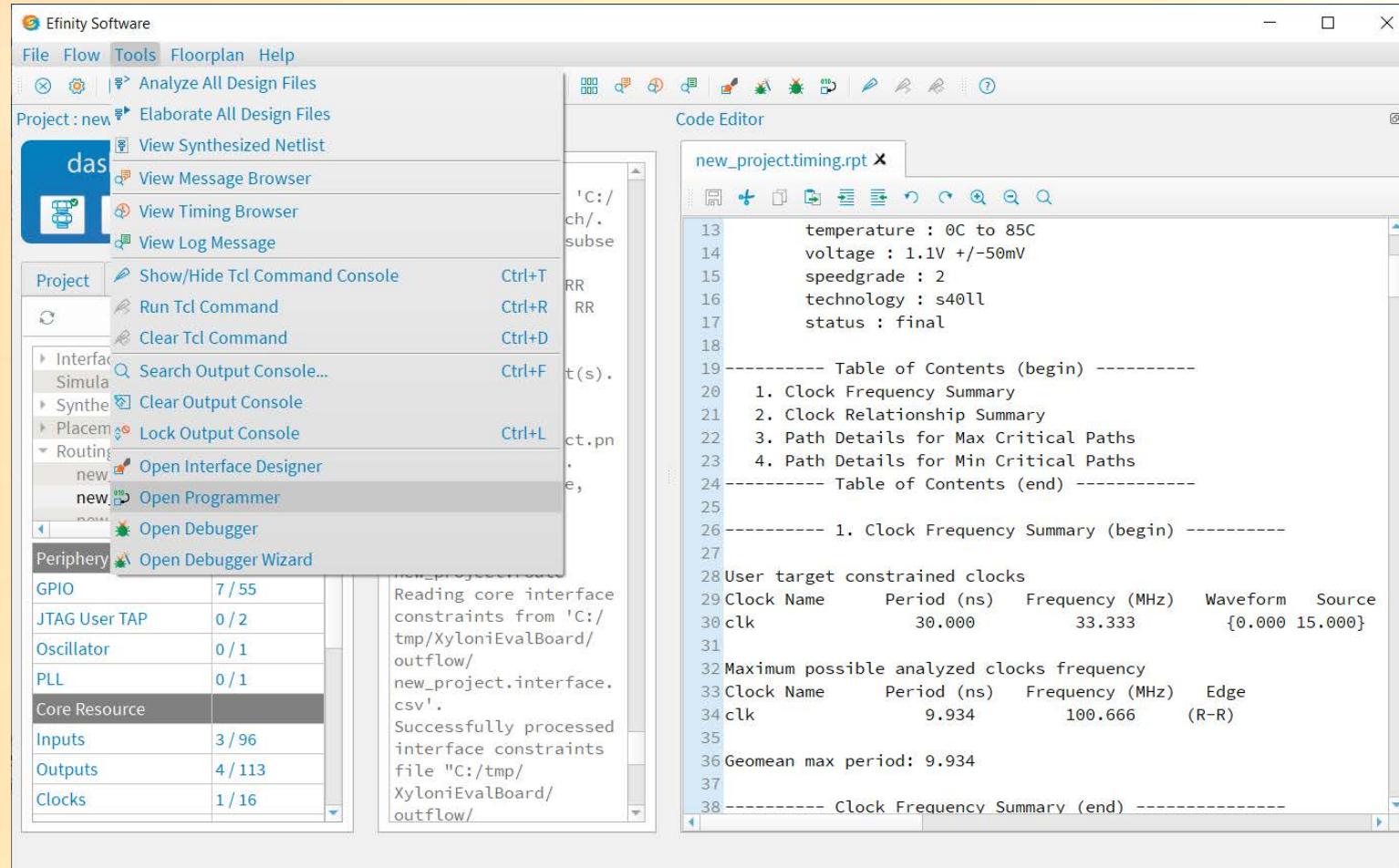
# Check Static Timing

Efinix Software  
File Flow Tools Floorplan Help  
Project: new\_project  
dashboard  
Project Netlist Result  
Interface Simulation Synthesis Placement Routing  
new\_project.route.rpt new\_project.timing.rpt new\_project.route.out  
Periphery Resource  
GPIO 6 / 55  
JTAG User TAP 0 / 2  
Oscillator 1 / 1  
PLL 0 / 1  
Core Resource  
Inputs 3 / 96  
Outputs 4 / 113  
Clocks 1 / 16  
Logic Elements 24 / 7384  
Console counterconstrain.sdc x new\_project.timing.rpt x  
Pass 0: Swept away 0 nets with no fanout.  
Pass 0: Swept away 0 blocks with no fanout.  
Swept away 0 nets and 0 blocks in total.  
Removed 0 LUT buffers.  
Successfully created VPR logical netlist from Verific binary DataBase file "C:/tmp/XylonIEvalBoard/new\_project.vdb".  
Netlist pre-processing took 0.0202929 seconds.  
Netlist pre-processing took 0.02 seconds (approximately) in total CPU time.  
Netlist pre-processing virtual memory usage: begin = 111.36 MB, end = 111.4 MB, delta = 0.04 MB  
Netlist pre-processing peak virtual memory usage = 231.272 MB  
Netlist pre-processing took 0.0202929 seconds.  
temperature : 0C to 85C  
voltage : 1.1V +/-50mV  
speedgrade : 2  
technology : s40ll  
status : final  
----- Table of Contents (begin) -----  
1. Clock Frequency Summary  
2. Clock Relationship Summary  
3. Path Details for Max Critical Paths  
4. Path Details for Min Critical Paths  
----- Table of Contents (end) -----  
----- 1. Clock Frequency Summary (begin) -----  
User target constrained clocks  
Clock Name Period (ns) Frequency (MHz) Waveform Source Clock Name  
clk 100000.000 0.010 {0.000 50000.000} virtu  
Maximum possible analyzed clocks frequency  
Clock Name Period (ns) Frequency (MHz) Edge  
clk 8.242 121.327 (R-R)  
Geomean max period: 8.242  
----- Clock Frequency Summary (end) -----

To check the static timing open the file `routing_new_project.timing.rpt`.

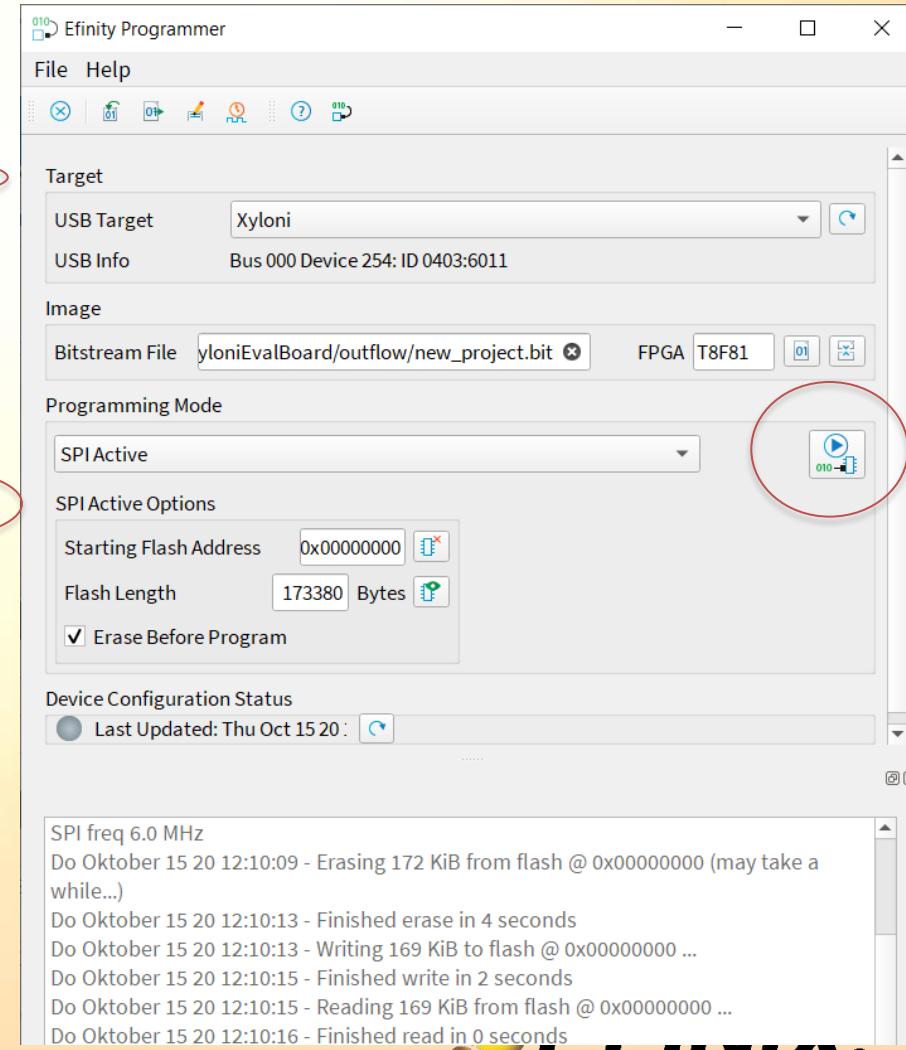
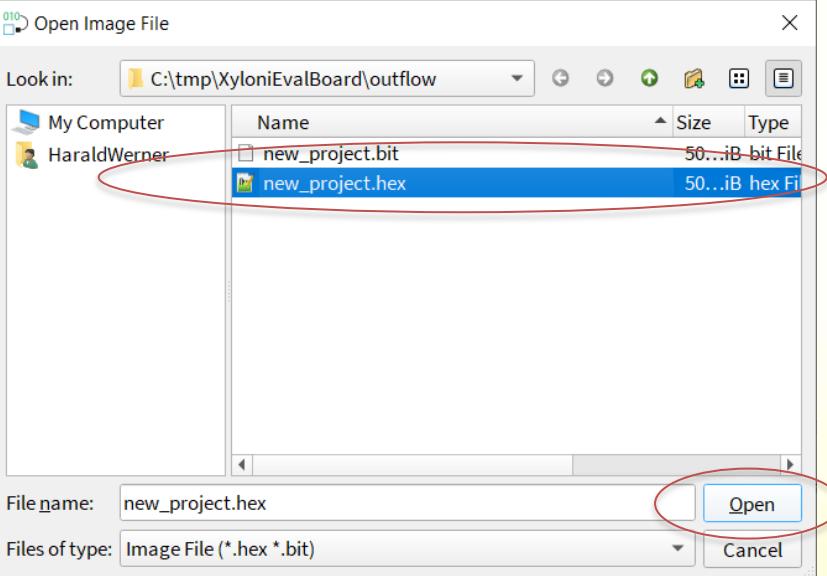
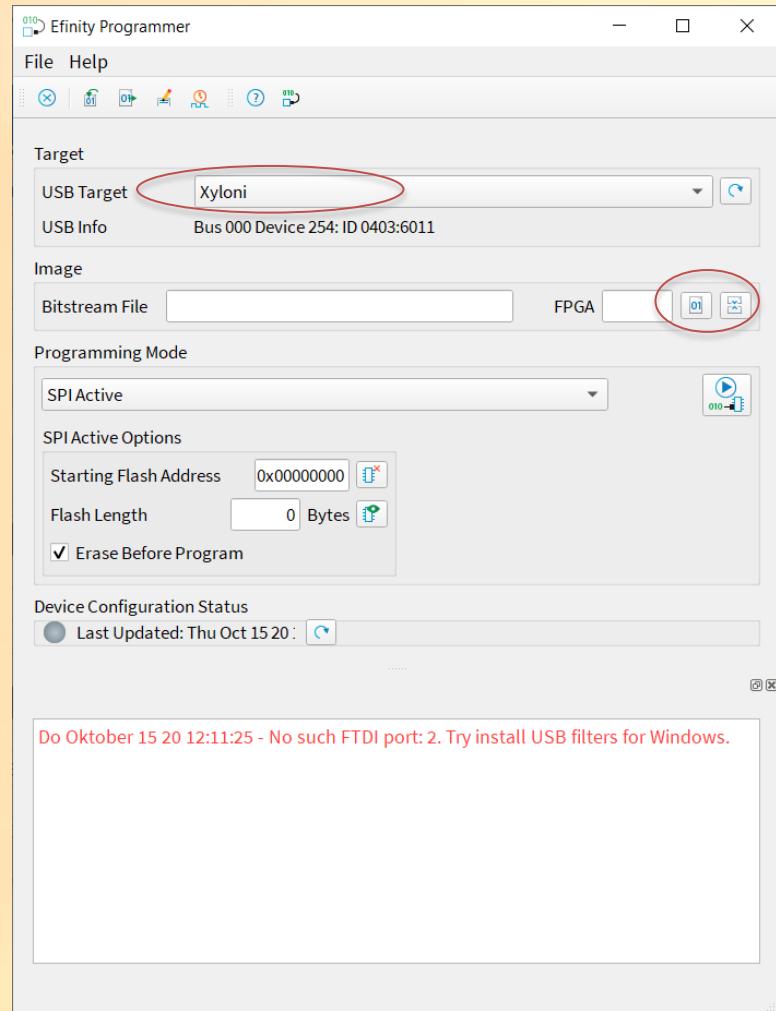
This file shows the constraints from the constraint file (clk :100000ns) and the result.

# Program the Device



Open the  
Programmer  
Tools->Open  
Programmer

# Select Image File, Start Program (Check USB Target: Xyloni)



# Information

- If you need the complete Project, extract the XyloniEvalBoardSolution.zip file. Here you will find the project with the I/O pin assignments