

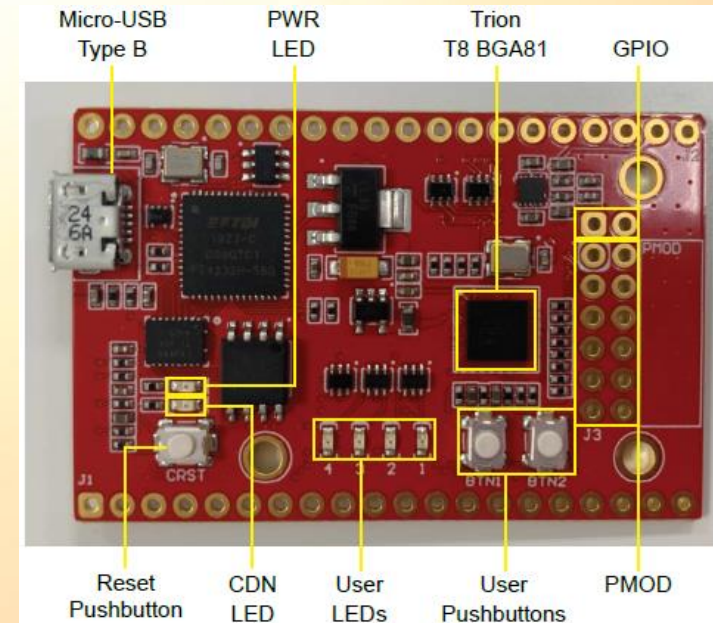


Accelerating Your Innovation

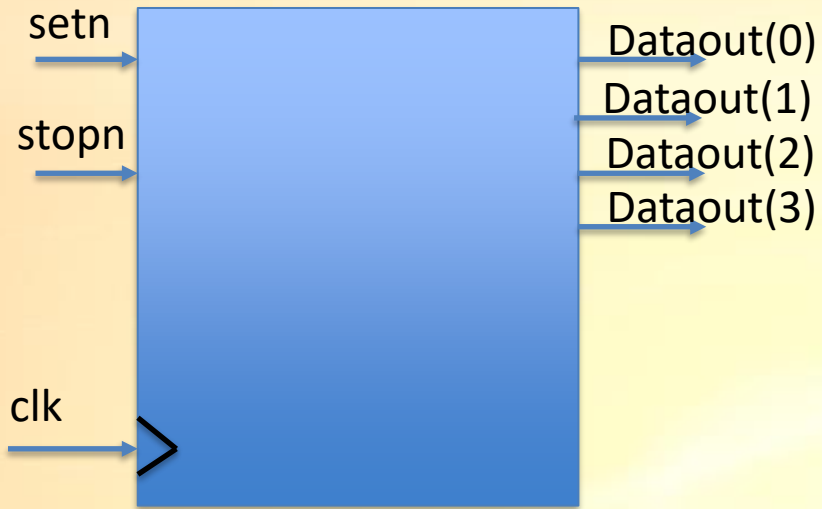
Trion Xyloni T8 LAB

By Harald Werner

Version: 1.0.2

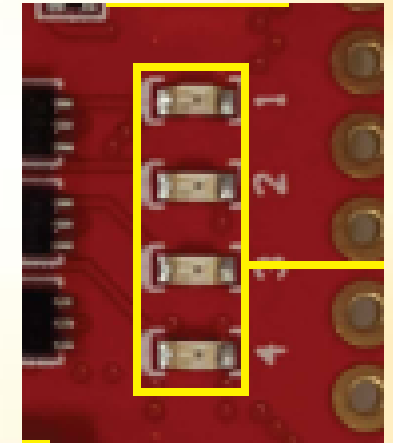
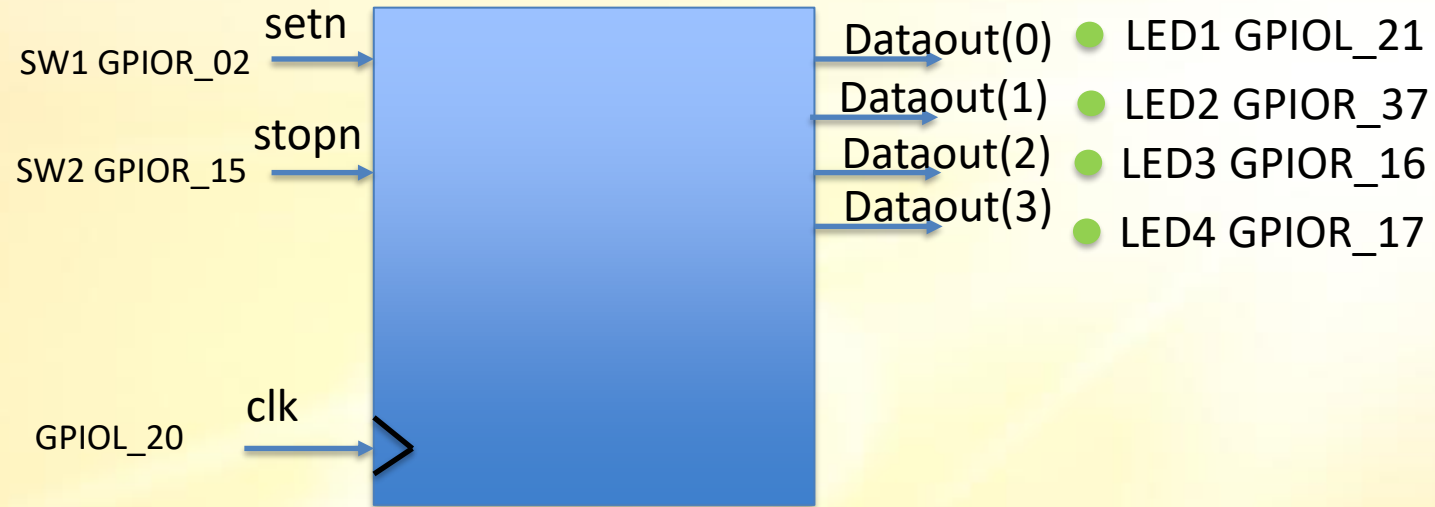


Design (simple up counter with set and stop)

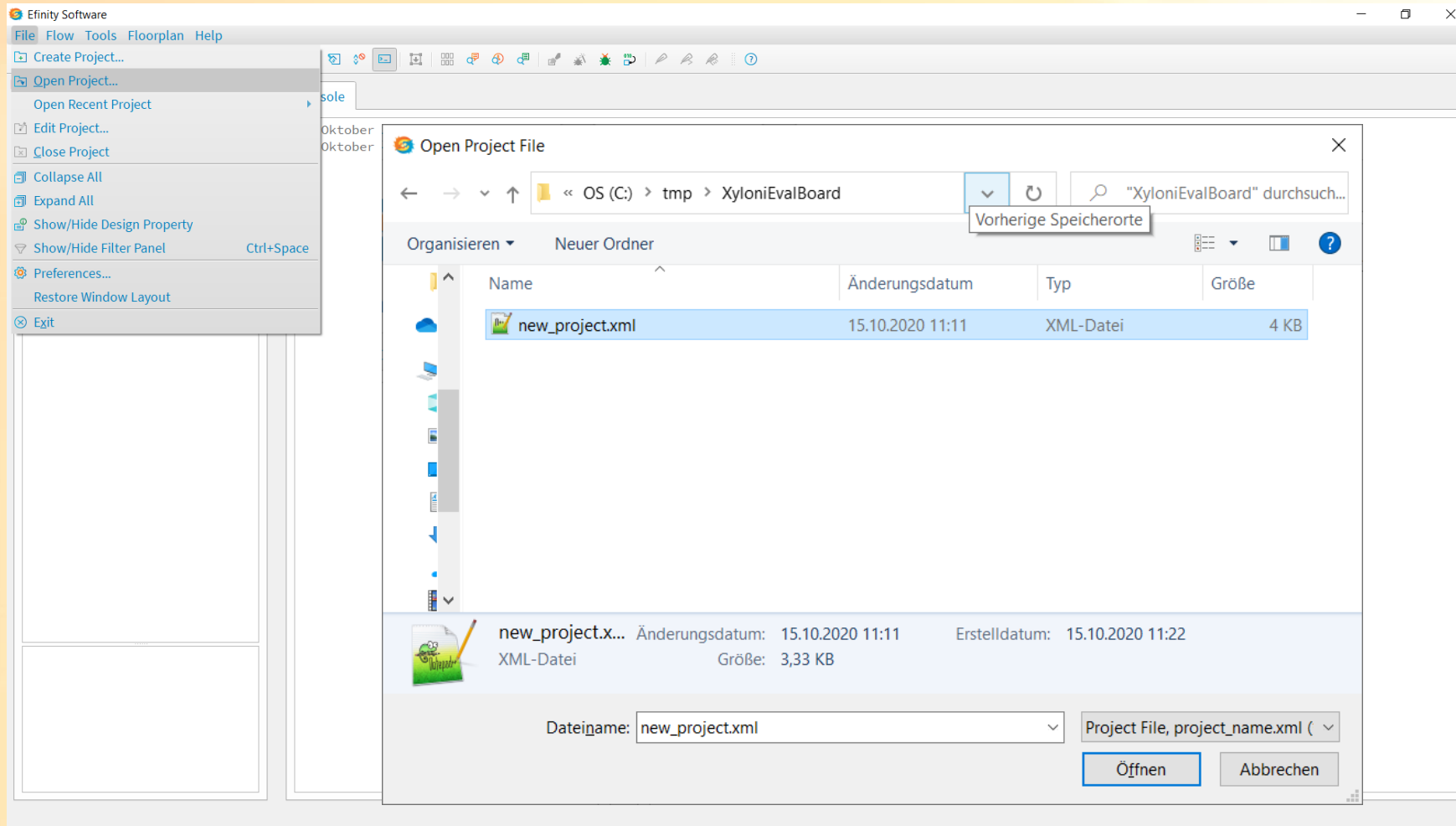


```
Code Editor
counter.vhd x
1 -- smal example design for the Xyloni Efinix Eval Board
2 -- By Harald Werner
3 -- 15.10.2020
4 library ieee;
5 use ieee.std_logic_1164.all;
6 use ieee.std_logic_unsigned.all;
7
8 entity counter is
9 port ( clk      : in std_logic;           -- clock input. Could be from internal osc (T8) or from the external 33.3MHz clock use GPIOL_20
10       setn     : in std_logic;           -- Set signal, low active; sett all outputs to '1' (LED are high active, means all LEDs msut be ON) GPIOR_02
11       stopn    : in std_logic;           -- Stop signal, low active Stop counting GPIOR_15
12       Dataout  : out std_logic_vector(3 downto 0)); -- Output data connected to the LEDs (low high); GPIOR_17,GPIOR_16,GPIOLR37,GPIOL_21
13 end counter;
14
15 architecture vers1 of counter is
16 signal cnt: std_logic_vector ( 29 downto 0) := (others => '0');
17 begin
18 cnt_proc : process(clk, setn)
19 begin
20     if setn = '0' then
21         cnt <= (others => '1');
22         dataout <= (others => '1');
23     elsif clk'event and clk = '1' then
24         if stopn = '0' then
25             cnt <= cnt;
26         else
27             cnt <= cnt +1;
28         end if;
29         Dataout <= cnt(17 downto 14); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
30         Dataout <= cnt(29 downto 26); --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
31     end if;
32 end process;
```

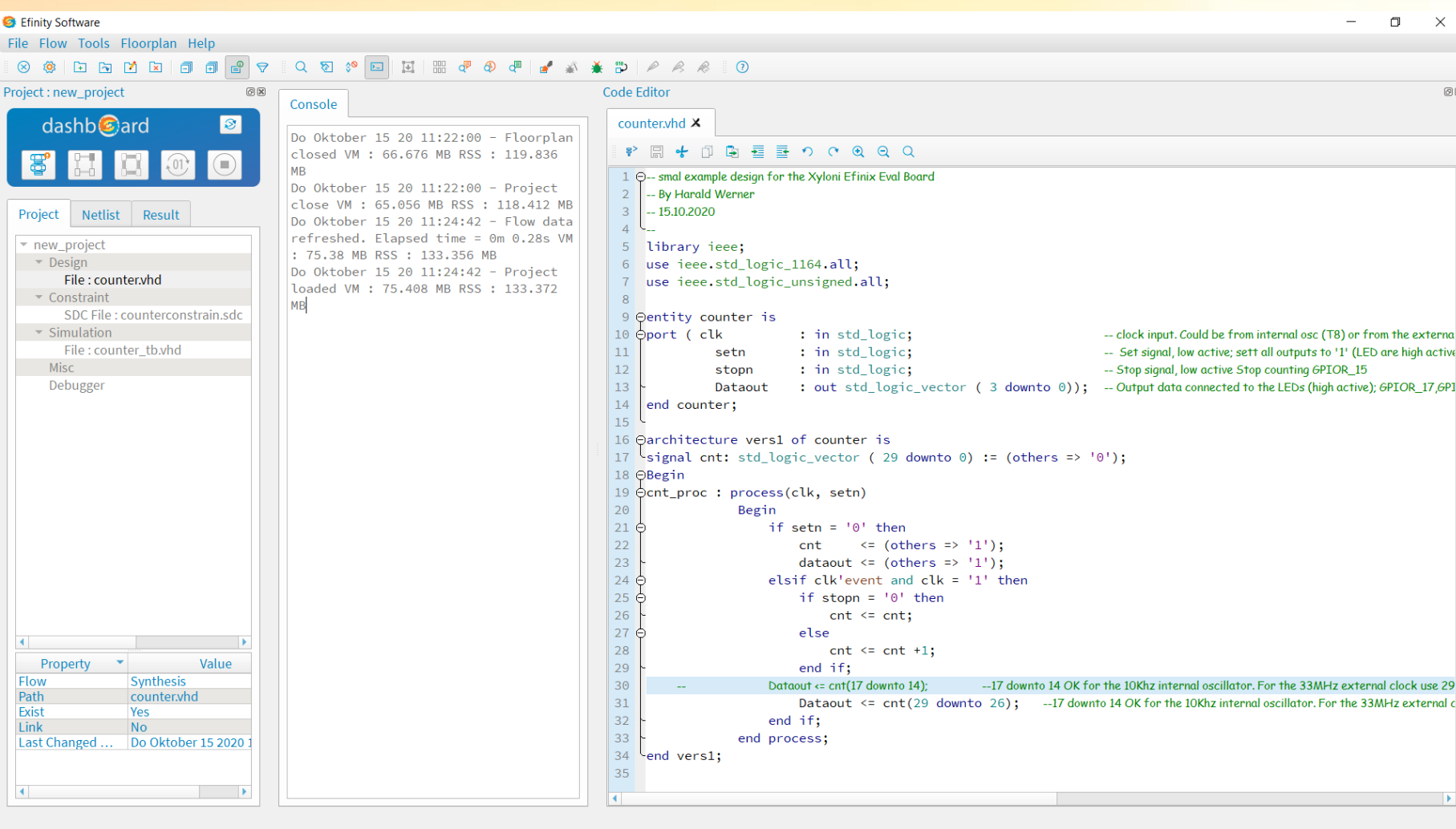
Design / Board connection



1. Open Efinity new_project.xml

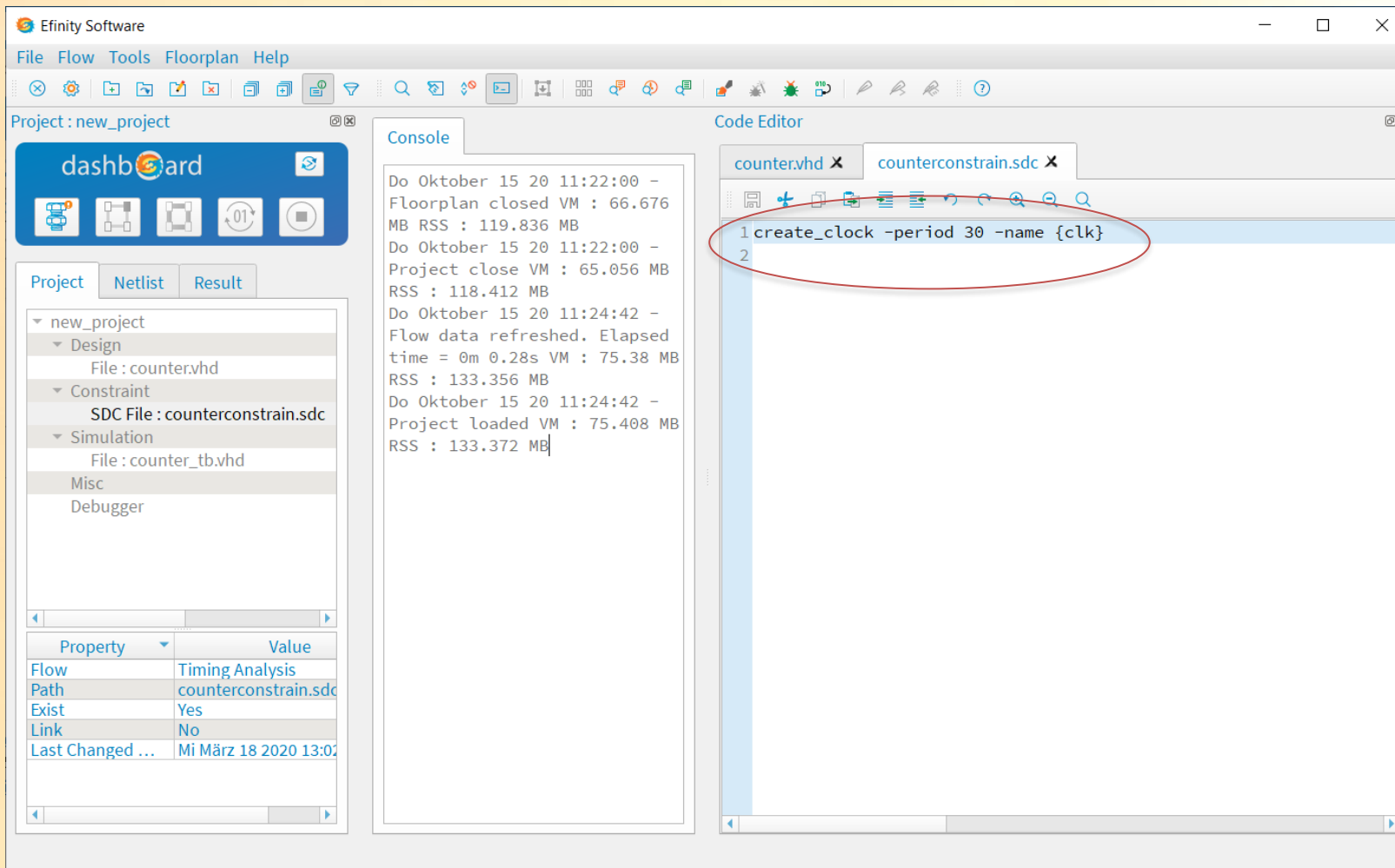


Double click on counter.vhd



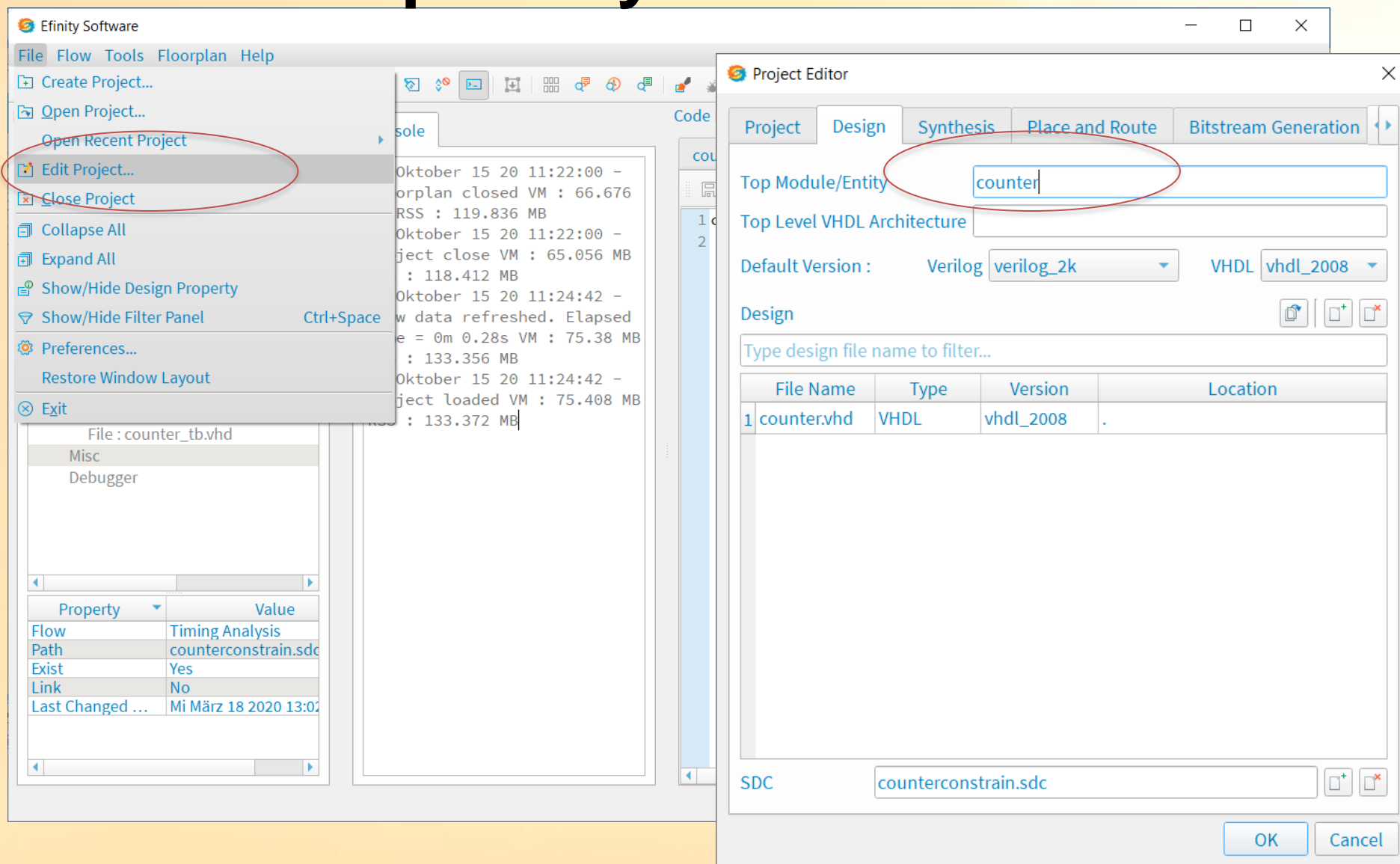
- The counter.vhd will show up in the Code Editor

Double click on the timing constrain counterconstrain.sdc



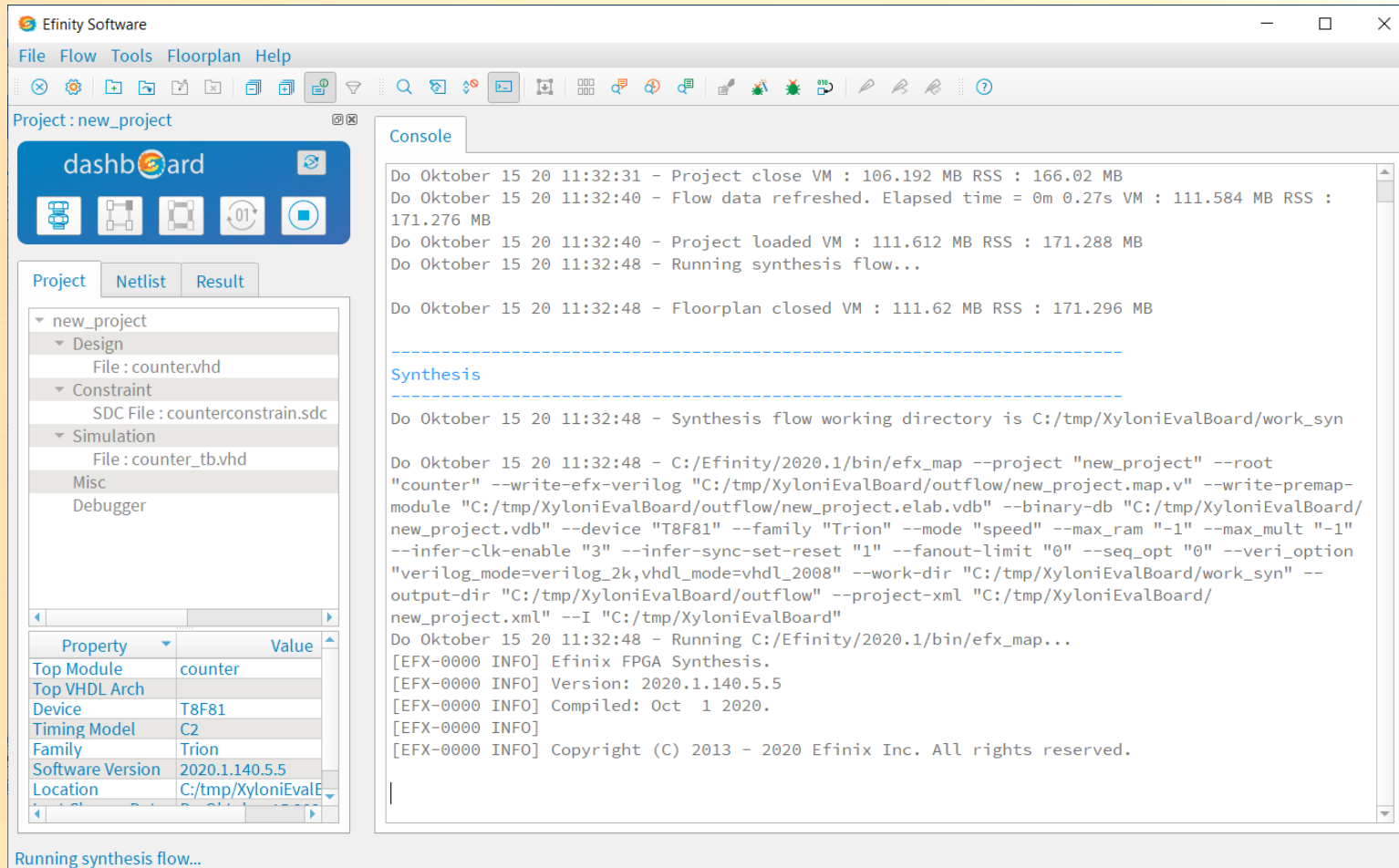
The counterconstrain.sdc will show up and you can see the 30ns period constrain for the 33MHz clock



Set the top entity name




Enter counter
to top
Module/Entity
and click OK

Run the whole flow or just Synthesis

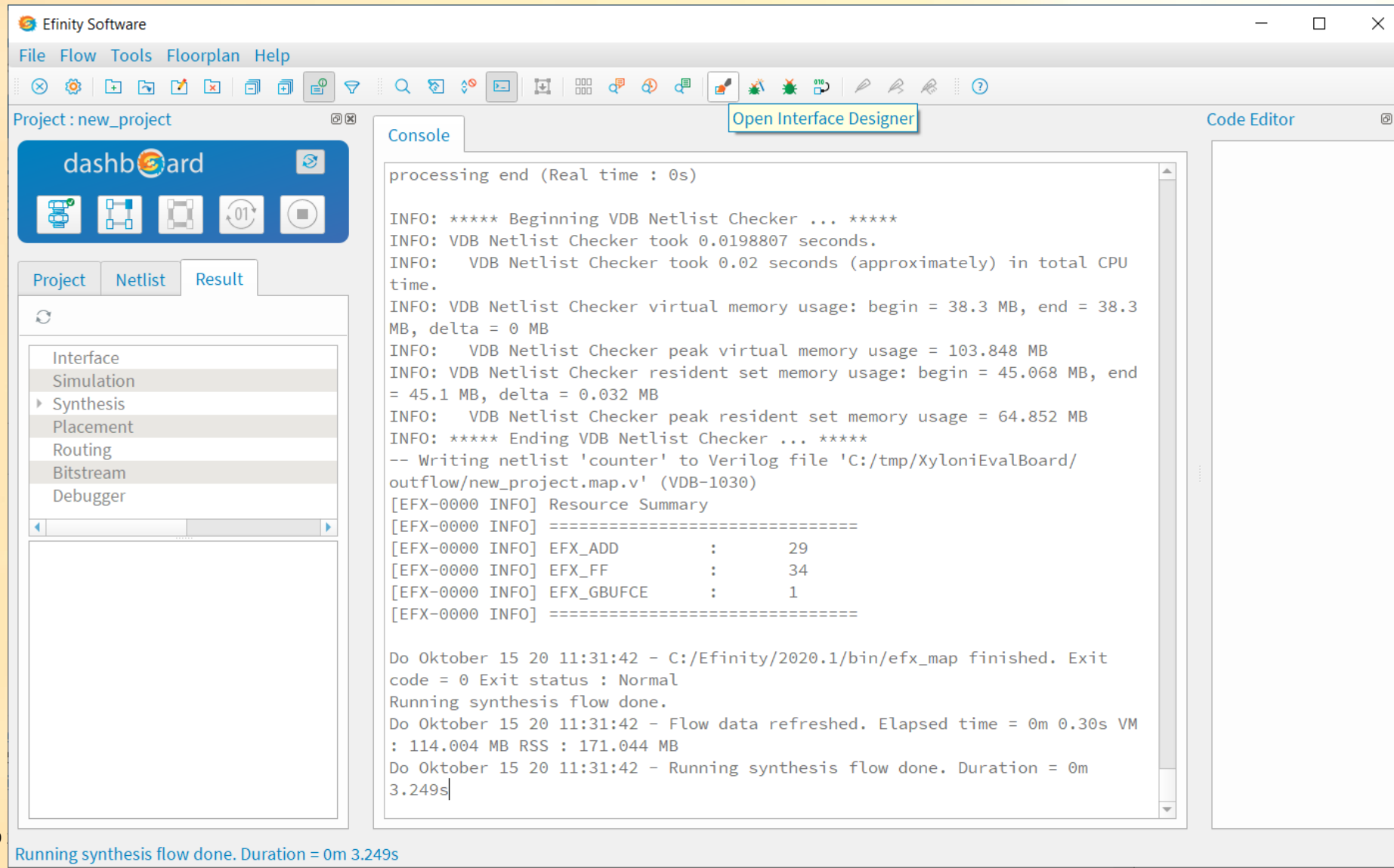


- If the Automated flow button is grayed out  click on the button to activate the automated flow. 

- Click on the synthesis icon and the flow will run automatically 

Assign the top level Signals to Pins.

1. Open Interface Designer

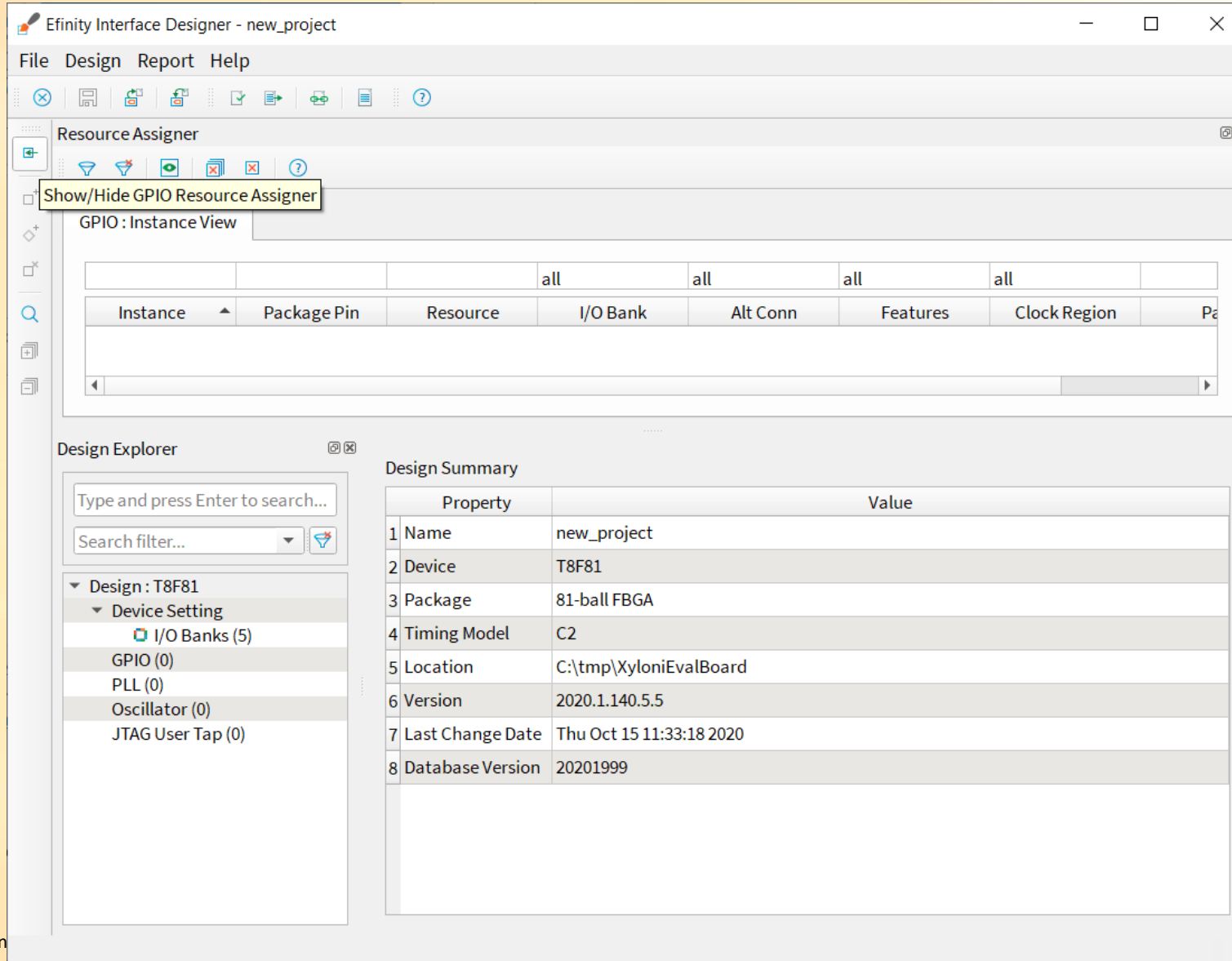


The screenshot displays the Efinity Software interface. The top menu bar includes File, Flow, Tools, Floorplan, and Help. The toolbar contains various icons for project management and design. The left sidebar shows a 'Project: new_project' section with a 'dashboard' and a list of project stages: Interface, Simulation, Synthesis (selected), Placement, Routing, Bitstream, and Debugger. The main area is divided into three panes: Console, Open Interface Designer (highlighted with a red box), and Code Editor. The Console pane shows the following log output:

```
processing end (Real time : 0s)
INFO: ***** Beginning VDB Netlist Checker ... *****
INFO: VDB Netlist Checker took 0.0198807 seconds.
INFO: VDB Netlist Checker took 0.02 seconds (approximately) in total CPU time.
INFO: VDB Netlist Checker virtual memory usage: begin = 38.3 MB, end = 38.3 MB, delta = 0 MB
INFO: VDB Netlist Checker peak virtual memory usage = 103.848 MB
INFO: VDB Netlist Checker resident set memory usage: begin = 45.068 MB, end = 45.1 MB, delta = 0.032 MB
INFO: VDB Netlist Checker peak resident set memory usage = 64.852 MB
INFO: ***** Ending VDB Netlist Checker ... *****
-- Writing netlist 'counter' to Verilog file 'C:/tmp/XyloniEvalBoard/outflow/new_project.map.v' (VDB-1030)
[EFX-0000 INFO] Resource Summary
[EFX-0000 INFO] =====
[EFX-0000 INFO] EFX_ADD      :      29
[EFX-0000 INFO] EFX_FF       :      34
[EFX-0000 INFO] EFX_GBUFCE   :       1
[EFX-0000 INFO] =====
Do Oktober 15 20 11:31:42 - C:/Efinity/2020.1/bin/efx_map finished. Exit code = 0 Exit status : Normal
Running synthesis flow done.
Do Oktober 15 20 11:31:42 - Flow data refreshed. Elapsed time = 0m 0.30s VM : 114.004 MB RSS : 171.044 MB
Do Oktober 15 20 11:31:42 - Running synthesis flow done. Duration = 0m 3.249s
```

At the bottom of the interface, a status bar indicates: Running synthesis flow done. Duration = 0m 3.249s.

Show GPIO Resource Assigner



The screenshot displays the Efinity Interface Designer software interface. The main window is titled "Efinity Interface Designer - new_project". The "Resource Assigner" panel is active, showing a table with columns: Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, Clock Region, and Package. A tooltip "Show/Hide GPIO Resource Assigner" is visible over the Resource Assigner icon. The "Design Explorer" panel on the left shows a tree view with "Design : T8F81" expanded, showing "Device Setting" and "I/O Banks (5)". The "Design Summary" panel on the right shows a table with properties and values.

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Package
----------	-------------	----------	----------	----------	----------	--------------	---------

Design Explorer

Type and press Enter to search...

Search filter...

- Design : T8F81
 - Device Setting
 - I/O Banks (5)
 - GPIO (0)
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Design Summary

Property	Value
1 Name	new_project
2 Device	T8F81
3 Package	81-ball FBGA
4 Timing Model	C2
5 Location	C:\tmp\XyloniEvalBoard
6 Version	2020.1.140.5.5
7 Last Change Date	Thu Oct 15 11:33:18 2020
8 Database Version	20201999

Select GPIO, RMB, Create Bus

The screenshot shows the Efinity Interface Designer software interface. The main window is titled "Efinity Interface Designer - new_project". The menu bar includes "File", "Design", "Report", and "Help". The toolbar contains various icons for file operations and design actions.

The **Resource Assigner** panel is active, showing the "GPIO : Instance View" tab. It contains a table with the following columns: Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, Clock Region, and Pad. The table is currently empty.

The **Design Explorer** panel is located on the left side. It has a search bar with the text "Type and press Enter to search..." and a "Search filter..." dropdown. Below the search bar, the design hierarchy is shown: "Design : T8F81" > "Device Setting" > "I/O Banks (5)". The "GPIO (0)" item is selected, and a right-click context menu is open, showing options: "Create Block", "Create Bus" (highlighted), "Expand All", and "Collapse All".

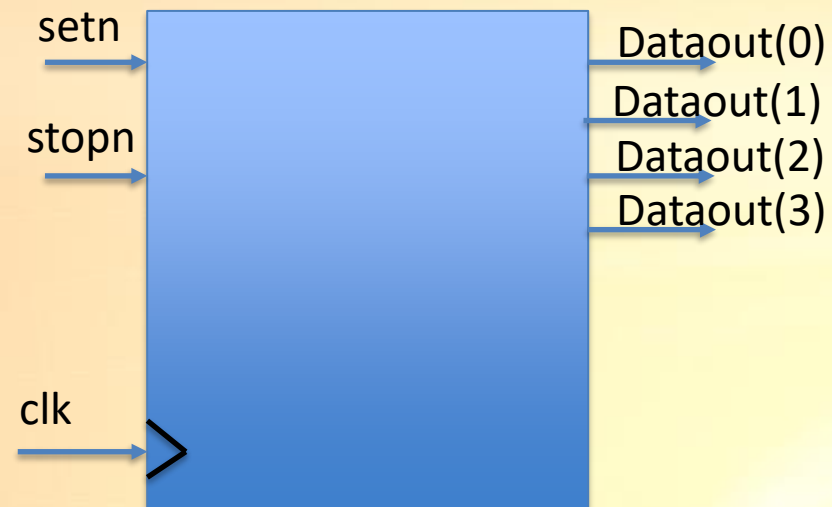
The **Block Summary** panel is located in the center. It displays a table with the following data:

Property	Value
1 Global Unused Setting	
2 State	input with weak pullup

The **Block Editor** panel is located on the right side. It shows the "Unused State" block with a dropdown menu set to "input with weak pullup".

At the bottom left, there is a button labeled "Add bus instance".

Create a Output BUS Dataout(3 downto 0)



A screenshot of a software dialog box titled 'Add New Bus'. The dialog has a title bar with a question mark and a close button. Inside, there is a back arrow and a pencil icon. The fields are as follows: 'Name' is 'Dataout'; 'MSB' is '3' and 'LSB' is '0'; 'Mode' is a dropdown menu with 'input', 'output' (selected), and 'inout' options; 'I/O Stand' is partially visible. At the bottom right are 'Next' and 'Cancel' buttons.

Name: Dataout

MSB: 3

LSB: 0

Mode: output

Click Next

Set drive strength to 3; click Next

?

×

← Add New Bus

Output

Pin Name

Dataout

Register Option

none

Drive Strength (1-weakest, 4-strongest)

1

2

3


4

Next

Cancel

Click Finish

? ×

←  Add New Bus

A new bus will be created with these properties

	Property	Value
1	Bus Name	Dataout
2	MSB	3
3	LSB	0
4	Mode	output
5	I/O Standard	3.3V LVTTL / LVCMOS
6	Output	
7	Pin Name	Dataout
8	Constant Output	none
9	Drive Strength	3
10	Enable Slew Rate	false
11	Register Option	none

Finish Cancel

Adding the additional Pins clk, stopn, setn

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[0]							
Dataout[1]							
Dataout[2]							

Design Explorer

Type and press Enter to search...

Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (4)**
 - Dataout [3:0]**
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Create Block
Create Bus
Expand All
Collapse All

Block Summary

Property	Value
1 Global Unused Setting	
2 State	input with weak pullup

Block Editor

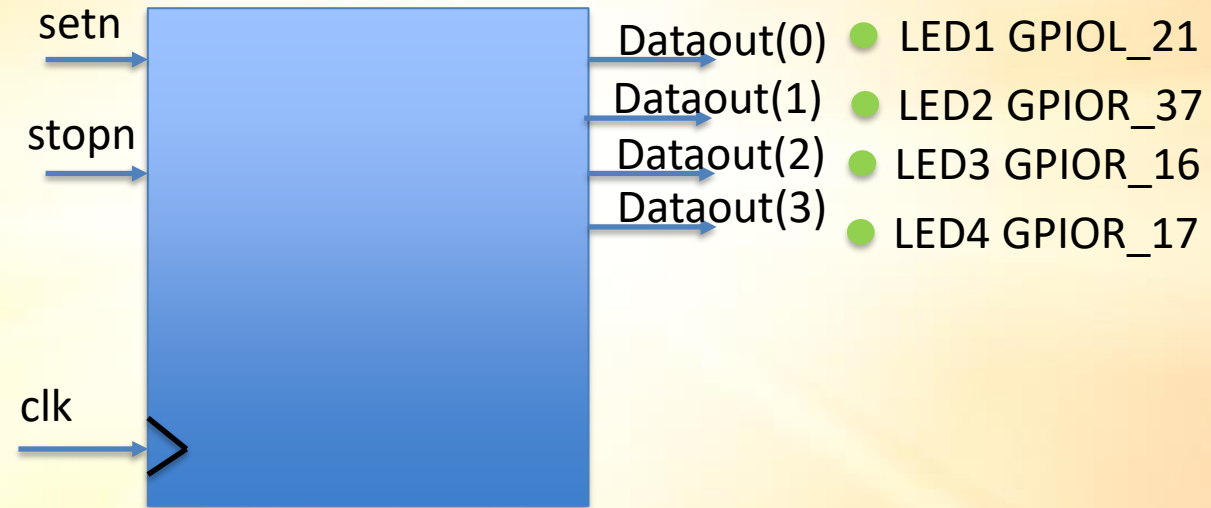
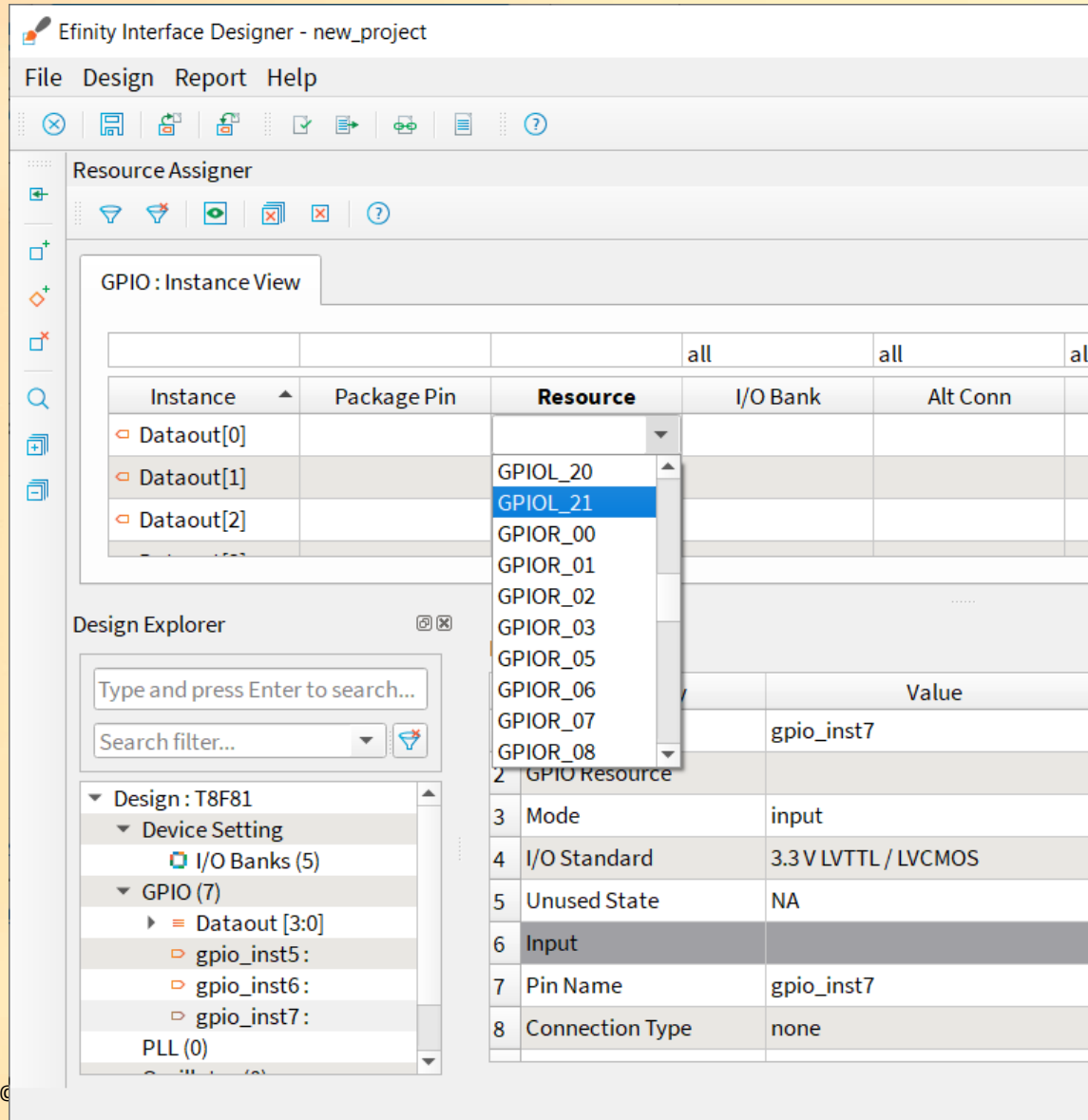
Unused State

input with weak pullup

Add periphery block instance

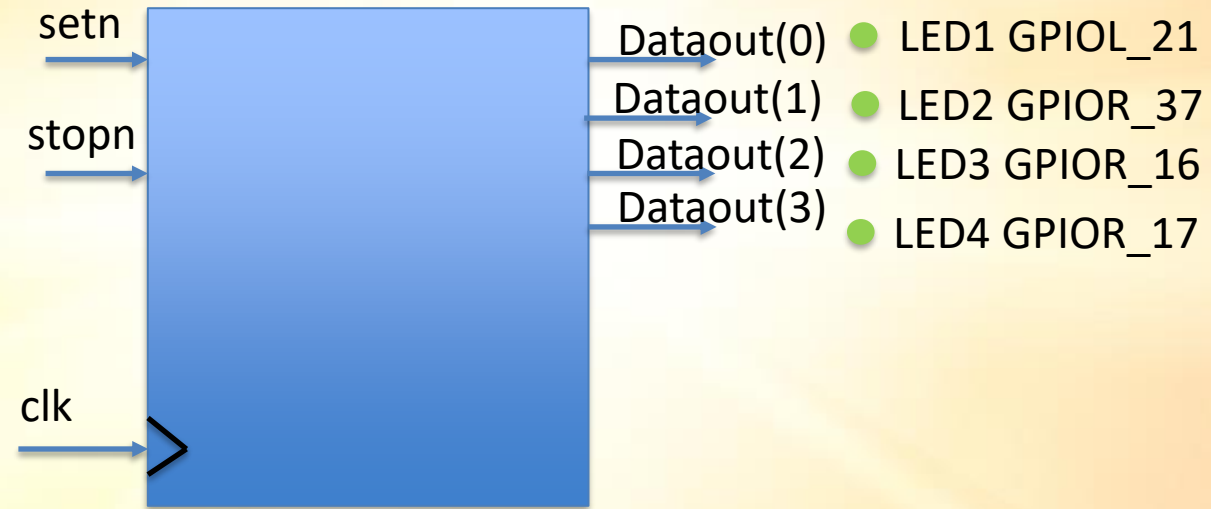
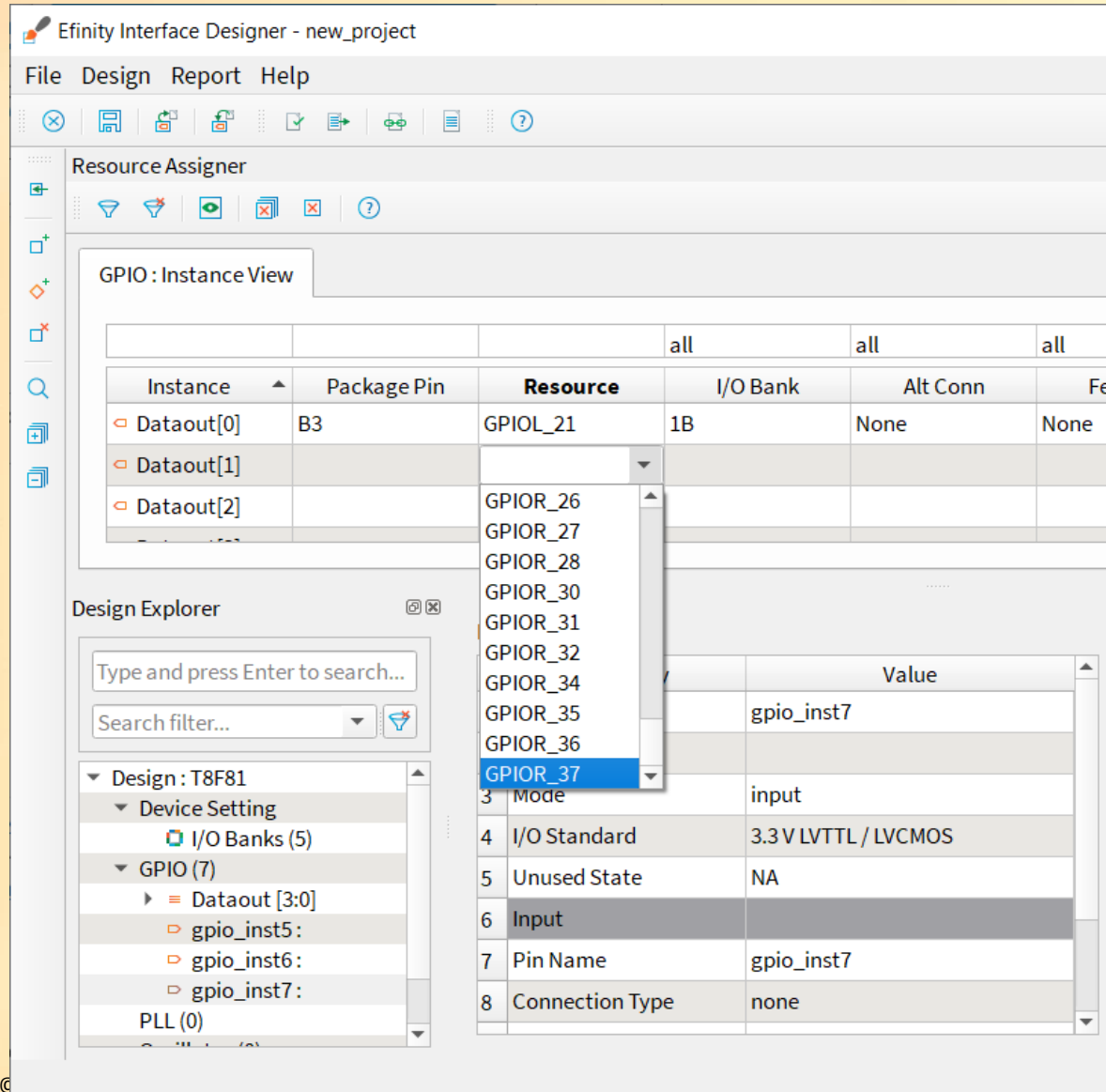
Select GPIO
Create Block
Select GPIO
Create Block
Select GPIO
Create Block

Select GPIO: Instance View Dataout[0]->Resource



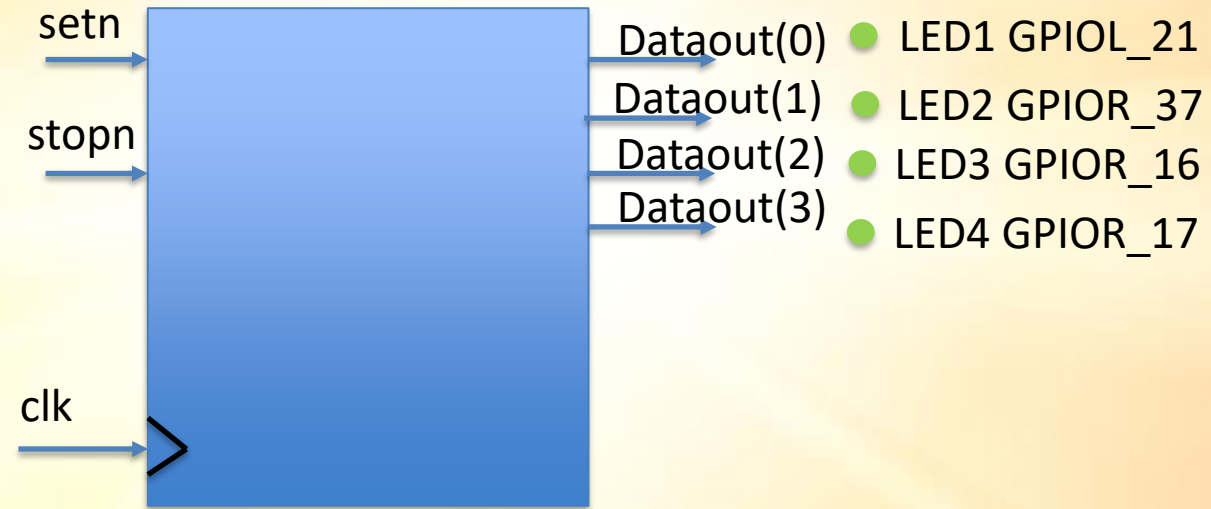
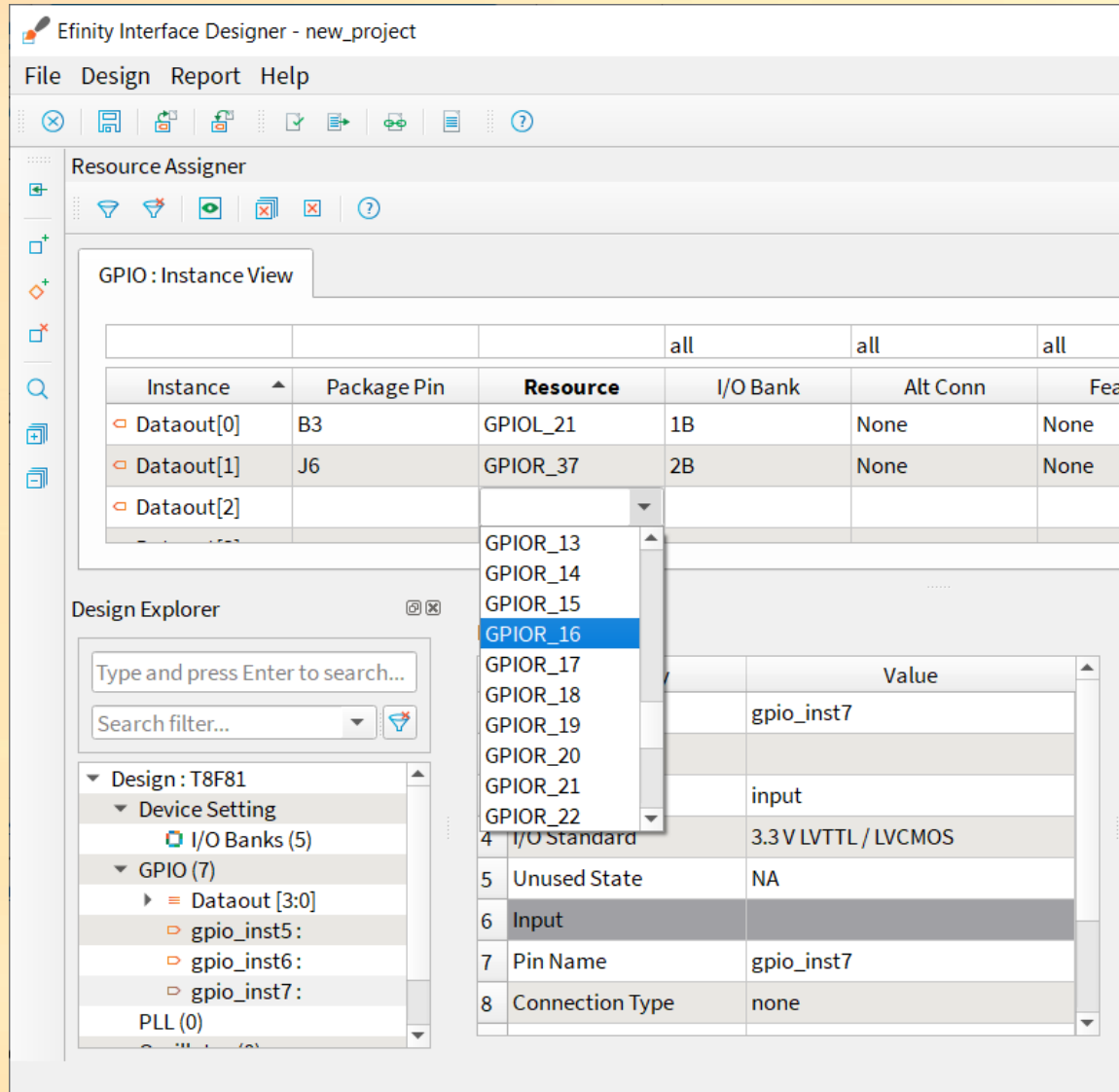
Dataout[0] ->GPIO_L_21

Select GPIO: Instance View Dataout[1]->Resource



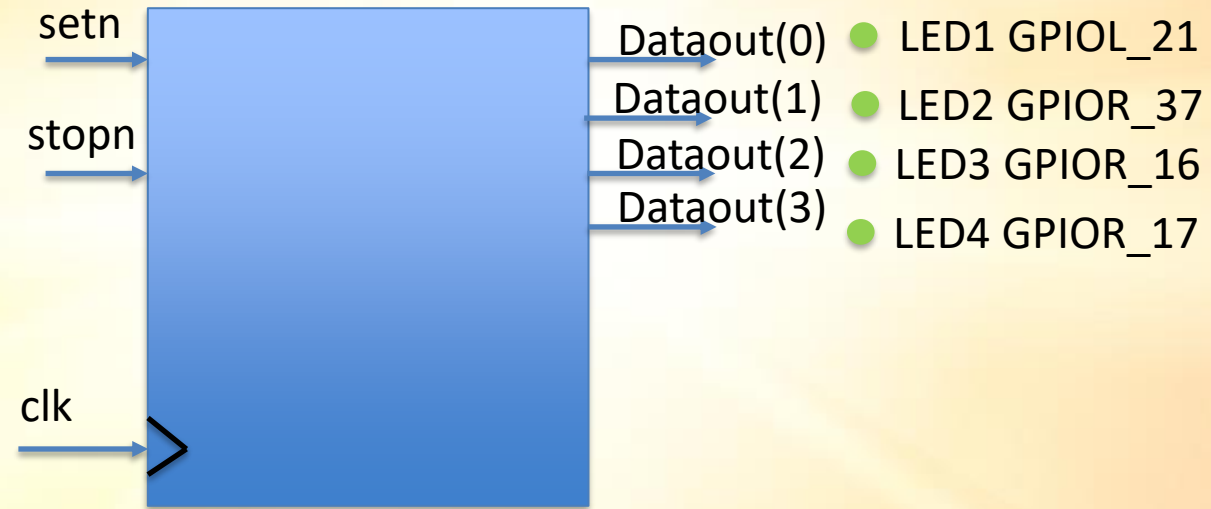
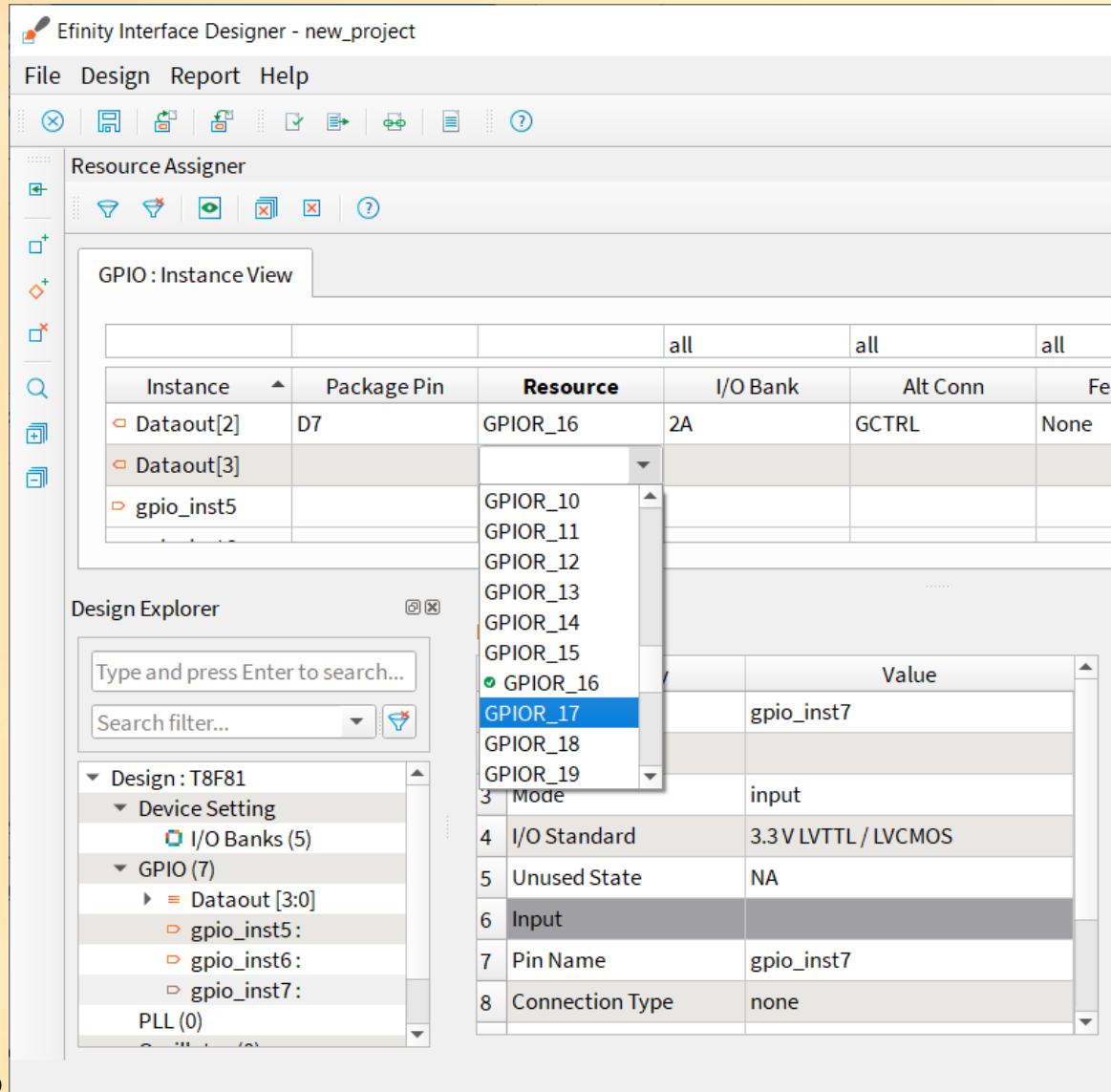
Dataout[1] ->GPIOR_37

Select GPIO: Instance View Dataout[2]->Resource



Dataout[2] -> GPIOR_16

Select GPIO: Instance View Dataout[3]->Resource



Dataout[3] -> GPIOR_17

Change the name from the remaining Inputs: clk

Select gpio_inst5
Enter name in the
Block Editor clk
and press enter !

The screenshot shows the Efinity Interface Designer interface. The Resource Assigner window displays a table of GPIO instances. The Design Explorer on the left shows the project hierarchy, with 'gpio_inst5' selected under 'GPIO (7)'. The Block Summary table lists properties for 'gpio_inst5'. The Block Editor on the right shows the 'Instance Name' field set to 'clk' and the 'Mode' set to 'gpio_inst5'.

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[2]	D7	GPIOR_16	2A	GCTRL	None	R1	GPIOR_16_CTRL7_CBUS1
Dataout[3]	D8	GPIOR_17	2A	GCTRL	None	R1	GPIOR_17_CTRL6_CBUS2
gpio_inst5							

Property	Value
1 Instance Name	gpio_inst5
2 GPIO Resource	
3 Mode	input
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	gpio_inst5
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false

Block Editor fields:

- Instance Name: clk
- Mode: gpio_inst5
- I/O Standard: 3.3 V LVTTTL / LVCMOS
- Input: Pin Name: gpio_inst5, Connection Type: none

setn

The screenshot shows the Efinity Interface Designer interface with the following components:

- Resource Assigner (GPIO : Instance View):** A table listing GPIO instances. The instance `gpio_inst6` is selected.
- Design Explorer:** A tree view on the left showing the project structure. The path `Design : T8F81 > Device Setting > I/O Banks (5) > GPIO (7) > clk > gpio_inst6` is highlighted with a red circle.
- Block Summary:** A table showing properties for the selected instance.
- Block Editor:** A form on the right for configuring the instance. The `Instance Name` field is circled in red and contains the text `setn`.

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[3]	D8	GPIOR_17	2A	GCTRL	None	R1	GPIOR_17_CTRL6_CBUS2
clk							
gpio_inst6							

Property	Value
1 Instance Name	gpio_inst6
2 GPIO Resource	
3 Mode	input
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	gpio_inst6
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false

Instance Name	setn
Mode	input
I/O Standard	3.3 V LVTTTL / LVCMOS
Input	
Pin Name	gpio_inst6
Connection Type	none

Select gpio_inst6
Enter name in the
Block Editor setn
and press enter !

stopn

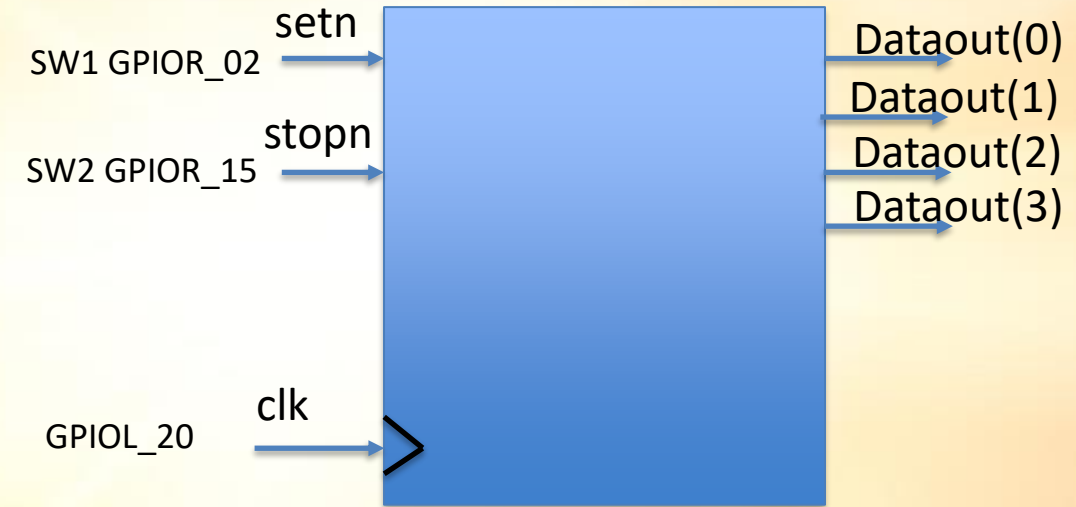
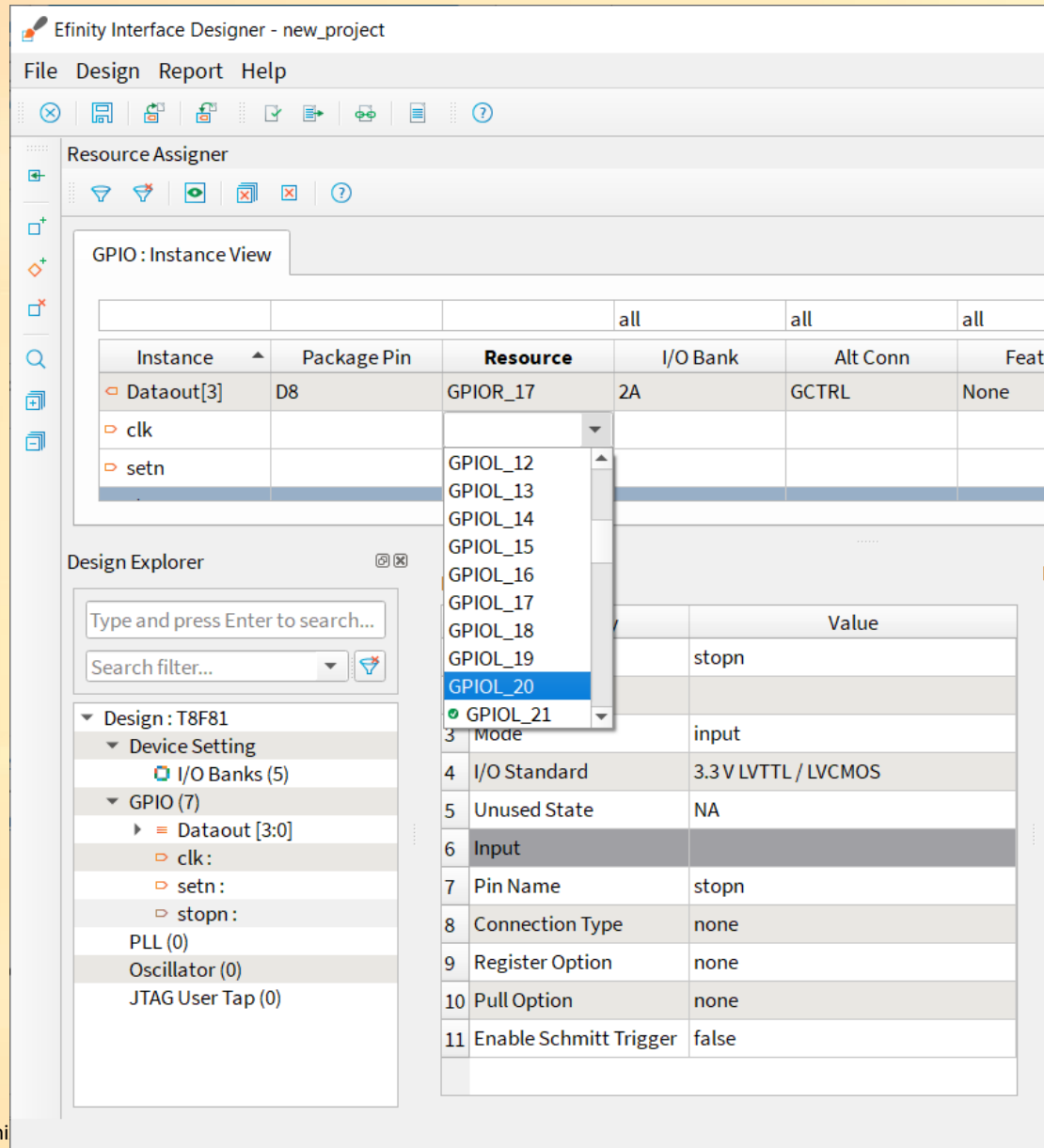
The screenshot shows the Efinity Interface Designer interface. The **Resource Assigner** panel at the top displays the **GPIO : Instance View** table. The **Design Explorer** on the left shows the project hierarchy with **gpio_inst7** selected. The **Block Summary** and **Block Editor** panels are visible at the bottom. In the **Block Editor**, the **Instance Name** field is highlighted with a red circle and contains the text **stopn**.

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
Dataout[3]	D8	GPIOR_17	2A	GCTRL	None	R1	GPIOR_17_CTRL6_CBUS2
clk							
gpio_inst7							

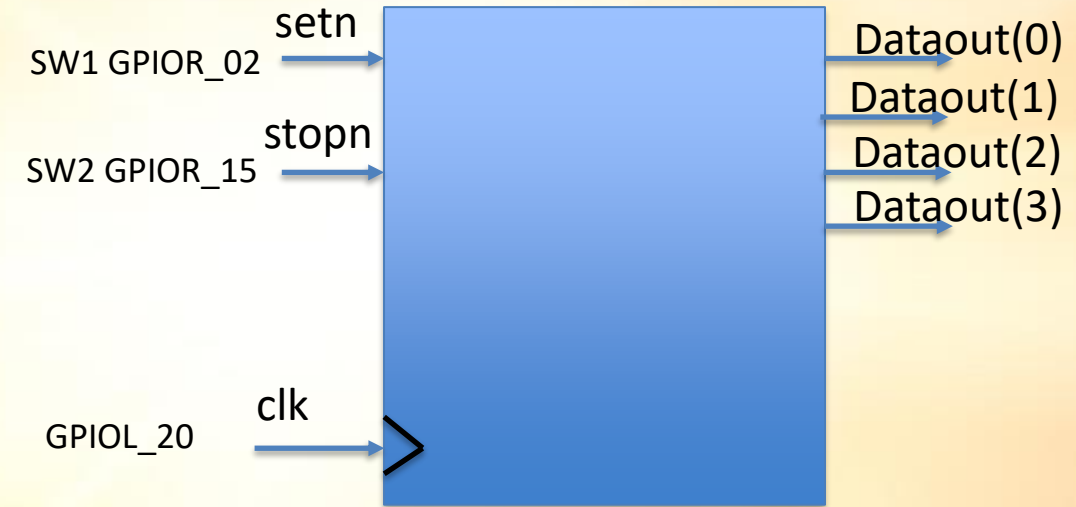
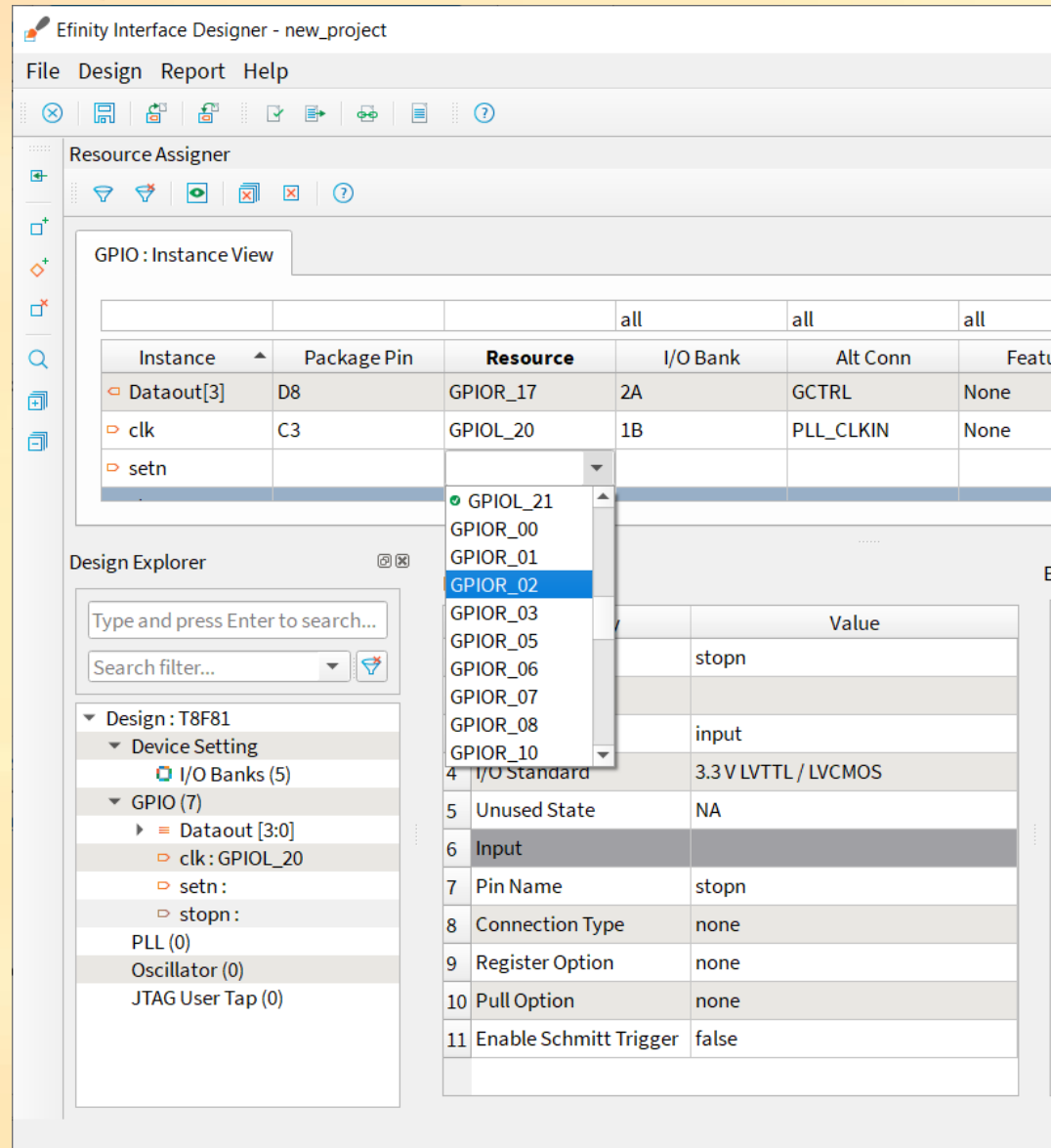
Property	Value
1 Instance Name	gpio_inst7
2 GPIO Resource	
3 Mode	input
4 I/O Standard	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	gpio_inst7
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false

Select gpio_inst8
Enter name in the
Block Editor stopn
and press enter !

Assign the Resource CLK=>GPIOL_20



Assign the Resource setn=>GPIOR_02



Assign the Resource stopn=>GPIOR_15

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Feat
clk	C3	GPIOL_20	1B	PLL_CLKIN	None
setn	C5	GPIOR_02	2A	None	None
stopn					

Design Explorer

Type and press Enter to search...

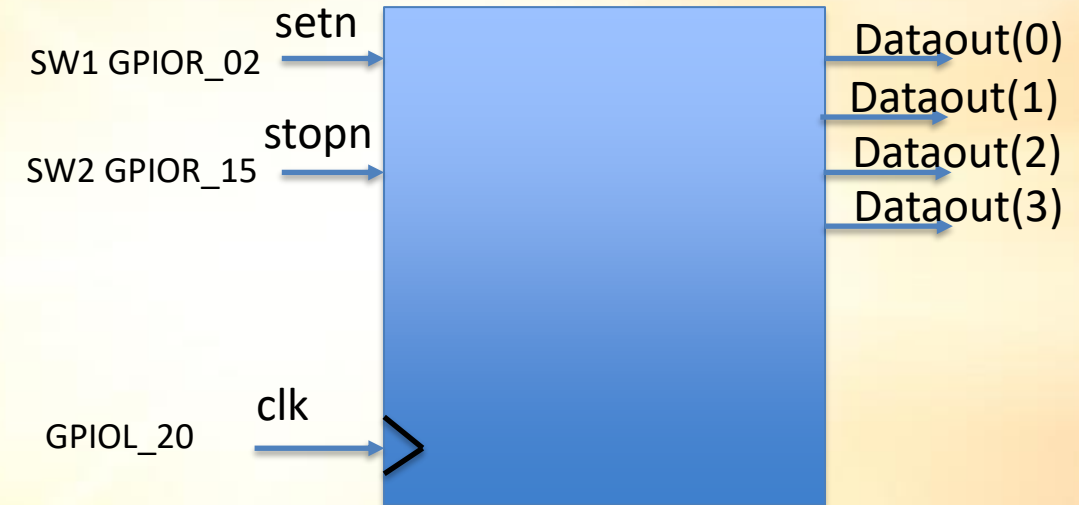
Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (7)
 - Dataout [3:0]
 - clk : GPIOL_20
 - setn : GPIOR_02
 - stopn :
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Value

GPIOR_10	
GPIOR_11	
GPIOR_12	
GPIOR_13	
GPIOR_14	
GPIOR_15	stopn
GPIOR_16	
GPIOR_17	
GPIOR_18	input
GPIOR_19	3.3 V LVTTTL / LVCMOS
5 Unused State	NA
6 Input	
7 Pin Name	stopn
8 Connection Type	none
9 Register Option	none
10 Pull Option	none
11 Enable Schmitt Trigger	false



Check the design and close the interface designer

The screenshot shows the Efinity Interface Designer window with the title 'Efinity Interface Designer - new_project'. The menu bar includes 'File', 'Design', 'Report', and 'Help'. The toolbar contains various icons, with the 'Check Design' icon (a green checkmark) circled in red. Below the toolbar is the 'Resource Assigner' section, which includes a 'GPIO : Instance View' table. The table has columns for Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, Clock Region, and Pad. It lists three instances: 'clk' (GPIO_L_20), 'setn' (GPIOR_02), and 'stopn' (GPIOR_15). Below the table is the 'Design Explorer' section, which shows a tree view of the design hierarchy. The 'Block Summary' section displays a table of properties for the selected 'stopn' instance. The 'Block Editor' section shows the configuration for the 'stopn' instance, including its name, mode, I/O standard, and input settings.

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
clk	C3	GPIO_L_20	1B	PLL_CLKIN	None	L1	GPIO_L_20_PLLIN
setn	C5	GPIOR_02	2A	None	None	R1	GPIOR_02_RESERVED_OUT
stopn	C9	GPIOR_15	2A	None	None	R1	GPIOR_15_CBUS0

Design Explorer

Type and press Enter to search...

Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (7)
 - Dataout [3:0]
 - clk : GPIO_L_20
 - setn : GPIOR_02
 - stopn : GPIOR_15
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Block Summary

Property	Value
1 Instance Name	stopn
2 GPIO Resource	GPIOR_15
3 Mode	input
4 I/O Standard	3.3V LVTTL / LVCMOS
5 Unused State	NA
6 Alternate Connection	None
7 Features	None
8 Clock Region	R1
9 I/O Bank	2A
10 Pad	GPIOR_15_CBUS0
11 Package Pin	C9
12 Input	

Block Editor

Instance Name

stopn

Mode

input

I/O Standard

3.3V LVTTL / LVCMOS

Input

Pin Name

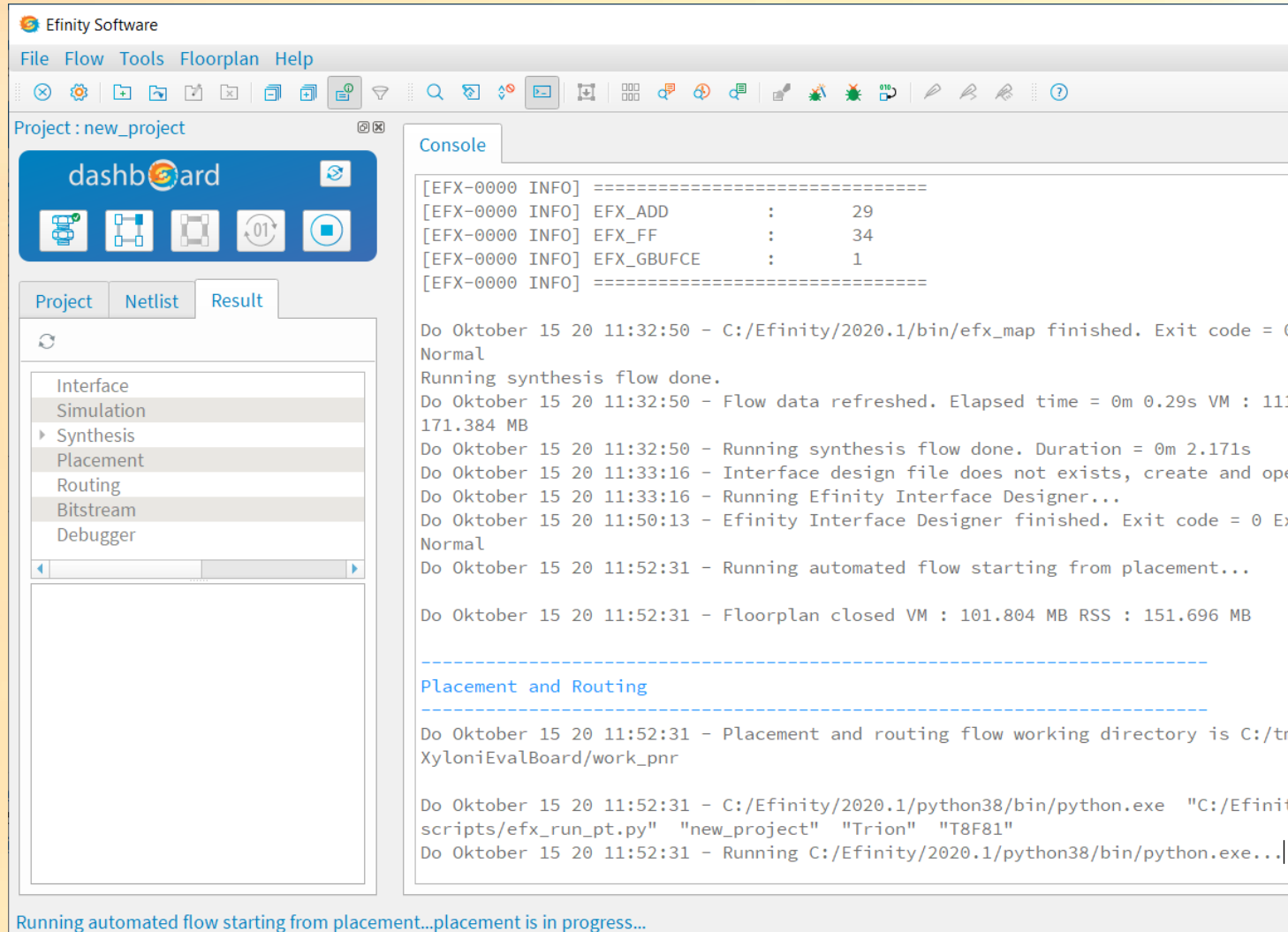
stopn



Connection Type

none

Check design...done. 0 issue.

Run the whole flow with clicking on placement



- If the Automated flow button is grayed out click on the button to activate the automated flow. 
- Click on the Place icon and the flow will run automatically 



If you have an unassigned pin, check the Placement report, go back to interface designer and fix the name and rerun the flow

The screenshot displays the Efinity Software interface with the following components:

- Project : new_project** (top left)
- dashbord** (top left, blue header)
- Project | Netlist | Result** (tabs)
- Placement** (selected in the left sidebar)
- Outputs** table:

Outputs	5 / 113
Clocks	1 / 16
Logic Elements	37 / 7384
Memory Blocks	0 / 24
Multipliers	0 / 8
Interface	
Missing Interface Pins	1
Unassigned Core Pins	1
Timing	
Least Slack	23.349 ns
clk	103.613 MHz
Debugger	
- Console** (middle left):

```
efinixprojects/T8EvalBoard/outflow/  
new_project.interface.csv'.  
Successfully processed  
interface constraints file  
"D:/user/efinixprojects/  
T8EvalBoard/outflow/  
new_project.interface.csv".  
  
SDC file 'D:/user/  
efinixprojects/T8EvalBoard/  
counterconstrain.sdc' parsed  
successfully.  
1 clocks (including virtual  
clocks), 0 inputs and 0  
outputs were constrained.  
  
Maximum possible analyzed  
clocks frequency  
Clock Name      Period (ns)  
Frequency (MHz)  Edge  
clk              9.651  
103.613         (R-R)  
  
Geomean max period: 9.651  
  
Launch Clock    Capture Clock  
Constraint (ns) Slack (ns)  
Edge           clk  
clk            33.000    23.349    (R-  
R)
```
- Code Editor** (right):
 - new_project.place.rpt** (selected):

```
11  
12 ----- Resource Summary (begin) -----  
13 Inputs: 3 / 96 (3.12%)  
14 Outputs: 5 / 113 (4.42%)  
15 Clocks: 1 / 16 (6.25%)  
16 Logic Elements: 37 / 7384 (0.50%)  
17   LE: LUTs/Adders: 31 / 7384 (0.42%)  
18   LE: Registers: 35 / 5280 (0.66%)  
19 Memory Blocks: 0 / 24 (0.00%)  
20 Multipliers: 0 / 8 (0.00%)  
21 ----- Resource Summary (end) -----  
22  
23 Elapsed time for packing: 0 hours 0 minutes 0 seconds  
24  
25 ----- IO Interface Summary (begin) -----  
26  
27 +-----+  
28 | Missing Interface Pins | Input/Output |  
29 +-----+  
30 | stop | Input |  
31 +-----+  
32  
33 ----- IO Interface Summary (end) -----  
34  
35 ----- IO Placement Summary (begin) -----  
36  
37 +-----+  
38 | Unassigned Core Pins | Input/Output |  
39 +-----+  
40 | stopn | Input |  
41 +-----+  
42  
43 ----- IO Placement Summary (end) -----  
44  
45 Elapsed time for placement: 0 hours 0 minutes 1 seconds  
46  
47
```

Typo in
Interface
designer:
stop instead
of **stopn**

Check static timing

The screenshot displays the Efinity Software interface with the following components:

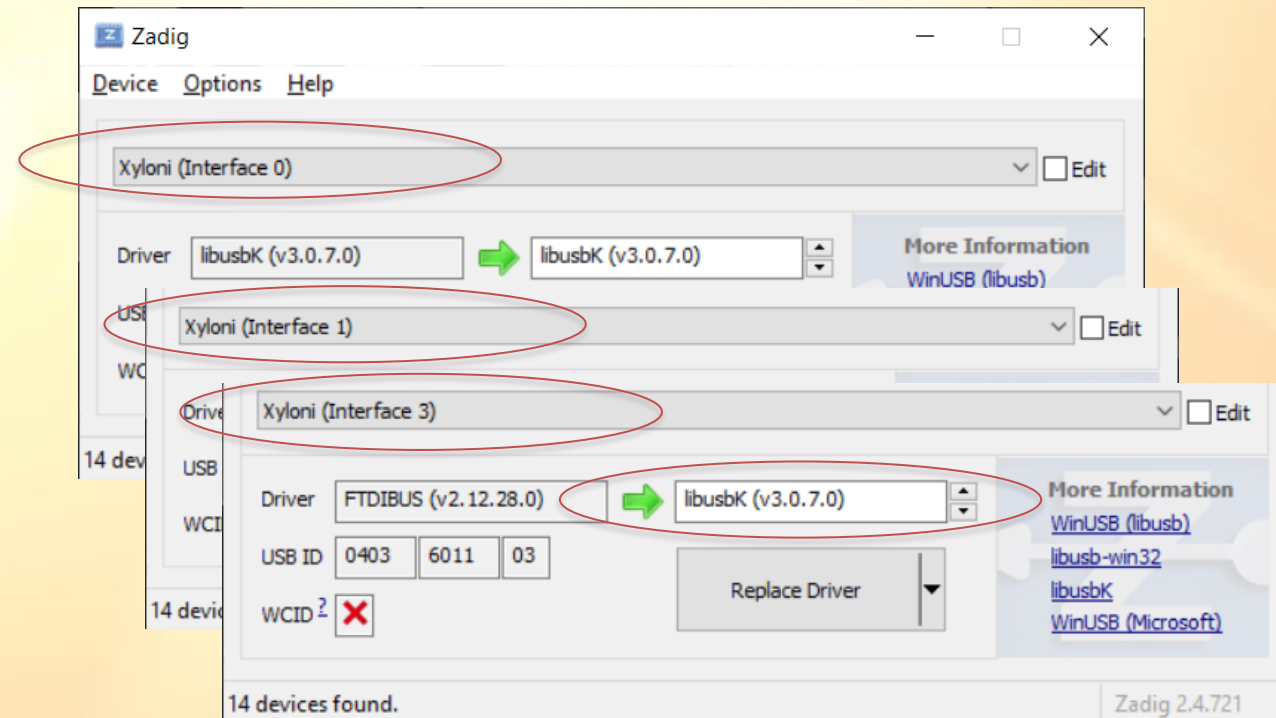
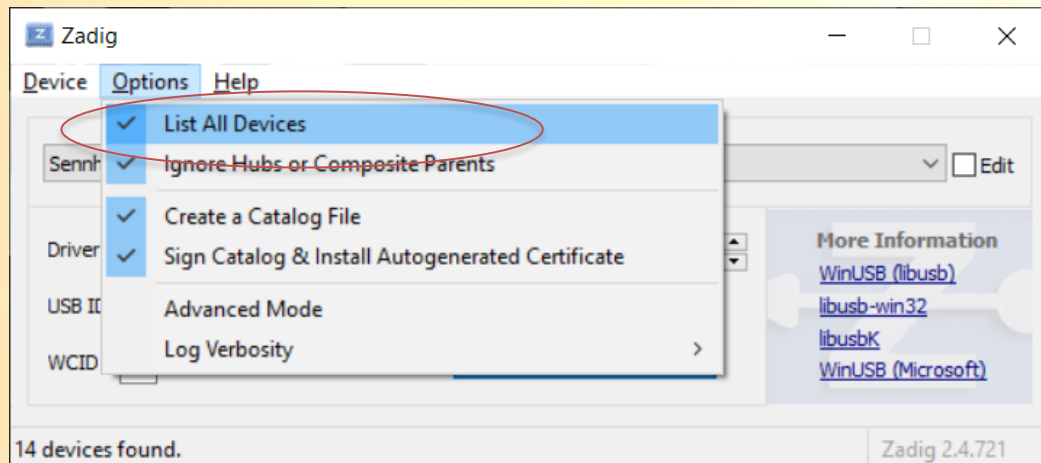
- Project:** new_project
- Console:** Shows the completion of parsing the switch_block file and the generation of 393829 RR nodes and 1460307 RR edges. It also indicates that the design has 0 global control net(s).
- Code Editor:** Displays the file new_project.timing.rpt. The file content includes:
 - temperature : 0C to 85C
 - voltage : 1.1V +/-50mV
 - speedgrade : 2
 - technology : s40ll
 - status : final
 - Table of Contents (begin)
 - 1. Clock Frequency Summary
 - 2. Clock Relationship Summary
 - 3. Path Details for Max Critical Paths
 - 4. Path Details for Min Critical Paths
 - Table of Contents (end)
 - 1. Clock Frequency Summary (begin)
 - User target constrained clocks
 - Table with 5 columns: Clock Name, Period (ns), Frequency (MHz), Waveform, Source.
 - Table with 2 columns: Clock Name, Period (ns), Frequency (MHz), Edge (R-R).
 - Geomean max period: 9.934
 - Clock Frequency Summary (end)

To check the static timing select routing_new_project.timing.rpt.

Here you will find the constrains from the constrain file (clk :30ns) and the result

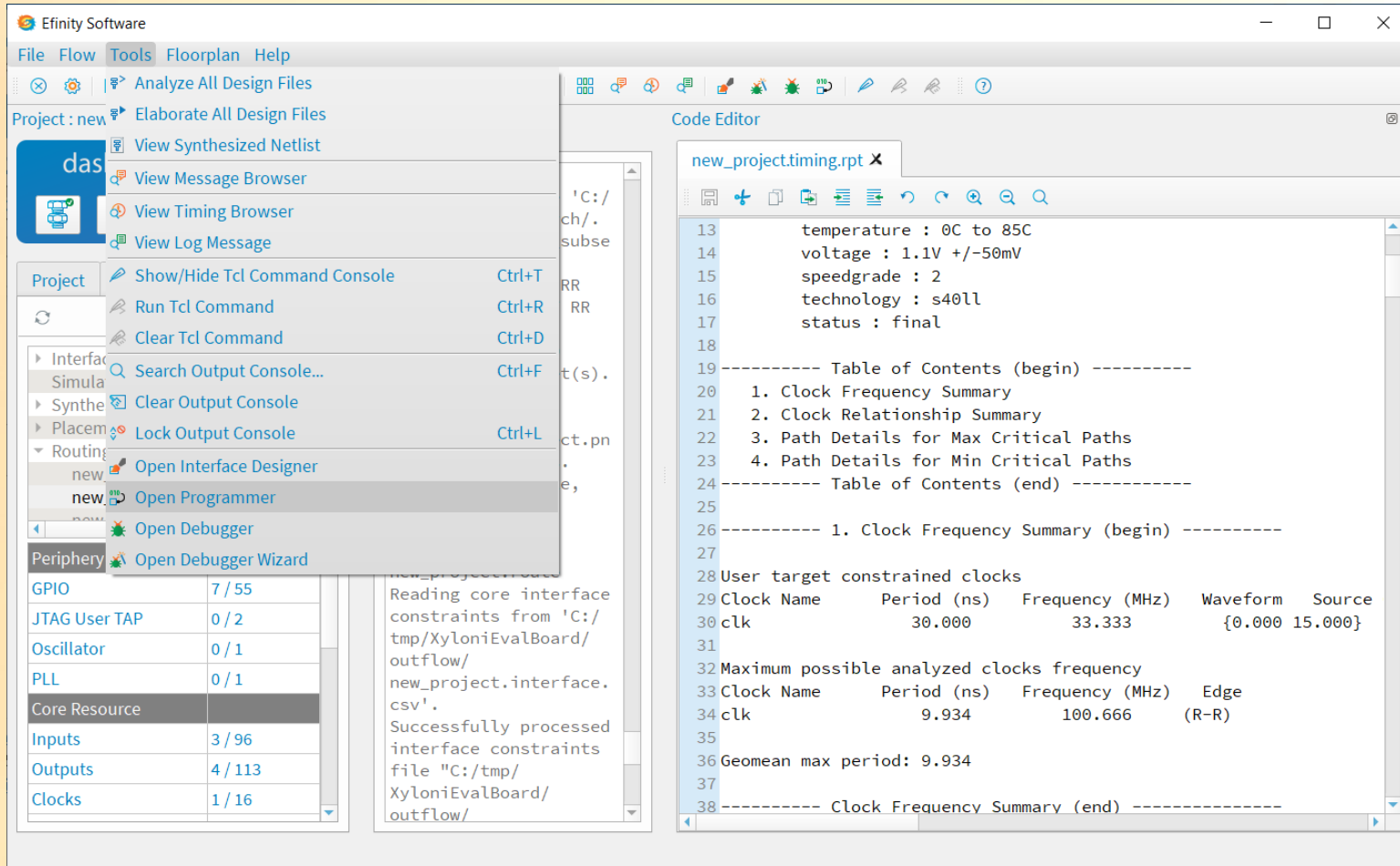
Program the Device

- To program the Device you have to install the USB driver first !
- Select Options->List All Devices
- Change the driver for Xyloni (Interface 0,1,3) to libusbK.
- Please do not choose WinUSB or select interface 2 !



Program the Device

Open Programmer
Tools->OpenProgrammer



Select Image File, Start Program (Check USB Target: Xyloni)

The image displays three screenshots of the Efinity Programmer software interface, illustrating the steps to select an image file and start a program.

Left Screenshot: The main window shows the 'Target' dropdown set to 'Xyloni' (circled in red). The 'USB Info' field displays 'ID: 0403:6011'. The 'Image' section has a 'Bitstream File' field and an 'FPGA' dropdown set to 'T8F81' (circled in red). The 'Programming Mode' is set to 'SPI Active'. The 'SPI Active Options' section includes 'Starting Flash Address' (0x00000000), 'Flash Length' (173380 Bytes), and a checked 'Erase Before Program' option. The 'Device Configuration Status' shows 'Last Updated: Mon Nov 16 20'.

Middle Screenshot: The 'Open Image File' dialog box is open, showing the 'Look in' path as 'C:\tmp\XyloniEvalBoard\outflow'. The file list shows 'new_project.bit' and 'new_project.hex' (circled in red). The 'File name' field is set to 'new_project.hex', and the 'Files of type' dropdown is set to 'Image File (*.hex *.bit)'. The 'Open' button is circled in red.

Right Screenshot: The main window shows the 'Target' dropdown set to 'Xyloni'. The 'USB Info' field displays 'Bus 000 Device 254: ID 0403:6011'. The 'Image' section has a 'Bitstream File' field set to 'yloniEvalBoard/outflow/new_project.bit' and an 'FPGA' dropdown set to 'T8F81'. The 'Programming Mode' is set to 'SPI Active'. The 'SPI Active Options' section includes 'Starting Flash Address' (0x00000000), 'Flash Length' (173380 Bytes), and a checked 'Erase Before Program' option. The 'Device Configuration Status' shows 'Last Updated: Thu Oct 15 20'. The 'Start' button (a blue play icon) is circled in red.

Bottom Screenshot: The 'Device Configuration Status' section shows a log of events:

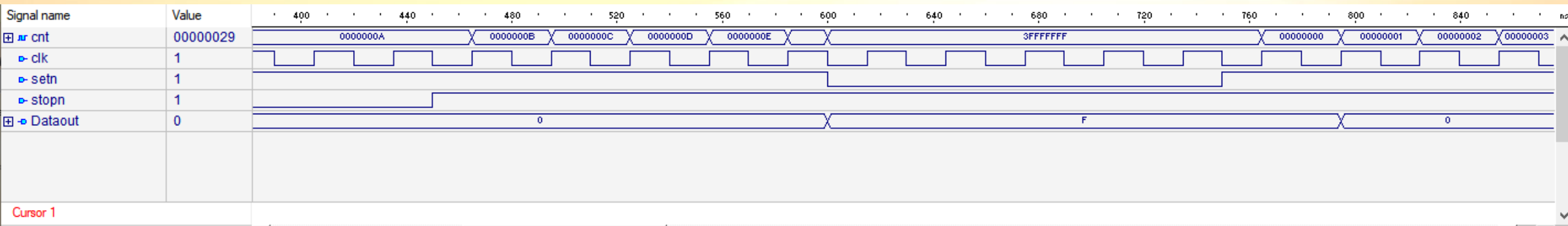
- Mo November 16 20 13:10:25 - Valid device ID found: 0x00000000
- SPI freq 6.0 MHz
- Do Oktober 15 20 12:10:09 - Erasing 172 KiB from flash @ 0x00000000 (may take a while...)
- Do Oktober 15 20 12:10:13 - Finished erase in 4 seconds
- Do Oktober 15 20 12:10:13 - Writing 169 KiB to flash @ 0x00000000 ...
- Do Oktober 15 20 12:10:15 - Finished write in 2 seconds
- Do Oktober 15 20 12:10:15 - Reading 169 KiB from flash @ 0x00000000 ...
- Do Oktober 15 20 12:10:16 - Finished read in 0 seconds

Problem solving

- All LED ON: Check VHDL if you have the correct setting for the frequency ! (29 downto 26) vs (17 downto 14)
- If you can not see the Xyloni, check if you installed the correct USB driver with zadig

Simulation

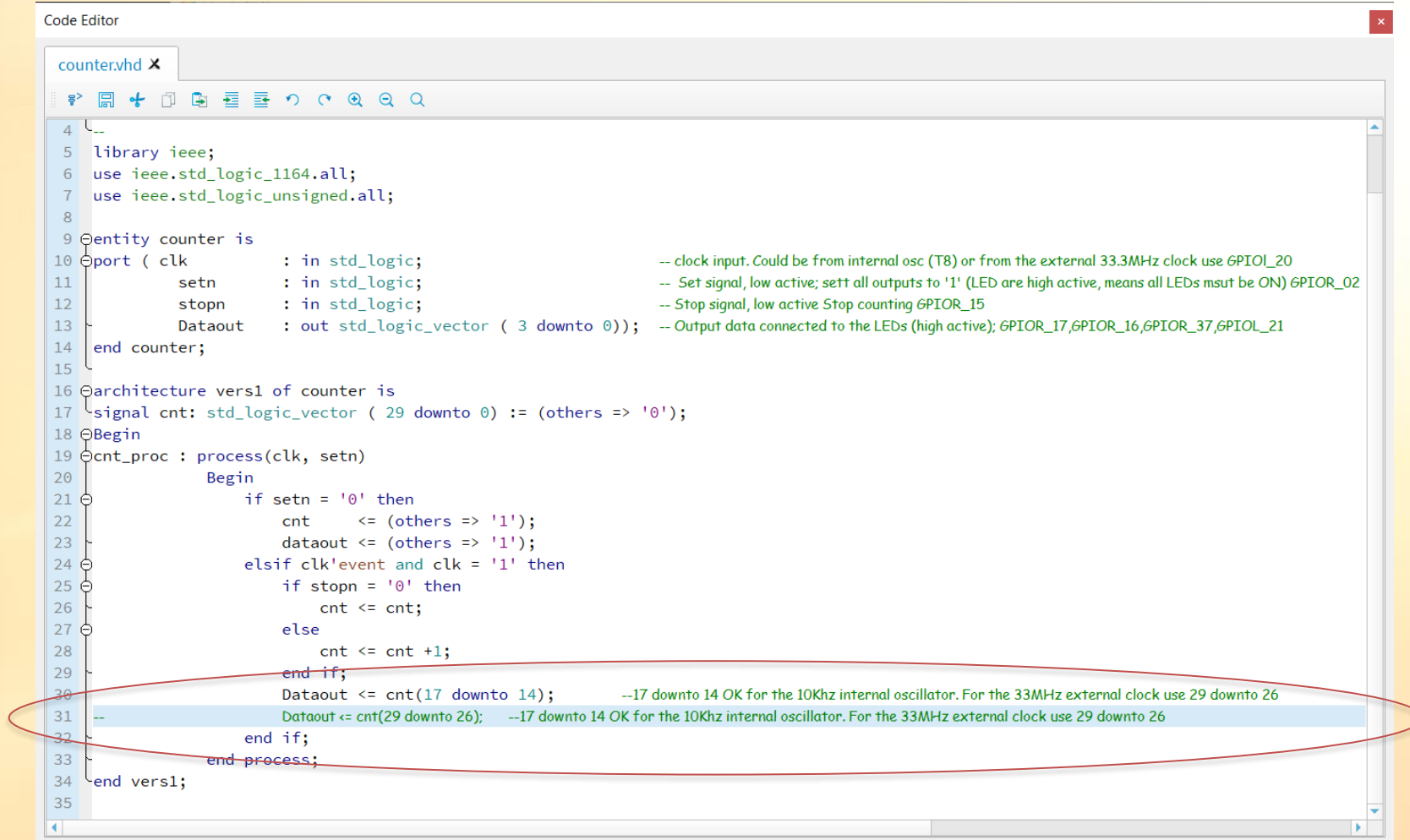
- For HDL simulation you can use any VHDL simulator. The testbench is included in the design.
- Here a wave form the design with testbench with an ALDEC HDL simulator.



- If you would like to simulate the synthesized netlist, include the new_project.dbg.map.v below the outflow folder and include the simulation libraries <installation path>\Efinity\2020.1\sim_models\verilog folder instead of the RTL Design

Design with OSC

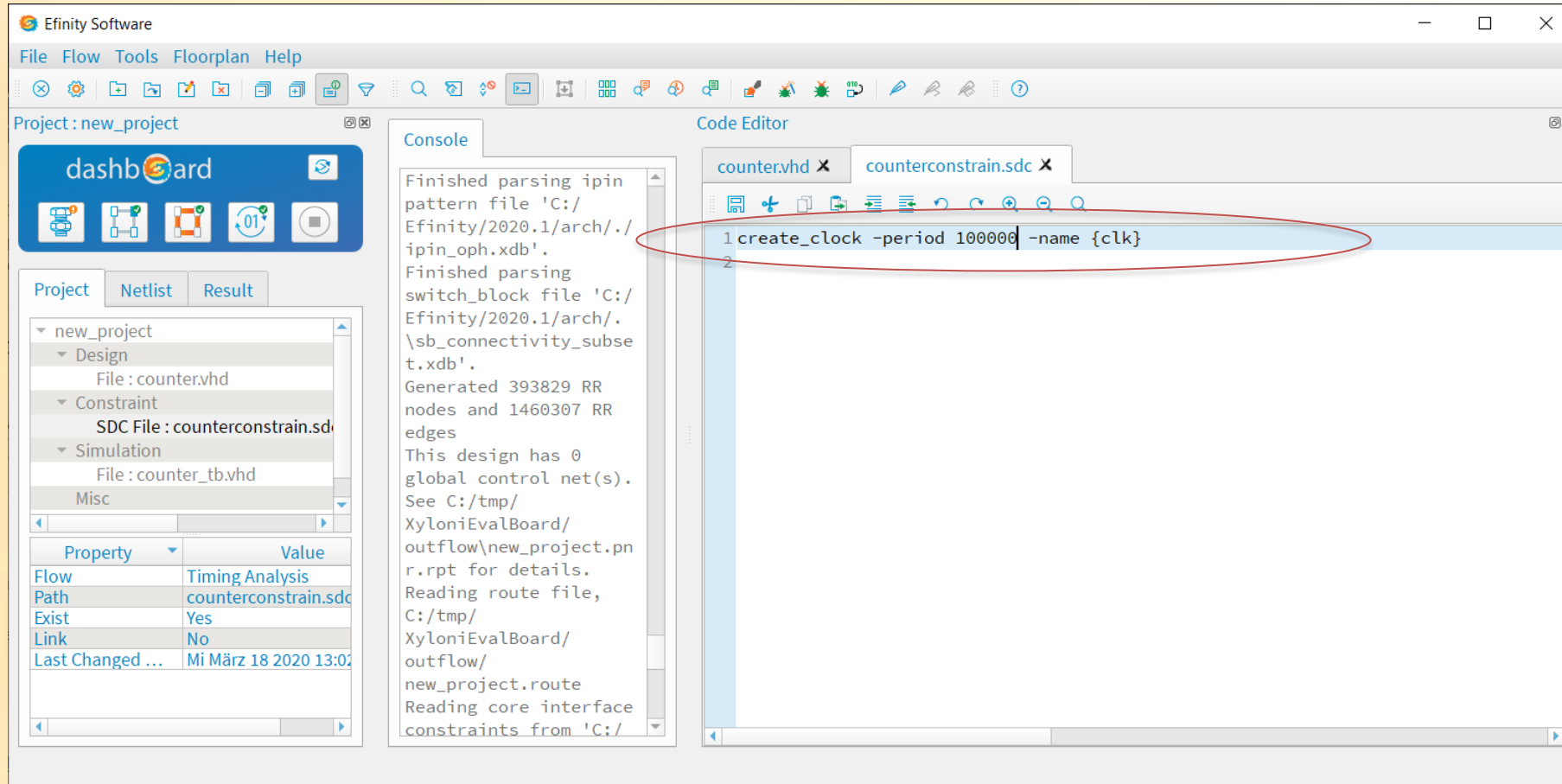
1. change VHDL file



```
4  --
5  library ieee;
6  use ieee.std_logic_1164.all;
7  use ieee.std_logic_unsigned.all;
8
9  entity counter is
10 port ( clk          : in std_logic;          -- clock input. Could be from internal osc (T8) or from the external 33.3MHz clock use GPIOL_20
11        setn         : in std_logic;          -- Set signal, low active; sett all outputs to '1' (LED are high active, means all LEDs msut be ON) GPIOR_02
12        stopn        : in std_logic;          -- Stop signal, low active Stop counting GPIOR_15
13        Dataout       : out std_logic_vector ( 3 downto 0)); -- Output data connected to the LEDs (high active); GPIOR_17,GPIOR_16,GPIOR_37,GPIOL_21
14 end counter;
15
16 architecture vers1 of counter is
17 signal cnt: std_logic_vector ( 29 downto 0) := (others => '0');
18 begin
19 cnt_proc : process(clk, setn)
20 begin
21     if setn = '0' then
22         cnt    <= (others => '1');
23         dataout <= (others => '1');
24     elsif clk'event and clk = '1' then
25         if stopn = '0' then
26             cnt <= cnt;
27         else
28             cnt <= cnt +1;
29         end if;
30         Dataout <= cnt(17 downto 14);          --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
31         -- Dataout <= cnt(29 downto 26);      --17 downto 14 OK for the 10Khz internal oscillator. For the 33MHz external clock use 29 downto 26
32     end if;
33 end process;
34 end vers1;
35
```

Design with OSC

2. change constrain file



Change Interface designer

- 3. Delete clk GPIO; Seelct clk->RMB->Delete

Design Explorer

Type and press Enter to search...

Search filter...

Design : T8F81

- Device Setting
 - I/O Banks (5)
 - GPIO (7)
 - Dataout [3:0]
 - clk : GPIOL_20**
 - setn : GPIOR_02
 - stopn : GPIOR_15
 - PLL (0)
 - Oscillator (0)
 - JTAG User Tap (0)

Block Summary

	Property	
1	Instance Name	clk
2	GPIO Resource	GPIOL_
3	Mode	input
4	I/O Standard	3.3 V LV
5	Unused State	NA
6	Alternate Connection	PLL_CI
7	Features	None
8	Clock Region	L1
9	I/O Bank	1B
10	Pad	GPIOL_
11	Package Pin	C3
12	Input	
13	Pin Name	clk
14	Connection Type	none

Block Editor

clk

Mode

input

I/O Standard

3.3 V LVTTTL / LVCMOS

Input

Pin Name

clk

Connection Type

none

Register Option

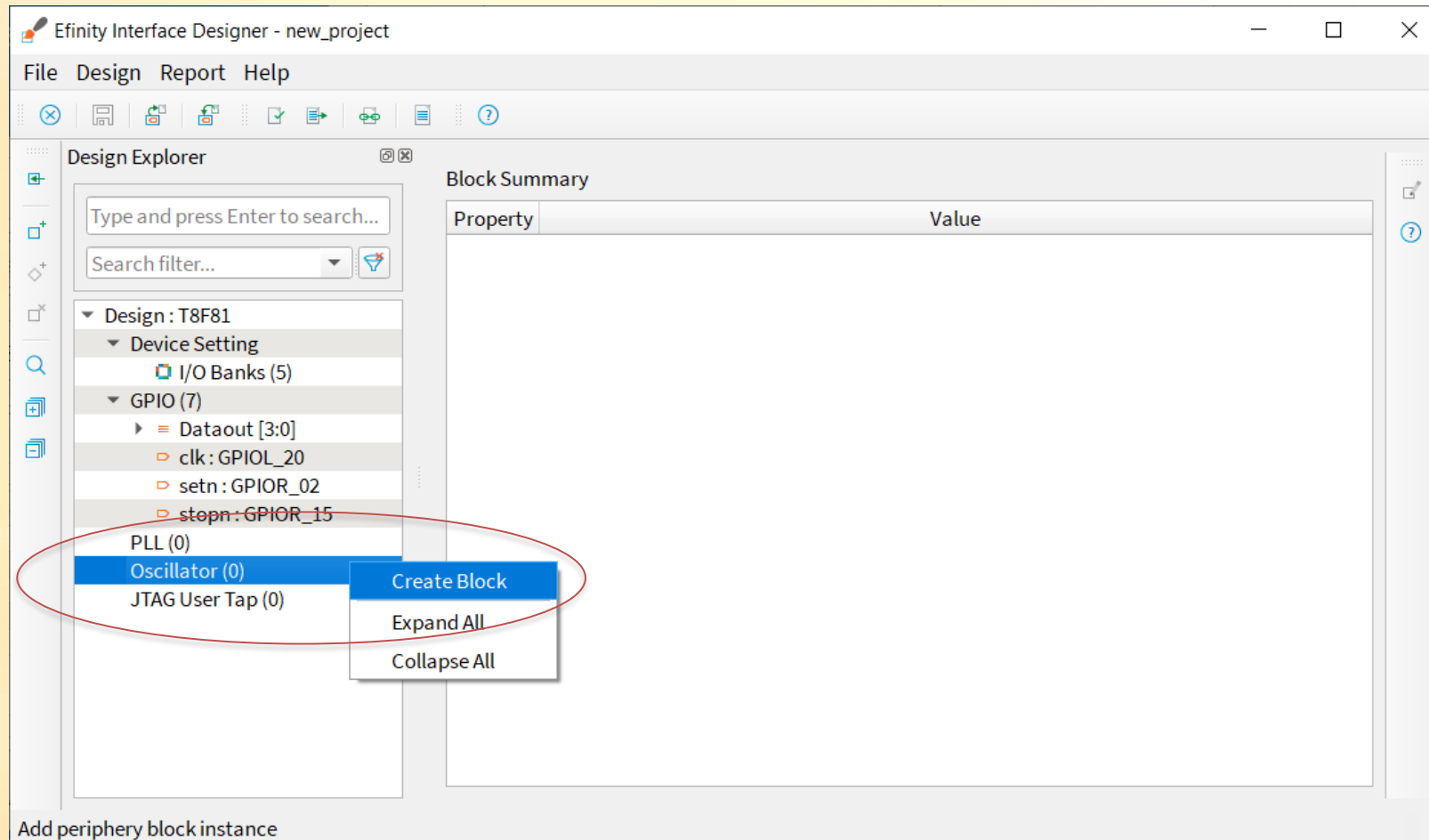
none

Clock

Delete peripheral block instance

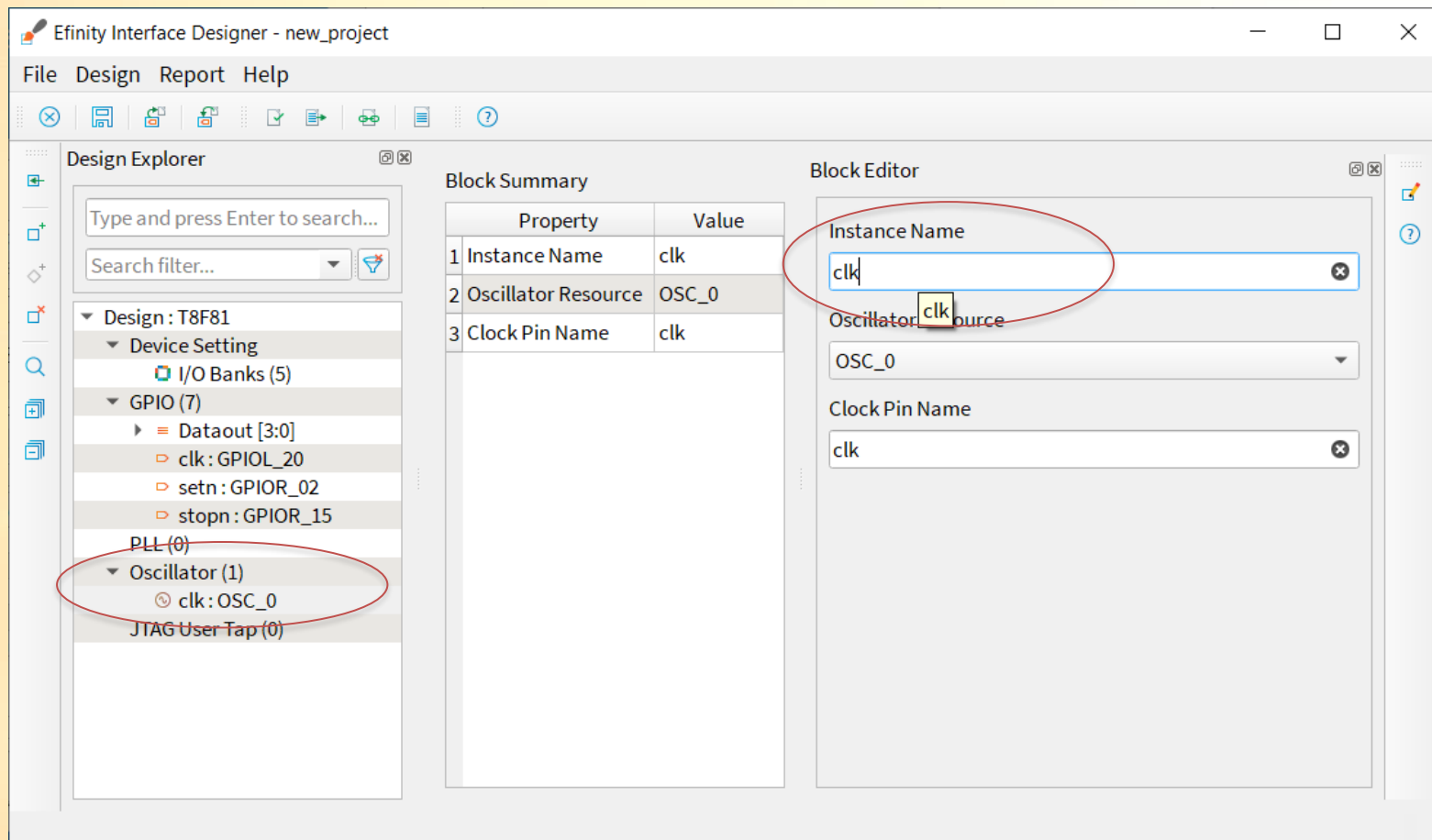
Change Interface designer

4. Add OSC; select Oscillator; RMB; Create Block

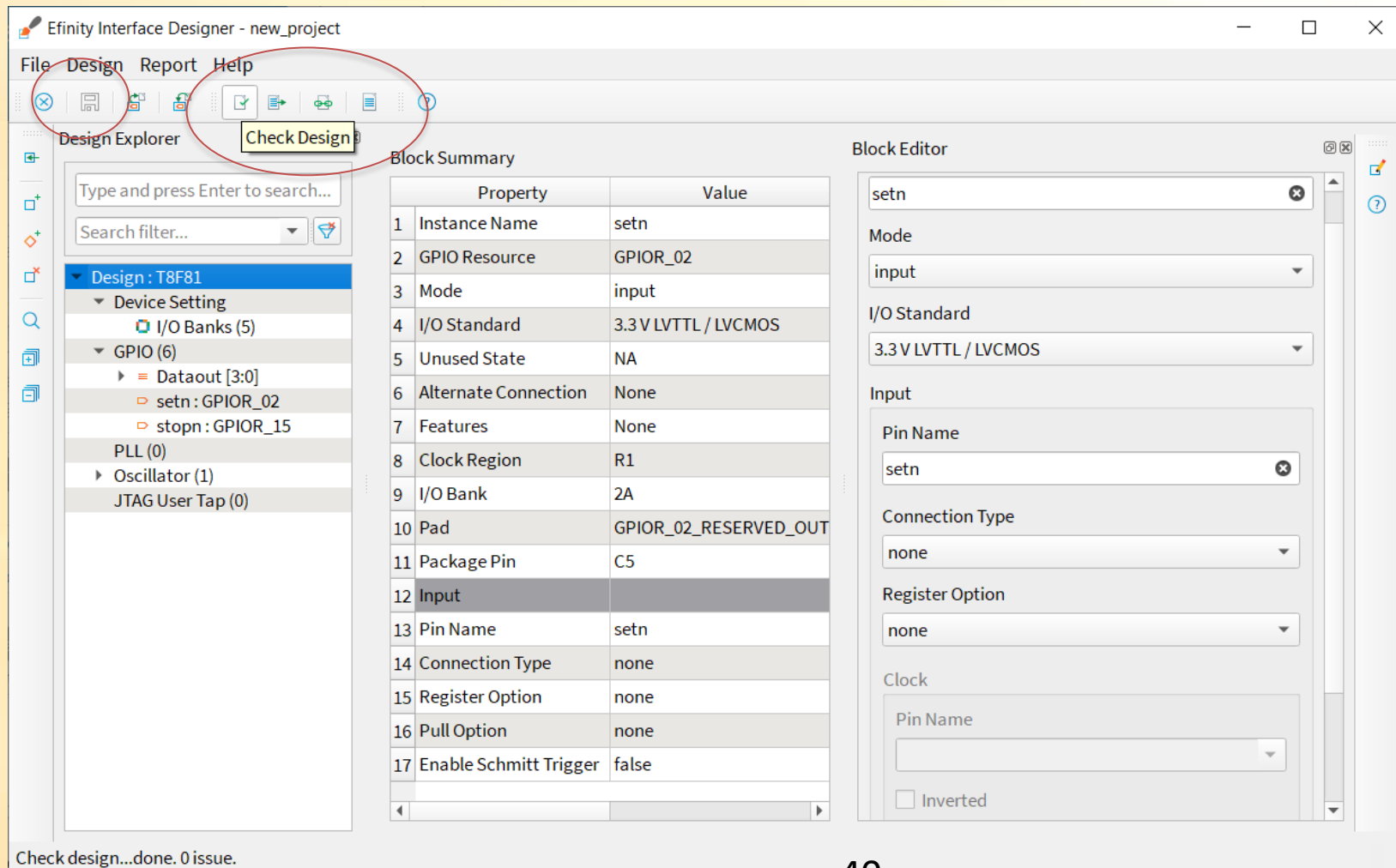


Change Interface designer

5. Assign clk to OSC Instance Name, **press ENTER !**



Check Design and save



Run the whole flow with pressing Synthesis



Efinity Software

File Flow Tools Floorplan Help

Project : new_project

dashboard

Project Netlist Result

new_project

- Design
 - File : counter.vhd
- Constraint
 - SDC File : counterconstrain.sdc
- Simulation
 - File : counter_tb.vhd
- Misc

Property	Value
Flow	Timing Analysis
Path	counterconstrain.sdc
Exist	Yes
Link	No
Last Changed ...	Mi März 18 2020 13:02

Console

```
INFO: Reading Mapping Library peak resident set memory usage = 37.312 MB
INFO: ***** Ending Reading Mapping Library ... *****
[EFX-0000 INFO] ... Pre-synthesis checks begin
[EFX-0000 INFO] ... Pre-synthesis checks end (Real time : 0s)
[EFX-0000 INFO] ... NameSpace init begin
[EFX-0000 INFO] ... NameSpace init end (Real time : 0s)
[EFX-0000 INFO] ... Mapping design "counter"
[EFX-0000 INFO] ... Hierarchical pre-synthesis "counter" begin

[EFX-0000 INFO] ... Hierarchical pre-synthesis "counter" end (Real time : 0s)
[EFX-0000 INFO] ... Flat optimizations begin
[EFX-0000 INFO] ... Flat optimizations end (Real time : 0s)
[EFX-0000 INFO] ... Flat synthesis begin
[EFX-0000 INFO] ... Flat synthesis end (Real time : 0s)
[EFX-0000 INFO] ... Flat optimizations begin
[EFX-0000 INFO] ... Flat optimizations end (Real time : 0s)
[EFX-0000 INFO] ... Check and break combinational loops begin
[EFX-0000 INFO] ... Check and break combinational loops end (Real time : 0s)
[EFX-0000 INFO] ... Top level netlist RUSHC IOs pre-synthesis begin
[EFX-0000 INFO] ... SOP modeling begin

[EFX-0000 INFO] ... SOP modeling end (Real time : 0s)
[EFX-0000 INFO] ... LUT mapping begin
```

Code Editor

counterconstrain.sdc

```
1 create_clock -peri
2
```

Running automated flow starting from synthesis...synthesis is in progress...

Check static timing

To check the static timing select routing_new_project.timing.rpt.

Here you will find the constrains from the constrain file (clk :100000ns) and the result

The screenshot displays the Efinity Software interface with the following components:

- Project:** new_project
- dashb@rd:** Includes icons for Project, Netlist, and Result.
- Project Tree:** Shows a hierarchy of files including new_project.route.rpt and new_project.timing.rpt.
- Periphery Resource:** A table listing resources and their counts.
- Core Resource:** A table listing core resources and their counts.
- Console:** Displays the output of the static timing analysis, including the netlist pre-processing time and the maximum possible analyzed clocks frequency.
- Code Editor:** Shows the content of the new_project.timing.rpt file, which includes the clock constraints and the static timing analysis results.

Periphery Resource Table:

Resource	Count
GPIO	6 / 55
JTAG User TAP	0 / 2
Oscillator	1 / 1
PLL	0 / 1

Core Resource Table:

Resource	Count
Inputs	3 / 96
Outputs	4 / 113
Clocks	1 / 16
Logic Elements	24 / 7384

Static Timing Analysis Results (from Console and Code Editor):

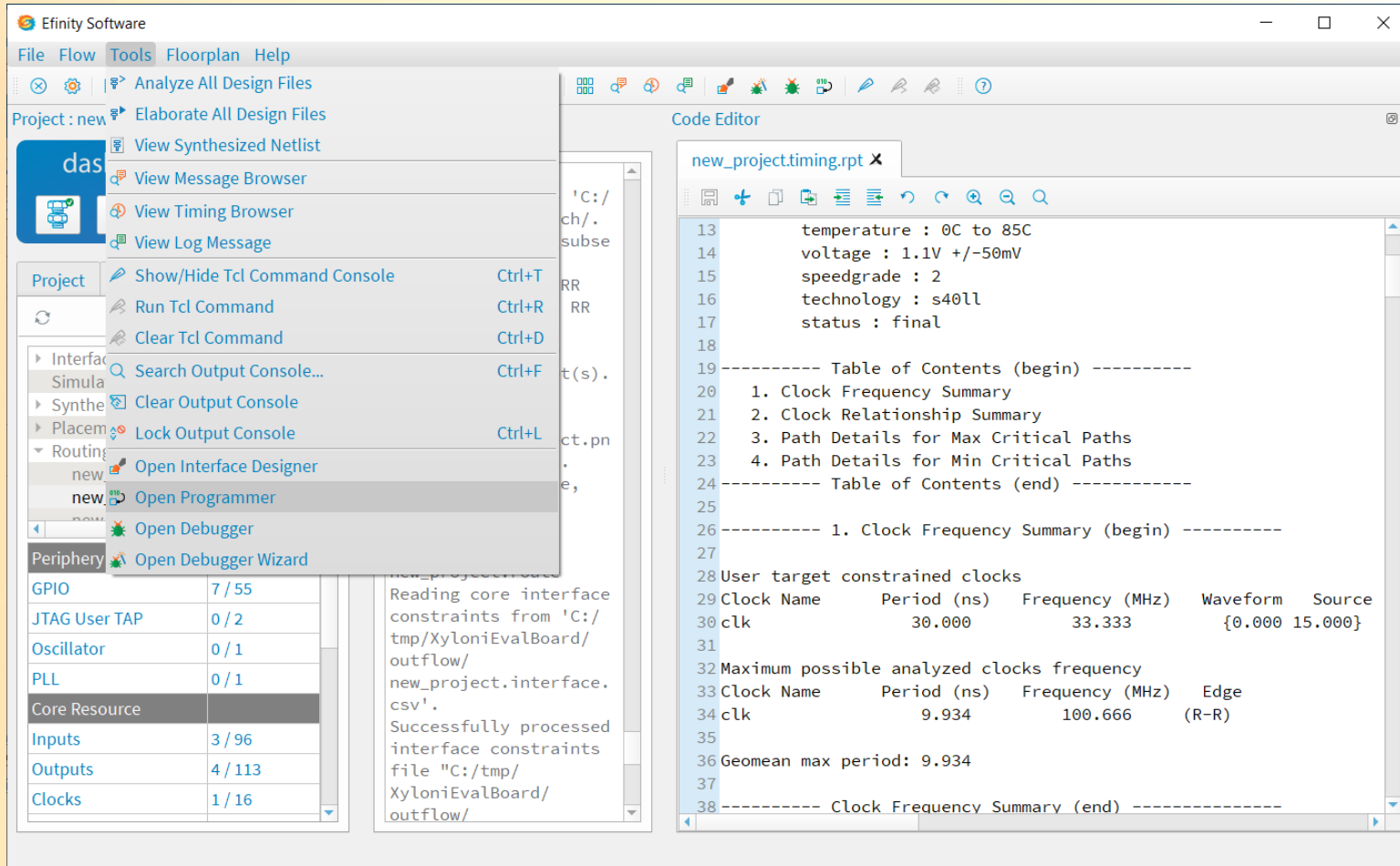
```
Pass 0: Swept away 0 nets with no fanout.
Pass 0: Swept away 0 blocks with no fanout.
Swept away 0 nets and 0 blocks in total.
Removed 0 LUT buffers.
Successfully created VPR logical netlist from Verific binary
DataBase file "C:/tmp/XyloniEvalBoard/new_project.vdb".
Netlist pre-processing took 0.0202929 seconds.
Netlist pre-processing took 0.02 seconds (approximately) in total CPU time.
Netlist pre-processing virtual memory usage: begin = 111.36 MB, end = 111.4 MB, delta = 0.04 MB
Netlist pre-processing peak virtual memory usage = 231.272 MB
Netlist pre-processing
```

Static Timing Analysis Results (from Code Editor):

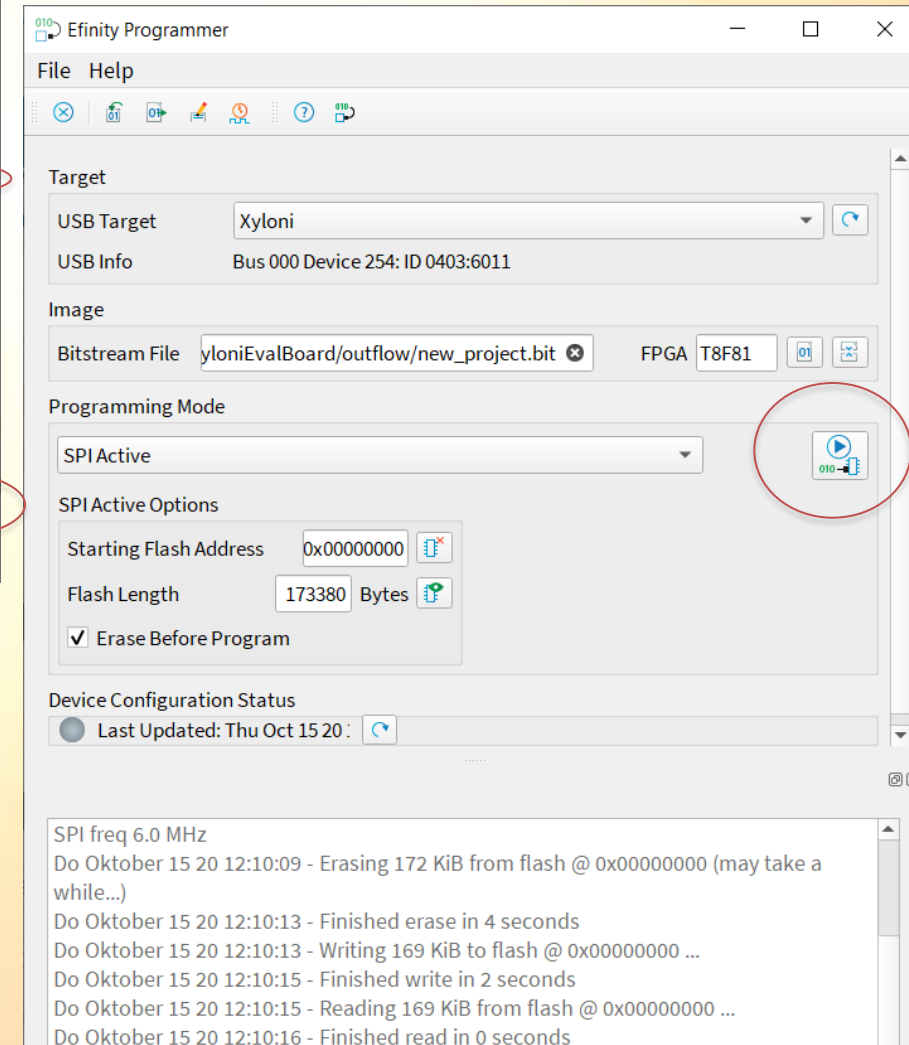
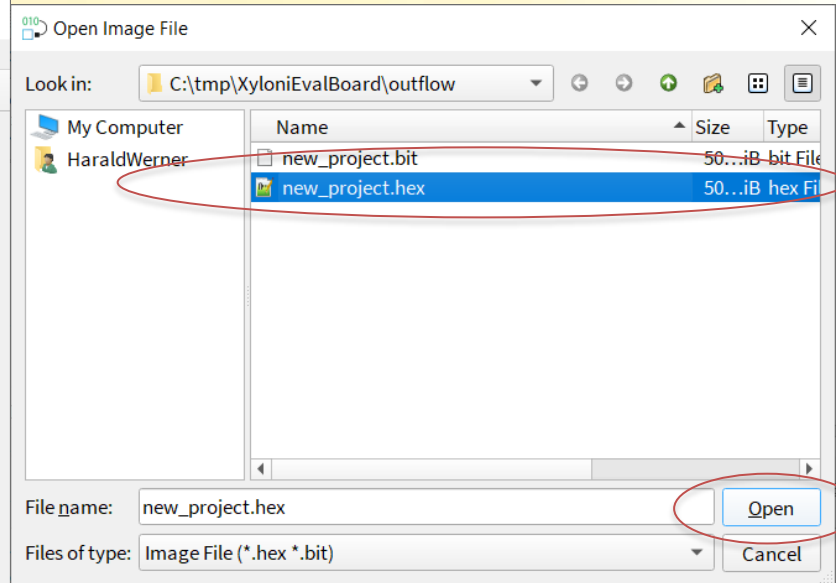
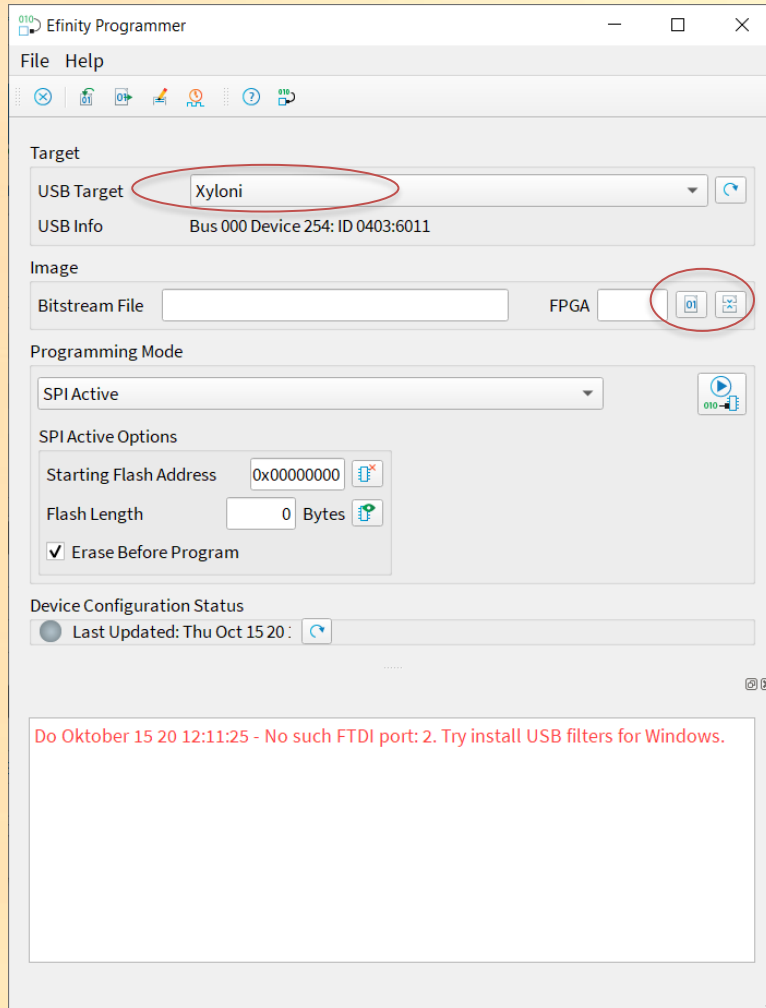
```
13 temperature : 0C to 85C
14 voltage : 1.1V +/-50mV
15 speedgrade : 2
16 technology : s4011
17 status : final
18
19 ----- Table of Contents (begin) -----
20 1. Clock Frequency Summary
21 2. Clock Relationship Summary
22 3. Path Details for Max Critical Paths
23 4. Path Details for Min Critical Paths
24 ----- Table of Contents (end) -----
25
26 ----- 1. Clock Frequency Summary (begin) -----
27
28 User target constrained clocks
29 Clock Name Period (ns) Frequency (MHz) Waveform Source Clock Name
30 clk 100000.000 0.010 {0.000 50000.000} virtu
31
32 Maximum possible analyzed clocks frequency
33 Clock Name Period (ns) Frequency (MHz) Edge
34 clk 8.242 121.327 (R-R)
35
36 Geomean max period: 8.242
37
38 ----- Clock Frequency Summary (end) -----
39
```

Program the Device

Open Programmer
Tools->OpenProgrammer



Select Image File, Start Program (Check USB Target: Xyloni)



Information

- If you need the complete Project, extract the XyloniEvalBoardSolution.zip file. Here you will find the project with the I/O pin assignments.