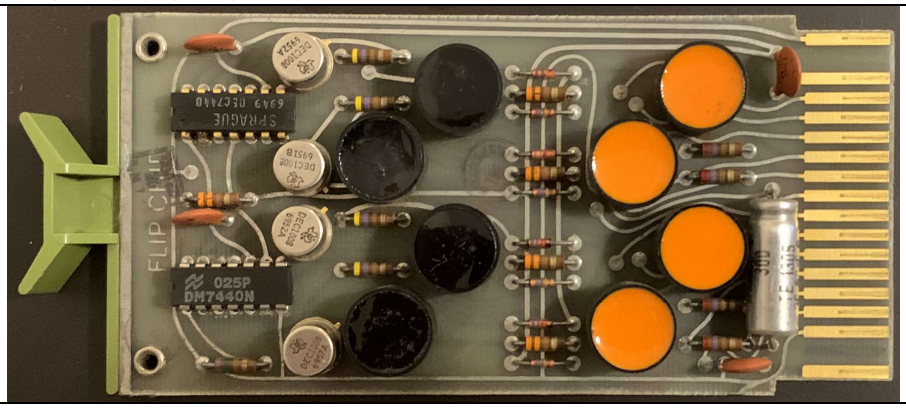
Test Data Sheet, G228, Inhibit Driver

Updated: 18-Sep-2022, test data sheet version v00

Test File	G228Sv2.TST (18-Sep-2022)
Tester Notes	G228 scope test. This test is not automatic. The tester provides a stimulus and measurements are performed using an oscilloscope. The tester will always report that the test passes unless the outputs are shorted.
PCB Rev	C
Board Rev	?
PDP-8/L slots	A23, B23, B24, C25, D25
Photo	

Test Procedure:

1. Setup:
   a. Turn off the UUT power switch on the tester, insert the board into the tester UUT socket.
   b. Load the test file as follows: From the tester main menu enter "1" to read test file, enter the test file name, "G228SV2.TST" and ENTER.
   c. Turn on the UUT power switch on the tester. From the tester main menu enter "4" and then "S" to run the scope loop test mode.
2. Output pulse gating test:
   For the following, set the scope timebase to about 500 µs per division.
   Connect scope CH2 to the tester LED3 testpoint on the tester circuit board which is the start of test pulse.
   Trigger the scope on the rising edge of CH2.
   a. Connect scope CH1 to tester pin AL2, "Output 00 collector".
      Observe a narrow negative pulse on CH1 about 100 µs before the CH2 rising edge. Reference ***Figure 1***.
   b. Connect scope CH1 to tester pin AK1, "Output 01 collector".
      Observe a narrow negative pulse on CH1 about 350 µs after the CH2 rising edge. Reference ***Figure 2***.
   c. Connect scope CH1 to tester pin AU2, "Output 10 collector".
      Observe a narrow negative pulse on CH1 about 800 µs after the CH2 rising edge. Reference ***Figure 3***.
   d. Connect scope CH1 to tester pin AS1, "Output 11 collector".
      Observe a narrow negative pulse on CH1 about 1250 µs after the CH2 rising edge. Reference ***Figure 4***.

CH1 Pin #	CH1 Signal	CH2 signal	Time base	Trig.	CH2↑ to CH1 pulse	Example Figure
AL2	Output 00 collector	LED3 T.P.	500 µs	CH2↑	-100 µs	***Figure 1***
AK1	Output 01 collector	LED3 T.P.	500 µs	CH2↑	+350 µs	***Figure 2***
AU2	Output 10 collector	LED3 T.P.	500 µs	CH2↑	+800 µs	***Figure 3***
AS1	Output 11 collector	LED3 T.P.	500 µs	CH2↑	+1250 µs	***Figure 4***

3. Output pulse shape test:

   For the following, set the scope timebase to about 1 µs per division.
   Trigger the scope on the falling edge of CH1.

   a. Connect scope CH1 to tester pin AL2 “Output 00 collector”.
      Observe a waveform on CH1 like the example is shown in ***Figure 5***.
   b. Connect scope CH1 to tester pin AK1 “Output 01 collector”.
      Observe a waveform on CH1 like the example is shown in ***Figure 5***.
   c. Connect scope CH1 to tester pin AU2 “Output 10 collector”.
      Observe a waveform on CH1 like the example is shown in ***Figure 5***.
   d. Connect scope CH1 to tester pin AS1 “Output 11 collector”.
      Observe a waveform on CH1 like the example is shown in ***Figure 5***.

CH1 Pin #	**CH1 Signal**	**Time base**	**Trig.**	**Example Figure**
AL2	Output 00 collector	1 µs	CH1↓	***Figure 5***
AK1	Output 01 collector	1 µs	CH1↓	***Figure 5***
AU2	Output 10 collector	1 µs	CH1↓	***Figure 5***
AS1	Output 11 collector	1 µs	CH1↓	***Figure 5***

Example Waveforms:

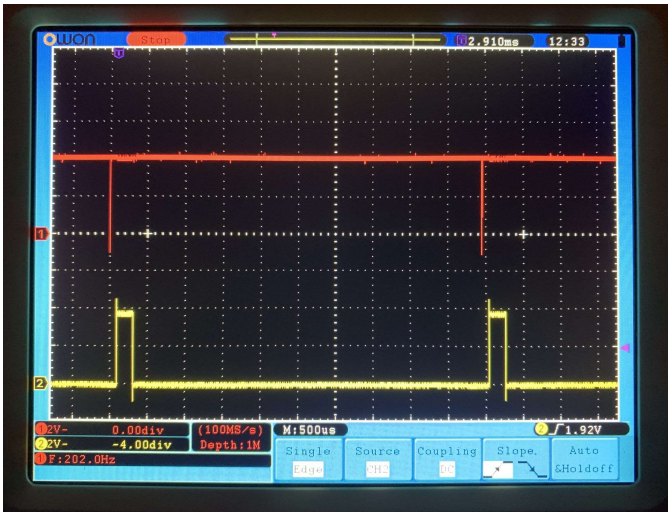


Figure 1, Pin AL2, Output 00 Collector, trigger CH2↑

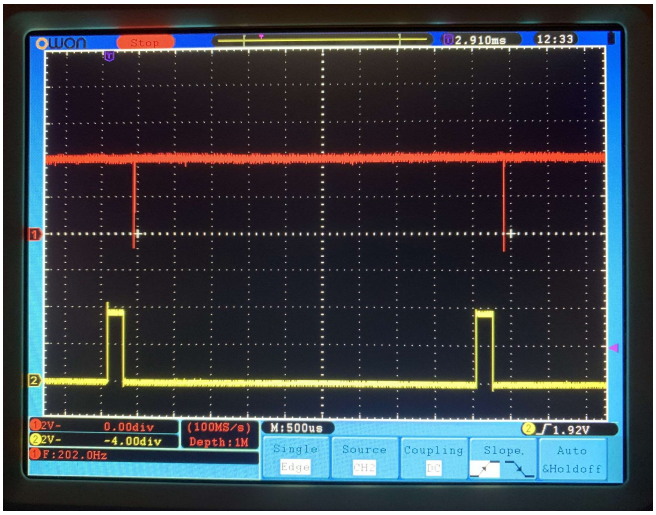


***Figure 2,* Pin AK1, Output 01 Collector, trigger CH2↑**

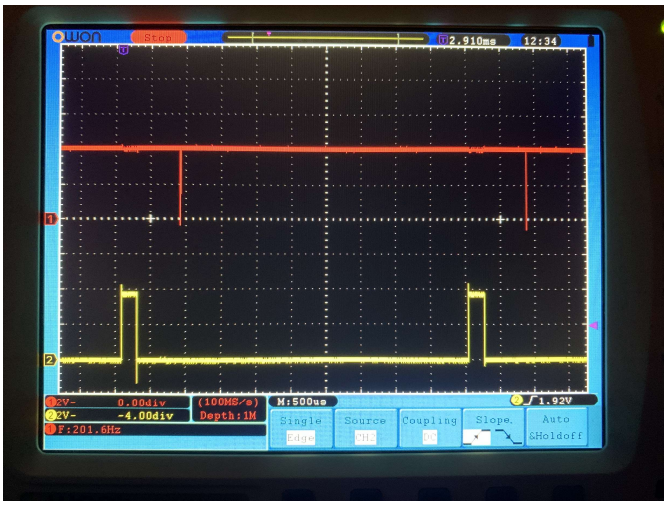


***Figure 3,* Pin AU2, Output 10 Collector, trigger CH2↑**

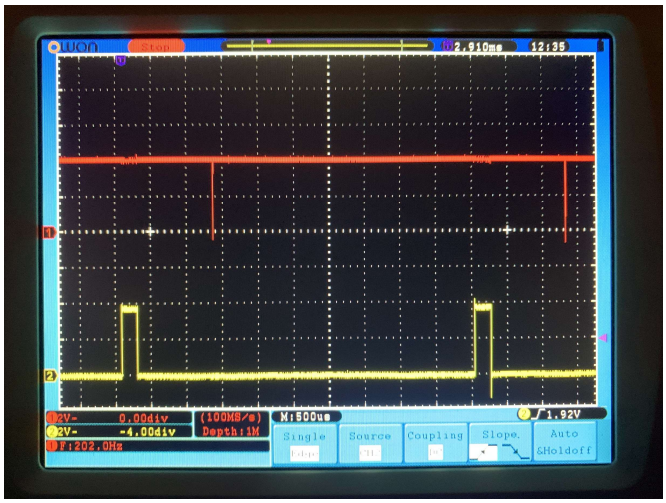


***Figure 4,* Pin AS1, Output 11 Collector, trigger CH2↑**

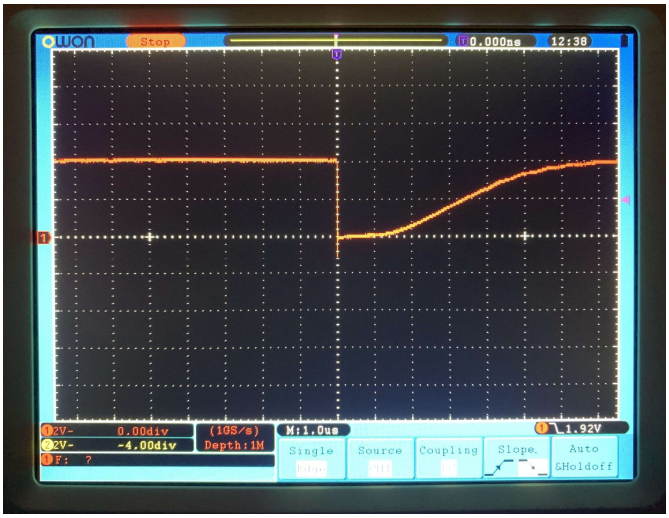


Figure 5,* Pin AL2, Output 00 Collector, *trigger CH1↓

Test File:

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G228 REV H SCHEMATIC    REV C PCB    INHIBIT DRIVER (2 7440)
update: 18-Sep-2022

Manual test, using Oscilloscope to check logic

NOTES   7440 outputs (active low) are not at connector (drive tranformers)
           but can be 'clipped' at the 330 ohm pullup (to +5V) resistors
           that connect thru the transformers to 7440 outputs
         output 00 is at the top (pin A is top)
         output 01 is next
         output 10 is next
         output 11 is at the bottom (pin V is bottom)
         actual outputs are pulses due to transformer coupling. Must scope them.

Note:  "P" for PULLUP OUTPUTS on the open collector outputs;
       Emitters are driven low.
       output pulses low (0.?? v) when active.
       pulse width is ???? when active

TODO:  still need a way to test diodes, output transformers

PINS
 1 I AA1  ENABLE      (NANDed into OUTPUT 00, OUTPUT 01, OUTPUT 10, OUTPUT 11)
 2 I AE2  ENABLE 0/1  (NANDed into OUTPUT 00, OUTPUT 01)
 3 I AN2  ENABLE 2/3  (NANDed into OUTPUT 10, OUTPUT 11)
 4 I AD2  BIT 00      NAND (ENABLE, ENABLE 0/1, BIT 00) is OUTPUT 00
 5 I AD1  BIT 01      NAND (ENABLE, ENABLE 0/1, BIT 01) is OUTPUT 01
 6 I AM2  BIT 10      NAND (ENABLE, ENABLE 2/3, BIT 10) is OUTPUT 10
 7 I AL1  BIT 11      NAND (ENABLE, ENABLE 2/3, BIT 11) is OUTPUT 11
 8 P AL2  OUTPUT 00 COLLECTOR (PULLUP SO CAN SCOPE OUTPUT)
 9 P AK1  OUTPUT 01 COLLECTOR (PULLUP SO CAN SCOPE OUTPUT)
10 P AU2  OUTPUT 10 COLLECTOR (PULLUP SO CAN SCOPE OUTPUT)
11 P AS1  OUTPUT 11 COLLECTOR (PULLUP SO CAN SCOPE OUTPUT)
12 I AF2  OUTPUT 00 EMITTER (ALWAYS GROUNDED)
13 I AE1  OUTPUT 01 EMITTER (ALWAYS GROUNDED)
14 I AP2  OUTPUT 10 EMITTER (ALWAYS GROUNDED)
15 I AM1  OUTPUT 11 EMITTER (ALWAYS GROUNDED)

IIIIIIIPPPPIIII
; turn on OUTPUT 00, then off with no glitch
;EENNNNccccceeee
1111000X1110000
1110000
; turn on OUTPUT 01, then off with no glitch
;EENNNNccccceeee
11101001X11
1110000
; turn on OUTPUT 10, then off with no glitch
;EENNNNccccceeee
111001011X1
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```
1110000
; turn on OUTPUT 11, then off with no glitch
;EENNNNccccceeee
1110001111X
1110000
; turn all off, no simultaneous change to prevent glitch
;EENNNNccccceeee
00000001111
00011111111
0011111
0101111
0111111
0001111
1001111
1001100
1011100
1000000
1100011
1100000
1110000
END
```