# Test Data Sheet, M700, Manual Timing Generator

Updated: 12-Sep-2022

Test Files	M700FL.TST (1-Sep-2022) observe operation of the filter circuit								
	M700R.TST (1-Sep-2022) observe pulse sequence MFTP 0, MFTP 1, MFTP 2 after RESTART/ pulse								
	M700TM.TST (2-Sep-2022) observe timing pulses gated by RESTART/, RUN/ and POWER CLEAR/								
Tester Notes	This test is not automatic. The tester provides a stimulus and measurements are performed using an								
	oscilloscope. The tester will always report that the test passes.								
PCB Rev	D, E								
Board Rev	?								
PDP-8/L slot	C2 & D2								
Photo	(PCB M700E shown)								

#### **Test Procedure:**

#### 1. Setup, filter test:

- a. Turn off the UUT power switch on the tester, insert the board into the tester UUT socket.
- b. Load the test file as follows: From the tester main menu enter "1" to read test file, enter the test file name, "M700FL.TST" and ENTER.
- c. Turn on the UUT power switch on the tester. From the tester main menu enter "4" and then "S" to run the scope loop test mode.

#### 2. Filter test:

For the following, set the scope timebase to about 20 ms per division.

Connect scope CH2 to tester pin AS2 "FILTER INPUT".

Trigger the scope on the falling edge of CH2.

- a. Connect scope CH1 to tester pin AM2 "MFTS 0".

  Observe a waveform on CH1 that falls about 55 ms after the CH2 falling edge. Also, observe that CH1 rises about 40 ms after the CH2 rising edge. An example is shown in *Figure 1*.
- b. Connect scope CH1 to tester pin AN2 "MFTS 0/".

  Observe a waveform on CH1 that rises about 55 ms after the CH2 falling edge. Also, observe that CH1 falls about 40 ms after the CH2 rising edge. This waveform is the inverse of the example shown in *Figure 1*.

CH1 Pin #	CH1 Signal	CH2 Pin#	CH2 signal	Time base	Trig.	CH2↓ to CH1	CH2↑ to CH1	Example Figure
AM2	MFTS 0	AS2	FILTER INPUT	20 ms	CH2↓	55 ms	40 ms	Figure 1
AN2	MFTS 0/	AS2	FILTER INPUT	20 ms	CH2↓	55 ms	40 ms	-

#### 3. Setup, pulse sequence test:

- a. Turn off the UUT power switch on the tester, insert the board into the tester UUT socket.
- b. Load the test file as follows: From the tester main menu enter "1" to read test file, enter the test file name, "M700R.TST" and ENTER.
- c. Turn on the UUT power switch on the tester. From the tester main menu enter "4" and then "S" to run the scope loop test mode.

#### 4. Pulse sequence test:

For the following, set the scope timebase to about 500 ns per division.

Connect scope CH2 to tester pin AR2, "RESTART".

Trigger the scope on the falling edge of CH2.

- a. Connect scope CH1 to tester pin AT2 "MFTP 0".
  - Observe a waveform on CH1 that rises about 50 ns after the CH2 falling edge and falls about 1.1  $\mu$ s after the CH2 falling edge. An example is shown in *Figure 2*.
- b. Connect scope CH1 to tester pin AE2 "MFTP 1".
  - Observe a waveform on CH1 that rises about 2.25  $\mu$ s after the CH2 falling edge and falls about 2.4  $\mu$ s after the CH2 falling edge. An example is shown in *Figure 3*.
- c. Connect scope CH1 to tester pin BD2 "MFTP 2".
  - Observe a waveform on CH1 that rises about 4.3  $\mu$ s after the CH2 falling edge and falls about 4.4  $\mu$ s after the CH2 falling edge. An example is shown in *Figure 4*.
- d. Connect scope CH1 to tester pin AJ2 "MFTS 1".
  - Observe a waveform on CH1 that rises about 50 ns after the CH2 falling edge and falls about 2.3  $\mu$ s after the CH2 falling edge. An example is shown in *Figure 5*.
- e. Connect scope CH1 to tester pin AK2 "MFTS 1/".
  - Observe a waveform on CH1 that falls about 50 ns after the CH2 falling edge and rises about 2.3  $\mu$ s after the CH2 falling edge. This waveform is the inverse of the example shown in *Figure 5*.
- f. Connect scope CH1 to tester pin AF2 "MFTS 2".
  - Observe a waveform on CH1 that rises about 2.3  $\mu$ s after the CH2 falling edge and falls about 4.4  $\mu$ s after the CH2 falling edge. An example is shown in *Figure 6*.
- g. Connect scope CH1 to tester pin AH2 "MFTS 2/".
  - Observe a waveform on CH1 that falls about 2.3  $\mu$ s after the CH2 falling edge and rises about 4.4  $\mu$ s after the CH2 falling edge. This waveform is the inverse of the example shown in *Figure 6*.

CH1	CH1	CH2	CH2	Time	Trigger	CH1 rises	CH1 falls	Example
Pin #	Signal	Pin #	signal	base		after CH2↓	after CH2↓	Figure
AT2	MFTP 0	AR2	RESTART	500 ns	CH2↓	50 ns	1.1 μs	Figure 2
AE2	MFTP 1	AR2	RESTART	500 ns	CH2↓	2.25 μs	2.4 μs	Figure 3
BD2	MFTP 2	AR2	RESTART	500 ns	CH2↓	4.3 μs	4.4 μs	Figure
								<b>4</b> Figure 2
AJ2	MFTS 1	AR2	RESTART	500 ns	CH2↓	50 ns	2.3 μs	Figure 5
AK2	MFTS 1/	AR2	RESTART	500 ns	CH2↓	2.3 μs	50 ns	-
AF2	MFTS 2	AR2	RESTART	500 ns	CH2↓	2.3 μs	4.3 μs	Figure 6
AH2	MFTS 2/	AR2	RESTART	500 ns	CH2↓	4.3 μs	2.3 μs	-

#### 5. Setup, timing pulse gating test:

- a. Turn off the UUT power switch on the tester, insert the board into the tester UUT socket.
- b. Load the test file as follows: From the tester main menu enter "1" to read test file, enter the test file name, "M700TM.TST" and ENTER.
- c. Turn on the UUT power switch on the tester. From the tester main menu enter "4" and then "S" to run the scope loop test mode.

#### 6. Timing pulse gating test:

For the following, set the scope timebase to about 200 µs per division.

Connect scope CH2 to tester pin AR2, "RESTART", and connect the scope external trigger to the tester start-of-test signal, "LED3", testpoint.

Trigger the scope on the rising edge of external trigger signal. Observe three negative pulses on CH2 that are between the rising edges of the external trigger. This interval is one cycle of the scope loop test. The falling edge of the first negative pulse on CH2 occurs while the start-of-test trigger, "LED3" testpoint, is high. It might be convenient to temporarily probe the trigger signal with CH1 to confirm this.

- a. Connect scope CH1 to tester pin AJ2 "MFTS 1".
   Observe a very narrow positive pulse on CH1 that is aligned with the falling edge of the first negative pulse on CH2. An example is shown in *Figure 7*.
- b. Connect scope CH1 to tester pin AK2 "MFTS 1/".
   Observe a very narrow negative pulse on CH1 that is aligned with the falling edge of the first negative pulse on CH2. The waveform on CH1 is the inverse of the example shown in *Figure 7*.
- c. Connect scope CH1 to tester pin AF2 "MFTS 2".

  Observe a very narrow positive pulse on CH1 that is aligned with the falling edge of the first negative pulse on CH2. The waveform will look like the example shown in *Figure 7*.
- d. Connect scope CH1 to tester pin AH2 "MFTS 2/".

  Observe a very narrow negative pulse on CH1 that is aligned with the falling edge of the first negative pulse on CH2. The waveform on CH1 is the inverse of the example shown in *Figure 7*.

CH1	CH1	CH2	CH2	Time	Trigger	Trigger signal	Example
Pin #	Signal	Pin#	signal	base			Figure
AJ2	MFTS 1	AR2	RESTART	200 μs	EXT↑	Flip Chip Tester start-of-test	Figure 7
AK2	MFTS 1/	AR2	RESTART	200 μs	EXT↑	Flip Chip Tester start-of-test	-
AF2	MFTS 2	AR2	RESTART	200 μs	EXT↑	Flip Chip Tester start-of-test	Figure
							<b>7</b> Figure 2
AH2	MFTS 2/	AR2	RESTART	200 μs	EXT个	Flip Chip Tester start-of-test	-

## **Example Waveforms:**

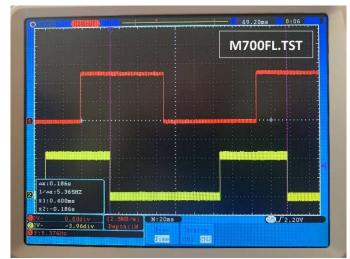


Figure 1, Pins AM2 "MFTS 0" (CH1), AS2 "FILTER INPUT" (CH2), trigger CH2↓

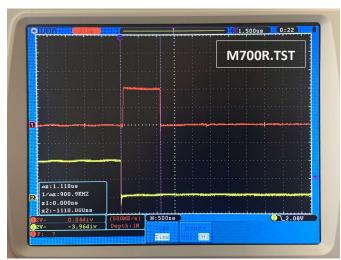


Figure 2, Pins AT2 "MFTP 0" (CH1), AR2 "RESTART" (CH2), trigger CH2↓

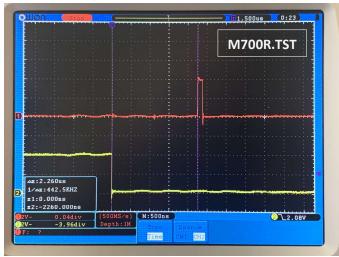


Figure 3, Pins AE2 "MFTP 1" (CH1), AR2 "RESTART" (CH2), trigger CH2↓

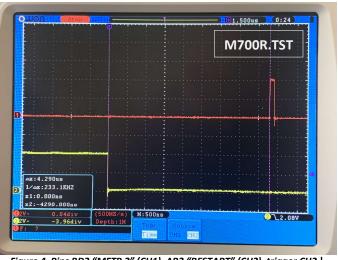


Figure 4, Pins BD2 "MFTP 2" (CH1), AR2 "RESTART" (CH2), trigger CH2↓

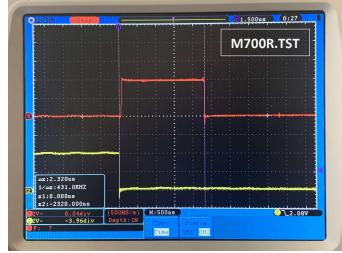


Figure 5, Pins AJ2 "MFTS 1" (CH1), AR2 "RESTART" (CH2), trigger CH2↓

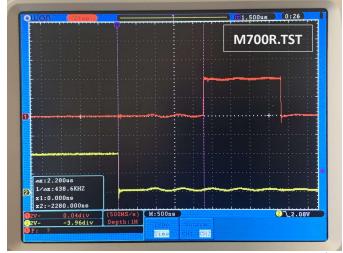


Figure 6, Pins AF2 "MFTS 2" (CH1), AR2 "RESTART" (CH2), trigger CH2↓

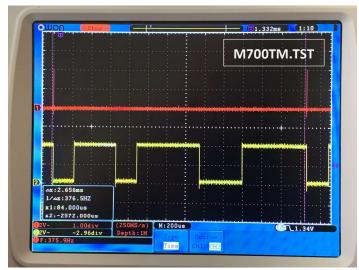


Figure 7, Pins AJ2 "MFTS 1" (CH1), AR2 "RESTART" (CH2), trigger CH2↓

### **Test Files:**

#### M700R.TST

END

```
M700 REV E PCB REV E MANUAL TIMING GENERATOR
updated: 1-Sep-2022
TEST TO OBSERVE MFTP 0, MFTP 1, MFTP 2 sequence
Use Oscilloscope to see pulses.
PINS
1 I AR2
         RESTART-N
2 I AP2 RUN-N
3 I AL2 POWER CLEAR-N
4 I AS2 FILTER INPUT
IIII
1110
; initial state, FILTER INPUT is always low for this test
; assert RESTART-N low, and leave RUN-N and POWER CLEAR-N inactive high
; set the RESTART-N inactive High
1
END
M700TM.TST
M700 REV E PCB REV E
                       MANUAL TIMING GENERATOR
updated: 2-Sep-2022
Test to observe timing pulses affected by RESTART-N, RUN-N and POWER CLEAR-N
Time of test is too large to observe delay between MFTP pulses.
Use Oscilloscope to observe pulses.
PINS
1 I AR2 RESTART-N
2 I AP2 RUN-N
3 I AL2 POWER CLEAR-N
4 I AS2 FILTER INPUT
IIII
1110
; initial state, FILTER INPUT is always low for this test
; assert RESTART-N low, and leave RUN-N and POWER CLEAR-N inactive high
0
; set the RESTART-N inactive High
; second pulse group, assert RUN-N, then assert RESTART-N \,
10
00
10
; set the RESTART-N and RUN-N inactive High
11
;third group, assert POWER CLEAR-N active low first, then pulse RESTART-N low, keep RUN-N inactive
110
010
; set the POWER CLEAR-N inactive High first, then RESTART-N inactive High
1110
```