HIGHLAND TECHNOLOGY

# T564 DIGITAL DELAY GENERATOR


## Technical Manual

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# Contents

# 1. Introduction

The T564 is a small, enclosed digital delay/pulse generator which is intended for use in embedded OEM applications. Given an internal or external trigger, it outputs four precisely-timed pulses. The T564-1 is the standard, packaged version, usable directly in many OEM applications and as the evaluation unit for custom versions.

Features of the T564-1 include:

- Four TTL-level pulse outputs, each programmable for delay and width up to 10 seconds each, with 10 picosecond resolution.
- DSP phaselock system combines crystal-clock delay accuracy with low jitter from asynchronous external trigger.
- Internal 10 MHz crystal oscillator timebase with external lock capability.
- 0-16 MHz DDS synthesizer for internal trigger rates.
- Programmable-level trigger input with divide/burst features and trigger GATE input.
- Advanced QUEUE, TRAIN, and FRAMES functions.
- Extruded enclosure with removable mounting flange.
- RS-232 serial interface.

The T564-2 version includes all the above features and adds 10/100-mbps Ethernet.

Customizable features include:

- Alternate timing algorithms
- Number of timing channels, 1 to 8
- Packaged or bare-board
- Alternate connector types and locations
- TCXO or OCXO timebases.
- Low impedance outputs, 4 volts min into 50 ohms.
- Extended temperature ranges and conformal coating

Highland can also provide benchtop pulse/delay generators or OEM timing packages that include picosecond-resolution time-interval measurement, ultrafast or high-voltage outputs, optical interfaces, and precision analog measurement.

Since creating new versions of the T564 involves hardware or firmware changes, customization is normally done under a contractual OEM agreement with associated purchase commitments. Custom versions will be identified by a "dash" number, starting with T564-10.

# 2. Specifications: T564 Delay/Pulse Generator

| | |
|---|---|
| FUNCTION | 4-channel digital delay and pulse generator |
| GATE FUNCTION | Programmable as level sensitive enable input, edge triggered burst enable input, or divisor enabled output |
| GATE INPUT | Programmable termination, 50 Ω or 500 Ω to +2.5 V<br>Logic low -0.3 V min, +0.7 V max<br>Logic high +2 V min, +5 V max |
| GATE OUTPUT | Logic low +0.1 V typical, +0.4 V max @ 50 mA<br>Logic high +5 V typical, +4 V min @ 50 mA |
| TRIGGER SOURCES | Internal DDS: 0 to 16 MHz, 0.02 Hz resolution<br>Internal clock: 80 MHz<br>Remote command<br>External signal |
| TRIGGER DIVISOR | 1 to $2^{32}$-1, 125 MHz max input |
| EXTERNAL TRIGGER INPUT | Programmable termination, 50 Ω or 10 kΩ to ground<br>Programmable trigger level (+0.25 to +3.3 volts) and slope |
| CHANNEL OUTPUTS A, B, C, D | Four pulse outputs, 5 V, 50 Ω source impedance, each programmable for delay, width, polarity |
| DELAY RANGE | 0 to 10 seconds, 10 ps resolution |
| WIDTH RANGE | 2 ns to 10 seconds, 10 ps resolution |
| INSERTION DELAY | 21 ns ±400 ps, external trigger to any output |
| DIFFERENTIAL NONLINEARITY | < 200 ps |
| JITTER | < 35 ps typical (50 ps max) RMS, external trigger to any output or between any outputs<br>Add clock jitter for delays > 500 µs |
| TRIGGER RATE | 0 to 16 MHz, limited to 1/(delay+width+60 ns) max |
| RISETIME | 750 ps max |
| FALLTIME | 750 ps max |
| CLOCK | Internal 10 MHz VCXO, 1 ppm initial accuracy, < 2 ppm/year drift<br>Added jitter below 10 ns per second of delay<br>TC below 0.2 PPM/°C<br>Connector provides clock in/out<br>Locks to external source<br>Clock jitter and delay errors are zero relative to external source<br>Optional higher-performance TCXO or OCXO |
| TIMING ACCURACY | ± 400 ps ± 7.5 ps/°C ± clock accuracy |

| | |
|---|---|
| BURST | Programmable to fire N times out of each M triggers<br>where N and M are 1 to $2^{32}$-1 |
| OPERATING TEMPERATURE | 0 to 50°C, non-condensing |
| STORAGE TEMPERATURE | -20 to 80°C |
| CALIBRATION INTERVAL | One year |
| POWER | +12 ±0.25 volts, 0.3 amps max; 0.4 amps max with Ethernet<br>Universal AC adapter supplied with evaluation package |
| COMMUNICATIONS | RS-232 standard, 38.4 kbaud<br>Optional 10/100 Ethernet |
| CONNECTORS | 7 SMB for trigger, gate, clock, outputs<br>2.5mm stereo jack for RS-232<br>0.25″ power connector<br>Optional RJ45 for Ethernet |
| INDICATORS | LEDs indicate shot, communications |
| PACKAGING | 4.75" (L) x 4.0" (W) x 1.25" (H) extruded aluminum enclosure |
| CONFORMANCE | OEM product has no UL/FCC/CE compliance requirements<br>Designed to meet UL/FCC/CE requirements |

# 3. Overview of the T564

The T564-1 is an embedded digital delay/pulse generator. It accepts a trigger pulse and generates up to four output pulses, with each pulse being individually programmable in delay and width. Triggers may be external, internal, or evoked through the communications interface. Timing has crystal-clock precision with picosecond jitter relative to an external trigger.

Each output is user programmable for delay (0-10 seconds) and width (0-10 seconds) with 10 ps resolution. When externally triggered, all delays are relative to the basic 20 ns insertion delay.

The T564 is fully backward compatible with the standard T560 DDG, but adds features...

- TRAIN facility generates multiple outputs from a single trigger.
- FRAME facility stores up to 8192 delay/width scenarios, with rapid reload.
- QUEUE installs new delay/width settings without disturbing ongoing cycles.
- Optional E and F outputs.
- Optional fast TTL-level isochronous serial communications.

## *3.1 Standard Packaging*

The standard T564-1 unit is packaged in a small extruded aluminum enclosure. The Ethernet connector is provided on the T564-2 version. Section 12 of this manual provides detailed dimensions.

## *3.2 Overall Block Diagram*

Figure 3.2 is the block diagram of the T564. OEM versions may include various features of the module. The optional Ethernet interface is not furnished on the standard T564-1 version.

The T564 digital delay generator creates delays by digitally counting a basic clock to create coarse delays to a resolution of 20 nanoseconds, and then adding a fine analog delay to interpolate the final times to picosecond resolution. The timing clock is derived from a 50 MHz gated oscillator which is started when an internal or external trigger is received. A DSP-based phaselock system digitizes and compares the waveforms generated by this oscillator to that of a precision 10 MHz crystal oscillator and servoes the gated oscillator to be as accurate as the crystal while still maintaining the timing relationship to the original trigger.

The T564-1 supplies four TTL pulse outputs, each programmable in delay and width. Custom versions of the T564 can provide up to eight independent delay outputs.

Because the all-digital phaselock system uses no analog signal storage elements, long-delay accuracy and jitter depend only in the quality of the internal or external 10 MHz timebase.

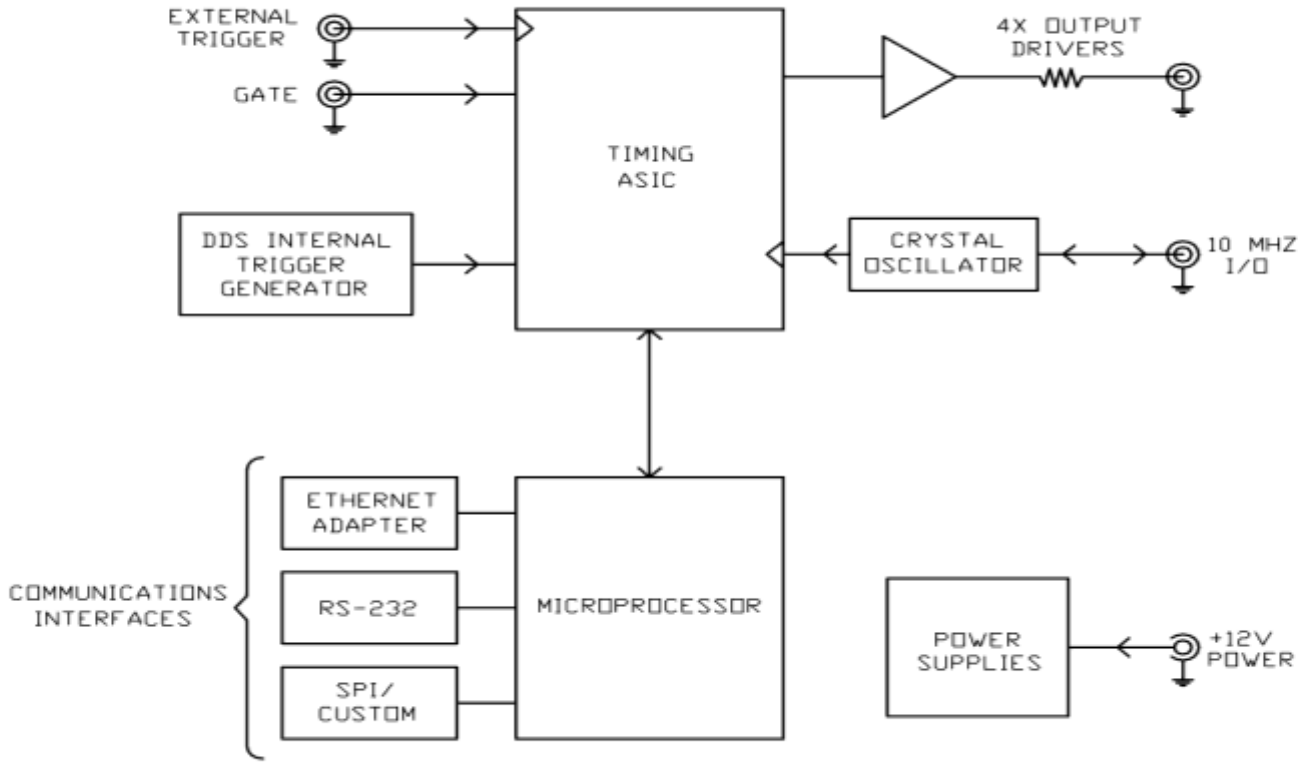



**Fig 3.2 T564 Basic Block Diagram**

## *3.3 Crystal Oscillator Timebase*

The standard T564 includes a 10 MHz VCXO crystal oscillator timebase. It is factory-set to an accuracy of ±1 PPM and may be expected to drift less than 2 PPM per year. A trim DAC is provided to allow user commands to readjust the oscillator frequency as desired, with the setting stored in nonvolatile memory.

A connector is provided which allows the internal oscillator to provide a 10-MHz output, or allows an external 10-MHz source to be accepted. This allows multiple T564s to be synchronized to each other or to an external 10-MHz reference. The external clock levels are 3.3 volt square-wave CMOS logic levels. The T564 can lock to an externally-applied

square wave of 10 MHz +-50 PPM, 3.3 to 5 volt positive logic levels, or to a 1 volt RMS sine wave.

The long-delay (millisecond range) jitter performance of the T564 is dominated by the phase noise of the internal crystal oscillator or the equivalent phase noise of a user-provided external reference.

Custom versions may include higher-precision TCXO or OCXO timebases. Multiple T564 units may be locked to one another to ensure timing coherence.

## *3.4 Trigger Inputs*

Figure 3.4 is a simplified diagram of the T564 trigger and sequence logic. Any one of five available trigger sources may be selected to fire the system: External+, External-, an internal 80-MHz clock, the internal 0-16 MHz DDS synthesizer, and the user software trigger. The selected trigger is divided by a programmable factor K from 1 to 2^32-1 and supplied to the cycle-start HIT flipflop. The hit flopflop is enabled by the gating/burst logic. Once the flipflop is fired, eight identical timing blocks generate delays A1 through D2, each programmable from 0 to 20 seconds in 10-ps steps. Pairs of delays are combined to result in four outputs, each a pulse whose delay and width are programmable with respect to the common trigger. When all delay blocks have timed out, the EOD (end-of-delay) logic resets the hit flipflop for about 50 ns, after which the system is enabled to accept another trigger.

The standard external trigger is a positive level, with trigger threshold programmable from +0.25 to +3.3 volts and selectable rising/falling edge. The trigger input may be programmed to be high impedance or a 50-ohm termination to ground. Maximum safe input levels are -0.3 to +5.0 volts.

The maximum allowed trigger rate is

$$R = 1 / (D + W + 60\ ns)$$

where D + W is the greatest channel sum of programmed delay plus width, and R is limited to 16 MHz max. If a channel is programmed OFF, its time settings are not relevant. If the T564 receives an internal or external trigger while a timing cycle is still busy, that trigger will be ignored. Some additional timing restrictions apply in QUEUE, TRAIN, and FRAME modes.

An internal 80 MHz clock (exactly 8x the main 10 MHz clock) may also be selected as the trigger source. When it is used, a trigger divisor K must be programmed to keep the trigger rate at or below 16 MHz.

The internal DDS synthesizer allows internal triggering at rates from 0 to 16 MHz with 0.02-Hz resolution. The DDS synthesizer has a period jitter of about 1 part in 20,000, which can be substantial in absolute terms at lower requested frequencies. Both period jitter and resolution can be improved by keeping the DDS frequency in the 2-10 MHz range and

using the internal trigger divisor facility to get lower trigger rates. The DDS trigger is not included on the V564-10.

External triggers up to 125 MHz can be accepted, given that a programmed divisor or the inherent busy-cycle limitation will restrict the actual trigger rate to some countdown fraction of the input frequency below 16 MHz.

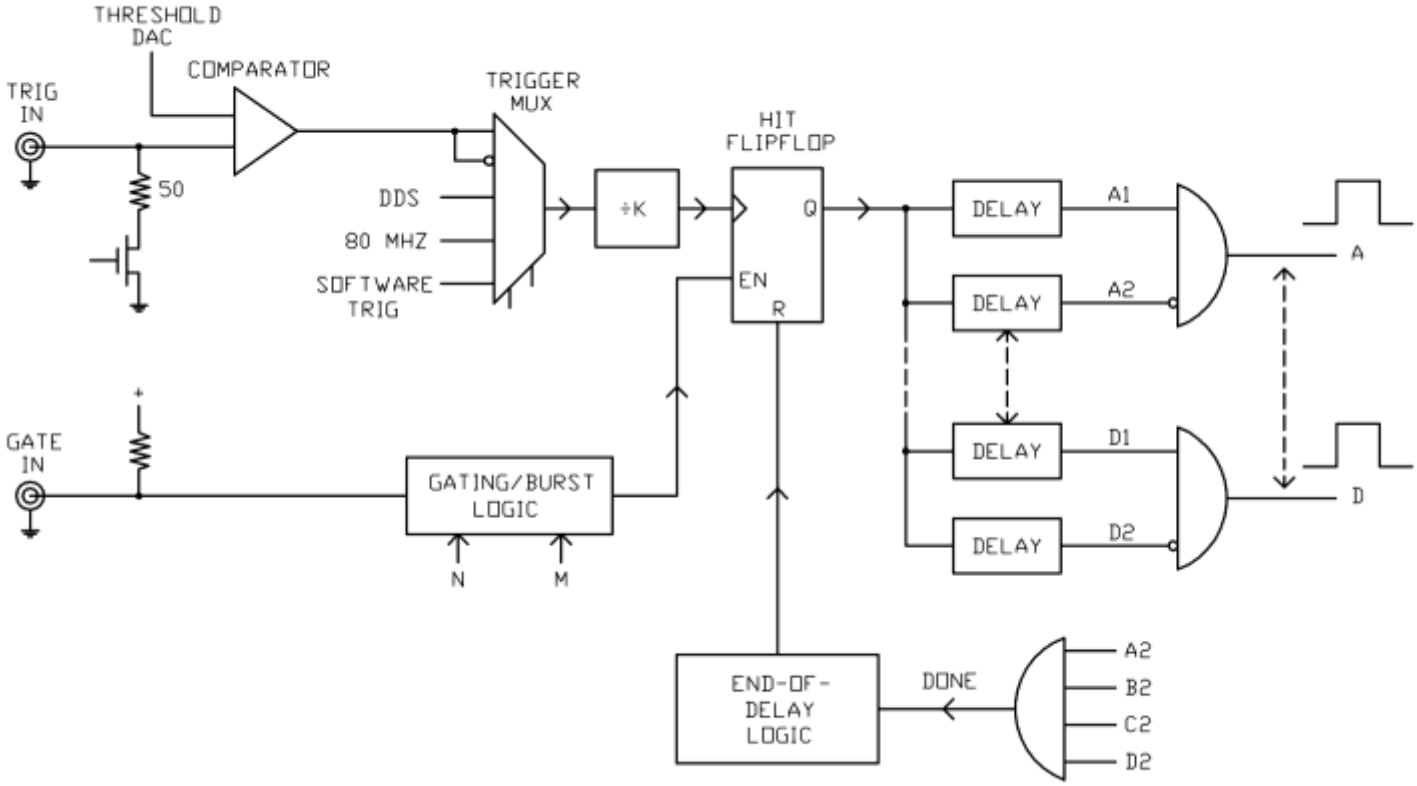



**Fig 3.4 Trigger and Sequencing Logic**

## *3.5 Burst Logic*

The burst logic allows the user to define two integers N and M, each in the range of 1 to 2^32-1. The T564, when triggered, will respond to a burst of N triggers every M triggers. For example, if N = 2 and M = 5, trigger response will be Fire, Fire, Skip, Skip, Skip, repeated indefinitely. N/M is thus the trigger duty cycle.

If either N or M is programmed to be 0, the burst logic is disabled.

Burst cycles may "free run", continuously generating N of every M possible cycles. The internal burst logic may be reset by a user command, so that the next trigger will start a new burst of N outputs.

A single burst of N cycles may be started under control of the GATE input or on software command. If GATE mode is set to BURST ( command **GAte BUrst**), the next active edge of the GATE input will enable a single burst of N cycles. Similarly, the **GAte REmote** mode enables a user-fired burst, started by the **GAte FIre** serial command. In both cases, M must be set greater than or equal to N. If M is greater than N, additional burst starts will be locked out until a full M triggers have been received.

## *3.6 Pulse Outputs*

Four pulse outputs are provided, called channels A, B, C, and D. Outputs are +5 volt CMOS levels with a 50-ohm source impedance. They can drive 5 volts into a non-terminating load, or 2.5 volts into a 50-ohm load. Because they are source terminated, they may drive a 50-ohm coaxial cable any distance into any termination impedance without significant reflection problems. For example, a 100 ohm termination will provide a clean 0 to +3.3 volt logic swing, and a high-impedance (such as CMOS) load will swing 5 volts. External passive components can be used to convert to ECL or PECL levels.

Each output is programmable for pulse delay and width relative to the trigger. If an output is programmed for delay D, the actual output pulse will occur at D + 20 ns after the external trigger, where 20 ns is the basic insertion delay of the T564. Pulse outputs are normally active-high, but may be programmed to operate active-low.

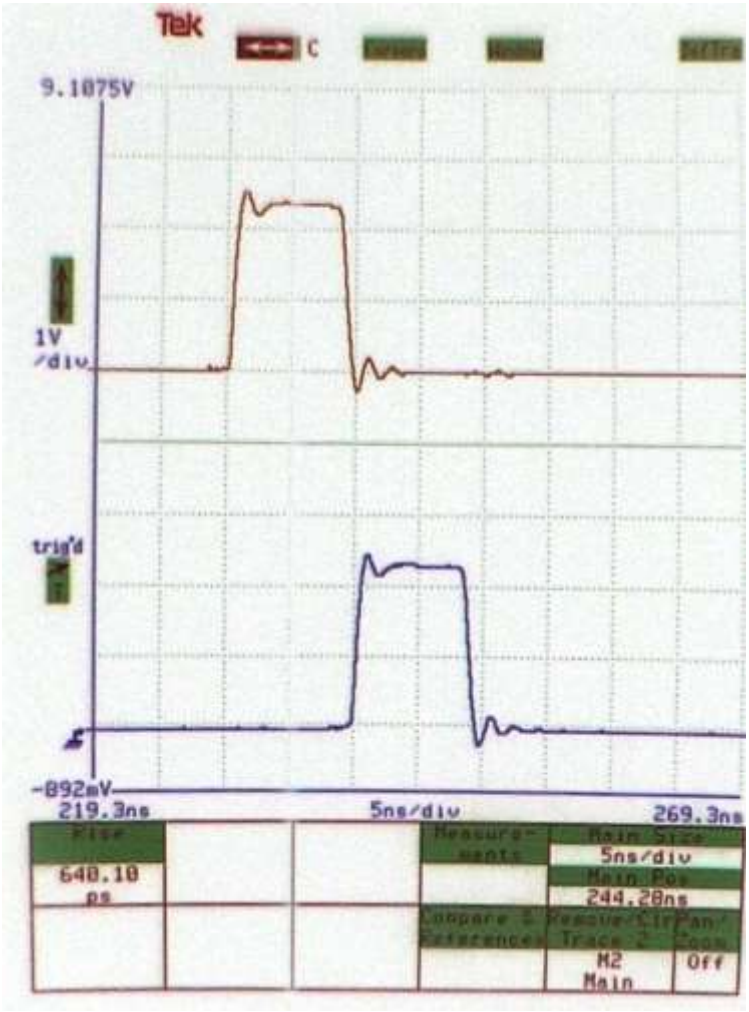



Fig 3.6

Typical T564 channel outputs into 50 ohms. Risetime is 640 ps.

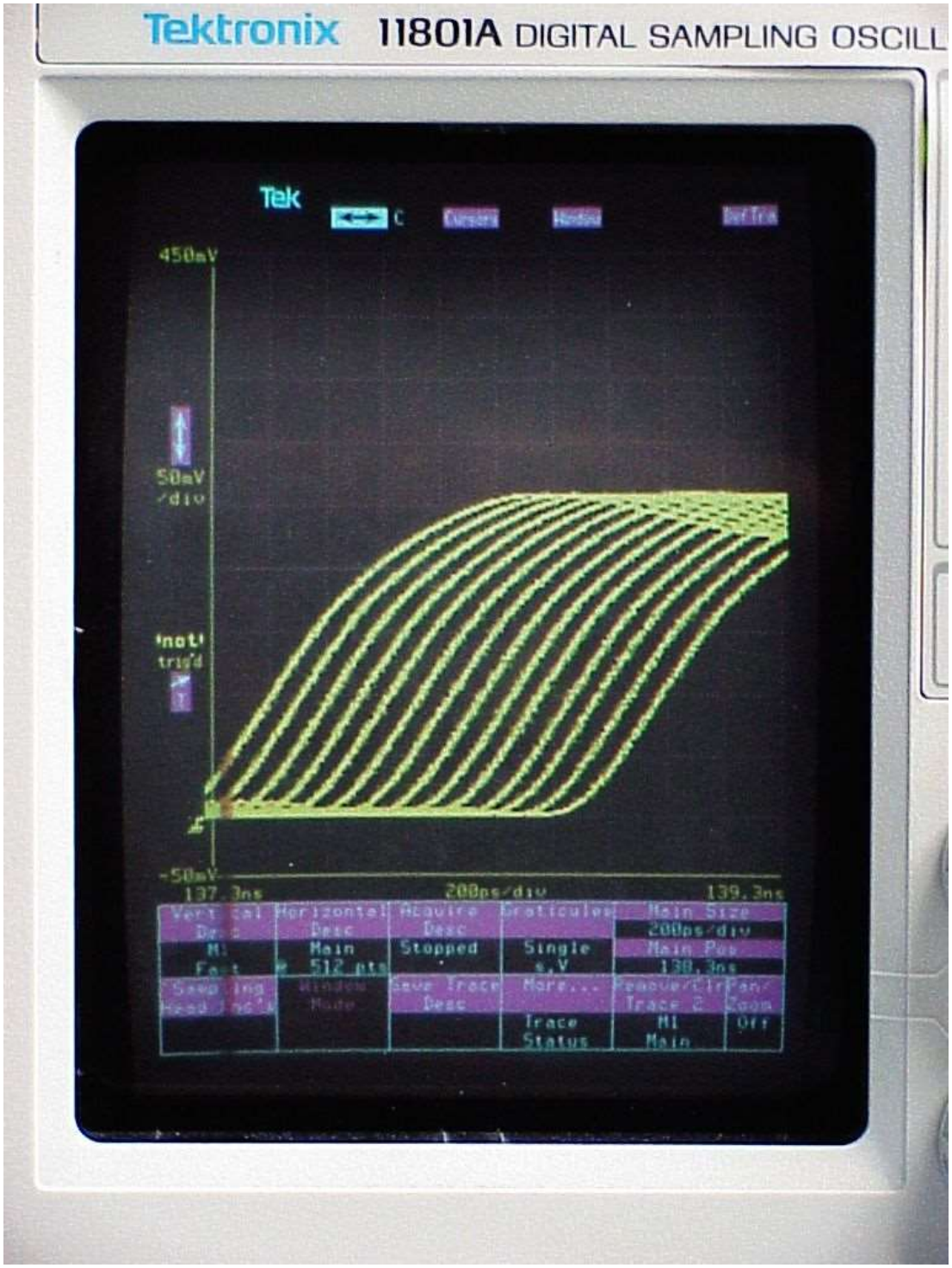



Fig 3.7 Output rising edge, 100 ps delay steps

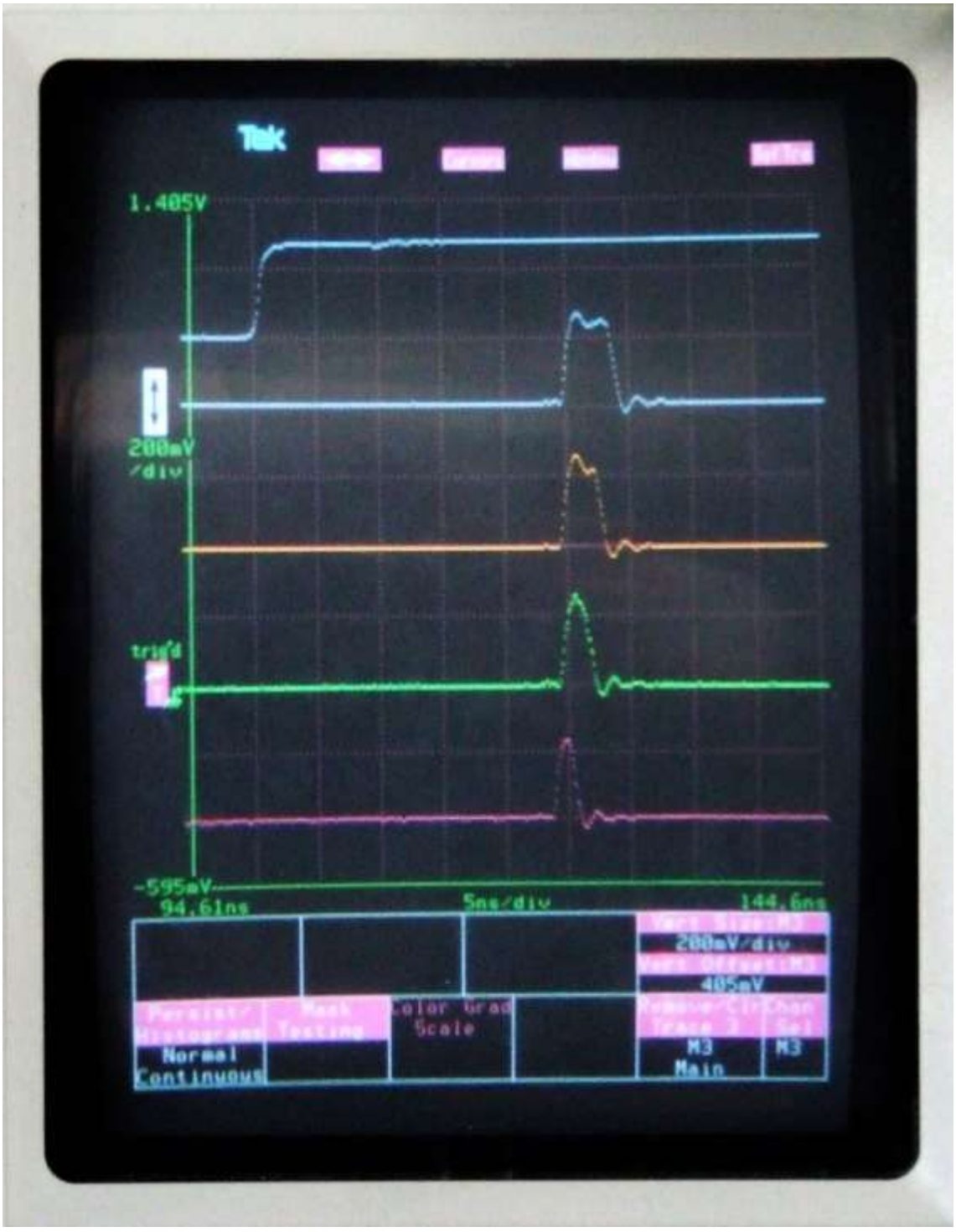



Fig 3.8 Trigger and output pulses, widths 4ns, 3 ns, 2 ns, and 1.5 ns

## 3.7 Gate I/O

A GATE coaxial connector is provided; it is pulled up to +5 volts through a 1K resistor or may, under software control, be terminated at 50 ohms to ground. GATE may be programmed as an input or as an output. As an input, it may be programmed to enable triggers, with high or low being the active level. As an output, it will go true (selectable high or low) to indicate that the HIT flipflop is armed and ready to accept triggers. The gate logic may also be used to enable a single burst of N pulses, with the burst being evoked by a rising edge at the GATE connector input or by remote command.

## 3.8 Communications and Control

The standard T564-1 is equipped with a 38.4-kbaud RS-232 interface. The T564-2 version adds a 10/100 Ethernet interface. If the Ethernet option is installed, both the Ethernet and RS-232 ports will be functional, but commands should not be sent to the T564 through both ports simultaneously.

## 3.9 Connectors

Standard logic-level connectors are right-angle SMBs.

Other connector types are available on OEM versions. Connectors may be straight or right-angle, SMB, MCX, or LEMO, mounted topside or bottom. Hirose H.FL or U.FL surface-mount connectors can also be provided on either side of the circuit board. Because of the close spacing of the connectors, SMA types are not recommended.

A three-foot SMB-to-BNC cable is available as Highland part number J53.

A miniature 2.5-mm stereo phone jack is used for the RS-232 serial interface; a mating connector and cable is available, terminated with a female D9 connector, and may be plugged into the serial port of a standard PC. The cable assembly is Highland Part Number T565.

Pinout of the serial connector is:

| | | |
|---|---|---|
| Tip | RXD serial data to T564 | to PC D9-3 |
| Ring | TXD serial data from T564 | to PC D9-2 |
| Ground | | to PC D9-5 |

The T564 is optionally available with a female D9 connector which provides both RS-232 and power connections, as might be suitable for high-vibration industrial or aerospace applications. OEM versions can be furnished with the J8 (alternate power input) and J14 (auxiliary i/o) connectors.

## 3.10 Power Input

The T564 requires +12 volts DC at 0.3 amps max, 0.4 amps for the Ethernet version. A wall-plug universal power supply is furnished with the evaluation kit, or users may supply +11.75 to +12.25 VDC power. The evaluation power supply with US plug is Highland part number J12. The international AC plug adapter kit is part number J14.

The standard power connector is a 2.1 x 5 mm coaxial power type, center positive. OEM versions can alternately be provided with a Phoenix terminal block for power input, or a D9 combined power/RS232 connector.

On OEM versions, power can also be applied to connector J8 pin 3, with J8 pins 5 and 6 being grounds. J8 pin 1 is at board coordinate X 0.500, Y 1.890; see fig 12.3.

The T564 power input is protected by a self-resetting polyfuse and a transzorb zener diode, and will withstand reasonable overvoltage or polarity reversal.

## 3.11 Custom Logic

Custom logic functions are available. Since the T564 incorporates eight internal delay generators, up to eight delay-only or delay-plus-fixed-width outputs can be provided.

## 3.12 Indicators

Three LED indicators are provided:

The green PWR LED indicates that power is available. It also blinks at a 1-Hz rate to indicate CPU heartbeat. Its color changes to yellow if any an internal error conditions are sensed.

The blue TRIG LED flashes whenever the T564 is triggered.

The COMM LED flashes yellow when any serial character is received and green when the T564 formats a reply.

## 3.13 Train and Frame Features

The TRAIN feature allows a single trigger to invoke a sequence of as many as 2^32 sets of programmed delays. See section 8.

The FRAME feature allows users to pre-load a list of up to 8192 delay and width settings, and enable the unit to rapidly reload these settings between shots, without realtime per-shot serial commands. See section 9.

TRAIN and FRAME may be used separately or together.

# 4. Programming

## *4.1 General Comments*

The T564 accepts ASCII serial commands from the standard RS-232 interface or from the optional 10/100 Ethernet adapter. Refer to Section 6 for details about configuring the Ethernet interface.

For evaluation, serial commands may be typed using any common serial communications program, for example HyperTerminal (for RS-232) or the standard "Telnet" utility for the Ethernet version. A family of **`HElp`** commands is available, summarizing serial commands and operating modes. The **`STatus`** command will send back a summary of T564 settings.

The standard baud rate is 38,400. The receive buffer is limited to 256 bytes, and the T564 ignores serial input while it is processing the current command line.

In the following section, text using this font...

**`TLevel <cr>`**

represents a command string sent to the T564, terminated with a carriage return character <cr>, and italic text...

***`1.25 <cr> <lf>`***

represents the reply from the T564. All commands must be terminated with semicolon or <cr>, and all reply lines are terminated by <cr> <lf>.

## *4.2 Command Strings*

Users send serial ASCII command strings to the T564, to which the T564 immediately replies. Because the standard baud rate is high, and because the T564 may spend a millisecond or more to process commands, user software must wait for a response to each command line before sending another command.

Each command consists of a command keyword, followed by an optional alpha or numeric argument. Multiple commands may be sent in a single line, separated by semicolons. When a full line is received, indicated by the final <cr> character, the buffered line is executed, in the order received.

Keywords may be fully spelled out, or may be sent as their first two letters; only the first two letters are significant. In this documentation, a word that has two possible forms is written with the short form capitalized, and the rest of the word in lower-case letters. The actual T564 protocol is case insensitive.

*Examples*

**TRigger** indicates that the short form is "**TR**", and the long form is **TRIGGER**, both of which are recognized commands.

All forms are case insensitive. One or more spaces are required to separate keywords from arguments.

A delay or width is sent as

```
ADelay 23.5u

CWidth 40n
```

Acceptable suffixes are:

p - pico (1E-12)
n - nano (1E-9)
u - micro (1E-6)
m - milli (1E-3)
s - seconds

and exponential notation is not supported. Default is nanoseconds.

Trigger levels are sent in volts, as **TLevel 1.50**

Most value-setting commands may be sent without an argument, in which case they become queries of the associated value.

**ADelay** (no argument)

evokes the reply

***02.123456789123***

which represents the delay setting for the rising edge of the A output, in seconds.

Since such long strings of numbers are difficult to read, a "verbose" mode is available, which will send times and other long numbers in the form

***02.123,456,789,123***

Certain incoming ASCII characters are treated specially:

All lowercase letters are converted to uppercase

TAB is treated as a space

ETX, ESC, and DEL are equivalent to BS, command line abort.

Colon is translated to semicolon, the command separator

Most other characters, including + - , * ? and linefeed, are ignored.

A "blank" input line, <cr> only, evokes the response ***T564 <cr> <lf>***

The T564 does not support hardware or software flow control. Other baud rates are available on special order.

## *4.3 Command Structure*

A command line begins with a command keyword (or its 2-letter abbreviation), followed by optional arguments. Multiple commands on a line may be separated by semicolons.

One or more spaces are required between a keyword and its argument. Whitespace may not break up a command token or an argument, but is otherwise allowed.

Query commands are requests for specific data. A query is often a "set"- type command without an argument.

Time-set commands are expressed as channel delays and widths, with the four pulse outputs identified as A, B, C, or D, corresponding to the four output pulse connectors.

All commands must be terminated by either an end of line indicator (carriage return, ASCII 13, denoted <cr> ) or the separator (`;`) for multiple commands on a line. Linefeeds are ignored.

Since the T564 receive buffer is limited to 256 bytes, users should not program multiple commands per line that might exceed this length. If at any time the <backspace> character (ASCII code 8) is received, the T564 will flush its receive buffer and ignore any previous input.

## 4.4 Reply Strings

Each received command will evoke a reply indicating the execution status of the command. For query commands, the reply is the requested data. For other commands, successful completion will yield a reply of ***OK***. If multiple commands are issued on one line, multiple responses will be sent back on a single line, separated by semicolons. For the command line...

```
TLEVEL 1.25; TLEVEL; TRIG POS
```

the reply will be of the form

```
OK;1.25;OK
```

All reply strings are terminated with carriage return/linefeed <cr> <lf> characters.

If an error occurs while processing a command, the reply ***??*** will be returned. If multiple commands are present on a command line, and any command produces an error, the erroneous command will respond with the ***??*** indicator and no remaining commands will be processed.

Numerical replies to queries will be in fixed-point decimal numeric form, with embedded commas included if Verbose mode is set.

## 4.5 Realtime Issues

User command lines are stored in a buffer until the <cr> character is received, at which time the entire command line is parsed and executed in the order received. Each command sends its reply characters, typically a requested value or the ***OK*** response, as the command is executed. Any additional incoming characters following the command-line <cr> are ignored until the entire command line is processed and the final response-line <cr> <lf> is returned.

Most simple commands execute in hundreds of microseconds, and their realtime execution rate is dominated by the 38.4 kbaud (3840 characters/second) serial communications rate. Shortform commands reduce communications overhead. Long reports are of course baud rate limited, with the **STatus** report or the longer **HElp** pages taking as long as 500 milliseconds.

When delay/width settings are changed via the **INstall** command (or an end-of-line autoinstall) or the trigger, burst, or gate parameters are changed, the firmware will immediately force the end-of-delay reset state, which will abort any timing cycles currently in progress. EOD will be asserted for about 350 microseconds, after which triggers will be re-enabled.

If aborting timing cycles is undesirable, one can disable triggers, wait until any possible timing cycle has finished, then do the desired operation. For example, if it were known that

all delay+width settings total under 40 milliseconds, one could sent the T564 the sequence...

```
TRIGGER OFF; WAIT 50000; CDELAY 2.5m; INSTALL; TRIGGER POS
```

to which it would reply

```
OK;OK;OK;OK;OK
```

with an additional 50 millisecond pause before the second ***OK***.

The T564 also features a **QUEUE** install mode, which allows delays to be reprogrammed without disrupting ongoing triggers; see section 4.7.2.

Command execution times are usually dominated by the 38 kbaud serial communications rate. If the isochronous interface is used, command execution can be much faster; see section 11.

## 4.6 T564 Command Summary

The following is a summary of commands which may be sent to the T564.

| LONG FORM | SHORT FORM | FUNCTION | |
|---|---|---|---|
| **ADELAY 45u** | **AD 45u** | set A delay | Note: all delays |
| **AWIDTH 25.5n** | **AW 25.5n** | set A width | and widths are |
| **ADELAY** | **AD** | delay A query | "pending" until |
| **AWIDTH** | **AW** | width A query | INSTALL time |
| **ASET ON** | **AS ON** | enable A output | |
| **ASET OFF** | **AS OF** | disable A output | |
| **ASET POS** | **AS PO** | set A polarity positive (normal) | |
| **ASET NEG** | **AS NE** | set A polarity negative (inverted) | |
| **ASET** | **AS** | query channel A settings | |
| **APENDING** | **AP** | query channel A pending settings | |
| **BDELAY 45u** | **BD 45u** | set B delay | |
| **BWIDTH 25.5n** | **BW 25.5n** | set B width | |
| **BDELAY** | **BD** | delay B query | |
| **BWIDTH** | **BW** | width B query | |
| **BSET ON** | **BS ON** | enable B output | |
| **BSET OFF** | **BS OF** | disable B output | |
| **BSET POS** | **BS PO** | set B polarity positive (normal) | |
| **BSET NEG** | **BS NE** | set B polarity negative (inverted) | |
| **BSET** | **BS** | query channel B settings | |
| **BPENDING** | **BP** | query channel B pending settings | |
| **CDELAY 45u** | **CD 45u** | set C delay | |
| **CWIDTH 25.5n** | **CW 25.5n** | set C width | |
| **CDELAY** | **CD** | delay C query | |
| **CWIDTH** | **CW** | width C query | |
| **CSET ON** | **CS ON** | enable C output | |
| **CSET OFF** | **CS OF** | disable C output | |
| **CSET POS** | **CS PO** | set C polarity positive (normal) | |
| **CSET NEG** | **CS NE** | set C polarity negative (inverted) | |
| **CSET** | **CS** | query channel C settings | |
| **CPENDING** | **CP** | query channel C pending settings | |
| **DDELAY 45u** | **DD 45u** | set D delay | |
| **DWIDTH 25.5n** | **DW 25.5n** | set D width | |
| **DDELAY** | **DD** | delay D query | |
| **DWIDTH** | **DW** | width D query | |
| **QDELAY 45u** | **QD 45u** | set all four (“quad”) delays | |
| **QWIDTH 25.5n** | **QW 25.5n** | set all four widths | |

| LONG FORM | SHORT FORM | FUNCTION |
|---|---|---|
| **DSET ON** | **DS ON** | enable D output |
| **DSET OFF** | **DS OF** | disable D output |
| **DSET POS** | **DS PO** | set D polarity positive (normal) |
| **DSET NEG** | **DS NE** | set D polarity negative (inverted) |
| **DSET** | **DS** | query channel D settings |
| **DPENDING** | **DP** | query channel D pending settings |
| | | |
| **INSTALL** | **IN** | apply pending channel settings immediately |
| **INSTALL 24** | **IN 24** | apply Frame settings immediately |
| **QUEUE** | **QU** | synchronous install at next EOD |
| **QUEUE 24** | **QU 24** | synchronous install Frame at next EOD |
| **AUTOINSTALL 1** | **AU 1** | apply pending settings at end of line |
| **AUTOINSTALL 2** | **AU 2** | queue pending settings at end of line |
| **AUTOINSTALL 0** | **AU 0** | cancel automatic mode |
| **UNDO** | **UN** | cancel all pending channel settings |
| | | |
| **TLEVEL 1.25** | **TL 1.25** | set external trigger level |
| **TLEVEL** | **TL** | query trigger level |
| **TRIGGER POS** | **TR PO** | trigger on external rising edge |
| **TRIGGER NEG** | **TR NE** | trigger on external falling edge |
| **TRIGGER INT** | **TR IN** | select internal 80 MHz trigger |
| **TRIGGER SYN** | **TR SY** | select internal DDS synthesizer |
| **TRIGGER REMOTE** | **TR RE** | select remote trigger |
| **TRIGGER OFF** | **TR OF** | disable triggers |
| **TRIGGER HIZ** | **TR HI** | trigger input is 10K to ground |
| **TRIGGER TERMINATE** | **TR TE** | trigger input is terminated at 50 ohms |
| **TDIV 5000** | **TD 5000** | set trigger divisor |
| **TDIV** | **TD** | query trigger divisor |
| **TRIGGER** | **TR** | trigger setup query |
| **TFREQ INPUT** | **TF IN** | set TFREQ to count trigger input signal |
| **TFREQ HITS** | **TF HI** | set TFREQ to count actual triggers |
| **TFREQ** | **TF** | return trigger frequency, Hz |
| **TPER** | **TP** | return trigger period, in ns |
| | | |
| **FIRE** | **FI** | fire remote trigger |
| **FEOD** | **FE** | force End Of Delay, abort timing cycle |
| | | |
| **SYNTHESIZE 3.579M** | **SY 3.579M** | set optional DDS synthesizer rate |
| **SYNTHESIZE** | **SY** | query DDS synthesizer rate |
| | | |
| **CLOCK HIZ** | **CL HI** | clock connector is unused |
| **CLOCK OUT** | **CL OU** | connector outputs 10 MHz |

| LONG FORM | SHORT FORM | FUNCTION |
|---|---|---|
| **CLOCK IN** | **CL IN** | external 10 MHz is accepted |
| **CLOCK** | **CL** | query clock settings and temperature |
| **CTRIM 2048** | **CT 2048** | set 10 MHz clock trim, 0...4095 |
| **CTRIM** | **CT** | query clock trim value |
| **CLOCK SAVE** | **CL SA** | save clock trim to flash memory |
| | | |
| **BNUM 555** | **BN 555** | set burst N, pulses output in burst |
| **BMOD 2000** | **BM 2000** | set burst M, total triggers/cycle |
| **BURST ON** | **BU ON** | enable burst mode |
| **BURST OFF** | **BU OF** | disable burst |
| **BURST RESET** | **BU RE** | reset burst counters |
| | | |
| **GATE OFF** | **GA OF** | disable gate functions |
| **GATE OUTPUT** | **GA OU** | make gate connector an output |
| **GATE INPUT** | **GA IN** | make gate an input |
| **GATE POS** | **GA PO** | gate in/out is active high (normal) |
| **GATE NEG** | **GA NE** | gate in/out is active low (inverted) |
| **GATE TERMINATE** | **GA TE** | gate input is terminated at 50 ohms |
| **GATE HIZ** | **GA HI** | gate input is 1K to +5 volts |
| **GATE BURST** | **GA BU** | enable single burst at gate input rise |
| **GATE REMOTE** | **GA RE** | enable single burst on command |
| **GATE FIRE** | **GA FI** | fire a single remote burst |
| | | |
| **TCOUNT OFF** | **TC OFF** | cancel pulse Train mode |
| **TCOUNT 2000** | **TC 2000** | add N pulses per trigger |
| **TSPACE 88U** | **TS 88U** | set train pulse spacing |
| | | |
| **FRAME OFF** | **FR OF** | cancel frame mode |
| **FRAME 12** | **FR 12** | store current settings into frame nnn |
| **FA 4** | **FA 4** | set start frame |
| **FB 24** | **FB 24** | set end frame |
| **FC 999** | **FC 999** | set frame repeat count |
| **FN** | **FN** | report frame load count. **FN 0** clears |
| **FP** | **FP** | report realtime frame pointer |
| **FRAME GO** | **FR GO** | start frame operation |
| **FRAME LAST** | **FR LA** | report last available frame index |
| **FRAME** | **FR** | report frame system status |
| **INSTALL 12** | **IN 12** | load saved frame N into hardware |
| **QUEUE 12** | **QU 12** | queue saved frame N into hardware |
| **FDUMP 8190** | **FD 8190** | display frame N contents, internal format |
| **FX** | **FX** | display frame diagnostic report |
| **RTEST** | **RT** | test frame memory |
| **RZAP** | **RZ** | clear frame memory |

| LONG FORM | SHORT FORM | FUNCTION |
|---|---|---|
| **STATUS** | **ST** | show T564 status report |
| **SAVE** | **SA** | save current setup |
| **RECALL** | **RE** | recall saved setup |
| **LOAD DEFAULT** | **LO DE** | load default setup |
| **RUN DEMO** | **RU DE** | run demonstration setup |
| **RSET** | **RS** | reset the T564 |
| | | |
| **SHOTS** | **SH** | query shot counter |
| **SHOTS 0** | **SH 0** | reset shot counter |
| **USEC** | **US** | query microsecond counter |
| **USEC 0** | **US 0** | reset microsecond counter |
| **IRQ** | **IR** | query 40 Hz interrupt counter |
| **WAIT 3400** | **WA 3400** | wait specified number of microseconds |
| | | |
| **IDENTIFY** | **ID** | return ID string |
| **ERRORS** | **ER** | return error status |
| **ERRORS 0** | **ER 0** | clear error flags |
| | | |
| **VERBOSE 1** | **VE 1** | show long numbers with commas |
| **VERBOSE 0** | **VE 0** | show long numbers without commas |
| **VERBOSE** | **VE** | query verbose setting |
| **COMMENT xxxx** | **CO xxxx** | command is ignored |
| | | |
| **HELP** | **HE** | return general HELP message |
| **HELP CHANNELS** | **HE CH** | return help on channel operations |
| **HELP TRIGGER** | **HE TR** | return Trigger help |
| **HELP CLOCK** | **HE CL** | return Clock help |
| **HELP BURST** | **HE BU** | return Burst help |
| **HELP GATE** | **HE GA** | return Gate help |
| **HELP PULSETRAIN** | **HE PU** | return Train help |
| **HELP FRAMES** | **HE FR** | return Frames help |
| **HELP MISC** | **HE MI** | return miscellaneous help |
| | | |
| **IS TX STRING** | **IS TX STRING** | send string to isoch transmit interface |
| **IS RX** | **IS RX** | get string from isoch receive interface |
| **IS LO STRING** | **IS LO STRING** | isoch loopback test |
| **IBLOCK 1** | **IB 1** | set isoch test flags |

## 4.7 Command Details

### 4.7.1 CHANNEL SET COMMANDS

The channel commands allow channel delays, widths, and modes to be set or queried.

Set a delay or width with the appropriate command, such as

**ADelay 65.81n**

**DWidth 55.2u**

where times may be specified with suffix characters **s,m,u,n,** or **p** for seconds, milliseconds, microseconds, nanoseconds, and picoseconds. The default is nanoseconds.

Interrogate a time setting with

**ADelay** which evokes the reply, in seconds,

*00.000000065810* in terse mode, or
*00.000,000,065,810* in verbose mode.

All channel settings are stored in a "pending" buffer until applied to the timing hardware. Two modes are available: INSTALL and QUEUE. See section 4.7.2.

The **UNdo** command cancels any pending channel settings.

**ASet ON** enables channel A output

**ASet OFf** disables channel A output. Its electrical output will stay low (or high, if channel is inverted) and its time settings are ignored.

**ASet POs** sets channel A polarity positive (normal)

**ASet NEg** sets A polarity negative (inverted)

**ASet** query channel A settings. A string will be returned...

***Ch A POS ON Dly 00.123,456,789,012 Wid 01.234,567,890,123***

**APending** query channel A pending settings. This produces a response identical to **ASET**, except that the pending values are presented.

The **QDelay** and **QWidth** "quad" commands set all four delays or widths.

Note that the channel polarity and on/off settings must be installed before taking effect, just as the channel delays and widths.

### *4.7.2 INSTALL AND QUEUE COMMANDS*

After one or more channel delay and width setting commands are transmitted, the new settings must be loaded into the delay generator hardware. This is inherently tricky, as delays may be in progress when the timing settings are changed.

When delay/width settings are changed via the **INstall** command (or an end-of-line autoinstall) or the trigger, burst, or gate parameters are changed, the firmware will immediately force the end-of-delay reset state, which will abort any timing cycles currently in progress. The EOD system reset will be asserted for about 300 microseconds, after which triggers will be re-enabled.

Use **INSTALL** when it is necessary to ensure that the very next trigger will use the latest-commanded timings.

The T564 also features a queued install mode, which allows delays to be reprogrammed without disrupting ongoing triggers. A **QUEUE** command will load the current time settings into the hardware at the next EOD, namely at the **end** of the next timing cycle. No cycles are lost or aborted.

**QUEUE** allows timings to be changed during ongoing triggers, without truncating timing cycles. The **QUEUE** operation requires a minimum delay from EOD until the next trigger of 10 microseconds, to allow vernier delay circuits to settle. Less delay may result in timing errors of as much as 20 ns.

The **AUtoinstall n** command enables either install or queue operations to be performed at the end of parsing the current command line.

| | |
|---|---|
| **AU 1** | enables "install" operation at end of line |
| **AU 2** | enables "queue" operation at end of line |
| **AU 0** | cancels automatic installs |

A typical command line might be

```
ADelay 45n; AWidth 130u; INstall
```

or

```
CDelay 33u; DWidth 500u; QUeue
```

where the final verbs are not needed if the appropriate autoinstall mode is enabled.

Both **INstall** and **QUeue** can accept an optional numeric argument to load frame data; see section 9.

### *4.7.3 TRIGGER SETUP COMMANDS*

The **TRigger** family of commands select the T564 trigger source and associated parameters.

| | |
|---|---|
| **TLevel 2.50** | Sets external trigger level; legal range is 0.25 to 3.30 |
| **TLevel** | Queries trigger level. The response would be ***2.50*** |
| **TRigger POs** | Trigger on external input, rising edge. |
| **TRigger NEg** | Trigger on external input, falling edge. |
| **TRigger OFf** | Disables triggers. |
| **TRigger INt** | Selects the internal 80 MHz trigger, 8x the internal 10 MHz clock. A divisor K of at least 5 is required to limit the trigger rate to the 16 MHz limit. |
| **TRigger SYn** | Selects optional internal DDS synthesizer as the trigger source. Its frequency may be set from 0.018 Hz to 16 MHz using the **SYN** command. |
| **TRigger REmote** | Enables software triggers, via the **FIRE** command. |
| **FIre** | Fires one remote trigger. |
| **TDivisor 80000** | Sets a trigger divisor integer K, from 1 to 2^32-1. When the divisor is loaded, the next trigger will fire the T564 (subject to other restraints) and then K-1 triggers will be skipped before another is enabled. **TD 0** disables the divide function. Divide can be combined with BURST. **CAUTION: a large trigger divisor can create the appearance of a triggering failure.** |
| **TRigger HIz** | Trigger input is 10K to ground. |
| **TRigger TErminate** | Enables 50 ohms terminator on TRIGGER input. |
| **TRigger** | Trigger setup query, evokes a response of... |

```
Trig   REM  50R  Level 1.250   Div   0,000,000,000  SYN 00,010,000.00
Hit Freq Hz 0,000,000,333      Period ns 0,003,002,800
```

The frequency of the electrical trigger source, or the actual DDG hit frequency, may be measured. The hit frequency can be lower than the incoming trigger rate if a divisor is programmed, gating is in use, or long delays result in missed triggers. After switching the measurement selection, wait at least two seconds for counts to settle. The frequency measurement timebase is one second.

| | |
|---|---|
| **TFreq INput** | selects the trigger input for measurement |
| **TFreq HIts** | selects the actual DDG hit rate for measurement |
| **TFreq** | returns the current trigger or hit frequency, in Hz |
| **TPer** | returns the corresponding period, in ns |

### *4.7.4 SYNTHESIZE COMMAND*

The T564 is furnished with a direct-digital frequency synthesizer that may be used to generate internal triggers from 0 to 16 MHz with 0.018 Hz resolution. This is not functional on the T564-10.

| | |
|---|---|
| **SYn 123.456K** | sets the frequency. Suffix characters may be K (kilohertz) or M (megahertz). The default is Hertz. |
| **SYn** | queries the current frequency |

### *4.7.5 BURST COMMANDS*

The **BURst** commands control the trigger burst logic. Burst allows a group of N pulses to be fired out of each group of M input triggers; that is, N successive triggers will be accepted, then M-N triggers will be skipped.

It is also possible to generate a burst of N triggers, invoked by the rising edge of the GATE input, or by remote command. See 4.7.5.

| | | |
|---|---|---|
| **BNum** | **555** | sets burst N, pulses output in burst |
| **BNum** | | queries burst N value |
| **BMod** | **2000** | sets burst M, total triggers/cycle |
| **BMod** | | queries burst M value |
| **BUrst** | **ON** | enables burst mode |
| **BUrst** | **OFf** | disables burst |
| **BUrst** | **REset** | reset burst counters; next trigger will be the first of N. |
| **BUrst** | | queries burst settings. This will return a string... |

***Burst OFF N 0,000,000,555 of M 0,000,002,000***

### *4.7.6 GATE COMMANDS*

The GATE coaxial connector may be used as an input or an output. As an input, it can enable or disable triggers under the control of an external TTL level. As an output, it can indicate when the internal hit flipflop is enabled to accept triggers.

If the gate is configured as an input, a true level allows triggers and a false level disables them. If BURST is also enabled, then whenever the input level is in the trigger disable

state, the burst counter logic is reset; the next time gate goes true, the burst logic will immediately enable a group of N triggers.

If gate is set to be an output, it will go active (high or low, as programmed) whenever the hit flipflop is armed to accept triggers. So in burst mode, it will go true during the active “N” pulses of the burst sequence. If a trigger divisor is programmed, it will go high only when the divisor enables triggers.

| | | |
|---|---|---|
| **GAte** | **OFf** | disable gate functions. |
| **GAte** | **OUtput** | make gate connector an output. The output level will be true when the hit flipflop is enabled to accept triggers |
| **GAte** | **INput** | make gate an input. When the external TTL level is true, triggers will be enabled. |
| **GAte** | **POs** | gate in/out is active high (normal) |
| **GAte** | **NEg** | gate in/out is active low (inverted) |
| **GAte** | **TErminate** | gate input is terminated at 50 ohms |
| **GAte** | **HIz** | gate input is 1K to +5 volts |
| **GAte** | **BUrst** | enable single burst at gate input rise |
| **GAte** | **REmote** | enable single burst on **GATE FIRE** command |
| **GAte** | **FIre** | fire a single burst |
| **GAte** | | gate setup query. Returns... |

***Gate OFF POS HIZ Shots 0,000,000,066***

### *4.7.7 CLOCK COMMANDS*

T564 timings are based on an internal 10 MHz crystal oscillator clock. The function or the CLOCK coaxial connector is controlled by this group of commands. If the connector is declared to be an input, the T564 accepts a 10 MHz TTL square wave input, or a sine wave of about 1 volt RMS, and will lock its crystal oscillator to this source. If the connector is set to be an output, the local 10-MHz oscillator frequency will be output from this connector.

The value used to trim the internal oscillator frequency is an integer in the range 0 to 4095, with 2048 being roughly the nominal center frequency. Since the internal crystal oscillator might be expected to drift 1-2 ppm per year, users may wish to occasionally trim its frequency if precise delays are required.

Clock-group serial commands are...

| | |
|---|---|
| **CLock HIz** | clock connector is unused |
| **CLock OUt** | connector outputs internal 10 MHz oscillator |
| **CLock IN** | external 10 MHz is accepted; oscillator phaselocks |
| **CTrim 2048** | sets 10 MHz clock trim, 0...4095, about 0.1 ppm/lsb. |
| **CTrim** | queries clock trim value |
| **CLock SAve** | save clock trim to flash memory. This value will be restored at powerup. |
| **CLock** | query clock settings; returns... |

***Clock OUT Trim 02048 Temp +32.4***

The ***Temp*** item is circuit board temperature in degrees C. It is typically about 10 degrees above ambient.

### *4.7.8 FEOD COMMAND*

The **FEod** (force end-of-delay) command briefly resets the timing hardware, aborting any timing cycle in progress. This is useful for terminating long delays.

### *4.7.9 SAVE, RECALL, LOAD COMMANDS*

The **SAve** command will save the overall T564 setup into nonvolatile memory. This setup will be restored at powerup, or may be installed via the **REcall** command.

| | |
|---|---|
| **SAve** | save current setup to nonvolatile memory |
| **REcall** | recall saved setup. Train and frame parameters are saved and recalled, but frame memory is not saved. |
| **LOad DEfault** | load default setup. The defaults are as shown in section 4.7.15. |
| **RUn DEmo** | run demonstration setup. This is the default setup, except that the T564 self-triggers at 20 KHz. |

***DEMO WAVEFORM***

***A***

***B***

***C***

***D***


### *4.7.10 USEC, WAIT, IRQ, SHOTS, COMMANDS*

The **`USec`** command returns the value of a free-running 32-bit counter that increments once each microsecond. **`USec 0`** resets the counter.

The **`WAit nnn`** command pauses command execution for a specified number of microseconds, up to 2^32-1, or about 4294 seconds.

The **`IRq`** command returns the value of the internal 40 Hz interrupt counter.

The **`SHots`** query returns the 32-bit shot counter. This counter increments every time the T564 is fired. **`SHots 0`** will clear the shot counter.

The following command line will return the approximate trigger rate in Hz:

```
SHOTS 0; WAIT 1000000; SHOTS
```

### *4.7.11 IDENTIFY COMMAND*

The **`IDentify`** command returns a string which identifies the T564 firmware version. The returned form is...

```
T564  Firmware 28E560-A
```

### *4.7.12 ERRORS COMMAND*

The **ERrors** command returns a string which identifies any T564 errors. The returned form is...

***Errs None***

Or

***Errs 00127 XTRIM RECAL CALIB LOGIC XLOCK TUNE DPLL***

where the integer value represents the error flags word. Bits are...

bit 0 VCXO trim value lost
bit 1 saved setup recall failed
bit 2 calibration table lost; default cals are used
bit 3 internal logic error
bit 4 VCXO failed to lock to external source
bit 5 powerup DPLL calibration error
bit 6 DPLL stability error

If any error bits are set, the string will also explicate the error bits in text. The "power" LED will turn yellow if any error bits are up.

The **ERrors 0** command will clear the error flags word.

### *4.7.13 VERBOSE COMMAND*

The **VErbose 1** command places the T564 in verbose mode, where commas are included in all long numeric strings that are returned. This mode makes time settings and 32-bit integers easier to read, but may not be compatible with external software.

The **VErbose 0** command will cancel verbose mode.

**VErbose** alone will query this setting.

### *4.7.14 HELP COMMANDS*

The **HElp** command, with no arguments, will display a short command summary, listing top-level commands. Specific commands will be explained with requests of the form **HElp TRigger** and such.

| | | |
|---|---|---|
| **HElp** | | return general HELP message |
| **HElp** | **CHannels** | return help on channel operations |
| **HElp** | **TRigger** | return Trigger help |
| **HElp** | **CLock** | return Clock help |

| | | |
|---|---|---|
| **HElp** | **BUrst** | return Burst help |
| **HElp** | **GAte** | return Gate help |
| **HElp** | **PUlsetrain** | return Train help |
| **HElp** | **FRames** | return Frames help |
| **HElp** | **MIsc** | return miscellaneous help |

### *4.7.15 STATUS COMMAND*

The **STatus** query returns a report of T564 settings. A typical report is shown below. Verbose mode was enabled. The default setup was loaded.

```
     Highland Technology  Model T564  Digital Delay Generator

Firmware 28E560-A  1034                 Cal date January 31, 2014

Trig   REM  50R  Level 1.250   Div   0,000,000,000  SYN 00,010,000.00
Hit Freq Hz 0,000,000,000      Period ns 0,000,000,000

Gate   OFF  POS  HIZ           Shots 0,000,000,066
Burst  OFF  N  0,000,000,016   of M  0,000,000,064

Verbos ON   Autoinstall FEOD   Usec 0,306,931,240  DPLL 00000
Clock  OUT  Trim 02048         Temp +35.6

Errs   None

Train count 0,000,000,000      Train spacing 0,000,000,003

Frames  OFF     FA 00000   FB 00009   FC 00000   FN 0,000,000,000

Ch A  POS  ON     Dly  00.000,000,000,000  Wid  00.000,002,000,000
Ch B  POS  ON     Dly  00.000,002,000,000  Wid  00.000,002,000,000
Ch C  POS  ON     Dly  00.000,004,000,000  Wid  00.000,002,000,000
Ch D  POS  ON     Dly  00.000,006,000,000  Wid  00.000,002,000,000
```

Since the report is subject to change of both format and contents, it is recommended that it not be parsed to extract T564 parameters.

#### *4.7.16 RSET COMMAND*

The **RSet** command performs a hardware reset/restart of the T564, equivalent to a power off/on cycle. The reset takes about 4 seconds, after which the T564 will respond with the string…

***Highland Technology T564 DDG <cr> <lf>***

The last-saved setup will be installed.

#### *4.7.17 PTRAIN, PSPACE, FRAME, AIM, GET COMMANDS*

See sections 8 and 9.

### *4.8 Firmware Upgrade Procedure*

T564 firmware may be field-upgraded, from a Windows PC with an RS-232 serial-port connection to the unit.

The PC must have the following Highland-provided files in a common folder:

| | |
|---|---|
| Flash1.bat | batch file for COM1 port |
| Flash2.bat | batch file for COM2 port |
| 28E560z.fls | script file to flash version 28E5640 |
| 28E560z.rom | application file to be loaded |
| Flash560_Win.exe | Windows flash manager program |

To reflash the T564 firmware, connect PC serial port COM1 or COM2 to the T564 using Highland cable part number T565 or equivalent, and start the appropriate Flash1.bat or Flash2.bat batch file.

The flash procedure should now run, reporting progress. At the end, verify that the displayed file and actual flash checksums are equal.

## 5. Powerup States and Saved Setups

Users may program the T564 as desired and then use the **SAve** command to copy all setups to nonvolatile flash memory. That saved setup may be recalled at any time via the **REcall** command. The saved setup is also recalled and installed at powerup, allowing the T564 to resume operation without any serial commands.

The powerup sequence takes about 4 seconds. During this time, channel outputs are electrically low and terminations are high-Z.

If the saved configuration programs channels to be inverted polarity, those outputs will transition from low to high when the initial powerup sequence is over.

# 6. Xport Ethernet Module Setup

The T564-2 uses a Lantronix Xport module as its Ethernet/TCP-IP interface.

Units are normally shipped set to IP address 192.168.254.183, port 2000. Most users will need to reassign the IP address to be compatible with their networks. If multiple T564s are used, assign a unique IP address to each. The Xport also supports dynamic IP address assignment.

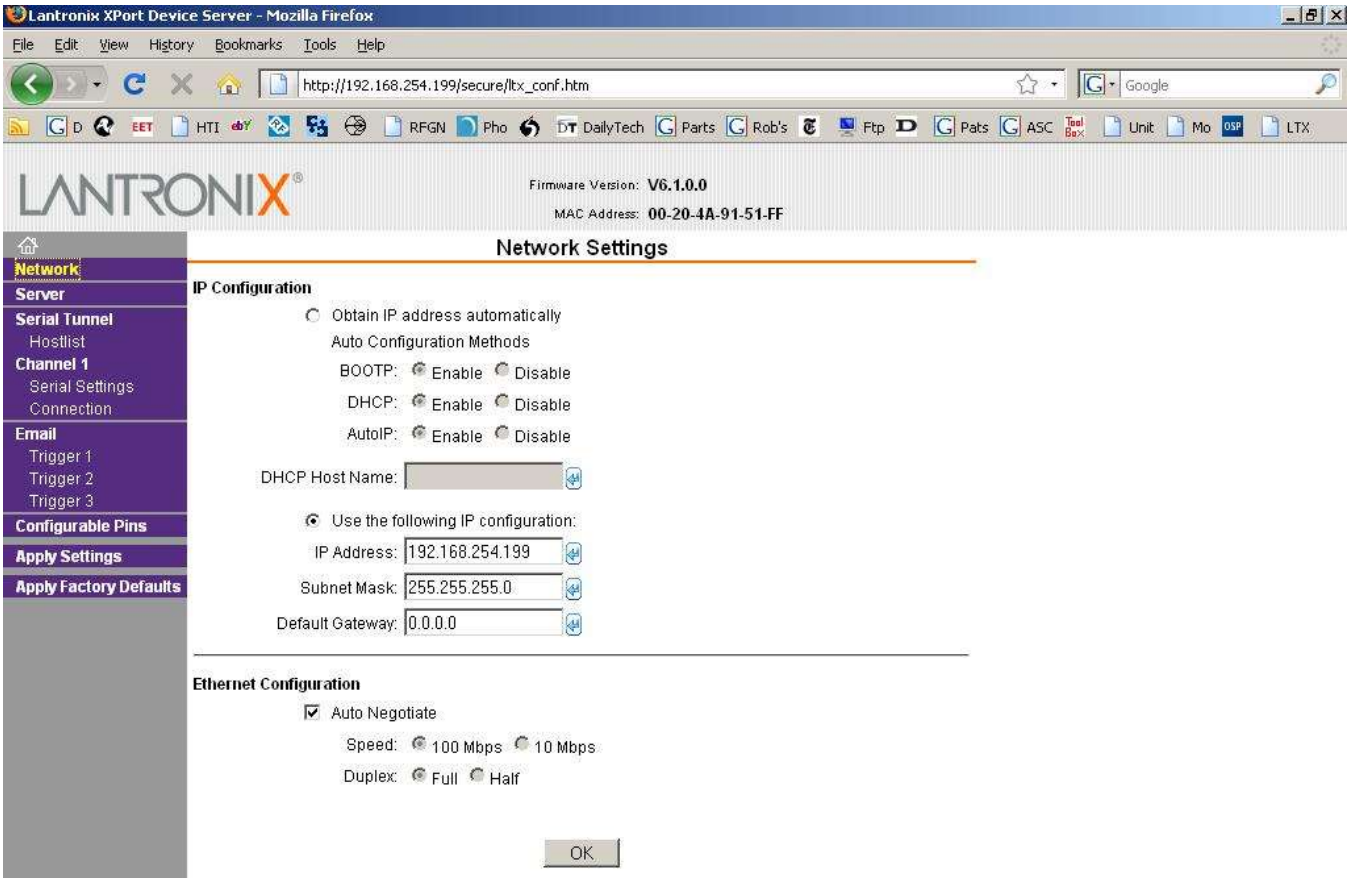
Lantronix provides a PC utility "XportInstaller" to locate an Xport module by MAC address and assign it an IP address. The Lantronix software utilities may be downloaded from

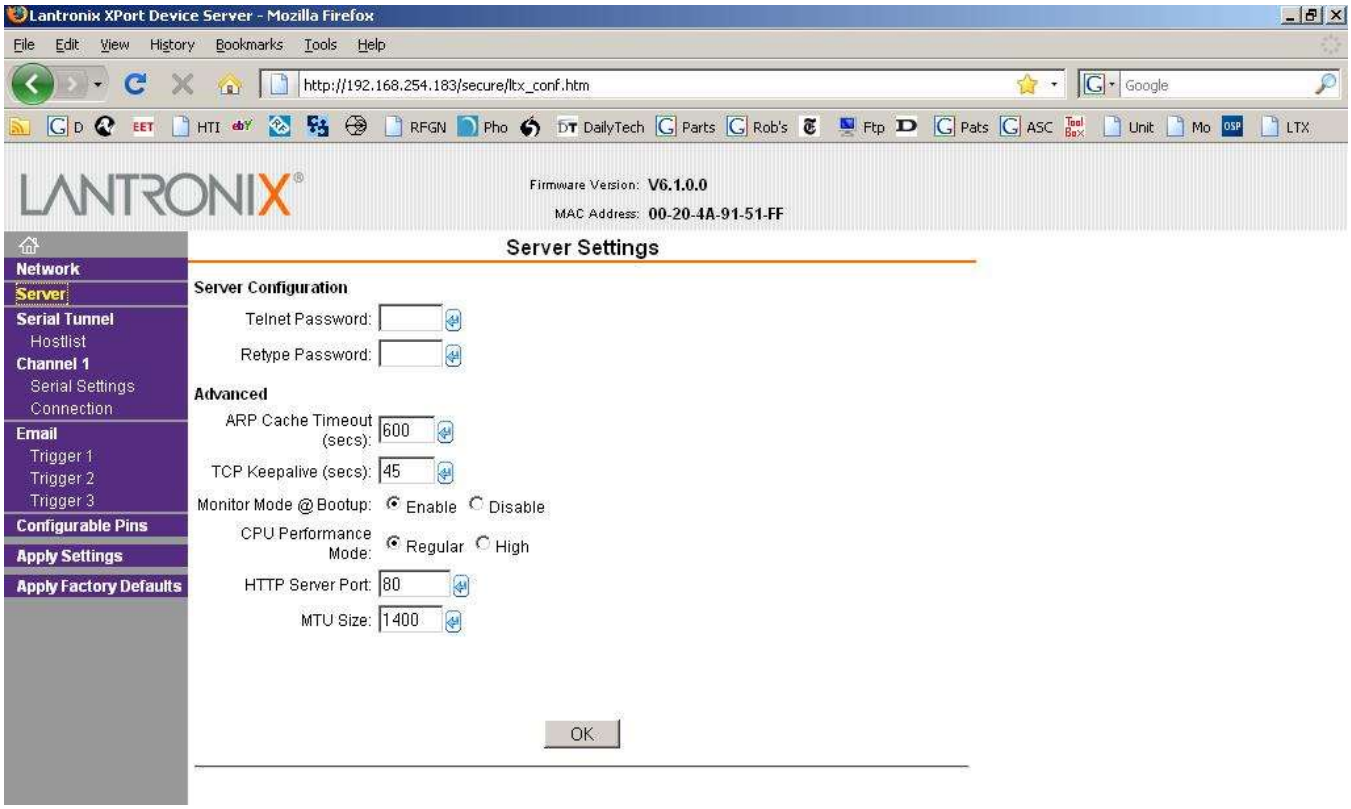
http://www.lantronix.com

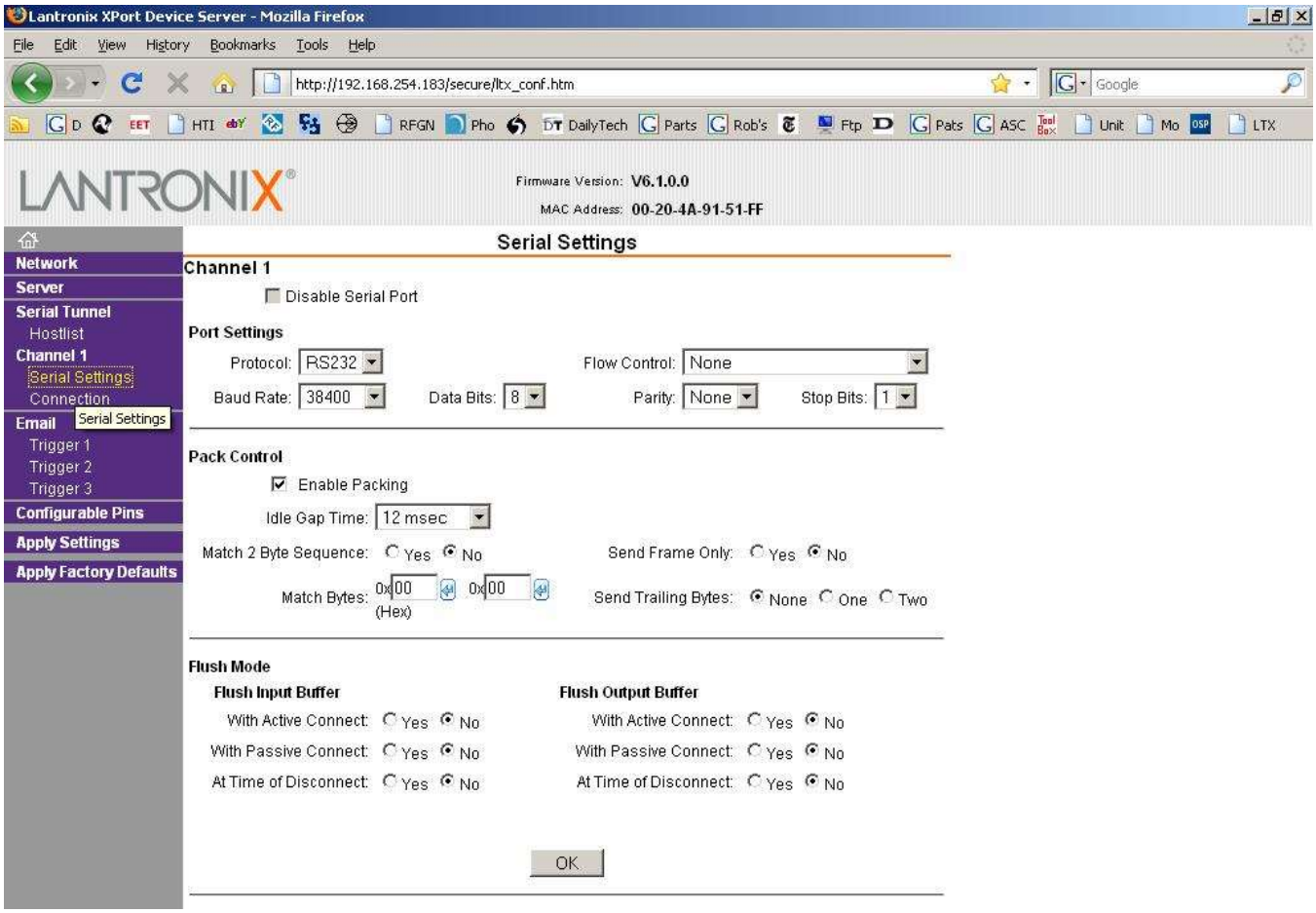
The XportInstaller IP address assignment pane looks like this:

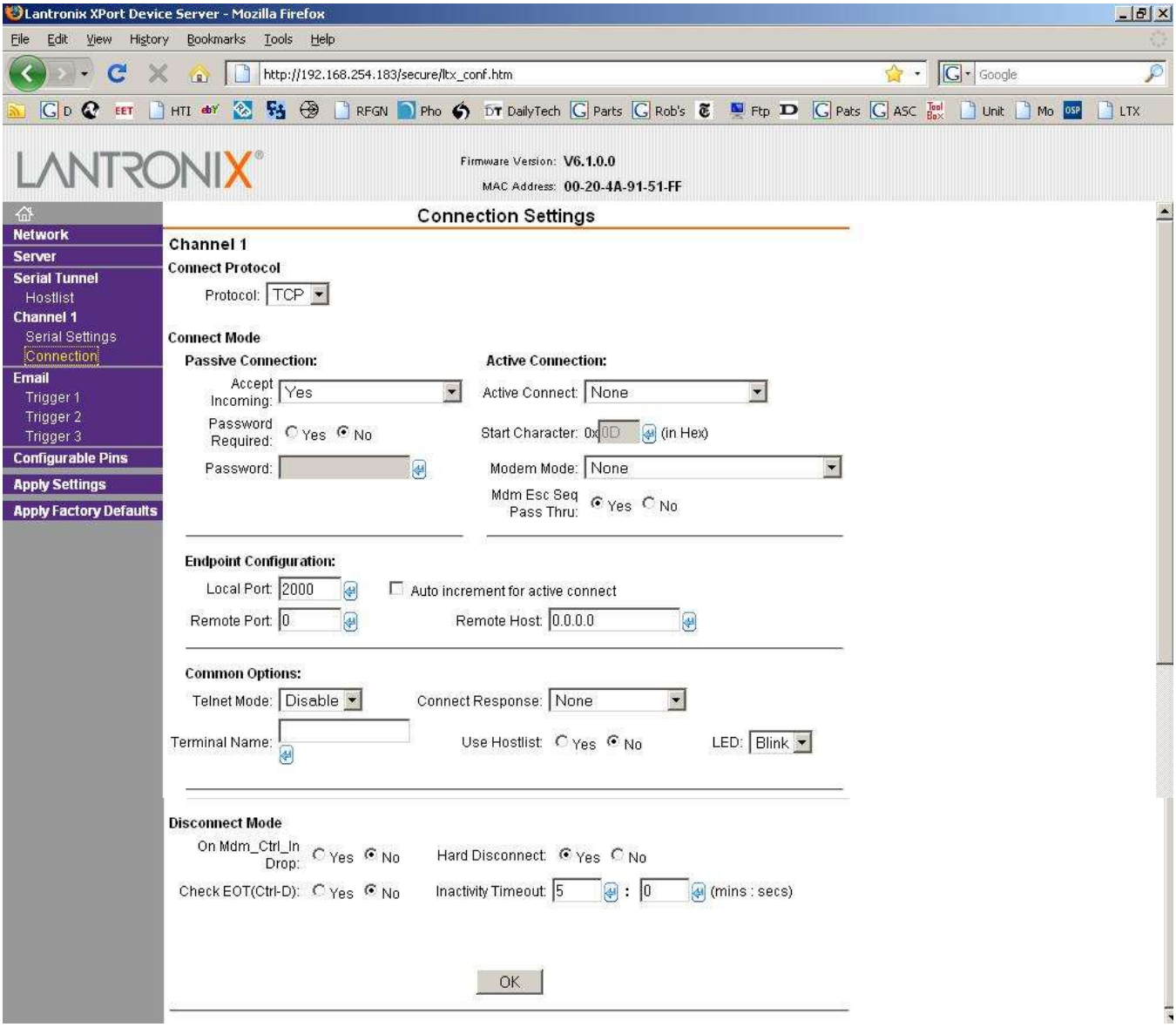

Once the Xport module has been assigned an IP address, a web browser can be used to access the Xport module as a web page; just type the IP address into the browser's address bar, after which settings may be edited. You need not initially enter a user name or password. The web page interface can also be used to change the IP address, so if your browser can access the Xport directly, you need not run the XportInstaller.

The following images represent the setup in which the Xports in the T564 are normally shipped. The usual IP address is actually 192.168.254.183.


Lantronix XPort Device Server - Mozilla Firefox
File Edit View History Bookmarks Tools Help
http://192.168.254.183/secure/ltx_conf.htm
LANTRONIX
Firmware Version: V6.1.0.0
MAC Address: 00-20-4A-91-51-FF
Network
Server
Serial Tunnel
Hostlist
Channel 1
Serial Settings
Connection
Email
Trigger 1
Trigger 2
Trigger 3
Configurable Pins
Apply Settings
Apply Factory Defaults
Server Settings
Server Configuration
Telnet Password:
Retype Password:
Advanced
ARP Cache Timeout (secs): 600
TCP Keepalive (secs): 45
Monitor Mode @ Bootup: Enable Disable
CPU Performance Mode: Regular High
HTTP Server Port: 80
MTU Size: 1400
OK


Lantronix XPort Device Server - Mozilla Firefox
File Edit View History Bookmarks Tools Help
http://192.168.254.183/secure/ltx_conf.htm
LANTRONIX
Firmware Version: V6.1.0.0
MAC Address: 00-20-4A-91-51-FF
Network
Server
Serial Tunnel
Hostlist
Channel 1
Serial Settings
Connection
Email
Trigger 1
Trigger 2
Trigger 3
Configurable Pins
Apply Settings
Apply Factory Defaults
Serial Settings
Channel 1
Disable Serial Port
Port Settings
Protocol: RS232
Flow Control: None
Baud Rate: 38400
Data Bits: 8
Parity: None
Stop Bits: 1
Pack Control
Enable Packing
Idle Gap Time: 12 msec
Match 2 Byte Sequence: Yes No
Send Frame Only: Yes No
Match Bytes: 0x00 0x00 (Hex)
Send Trailing Bytes: None One Two
Flush Mode
Flush Input Buffer
With Active Connect: Yes No
With Passive Connect: Yes No
At Time of Disconnect: Yes No
Flush Output Buffer
With Active Connect: Yes No
With Passive Connect: Yes No
At Time of Disconnect: Yes No
OK




Note that the Xport allows only one TCP/IP connection to be open at any one time, and will time out and disconnect after the time set for a hard disconnect. Enter 0 to disable automatic disconnect. It is usually prudent to set up the Xport to disconnect after some inactivity period, to avoid having an inactive connection lock out access.

A periodic ping, such as sending a single null character every minute or so, will keep a TCP/IP session open.

# 7. Jitter Notes

Jitter is defined as the 1-sigma standard deviation of delay. It is the shot-to-shot time uncertainty from the external trigger to any output rising or falling edge, or the uncertainty between edges of channel outputs. Jitter is measured in RMS picoseconds. Visual peak-to-peak jitter is roughly 5 times that of RMS.

"Jitter" is usually accepted to indicate time variance as observed over an interval of 0.1 seconds, with the term "wander" used to describe slower changes of delay. Wander thus encompasses changes in delay driven by temperature changes and other slow effects. The T564 jitter specs are valid for observation periods up to 10 seconds in the absence of radical temperature changes. Note that coaxial cable propagation delay can change considerably with temperature and can contribute to observed timing variance.

Uncorrelated jitters add trigonometrically, as the square root of the sum of the squares of all jitter contributors.

Jitter can be difficult to measure. The trigger input to the T564 must be clean and fast (< 2 ns risetime) and the measuring instrument must have a jitter noise floor well below that of the T564. Most oscilloscopes and counters are not capable of resolving T564 jitter performance, especially so for longer delays. For example, a Tektronix 11801C sampling oscilloscope (or the newer DSA8200 without the optional phaselock module) has a short-delay jitter well below that of the T564, but has added jitter on the order of 20 microseconds per second of delay, whereas the T564 starts with a greater basic jitter but typically adds about 4 ns of jitter per second of delay.

For lowest jitter from an external trigger, the T564 trigger level should be set to the steepest part of the input edge, typically 1/3 to 1/2 of the peak amplitude.

Jitter is a function of the generated time delays. Very short delays have a baseline jitter that depends on fundamental triggered-oscillator phase noise. After about 500 ns, the DSP stabilization loop becomes active and disciplines the triggered oscillator, limiting its jitter accumulation.

Long delays, in the milliseconds range, become dominated by the phase noise of the internal crystal oscillator, typically about 4 ns per second of delay. Long-delay effects are zero relative to a user-provided 10 MHz reference clock.

Jitter between successive triggers, referred to as "period jitter", depends on the quality of the trigger source. The internal DDS trigger synthesizer has jitter typically about one part in 20,000 of the trigger period. DDS jitter is best if its frequency is in the 2-10 MHz range, where the period jitter, measured at a channel output, is typically about 25 ps RMS. For lowest DDS jitter at lower rates, keep the DDS synthesizer frequency in this range and use a trigger divisor to get lower trigger rates.

Dividing down the internal 80 MHz clock results in period jitter in the neighborhood of 40 ps RMS, until millisecond-range periods when crystal oscillator phase noise again becomes important.

The graph below summarizes typical T564 jitter versus delay. Here, "delay" refers to the time from an external trigger to any output edge. The rise which begins at about 1 millisecond is caused by internal crystal oscillator phase noise, and will not be present relative to an external 10 MHz reference. The T564 is also available with optional, lower phase-noise TCXO or OCXO oscillators. The graphed data includes jitter contributed by the P400 trigger source and the 11801C oscilloscope, so actual T564 jitter is somewhat less.

Jitter between outputs is similar.

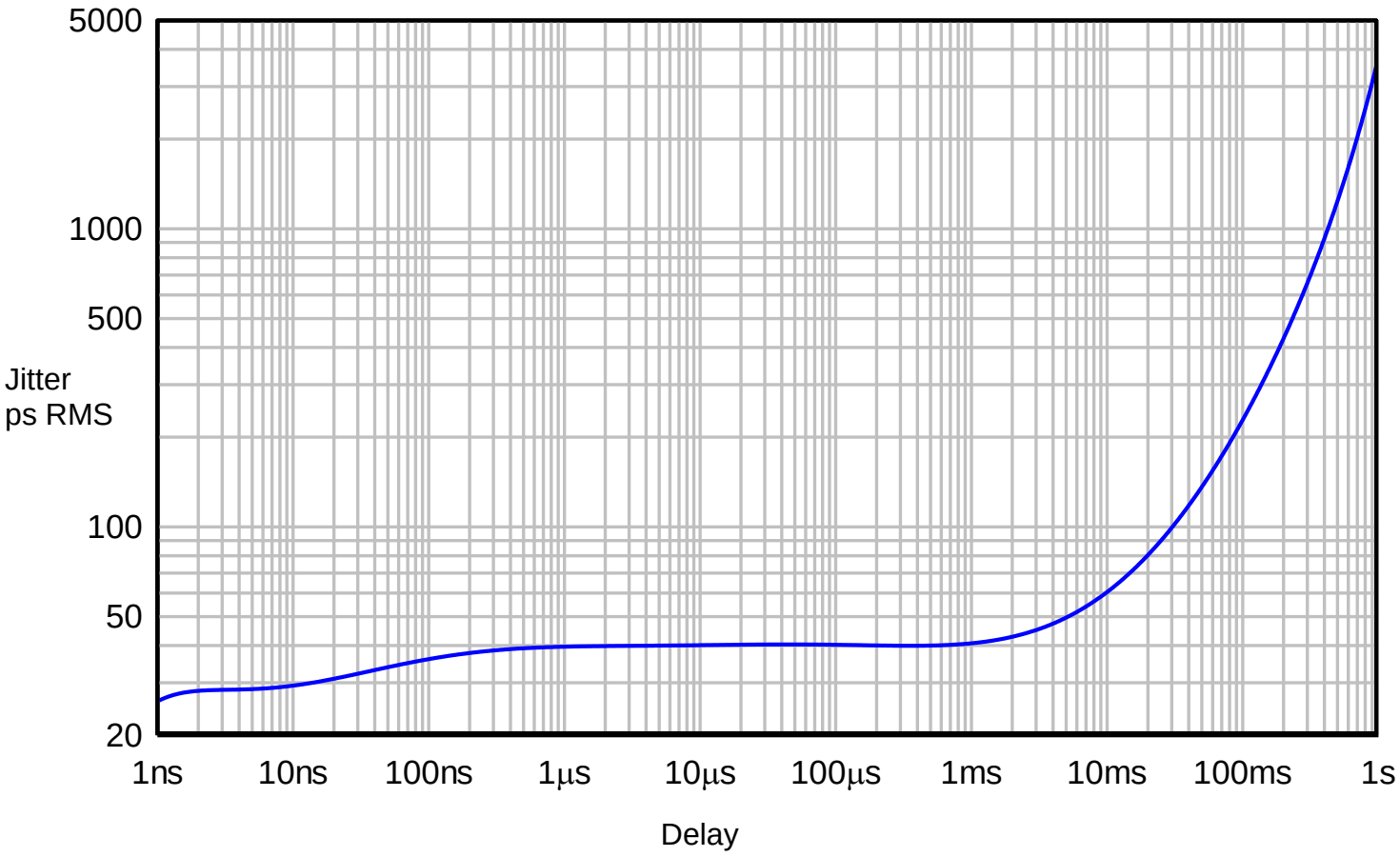



Fig 7.1 Typical T564 jitter in ps RMS versus delay

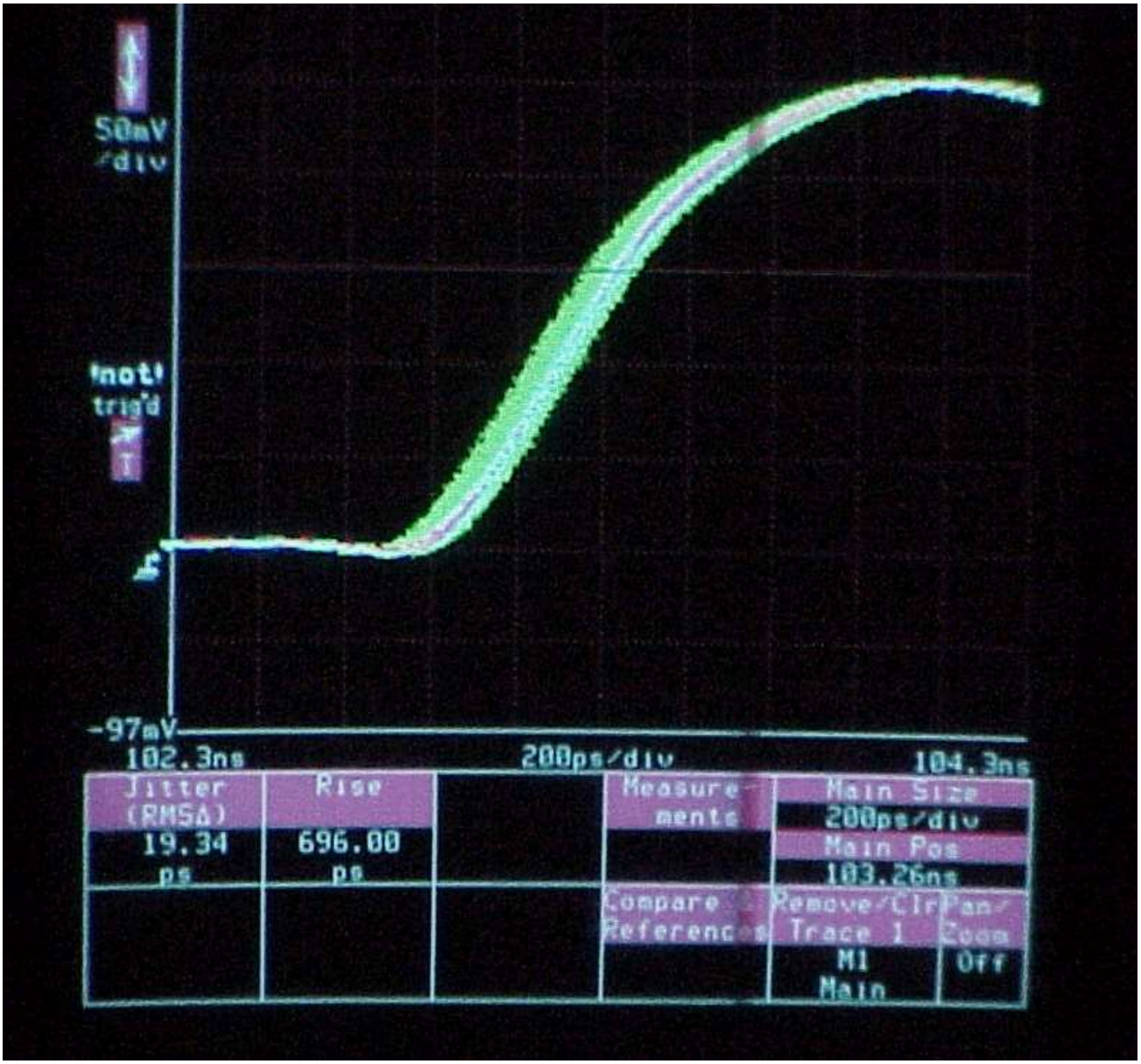



Fig 7.2 Typical T564 Rising Edge, Externally triggered, delay = 100 ns

This was measured on a Tektronix 11801A sampling oscilloscope, with the scope and the T564 triggered by a Highland P400 digital delay generator. Indicated jitter is 19.3 ps RMS, risetime 696 ps. Indicated jitter includes the P400 and oscilloscope contributions.

# 8. Pulse Trains

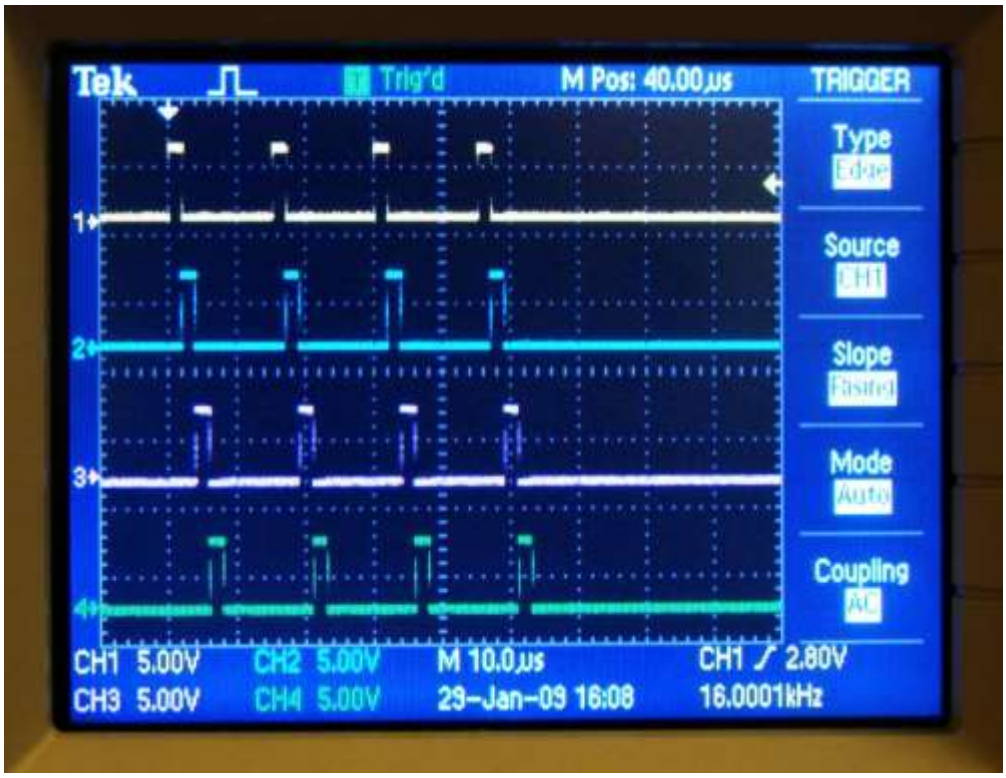
The T564 may be programmed to produce pulse trains, namely to make a sequence of delay cycles starting with a single trigger. The associated waveforms are shown below...

A

B

C

D




The first set of A/B/C/D outputs are the usual ones, as programmed by the standard channel delay and width commands. After these are finished, additional sets are generated, spaced from the original set by time T2. This particular sequence was invoked by the **`TCount 3`** command. Note that the numeric argument to the **`TCount nnn`** command is the number of additional pulses added to the normal pulse output.

The pulse spacing T2 is set by the **`TS ddd`** command, **`TS 750`** for a 15 us group spacing in this example. The time is expressed in units of 20 ns. Up to 2^32-1 pulses can be generated by the train facility, with spacing T2 from 80 ns to 10 seconds. T2 must be set to time W+80 ns minimum, where W is the time from the first edge (here, the rise of A) to the last edge (here, the fall of D.)

The T2 intervals are quantized to 20 ns, and are exact to the accuracy of the internal crystal oscillator timebase.

After all pulses are over, the standard EOD (end-of-delay) system reset occurs.

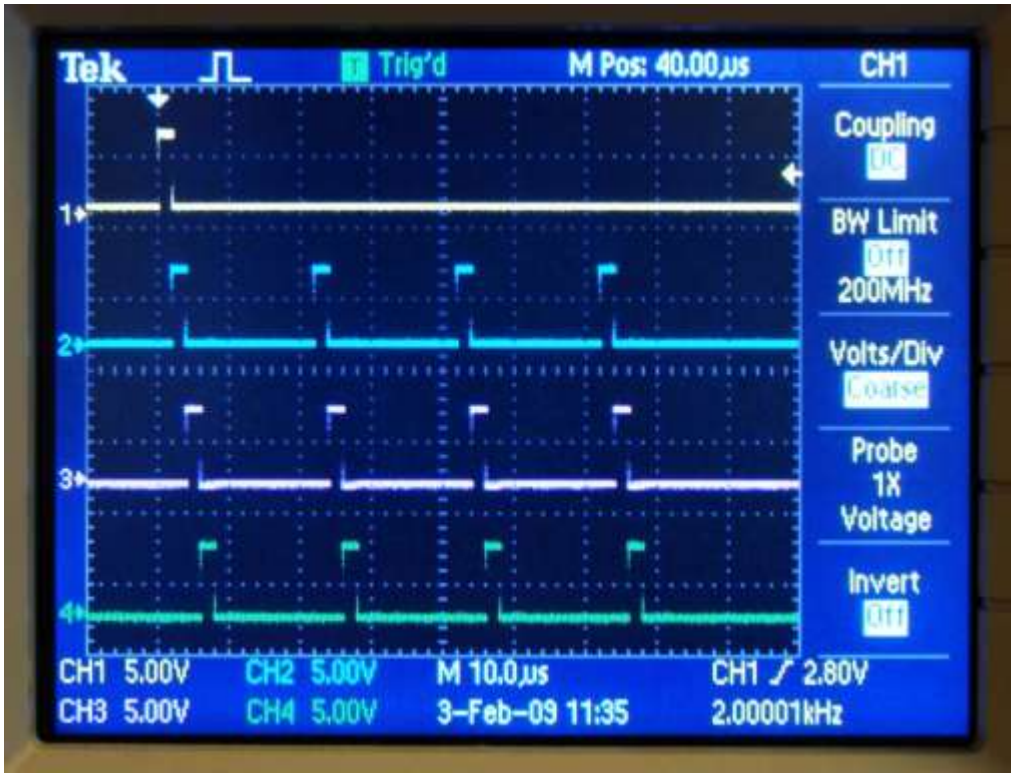
The associated serial commands are...

| | | | |
|---|---|---|---|
| **TCOUNT** | **OFF** | **TC OFF** | cancel Train mode |
| **TCOUNT** | **2000** | **TC 2000** | make a train of 2001 pulses per trigger |
| **TSPACE** | **88** | **TS 88** | set train T2 spacing to 1760 ns |

**TCount OFF** resets the train subsystem. This immediately clears the pending, actual, and hardware Tcount values. **TCount 0** disables train operation but operates like a normal timing parameter, requiring an **INSTALL** or **QUEUE** command to become effective.

The train parameters must be installed before becoming active, using the **INSTALL** or **QUEUE** commands, or their autoinstall equivalents. Train parameters are saved in Frames.

If any channel is programmed for a delay below 20 ns in Train mode, only the first, single pulse will appear. This is defined as a feature, as it allows a single "train start" output pulse to be generated. In the example below, the channel A delay is set to zero, so it makes only one initial pulse in Train mode.



# 9. Frames

The T564 allows a schedule of multiple delay setups to be stored in local volatile memory, with new settings loaded rapidly after each trigger/delay sequence.

Delay setups are compiled and stored in "frames". Each frame includes channel delays, widths, channel enable bits, channel polarities, and TRAIN parameters. Users may program a group of settings and store that setup to a numbered frame.

At runtime, initializing the frame system will allow a number of DDG shots to be fired, using parameters extracted from sequential frames. The T564 can store up to 8192 frames.

The frame controller logic has three states:

OFF frame system is disabled. DDG operates normally.

RUN frames are being loaded at each end-of-delay, namely at the end of each timing cycle.

DONE last frame has been loaded and run, and triggers are inhibited.

The associated serial commands are...

| | |
|---|---|
| **FRAME OFF** | disable frame mode |
| **FRAME nnn** | save current settings to frame nnn, in range 0 to 8191. |
| **FA nnn** | set first frame to execute. **FA** with no argument is a query. |
| **FB nnn** | set last frame to execute. FB must be greater than FA |
| **FC nnn** | set frame loop count, 0 to 65534. Value 65536 sets infinite loop. |
| **FRAME GO** | enter RUN state and start frame execution, from first to last. |
| **FRAME LAST** | report maximum available frame index, usually 8191 |
| **FN** | report number of frames loaded into hardware. **FN 0** clears count |
| **FP** | report realtime frame pointer |
| **FRAME** | report frame system state |
| **INSTALL nnn** | unpack frame nnn and load immediately into DDG hardware |
| **QUEUE nnn** | unpack frame nnn and queue into DDG hardware |

The **FRAME GO** command loads the start (FA) frame into the hardware and queues the next sequential frame to be installed into the timing registers at the next EOD, namely at the end of the next shot sequence. Subsequent triggers use the timings extracted from sequential frames. After the last (FB) frame is used, triggers are disabled until another **FRAME GO** or **FRAME OFF** command is issued.

**FRAME GO** will produce the error response ***??*** if FB is not greater than FA.

The **FRAME** command, with no argument, returns ***OFF*** or ***DONE*** if frame execution is not active, or an integer from 0 to 8191 identifying the next frame to be executed if the sequence is active.

The **FRAME OFF** command returns the DDG to normal operating mode. The last-sent group of channel settings is re-installed, and triggers will be re-enabled if the trigger settings allow. One can issue the **TRIGGER OFF** command before the **FRAME OFF** command if this sequence might produce undesired outputs.

If the FC parameter is zero, a **FRAME GO** command will load frames FA through FB into the hardware then stop, responding to (FB-FA+1) triggers. If the FC loop parameter is in the range of 1 to 65534, that sequence will be repeated FC times, responding to (FB-FA+1) * (FC+1) triggers, about 536 million triggers in the extreme case. If FC is set to 65535 and **FRAME GO** is executed, the frame system will loop forever, executing frames FA through FB until terminated by **FRAME OFF.**

To speed up loading frames, it is recommended that Autoinstall be off (zero), and it is not necessary to issue an **INSTALL** command before saving a frame.

The FA, FB, and FC parameters may be queried at any time, but it is illegal to change them while frames are actively running. The command **FB 222** will invoke the ***??*** response if frames are running.

There are some realtime limitations to frame performance. Trigger rate may not exceed 15 KHz, and there must be a minimum delay between EOD and the next trigger of 10 microseconds, where EOD is the time of the trailing edge of the last active channel. Violating these limits may cause triggers to be missed.

Another note is that calibration and delay temperature compensation math is performed at the instant a frame is compiled and saved, so later playback of frames may result in more than normal temperature drift, as much as 20 ps per degree C. So it is best to load "fresh" frames for maximum accuracy.

If frames have been loaded but frame operation is inactive, one can issue the **INSTALL nnn** or **QUEUE nnn** commands to load the setup of frame nnn into the DDG timing hardware. This allows the frame buffer to be used to store up to 8192 saved timing setups, any of which can be recalled with a relatively short serial command. These commands are also useful for testing frame setups. Set Autoinstall mode to zero when using these commands; otherwise an end-of-line autoinstall will override any recalled frame settings.

After such an **INSTALL nnn** or **QUEUE nnn** command, queries of channel delay or width settings will reflect the last values sent by normal **DELAY** or **WIDTH** commands, and not the values just recalled from frame memory.

Since channel on/off and pos/neg polarity states are saved in frames, it is possible to have channels selectively fire on a frame-by-frame basis. One can also program a channel to be off, but still flip its polarity on a per-frame basis, effectively creating a static TTL output that is controllable in each frame.

Some diagnostic commands are...

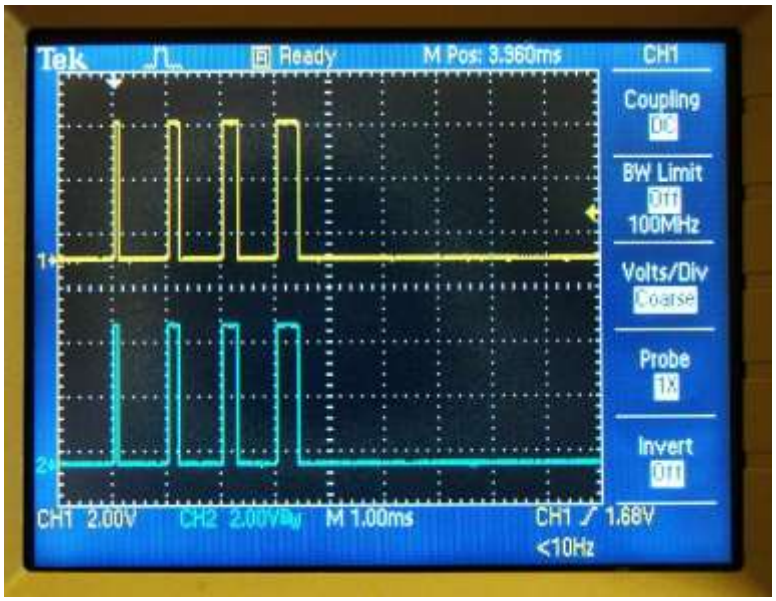
| | | |
|---|---|---|
| **FDUMP 8190** | **FD 8190** | display frame N contents, internal format |
| **FX** | **FX** | display frame diagnostic report |
| **FM** | **FM** | display frame trigger down-counter |
| | | |
| **RTEST** | **RT** | test frame memory |
| **RZAP** | **RZ** | clear frame memory |

The following is a simple example of frame operation. The following serial commands are sent to the T564:

```
LOAD DEFAULT
QDELAY 0
QWIDTH 100U; FRAME 1
QWIDTH 200U; FRAME 2
QWIDTH 300U; FRAME 3
QWIDTH 400U; FRAME 4
FA 1; FB 4
TDIV 80000
FRAME GO
TRIGGER INTERNAL
```

This will result in four triggers being fired at a 1 KHz rate, producing pulses of 100, 200, 300, and 400 microseconds on all four output connectors. The **LOAD DEFAULT** command cleared the frame loop counter FC, so frames 1 through 4 are scanned only once. The FN counter is incremented by five, the number of triggers plus one.

The resulting waveform is shown below, with the A and B outputs displayed.

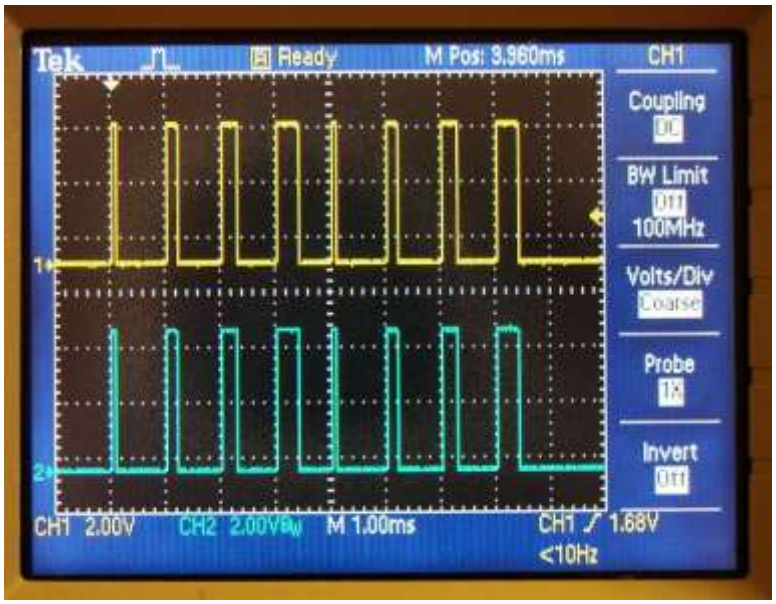



Another **FRAME GO** command will repeat this sequence.

If we then issue the commands

```
FC 1
FRAME GO
```

the four programmed frames will be executed twice, accepting a total of 8 triggers. The FN count will increment by 9.



# 10. Optional E and F Outputs

The T564 can be furnished with optional E and F electrical outputs.

E produces a short (8 ns nom) positive pulse at the rising edge of the standard channel A output, and F produces a similar pulse at the falling edge of A.

A

E

F


In figure 12.3, the E output connector is in the position to the left of the D output, and F is immediately to the right of the A output.

# 11. J14 Auxiliary Connector

The T564-10 version is provided with a bottom-side single-row female box connector which provides additional control and communications features.

## 11.1 J14 Pinout

J14 pinout is as follows:

| Pin | Name | Description |
|---|---|---|
| 1 | TRIGMON | Buffered copy of the trigger comparator output. If the T564 is triggered by an external falling edge, this is inverted; otherwise it is true. |
| 2 | ARM | Logic level input to the T564, with an internal pull up resistor. When pulled low, triggering is disabled. When pulled up or left floating, triggering is enabled. |
| 3 | SRD | Isochronous serial reply data from the T564 |
| 4 | AUXTRIG | Auxiliary trigger |
| 5 | SPD | Isochronous serial command data to the T564 |
| 6 | SCLK | Externally-generated isochronous serial clock, in the 1-5 MHz range |
| 7 | NC | No connection |
| 8 | NC | No connection |
| 9 | GND | Signal ground |
| 10 | GND | Signal ground |
| 11 | NC | No connection |
| 12 | NC | No connection |
| 13 | NC | No connection |
| 14 | GND | Signal ground |

Logic levels are 3.3 volt CMOS.

## 11.2 Isochronous Serial Interface

The T564 is available with an optional SPI-like fast, TTL-level serial command interface. This interface is in addition to, and operates concurrently with, the standard RS-232 serial interface. The command protocol is identical to the RS-232.

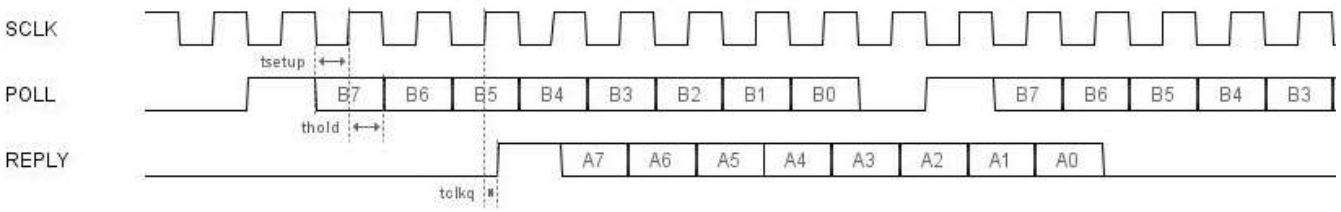
The interface uses three TTL-level signals:

SCLK continuous serial clock, user-furnished, 4 MHz nom

SPD poll (command) serial data, from user to T564; T564 "receive"

SRD reply serial data, from T564 to user; T564 "transmit"

Serial data lines idle electrically low. A byte is sent as a single high "start" bit, eight data bits, and a low stop bit.




| | | |
|---|---|---|
| $f_{clk}$ | SCLK frequency | 5 MHz recommended max |
| $t_{clkw}$ | SCLK high/low pulse width | 65 ns min |
| $t_{setup}$ | POLL change to SCLK rising edge | 30 ns min |
| $t_{hold}$ | SCLK rising edge to POLL change | 10 ns min |
| $t_{clkq}$ | SCLK rising edge to REPLY change | 30 ns min<br>80 ns max |
| $V_{ip}$ | Logic high input voltage | 2.4V min |
| $V_{il}$ | Logic low input voltage | 0.6V max |
| $V_{oh}$ | Logic high output voltage | 2.9V min ($I_L$ = 100 uA)<br>2.3V min ($I_L$ = 24 mA) |
| $V_{ol}$ | Logic low output voltage | 0.1V max ($I_L$ = 100 uA)<br>0.55V max ($I_L$ = 24 mA) |

The SPD (serial poll data) signal is the serial data from the master to the T564. The SRD (serial reply data) signal is the serial data from the T564 to the master. Logic input circuitry (SCLK, SPD) is a 1K series resistor, a 33pF capacitor to ground, and a 3.3V Schmitt trigger input. Logic output SRD is a 3.3V LVC series output.

At frequencies below the recommended maximum $f_{clk}$ of 5 MHz, a serial master may read SRD at the same time the rising edge of SCLK is generated and update SPD at the same time the falling edge of SCLK is generated with no timing concerns.

When no data is being transmitted, the data lines idle low. Data is transmitted in 8 bit frames, starting with a logic high start bit, then the data (MSB first), then a logic low stop bit. Data follows the same rules described in the Programming chapter of the manual, i.e. ASCII characters followed by a carriage return (0x0D) to mark the end of transmission. The T564 will process the commands normally, and respond with an ASCII string, terminated by a carriage return.

Four RS-232 port serial commands are provided to test the isochronous interface.

| | |
|---|---|
| **IS TX STRING** | send string to isoch transmit (reply) interface |
| **IS RX** | get string from isoch receive (poll) interface |
| **IS LO STRING** | isoch loopback test |
| | |
| **IBLOCK 1** | don't parse incoming isoch command strings |
| **IBLOCK 2** | send isoch receive (poll) data to the RS232 interface |
| **IBLOCK 256** | suppress all command reply data, isoch or RS232 |

The **IS TX TEXT** command sends the remainder of the line " TEXT" out the isoch transmit (reply) interface.

The **IS RX** command essentially empties the receive (poll) FIFO and sends any non-null bytes to the RS232 transmit interface. This allows inspection of the contents of the isoch receive buffer.

The **IS LO** command combines **IS TX** and **IS RX**.

Because the command parser is normally trying to absorb and execute commands coming into the isoch receive port, it can interfere with testing. The **IBLOCK 1** command will disable such parsing.

If a loopback tester is connected to the T564 isoch interface connector, one can set the **IBLOCK 1** state; now the command **IS TX HELLO** will send " HELLO" out, and a subsequent **IS RX** will fetch the looped-back " HELLO" string which will be returned by the RS232 interface.

The **IBLOCK 2** command will divert any characters that would normally go out the isoch transmit interface into the RS232 transmit port.

If a loopback tester is operating and the **IBLOCK 2** state is in effect, an RS232 command such as **IS TX ST** will loop back the " ST" into the isoch receive interface, the parser will interpret the command and generate the T564 status report, and the resulting report will be diverted to the RS232 port.

**IBLOCK 0** will restore normal operation. Any command error will clear the IBLOCK parameter.

The interface uses connector J14.

J14 pin 6 is the externally-generated clock SCLK, in the 1-5 MHz range

J14 pin 5 is command/poll data SPD to the T564

J14 pin 3 is reply data SRD from the T564

J14 pins 9 and 10 are ground.

Logic levels are 3.3 volt CMOS.

J14 pin 1 is at board coordinate X 1.770, Y 0.530. J14 pins are spaced at 0.1 inch centers. See fig 12.3.

With Autoinstall off, some typical command execution times, are, in microseconds,

```
AD 1                  102
AD 123.456N           164
AD                    160
AD 1;AW 1             198
AD 1.234M;AW 1.234M   370
DD 1                  116
QD 123.456U           202
IN                    312
QU                    312
FEOD                  74
FIRE                  72
CO                    72
TL 1.25               256
TL                    160
TS 1234               190
TS                    206
ST                    4.2 MSEC
ST                    230 MSEC RS232 OUTPUT
```

Each extra character in a command, beyond the required first two, adds about 6 microseconds to command execution.

# 12. Dimensions and Mounting

T564 mechanical dimensions are shown below. The evaluation T564 is furnished with the T566 mounting flange bolted to the bottom of the extruded enclosure to make it easier to install on mounting surfaces which do not have rear access.

The T564 may be mounted using the flange supplied, or the flange may be removed and the unit mounted with four 4-40 machine screws from below.

**CAUTION: Mounting screws may not penetrate more than 0.160 inches (4 mm) into the T564 enclosure.**

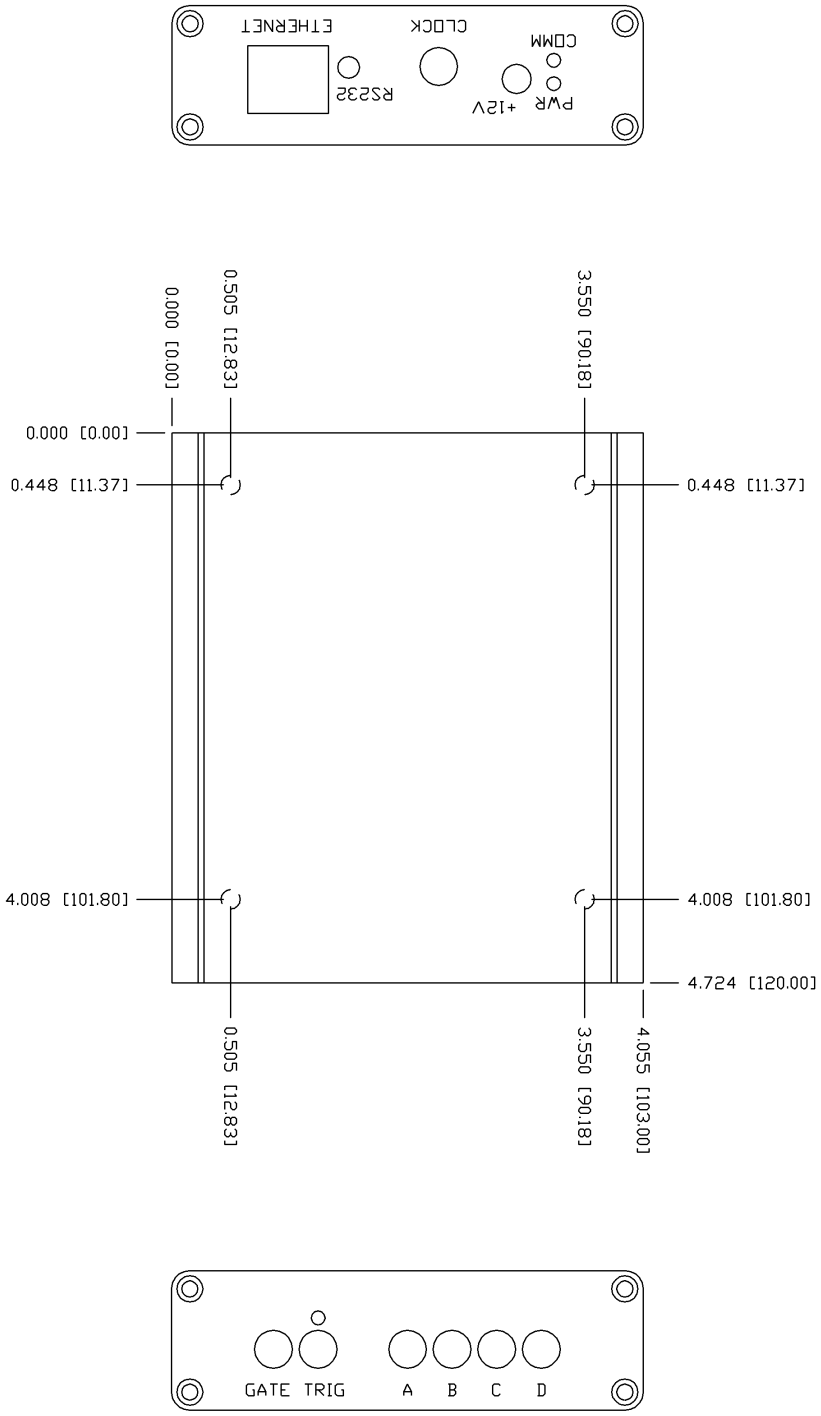



**Fig 12.1 T564 Outline and Mounting**

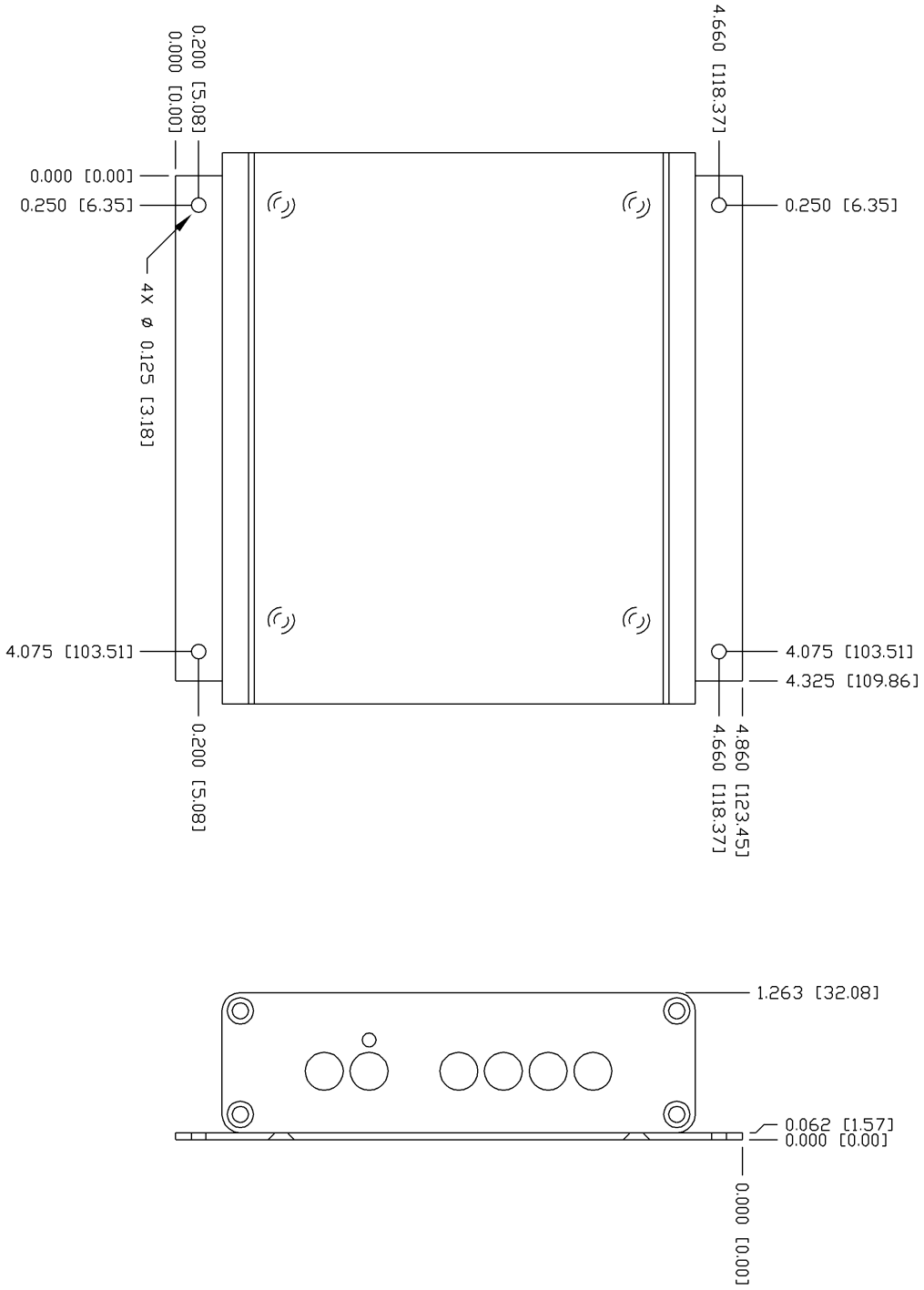



**Fig 12.2 Flange Mounting Dimensions**

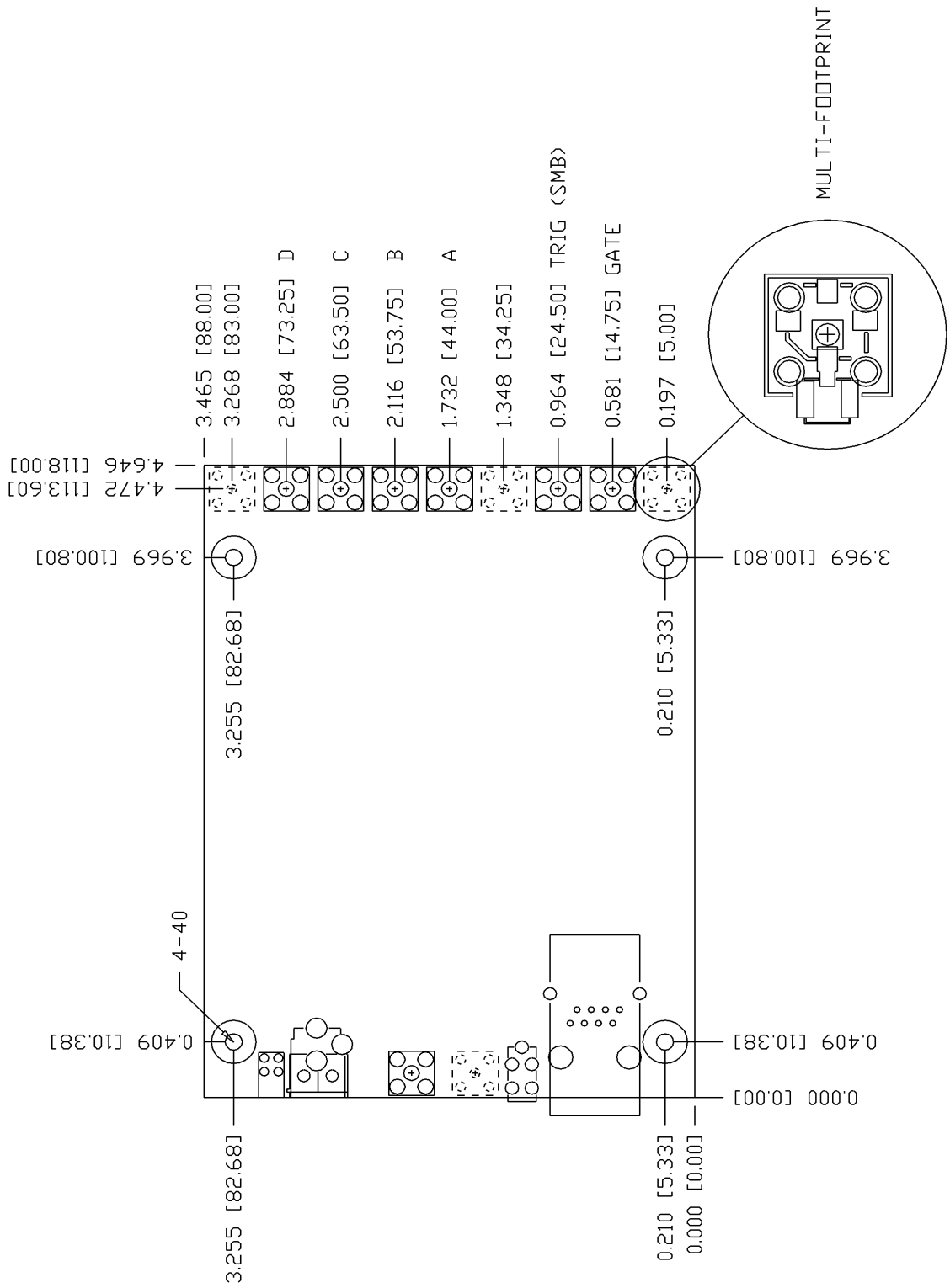
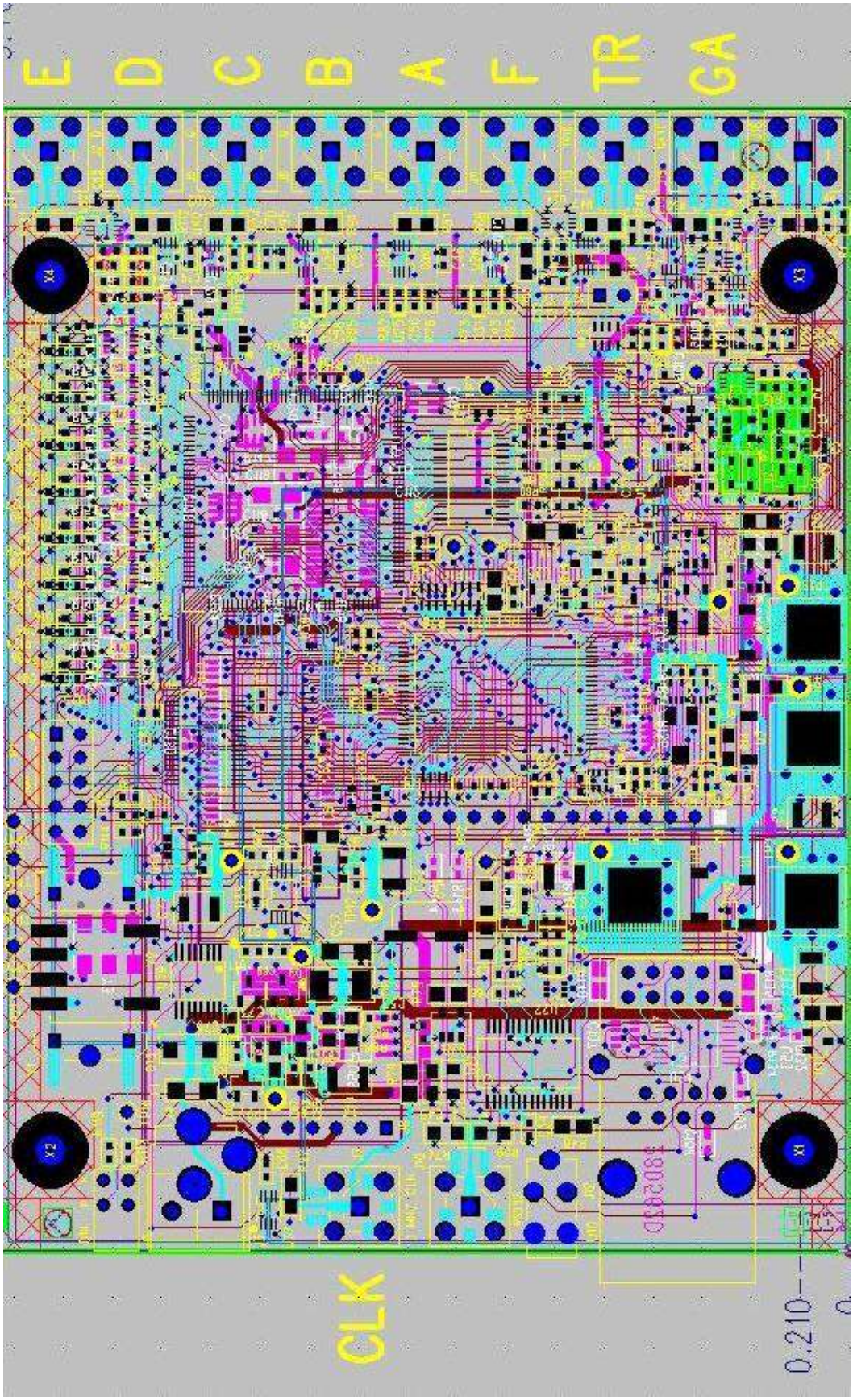



**Fig 12.3 Printed-Circuit Board Dimensions**


E D C B A F TR GA
CLK

# 13. Demo Software

Win560.EXE is a Windows program that communicates with the T564 using serial commands. Device settings are displayed on screen, and can be sent to the T564, or the current state of the T564 can be downloaded to the program and displated.

Communications access to the T564 is available via RS-232 or the Ethernet port.

Further information on running the program is available via the in-program Help screens. Win560 requires Windows 2000 or later.

# 14. Versions

T564-1: 4-channel compact advanced digital delay and pulse train generator with RS-232 interface

T564-2: 4-channel compact advanced digital delay and pulse train generator with RS-232 and Ethernet interface

T564-9: 4-channel compact advanced digital delay and pulse train generator Evaluation Kit (Includes 2 SMB cables, RS-232 interface, Ethernet interface, RS-232 cable, power supply, mounting flange, CD and manual)

# 15. Customization

Consult factory for information about additional custom versions.

# 16. Revision History

## 16.1 Hardware Revisions

| | |
|---|---|
| Revision J | January 2014<br>Replaced timing element with GaAsFETs to improve timing accuracy and reduce crosstalk between outputs. Increased insertion delay to 21 ns. Requires switch to 28A560 series firmware. |
| Revision H | February 2012<br>Improved manfacturability. Functionally equivalent to Revision A. |
| Revision G | December 2011<br>Improved manfacturability. Functionally equivalent to Revision A. |
| Revision F | December 2010<br>Replaced obsolete regulator package. Functionally equivalent to Revision A. |
| Revision E | July 2009<br>Improved manfacturability. Functionally equivalent to Revision A. |
| Revision D | May 2009<br>Renamed revision A to match major subassembly. Identical to revision A. |
| Revision A | May 2009<br>Initial production release. Insertion delay 20 ns. |

## 16.2 Firmware Revisions

| | |
|---|---|
| 28E560-B | August 2015<br>For hardware revisions J-K<br>Fixed bug with T564 identification on some models |
| 28E560-A | January 2014 – Hardware revision J.<br>Changed pinning to match new hardware. Improved timing calibration linearity. |
| 28E564-G | March 2011 – Hardware revision E-F<br>TRIGMON logic was changed to invert the output when a falling edge trigger is selected. |

| | |
|---|---|
| 28E564-F | December 2010 – Hardware revision E<br>FPGA changes fixed a problem that prevented powerup self-calibration if the optional J14 ARM input was pulled low.. |
| 28E564-E | February 2010 – Hardware revision E<br>Added frame looping logic. Corrected a number of minor issues were corrected. |
| 28E564-D | November 2009 – Hardware revision E<br>Fixed bug where settings loaded at powerup time were not properly installed. |
| 28E564-C | October 2009 – Hardware revision E<br>Removed requirement for trigger termination changes to be installed. Fixed frames conflict. Fixed isochronous communication debugging loops. |
| 28E564-B | Internal release only. |
| 28E564-A | March 2009 – Hardware revision A-D<br>Initial release. |

## 16.3 Accessories

J12 12 volt power supply

J14 International plug adapter set for J12

J53 3' SMB to BNC cable

J53-2 6" SMB to BNC cable

J720 single-channel compact electrical-to-fiberoptic converter

J724 single-channel compact buffered electrical-to-fiberoptic converter

J730 single-channel compact fiberoptic-to-electrical converter

J740 single-channel compact fast fiberoptic-to-electrical converter

T565 RS-232 cable

T566 Mounting flange

T750 4-channel compact high-voltage driver

T760 dual-channel compact high voltage optical-to-electrical converter

T860 single-channel compact logic buffer and driver

P730 dual 1:4 benchtop optical-to-electrical fanout buffer