GLADICOS IP

BRIF

GLADIC

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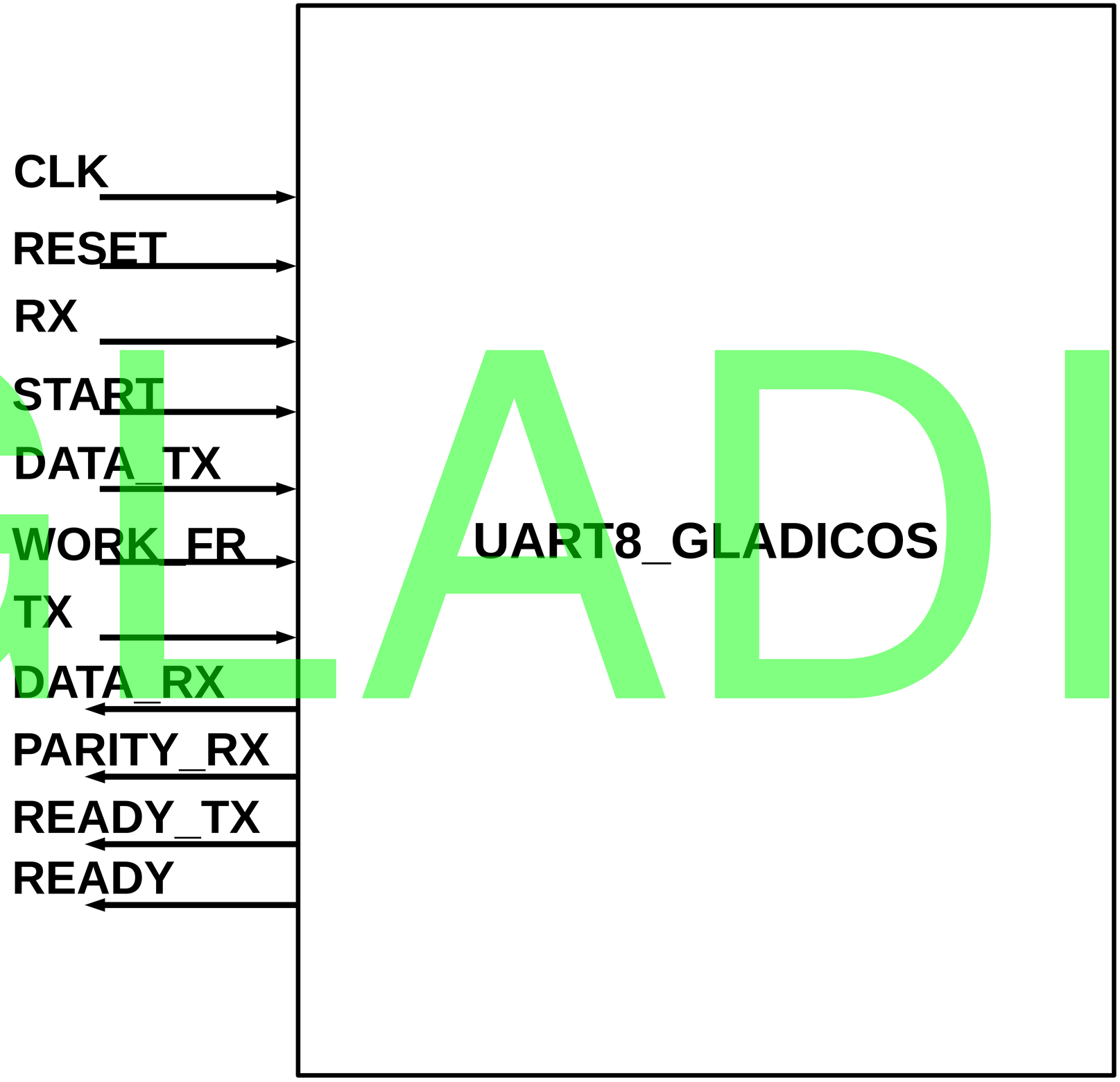
SUMMARY

- TOP BLOCK DIAGRAM
- TOP BLOCK PIN DESCRIPTION
- ENVIRONMENT DIAGRAM
- SYSTEMC MODEL
- USEFUL LINKS

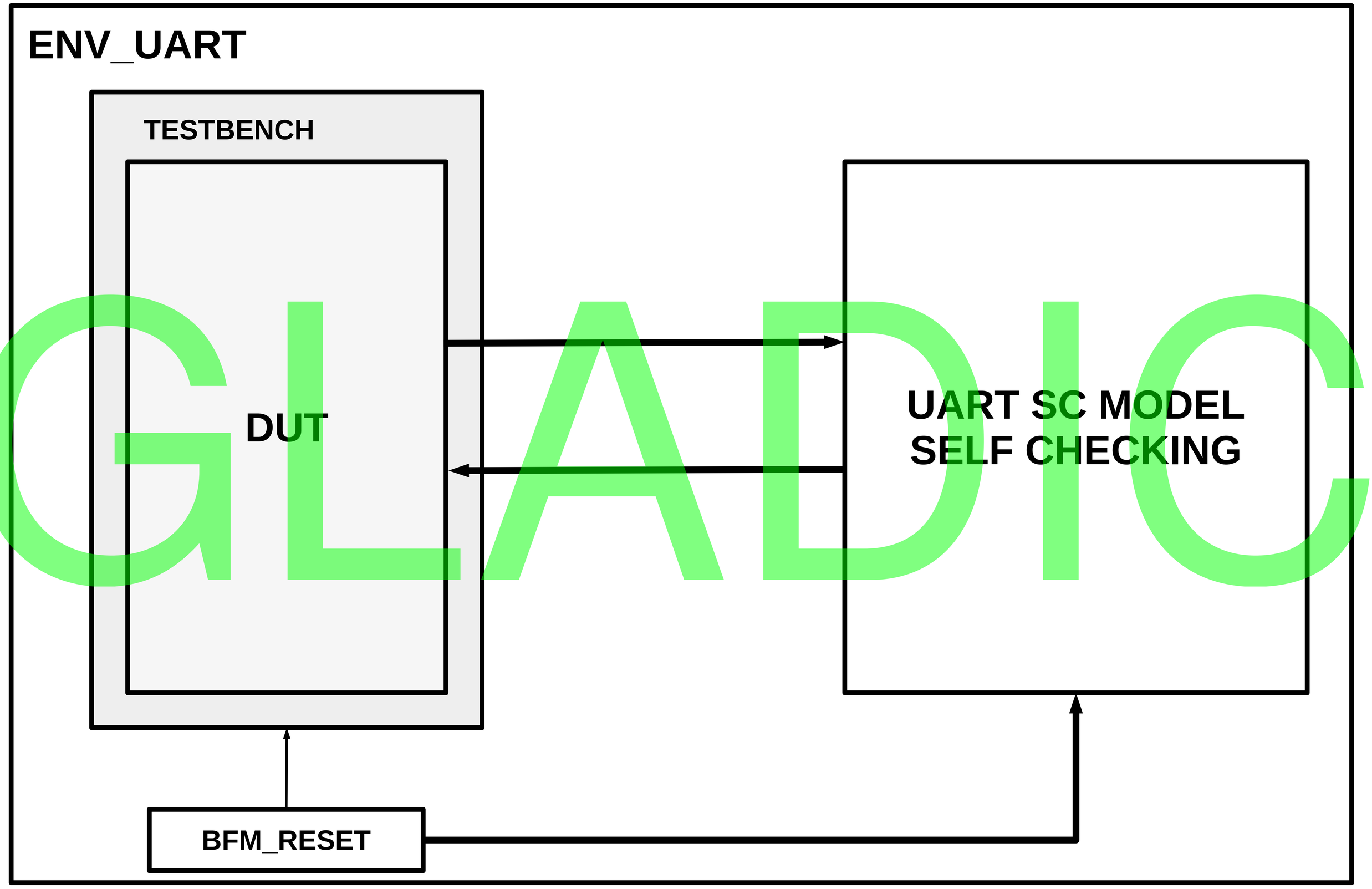
TOP BLOCK DIAGRAM



TOP BLOCK PIN DESCRIPTION

PIN DESCRIPTION			
PIN NAME	**DIRECTION**	**SIZE**	**DESCRIPTION**
CLK	INPUT	1	Posedge Clock
RESET	INPUT	1	Reset HIGH
RX	INPUT	1	Data input
START	INPUT	1	Start TX state machine after you set DATA_TX
DATA_TX	INPUT	8	Insert byte to be send to another device
WORK_FR	INPUT	12	Value seted in UART like a baud rate
TX	OUTPUT	1	Used to Transmit data
DATA_RX	OUTPUT	1	Data received from RX
PARITY_RX	OUTPUT	8	Parity received from RX
READY_TX	OUTPUT	1	This notice TX module finished transmit
READY	OUTPUT	1	This notice RX received data

ENVIRONMENT DIAGRAM



SYSTEMC MODEL

Check Description	
TEST	
SEND DATA	Data start in 1 and be incremented each final byte send
RECEIVE DATA	This receive data whit parity and check if data is correct with parity
PARITY	Check parity with data stored in previous with you get on RX
DATA CHECK	Check data stored in a vector is equal data received from RX

USEFUL LINKS

- **UART PC8250A**
- **UART TUTORIAL**
- **DIGILENT UART SPEC**
- **UART TUTORIAL 2**