Computer Architecture - Assignment 1

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Answer 1 -

Given L_2 cache,
no. of accesses per secs = 50000000=5*10^7
leakage power = 0.07W , Dynamic power = 0.8 * 10^9J/access
time of execution of application is 1 sec.
Leakage energy = 0.07J
And Dynamic Energy = (Dynamic power/access)*no. of accesses
$\implies$ Dynamic Energy = (0.8*10^-9)*(5*10^7)*1=0.04J
Total Energy = Dynamic + power = 0.04+0.07=0.11J
percent of leakage energy = ((0.07)*100)/(0.11)= 0.63

Answer 2 -

Reach Of TLB = (no. of entries)* Page size

Page size	Entries	Associativity	Reach
4KB	64	4-way	256KB
2MB	32	8-way	64MB
1GB	08	fully-associative	8GB

1 Answer 3 -

For Cache 1 : Sequence 1 -

Decimal	Binary	Tag	Set	Hit/Miss
0	00000000	000	0	Miss
63	00111111	001	7	Miss
1	00000001	000	0	Hit
62	00111110	001	7	Hit
2	00000010	000	0	Hit
61	00111101	001	7	Hit
3	00000011	000	0	Hit
60	00111100	001	7	Hit
4	00000100	000	1	Miss
59	00111011	001	6	Miss
5	00000101	000	1	Hit
58	00111010	001	6	Hit
6	00000110	000	1	Hit
57	00111001	001	6	Hit
7	00000111	000	1	Hit
56	00111000	001	6	Hit
8	00001000	000	2	Miss
55	00110111	001	5	Miss
9	00001001	000	2	Hit
54	00110110	001	5	Hit
10	00001010	000	2	Hit
53	00110101	001	5	Hit
11	00001011	000	2	Hit
52	00110100	001	5	Hit

Here,
Total no. of hits = 18
Total no. of misses =6
Hit Ratio = 18/24 = 3/4

For Cache 2 : Sequence 1 -

Decimal	Binary	Tag	Set	Hit/Miss
0	00000000	000	0	Miss
63	00111111	111	7	Miss
1	00000001	001	0	Miss
62	00111110	011	7	Miss
2	00000010	010	0	Miss
61	00111101	101	7	Miss
3	00000011	110	0	Miss
60	00111100	100	7	Miss
4	00000100	100	0	Miss
59	00111011	011	7	Miss
5	00000101	101	0	Miss
58	00111010	010	0	Miss
6	00000110	110	0	Miss
57	00111001	001	7	Miss
7	00000111	111	0	Miss
56	00111000	000	7	Miss
8	00001000	000	1	Miss
55	00110111	111	6	Miss
9	00001001	001	1	Miss
54	00110100	100	6	Miss
10	00001010	010	1	Miss
53	00110101	101	6	Miss
11	00001011	011	1	Miss
52	00110100	100	6	Miss

Total no. of hits = 0
Total no. of misses = 24
Hit Ratio = 0/24 = 0

For Cache1, sequence2

Decimal	Binary	Tag	Set	Hit/Miss
0	00000000	000	0	Miss
64	01000000	010	0	Miss
128	10000000	100	0	Miss
192	11000000	110	0	Miss
1	00000001	000	0	Miss
65	01000001	010	0	Miss
129	10000001	100	0	Miss
193	11000001	110	0	Miss
11	00001011	000	2	Miss
75	01001011	010	2	Miss
139	10001011	100	2	Miss
203	11001011	110	2	Miss
9	00001001	000	2	Miss
137	10001001	100	2	Miss
201	11001001	110	2	Miss
73	01001001	010	2	Miss

Number of Hits = 0,
Number of misses = 10
Hit Ratio = 0/16=0

For Cache2, sequence2

Decimal	Binary	Tag	Set	Hit/Miss
0	00000000	000	0	Miss
64	01000000	000	0	Hit
128	10000000	000	0	Hit
192	11000000	000	0	Hit
1	00000001	001	0	Miss
65	01000001	001	0	Hit
129	10000001	001	0	Hit
193	11000001	001	0	Hit
11	00001011	011	1	Miss
75	01001011	011	1	Hit
139	10001011	011	1	Hit
203	11001011	011	1	Hit
9	00001001	001	1	Miss
137	10001001	001	1	Hit
201	11001001	001	1	Hit
73	01001001	001	1	Hit

Number of Hits = 12,
Number of misses = 4
Hit Ratio = 12/16 =3/4

Answer 4 -

Here,
Freq. of P1 = 2.2GHz
Freq. of P2 = 1.6GHz
Total no. of instructions
For Class A = $2*10^5$
For Class B = $2.5*10^5$
For Class C = $4.5*10^5$
For Class D = $1*10^5$
Time Taken = $\sum_1^4$(no. of instructions)* CPI * $(\frac{1}{frequency})$
Time for P1 = 0.00113 sec
Time for P2 = 0.00125 sec Hence, P1 is Faster.

Answer 5.

No.	P0	P1	P2	P3	P5
1	1	0	0	0	0
2	0	1	0	0	1
3	0	0	0	1	1
4	0	0	1	1	0
5	0	0	1	0	1
6	1	0	1	0	0

Answer 6.

For application1: L2 cache misses with 2 and 6 ways (of last level cache) are 1000 and 400, respectively.
For application2: L2 cache misses with 2 and 6 ways (of last level cache) are 2000 and 1800, respectively
Let m1 and m2 be misses for Application 1 and Application 2 respt.

Let w1 and w2 be ways for Application 1 and Application 2 respt.
Now , Using Linear Interpolation,
m1=(-150)*w1 + 1300
m2 =(-50)*w2 + 2100
Now we assume w be the ways given to application 1, then for application 2 ways = 8-w
So to minimize the cache misses we have to minimize
(−150 * w + 1300) + (−50 * (8 − w) + 2100) = (3000 - 100* w)
w ranges from 2-6, the minimum of (3000 - 100* w) occur at w = 6
so application1 needs 6 ways and 2 for application2

Answer.7

Given the transaction rates, P = 34/min,
Q = 58/min,
R = 81/min
And They run sequentially.
Total no. of transactions = 500*3=1500
For average rate , we need Harmonic Mean
Let, x1=(500/rate-P)
x2=(500/rate-Q)
x3=(500/rate-R)

Av. Rate = $\frac{(No.of transactions)}{(x1+x2+x3)}$
$\implies$ 3/0.05899
the average rate is 50.856 transcation/minutes

Answer.8

Given, for system0
percentage of time for Initialization = 25/100,
percentage of time visual processing = 37/100
percentage of time signal processing = 38/100
Now, For System 1
SpeedUp in visual processing = 6X
SpeedUp in signal processing = 10X
SpeedUP of system 1 over system 0 = $\frac{1}{(1-time)+\frac{VP-time}{6}+\frac{SP-time}{10}}$
$\implies$ $\frac{1}{0.25+37/(6*100)+38/(10*100)}$ $\implies$ 100/34.966 $\implies$ SpeedUP = 2.8598

Answer.9

Given,
Frequency, f = 3GHz,
Volatage, v = 1V
dynamic power = 80W
leakage power = 30W
As relationship of voltage and frequency is linear,
(i) For smallest time, the frequency should be maximum,
for maximum corresponding volate 1.2V
max. frequency = $\frac{1.2}{1} \times 3 = 3.6$GHz
time = $\frac{3}{3.6} \times 30 = 25$s
(ii) Total power = Dynamic + leakage
dynamic power $\alpha voltage^2 \times capacitance \times activity \times frequency$
leakage power $\alpha voltage \times capacitance$ smallest allowed voltage = 0.8V, corresponding frequency = $\frac{0.8}{1} \times 3 = 2.4$GHz

fractional change in voltage and freq , x = $\frac{4}{5}$
new dynamic power = $80 \times (\frac{4}{5})^3 = 40.96$W
new leakage power = $30 \times \frac{4}{5} = 24$W
Total power = 40.96 + 24 = 64.96W
(iii) For minimum energy, minimum power multiplied by time

in this case changing frequency will not have any effect as it will be managed
by time.
time = 30s
Energy= $(80 \times x^2 + 30) \times time$
Energy = 2436J

Answer.10

Virtual Address size = 48 bit
Physical Memory = 2GB, Bytes required = 31
Page Size = 2KB , Bits required =11
Page offset = 11 bits
Hence ,bits required for page no = 31 - 11 = 20
Now considering 14 bits from virtual address also remains unchanged and the rest (48 - 11) bits are required for virtual to physical translation.
Now in TLB no. of bits per entry = 37 +20 =57
So, size of TLB = 57 *32 =228 bytes

Answer.11

The addresses -
0x4795BA21, 0x4795BB21, 0x5795BA21 and 0x4785BA21.
Here, in bit representation the last 10 bits are not used.
Addresses of 1st and 2nd are same , whereas of 3rd and 4th are different.
thus, total accesses =3.

Answer. 12

a) LRU :

address	Hit/Miss
A	Miss
B	Miss
C	Miss
D	Miss
A	Miss
B	Miss
C	Miss
D	Miss
A	Miss
B	Miss
C	Miss
D	Miss

b) MRU

address	Hit/Miss
A	Miss
B	Miss
C	Miss
D	Miss
A	Hit
B	Miss
C	Miss
D	Hit
A	Miss
B	Miss
C	Hit
D	Miss

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