STM32MP157A

Arm® dual Cortex®-A7 650 MHz + Cortex®-M4 MPU, 3D GPU, TFT/DSI, 37 comm. interfaces, 29 timers, adv. analog

Datasheet - production data

Features

Core

- 32-bit dual-core Arm® Cortex®-A7
  - L1 32-Kbyte I / 32-Kbyte D for each core
  - 256-Kbyte unified level 2 cache
  - Arm® NEON™ and Arm® TrustZone®
- 32-bit Arm® Cortex®-M4 with FPU/MPU
  - Up to 209 MHz (Up to 703 CoreMark®)

Memories

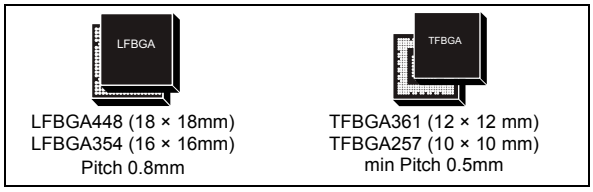
- External DDR memory up to 1 Gbyte
  - up to LPDDR2/LPDDR3-1066 16/32-bit
  - up to DDR3/DDR3L-1066 16/32-bit
- 708 Kbytes of internal SRAM: 256 Kbytes of AXI SYSRAM + 384 Kbytes of AHB SRAM + 64 Kbytes of AHB SRAM in Backup domain and 4 Kbytes of SRAM in Backup domain
- Dual mode Quad-SPI memory interface
- Flexible external memory controller with up to 16-bit data bus: parallel interface to connect external ICs and SLC NAND memories with up to 8-bit ECC

Security/safety

- TrustZone® peripherals, active tamper
- Cortex®-M4 resources isolation

Reset and power management

- 1.71 V to 3.6 V I/Os supply (5 V-tolerant I/Os)
- POR, PDR, PVD and BOR
- On-chip LDOs (RETRAM, BKPSRAM, DSI 1.2 V, USB 1.8 V, 1.1 V)
- Backup regulator (~0.9 V)
- Internal temperature sensors
- Low-power modes: Sleep, Stop and Standby
- LPDDR2/3 retention in Standby mode



LFBGA448 (18 × 18mm)
LFBGA354 (16 × 16mm)
Pitch 0.8mm

TFBGA361 (12 × 12 mm)
TFBGA257 (10 × 10 mm)
min Pitch 0.5mm

- Controls for PMIC companion chip

Low-power consumption

- Total current consumption down to 2 µA (Standby mode, no RTC, no LSE, no BKPSRAM, no RETRAM)

Clock management

- Internal oscillators: 64 MHz HSI oscillator, 4 MHz CSI oscillator, 32 kHz LSI oscillator
- External oscillators: 8-48 MHz HSE oscillator, 32.768 kHz LSE oscillator
- 6 × PLLs with fractional mode

General-purpose input/outputs

- Up to 176 I/O ports with interrupt capability
  - Up to 8 secure I/Os
  - Up to 6 Wakeup, 3 tampers, 1 active tamper

Interconnect matrix

- 2 bus matrices
  - 64-bit Arm® AMBA® AXI interconnect, up to 266 MHz
  - 32-bit Arm® AMBA® AHB interconnect, up to 209 MHz

3 DMA controllers to unload the CPU

- 48 physical channels in total
- 1 × high-speed general-purpose master direct memory access controller (MDMA)

- 2 × dual-port DMAs with FIFO and request router capabilities for optimal peripheral management

Up to 37 communication peripherals

- 6 × I^2C FM+ (1 Mbit/s, SMBus/PMBus)
- 4 × UART + 4 × USART (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, SPI slave)
- 6 × SPI (50 Mbit/s, including 3 with full duplex I^2S audio class accuracy via internal audio PLL or external clock)
- 4 × SAI (stereo audio: I^2S, PDM, SPDIF Tx)
- SPDIF Rx with 4 inputs
- HDMI-CEC interface
- MDIO Slave interface
- 3 × SDMMC up to 8-bit (SD / *e*•MMC™ / SDIO)
- 2 × CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TTCAN)
- 2 × USB 2.0 high-speed Host + 1 × USB 2.0 full-speed OTG simultaneously
  - or 1 × USB 2.0 high-speed Host + 1 × USB 2.0 high-speed OTG simultaneously
- 10/100M or Gigabit Ethernet GMAC
  - IEEE 1588v2 hardware, MII/RMII/GMII/RGMII
- 8- to 14-bit camera interface up to 140 Mbyte/s

6 analog peripherals

- 2 × ADCs with 16-bit max. resolution (12 bits up to 4.5 Msps, 14 bits up to 4 Msps, 16 bits up to 3.6 Msps)
- 1 × temperature sensor
- 2 × 12-bit D/A converters (1 MHz)
- 1 × digital filters for sigma delta modulator (DFSDM) with 8 channels/6 filters
- Internal or external ADC/DAC reference V_{REF+}

Graphics

- 3D GPU: Vivante® - OpenGL® ES 2.0
  - Up to 26 Mtriangle/s, 133 Mpixel/s
- LCD-TFT controller, up to 24-bit // RGB888
  - up to WXGA (1366 × 768) @60 fps
  - Two layers with programmable colour LUT
- MIPI® DSI 2 data lanes up to 1 GHz each

Up to 29 timers and 3 watchdogs

- 2 × 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2 × 16-bit advanced motor control timers
- 10 × 16-bit general-purpose timers (including 2 basic timers without PWM)
- 5 × 16-bit low-power timers
- RTC with sub-second accuracy and hardware calendar
- 2 × 4 Cortex®-A7 system timers (secure, non-secure, virtual, hypervisor)
- 1 × SysTick M4 timer
- 3 × watchdogs (2 × independent and window)

Hardware acceleration

- HASH (MD5, SHA-1, SHA224, SHA256), HMAC
- 2 × true random number generator (3 oscillators each)
- 2 × CRC calculation unit

Debug mode

- Arm® CoreSight™ trace and debug: SWD and JTAG interfaces
- 8-Kbyte embedded trace buffer

3072-bit fuses including 96-bit unique ID, up to 1184-bit available for user

All packages are ECOPACK2 compliant

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32MP157A microprocessors.

This document should be read in conjunction with the STM32MP157 reference manual (RM0436), available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-A7 and Cortex®-M4 cores, refer to the Cortex®-A7 and Cortex®-M4 *Technical Reference Manuals*.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32MP157A devices are based on the high-performance dual-core Arm® Cortex®-A7 32-bit RISC core operating at up to 650 MHz. The Cortex-A7 processor includes a 32-Kbyte L1 instruction cache for each CPU, a 32-Kbyte L1 data cache for each CPU and a 256-Kbyte level2 cache. The Cortex-A7 processor is a very energy-efficient application processor designed to provide rich performance in high-end wearables, and other low-power embedded and consumer applications. It provides up to 20% more single thread performance than the Cortex-A5 and provides similar performance than the Cortex-A9.

The Cortex-A7 incorporates all features of the high-performance Cortex-A15 and Cortex-A17 processors, including virtualization support in hardware, NEON™, and 128-bit AMBA®4 AXI bus interface.

The STM32MP157A devices also embed a Cortex® -M4 32-bit RISC core operating at up to 209 MHz frequency. Cortex-M4 core features a floating point unit (FPU) single precision which supports Arm® single-precision data-processing instructions and data types. The Cortex® -M4 supports a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32MP157A devices also embed a 3D graphic processing unit (Vivante® - OpenGL® ES 2.0) running at up to 533 MHz, with performances up to 26 Mtriangle/s, 133 Mpixel/s.

The STM32MP157A devices provide an external SDRAM interface supporting external memories up to 8-Gbit density (1 Gbyte), 16 or 32-bit LPDDR2/LPDDR3 or DDR3/DDR3L up to 533 MHz.

The STM32MP157A devices incorporate high-speed embedded memories with 708 Kbytes of Internal SRAM (including 256 Kbytes of AXI SYSRAM, 3 banks of 128 Kbytes each of AHB SRAM, 64 Kbytes of AHB SRAM in backup domain and 4 Kbytes of SRAM in backup domain), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, a 32-bit multi-AHB bus matrix and a 64-bit multi layer AXI interconnect supporting internal and external memories access.

All the devices offer two ADCs, two DACs, a low-power RTC, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG). The devices support six digital filters for external sigma delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Six I^2Cs
  - Four USARTs and four UARTs
  - Six SPIs, three I^2Ss full-duplex master/slave. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIF Rx interface
  - Management data input/output slave (MDIOS)
  - Three SDMMC interfaces
  - An USB high-speed Host with two ports two high-speed PHYs and a USB OTG high-speed with full-speed PHY or high-speed PHY shared with second port of USB Host.
  - Two FDCAN interface, including one supporting TTCAN mode
  - A Gigabit Ethernet interface
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A DSI Host interface.

Refer to *Table 1: STM32MP157A features and peripheral counts* for the list of peripherals available on each part number.

A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32MP157A devices are proposed in 4 packages ranging from 257 to 448 balls with pitch 0.5 mm to 0.8 mm. The set of included peripherals changes with the device chosen.

These features make the STM32MP157A suitable for a wide range of consumer, industrial, white goods and medical applications.

shows the general block diagram of the device family.

Table 1. STM32MP157A features and peripheral counts

Features			STM32MP157AADxx TFBGA257	STM32MP157AABxx LFBGA354	STM32MP157AACxx TFBGA361	STM32MP157AAAxx LFBGA448	Miscella-neous
Package		Body size (mm)	10x10	16x16	12x12	18x18	-
		Pitch (mm)	0.5(1)	0.8	0.5(1)	0.8	
		Ball size (mm)	0.30	0.40	0.30	0.40	
		Thickness (mm)	<1.2	<1.4	<1.2	<1.4	
		Ball count	257	354	361	448	
CPU			Dual-core Cortex-A7 FPU Neon TrustZone				-
		Caches size	2 × 32-Kbyte L1 data cache				
			2 × 32-Kbyte L1 instruction cache				
			256-Kbyte level 2 unified coherent cache				
		Frequency	2 × 650 MHz				
GPU			Vivante - Open GL ES 2.0				-
for 3D graphics		Frequency	533 MHz				
MCU core			Cortex-M4 FPU				-
		Frequency	209 MHz				
ROM			128 Kbytes (secure)				-
Embedded SRAM		CPU system	256 Kbytes (securable)				708 Kbytes
		MCU subsystem	384 Kbytes				
		MCU retention	64 Kbytes				
		Backup	4 Kbytes (securable, tamper protected)				
SDRAM (securable)	LPDDR2/3	16-bit 533 MHz	Up to 1 Gbyte, single rank	-	Up to 1 Gbyte, single rank	-	-
		32-bit 533 MHz	-	-		-	
	DDR3/3L	16-bit 533 MHz	Up to 1 Gbyte, single rank				
		32-bit 533 MHz	-	-			
Backup registers			128 bytes (32x32-bit, securable, tamper protected)				-
Timers	Advanced	16 bits	2				29 timers
	General purpose	16 bits	8				
		32 bits	2				
	Basic	16 bits	2				
	Low power	16 bits	5				
	A7 timers	64 bits	2 × 4 (secure, non-secure, virtual, hypervisor)				
	M4 SysTick	24 bits	1				
	RTC/AWU		1 (securable)				

Table 1. STM32MP157A features and peripheral counts (continued)

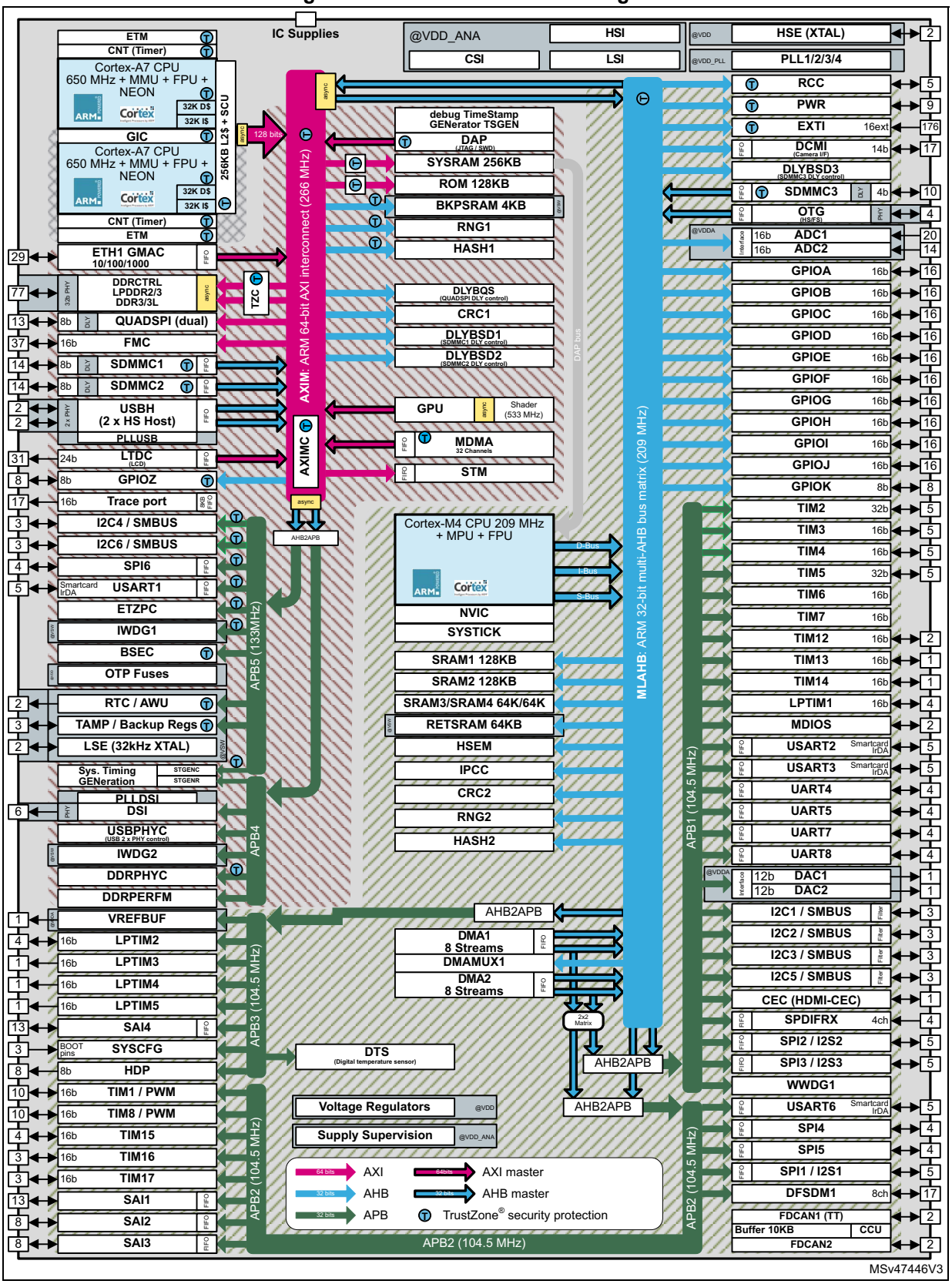
Features			STM32MP157 AADxx TFBGA257	STM32MP157 AABxx LFBGA354	STM32MP157 AACxx TFBGA361	STM32MP157 AAAxx LFBGA448	Miscella-neous
Watchdog			3 (independent, independent secure, window)				-
Communication peripherals	SPI		6 (1 securable)				-
		Having I2S	3				
	I2C (with SMB/PMB support)		6 (2 securable)				-
	USART (smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + 4 (including 1 securable USART) some can be a boot source				Boot
	SAI		4 (up to 8 audio channels), with I2S master/slave, PCM input, SPDIF-TX				Boot
	USB	EHCI/OHCI Host	2 ports				-
			Embedded HS PHY with BCD				-
		OTG HS/FS (dual role port)	Yes, embedded FS or HS PHY with BCD, can be a boot source				Boot
		Embedded PHYs	3 (2 × high-speed + 1 × full-speed)				-
	SPDIF-RX		4 inputs				-
	FDCAN		2 (1 × TTCAN), clock calibration, 10 Kbyte shared buffer				-
	HDMI-CEC		1				-
	Including the following securable		1 × USART, 1 × SPI, 2 × I2C		1 × USART, 1 × SPI, 2 × I2C on securable GPIOs		-
SDMMC (SD, SDIO, *e*•MMC)			3 (8 + 8 + 4 bits), *e*•MMC or SD can be a boot source				Boot
QuadSPI			Yes (dual-quad), can be a boot source				Boot
FMC	Parallel address/data 8/16-bit		-		4 × CS, up to 4 × 64 Mbyte		No boot
	Parallel AD-Mux 8/16-bit		4 × CS, up to 4 × 64 Mbytes				
	NAND 8/16-bit		Yes, 1 × CS, SLC, BCH4/8, can be a boot source				Boot
Gigabit Ethernet			-		MII, RMII, GMII, RGMII with PTP and EEE		-
10/100M Ethernet			MII, RMII with PTP and EEE				
LCD-TFT		Parallel interface	up to 24-bit data (up to 1366×768 60 fps)				-
Display serial interface (DSI)			2 × data lanes 1 GHz each (up to 1366×768 60 fps)				-
DMA			3 instances (1 securable), 48 physical channels in total				-
Hash			SHA-256, MD5, HMAC dual instances (secure and non-secure)				-
True random number generator			True-RNG, dual instances (secure and non-secure)				-
Fuses (one-time programmable)			3072 effective bits (secure, >1500 bits available for user)				-
Camera interface		Bus width	14-bit				-

Table 1. STM32MP157A features and peripheral counts (continued)

Features		STM32MP157 AADxx TFBGA257	STM32MP157 AABxx LFBGA354	STM32MP157 AACxx TFBGA361	STM32MP157 AAAxx LFBGA448	Miscella-neous
GPIOs with interrupt (total count)		98		148	176	-
	Securable GPIOs	-		8		
	Wakeup pins	4		6		
	Tamper pins (active tamper)	2 (1)		3 (1)		
DFSDM		8 input channels with 6 filters				-
Up to 16-bit synchronized ADC		2 (up to 3.6/4/4.5/5/6 Msps on 16/14/12/10/8-bit each)				-
	Low noise 16 bit (differential)	-		2 (1)		
	16 bit (differential)	17 (4)		20 (4)		
	ADC channels in total(2)	17		22		
12-bit DAC		2				-
Internal ADC/DAC VREF		1.5 V, 1.8 V, 2.048 V, 2.5 V or VREF+ input				-
	VREF+ input pin	Yes				

1. With inner matrix balls having 0.65 mm pitch to allow optimized PCB routing for supplies.
2. In addition, there is also 6 internal channels for temperature, internal voltage reference, V_{DDCORE}, $V_{BAT}/4$, DAC1 or DAC2 acquisitions.

Figure 1. STM32MP157A block diagram



3 Functional overview

3.1 Dual-core Arm® Cortex®-A7 subsystem

3.1.1 Features

- ARMv7-A architecture
- 32-Kbyte L1 instruction cache for each CPU
- 32-Kbyte L1 data cache for each CPU
- 256-Kbyte level2 cache
- Arm® + Thumb®-2 instruction set
- Arm® TrustZone® security technology
- Arm® NEON™ Advanced SIMD
- DSP and SIMD extensions
- VFPv4 floating-point
- Hardware virtualization support
- Embedded trace module (ETM)
- Integrated generic interrupt controller (GIC) with 256 shared peripheral interrupts
- Integrated generic timer (CNT)

3.1.2 Overview

The Cortex-A7 processor is a very energy-efficient applications processor designed to provide rich performance in high-end wearables, and other low-power embedded and consumer applications. It provides up to 20 % more single thread performance than the Cortex-A5 and provides similar performance than the Cortex-A9.

The Cortex-A7 incorporates all features of the high-performance Cortex-A15 and Cortex-A17 processors, including virtualization support in hardware, NEON™, and 128-bit AMBA®4 AXI bus interface.

The Cortex-A7 processor builds on the energy-efficient 8-stage pipeline of the Cortex-A5 processor. It also benefits from an integrated L2 cache designed for low-power, with lower transaction latencies and improved OS support for cache maintenance. On top of this, there is improved branch prediction and improved memory system performance, with 64-bit load-store path, 128-bit AMBA 4 AXI buses and increased TLB size (256 entry, up from 128 entry for Cortex-A9 and Cortex-A5), increasing performance for large workloads such as web browsing.

Thumb-2 technology

Delivers the peak performance of traditional Arm® code while also providing up to a 30 % reduction in memory requirement for instructions storage.

TrustZone technology

Ensures reliable implementation of security applications ranging from digital rights management to electronic payment. Broad support from technology and industry partners.

NEON

NEON technology can accelerate multimedia and signal processing algorithms such as video encode/decode, 2D/3D graphics, gaming, audio and speech processing, image processing, telephony, and sound synthesis. The Cortex-A7 provides an engine that offers both the performance and functionality of the Cortex-A7 floating-point unit (FPU) and an implementation of the NEON advanced SIMD instruction set for further acceleration of media and signal processing functions. The NEON extends the Cortex-A7 processor FPU to provide a quad-MAC and additional 64-bit and 128-bit register set supporting a rich set of SIMD operations over 8-, 16- and 32-bit integer and 32-bit floating-point data quantities.

Hardware virtualization

Highly efficient hardware support for data management and arbitration, whereby multiple software environments and their applications are able to simultaneously access the system capabilities. This enables the realization of devices that are robust, with virtual environments that are well isolated from each other.

Optimized L1 caches

Performance and power optimized L1 caches combine minimal access latency techniques to maximize performance and minimize power consumption. There is also the option of cache coherence for enhanced inter-processor communication, or support of a rich SMP capable OS for simplified multicore software development.

Integrated L2 cache controller

Provides low-latency and high-bandwidth access to cached memory in high-frequency, or to reduce the power consumption associated with off-chip memory access.

Cortex-A7 floating-point unit (FPU)

The FPU provides high-performance single and double precision floating-point instructions compatible with the Arm VFPv4 architecture that is software compatible with previous generations of Arm floating-point coprocessor.

Snoop control unit (SCU)

The SCU is responsible for managing the interconnect, arbitration, communication, cache to cache and system memory transfers, cache coherence and other capabilities for the processor.

This system coherence also reduces software complexity involved in maintaining software coherence within each OS driver.

Generic interrupt controller (GIC)

Implementing the standardized and architected interrupt controller, the GIC provides a rich and flexible approach to inter-processor communication and the routing and prioritization of system interrupts.

Supporting up to 288 independent interrupts, under software control, each interrupt can be distributed across A7 cores, hardware prioritized, and routed between the operating system and TrustZone software management layer.

This routing flexibility and the support for virtualization of interrupts into the operating system, provides one of the key features required to enhance the capabilities of a solution utilizing a hypervisor.

3.2 Arm® Cortex®-M4 with FPU

The Arm® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

Memory protection unit (MPU)

The memory protection unit (MPU) manages the Cortex®-M4 access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows the definition of up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Graphic processing unit (GPU)

The STM32MP157A includes a 3D graphics engine (Vivante).

The GPU is a dedicated graphics processing unit accelerating numerous 3D graphics applications such as graphical user interface (GUI), menu display or animations.

It works together with an optimized software stack design for industry-standard APIs with support for Android™ and Linux® embedded development platforms.

Hardware features:

- OpenGL ES 2.0 / 1.1 compliance, including extensions; OpenVG 1.1
- IEEE 32-bit floating-point pipeline
- Ultra-threaded, unified vertex and fragment (pixel) shaders
- Low memory bandwidth at both high and low data rates
- Low CPU loading
- Up to 12 programmable elements per vertex
- Dependent texture operation with high-performance
- Alpha blending
- Depth and stencil compare
- Support for 8 fragment shader simultaneous textures
- Support for 4 vertex shader simultaneous textures
- Point sampling, bi-linear sampling, tri-linear filtering, and cubic textures
- 8 k x 8 k texture size and 8 k x 8 k rendering target
- 4 Vertex DMA streams

API support:

- OpenGL ES 1.1 and 2.0
- OpenVG 1.1
- EGL 1.4
- OpenGL 2.1

Performance up to:

- 26 Mtriangle/s
- 133 Mpixel/s

3.4 Memories

3.4.1 External SDRAM

The STM32MP157A devices embed a controller for external SDRAM which support the following devices

- LPDDR2 or LPDDR3, 16- or 32-bit data, up to 1 Gbyte, up to 533 MHz clock.
- DDR3 or DDR3L, 16- or 32-bit data, up to 1 Gbyte, up to 533 MHz clock.

3.4.2 Embedded SRAM

All devices feature:

- SYSRAM in MPU domain: 256 Kbytes
- SRAM1 in MCU domain: 128 Kbytes
- SRAM2 in MCU domain: 128 Kbytes
- SRAM3 in MCU domain: 64 Kbytes
- SRAM4 in MCU domain: 64 Kbytes
- RETRAM (retention RAM): 64 Kbytes

  The content of this area can be retained in Standby or V_{BAT} mode.
- BKPSRAM (backup SRAM): 4 Kbytes

  The content of this area is protected against possible unwanted write accesses, and can be retained in Standby or V_{BAT} mode.

  BKPSRAM can be defined (in ETZPC) as accessible by secure software only.

3.5 DDR3/DDR3L/LPDDR2/LPDDR3 controller (DDRCTRL)

DDRCTRL combined with DDRPHYC provides a complete memory interface solution for DDR memory subsystem.

- Two 64-bit AMBA 4 AXI4 ports interface (XPI)
- AXI clock asynchronous to the controller
- Supported standards:
  - JEDEC DDR3 SDRAM specification, JESD79-3E for DDR3/3L with 32-bit interface
  - JEDEC LPDDR2 SDRAM specification, JESD209-2E for LPDDR2 with 32-bit interface
  - JEDEC LPDDR3 SDRAM specification, JESD209-3B for LPDDR3 with 32-bit interface
- Advanced scheduler and SDRAM command generator
- Programmable full data width (32-bit) or half data width (16-bit)
- Advanced QoS support with 3 traffic class on read and 2 traffic classes on write
- Options to avoid starvation of lower priority traffic
- Guaranteed coherency for write-after-read (WAR) and read-after-write (RAW) on AXI ports
- Programmable support for burst length options (4, 8,16)
- Write combine to allow multiple writes to the same address to be combined into a single write
- Single rank configuration
- Supports automatic SDRAM power-down entry and exit caused by lack of transaction arrival for programmable time
- Supports automatic clock stop (LPDDR2/3) entry and exit caused by lack of transaction arrival
- Supports automatic low power mode operation caused by lack of transaction arrival for programmable time via hardware low power interface
- Programmable paging policy
- Supports automatic or under software control self-refresh entry and exit
- Support for deep power-down entry and exit under software control (LPDDR2)
- Support for explicit SDRAM mode register updates under software control
- Flexible address mapper logic to allow application specific mapping of row, column, bank bits
- User-selectable refresh control options
- DDRPERFM associated block to help for performance monitoring and tuning

DDRCTRL and DDRPHYC can be defined (in ETZPC) as accessible by secure software only.

3.6 TrustZone address space controller for DDR (TZC)

TZC is used to filter read/write accesses to DDR controller according to TrustZone rights and according to non-secure master (NSAID) on up to 9 programmable regions.

- Configuration is supported by trusted software only
- 2 filter units working concurrently
- 9 regions:
  - region 0 is always enabled and covers the whole address range.
  - regions 1 to 8 have programmable base/end address and can be assigned to any one or both filters.
- Secure and non-secure access permissions programmed per region
- Non-secure accesses are filtered according to NSAID
- Regions controlled by same filter must not overlap
- Fail modes with error and/or interrupt
- Acceptance capability = 256
- Gate keeper logic to enable and disable of each filter
- Speculative accesses

3.7 Boot modes

At startup, the boot source used by the internal BootROM is selected by the BOOT pin and OTP bytes.

Table 2. Boot modes

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB(1)	Wait incoming connection on: – USART2/3/6 and UART4/5/7/8 on default pins – USB high-speed device(2)
0	0	1	Serial NOR Flash(3)	Serial NOR Flash on QUADSPI(4)
0	1	0	*e*•MMC(3)	*e*•MMC on SDMMC2 (default)(4)(5)
0	1	1	NAND Flash(3)	SLC NAND Flash on FMC
1	0	0	Reserved (NoBoot)	Used to get debug access without boot from Flash memory
1	0	1	SD card(3)	SD card on SDMMC1 (default)(4)(5)
1	1	0	UART and USB(1)(3)	Wait incoming connection on: – USART2/3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins(2)
1	1	1	Serial NAND Flash(3)	Serial NAND Flash on QUADSPI(4)

1. can be disabled by OTP settings.
2. USB requires 24 MHz HSE clock/crystal if OTP is not programmed for different frequency.
3. Boot source can be changed by OTP settings (e.g. initial boot on SD card, then *e*•MMC with OTP settings).
4. Default pins can be altered by OTP.
5. Alternatively, another SDMMC1 or SDMMC2 interface than this default can be selected by OTP.

3.8 Power supply management

3.8.1 Power supply scheme

- The V_{DD} is the main supply for I/Os and internal part kept powered during Standby mode. Useful voltage range is 1.71 V to 3.6 V (e.g. 1.8 V, 2.5 V, 3.0 V or 3.3 V typ.)
  - V_{DD_DSI}, V_{DD_PLL} and V_{DD_ANA} must be star-connected to V_{DD}.
- The V_{DDCORE} is the main digital voltage and is usually shutdown during Standby mode. Voltage range is 1.18 V to 1.25 V (1.2 V typ.).
- The VBAT pin can be connected to the external battery (1.2 V < V_{BAT} < 3.6 V). If no external battery is used, it is mandatory to connect this pin to V_{DD}.
- The VDDA pin is the analog (ADC/DAC/VREF), supply voltage range is 1.71 V to 3.6 V. DAC can only be used when V_{DDA} is above or equal 1.8 V. Using Internal V_{REF+} requires V_{DDA} equal to or higher than V_{REF+} + 0.3 V.
- The VDDA1V8_REG pin is the output of internal regulator and connected internally to USB PHY and USB PLL. Internal V_{DDA1V8_REG} regulator is enabled by default and can be controlled by software. It is always shut down during Standby mode.

  There is specific BYPASS_REG1V8 pin that must be connected either to V_{SS} or V_{DD} to activate or deactivate the voltage regulator. It is mandatory to bypass the 1.8 V regulator when V_{DD} is below 2.25 V (BYPASS_REG1V8 = $V_{DD)}$. In that case, VDDA1V8_REG pin must be connected to V_{DD} (if below 1.98 V) or to a dedicated 1.65 V - 1.98 V supply (1.8 V typ.).
- V_{DDA1V8_DSI} is the analog DSI supply. Voltage range is 1.65 V to 1.98 V. (1.8 V typ.) Should be connected to V_{DDA1V8_REG}.
- VDDA1V1_REG pin is the output of internal regulator connected internally to USB PHY. Internal V_{DDA1V1_REG} regulator is enabled by default and can be controlled by software. It is always shut down during Standby mode.
- VDDA1V2_DSI_REG pin is the output of internal regulator and connected internally to DSI PLL.
- $V_{DDA1V2\_DSI\_PHY}$ is the analog DSI PHY supply and should be connected to $V_{DDA1V2\_DSI\_REG}$.
- V_{DD3V3_USBHS} and V_{DD3V3_USBFS} are respectively the USB high-speed and full-speed PHY supply. Voltage range is 3.07 V to 3.6 V. V_{DD3V3_USBFS} is used to supply VBUS and ID pins. So, V_{DD3V3_USBFS} must be supplied as well when USB high-speed OTG device is used. If not used, must be connected to V_{DD}.

Caution: V_{DD3V3_USBHS} must not be present unless V_{DDA1V8_REG} is present, otherwise permanent STM32MP157A damage could occur. Must be ensured by PMIC ranking order or with external component in case of discrete component power supply implementation.

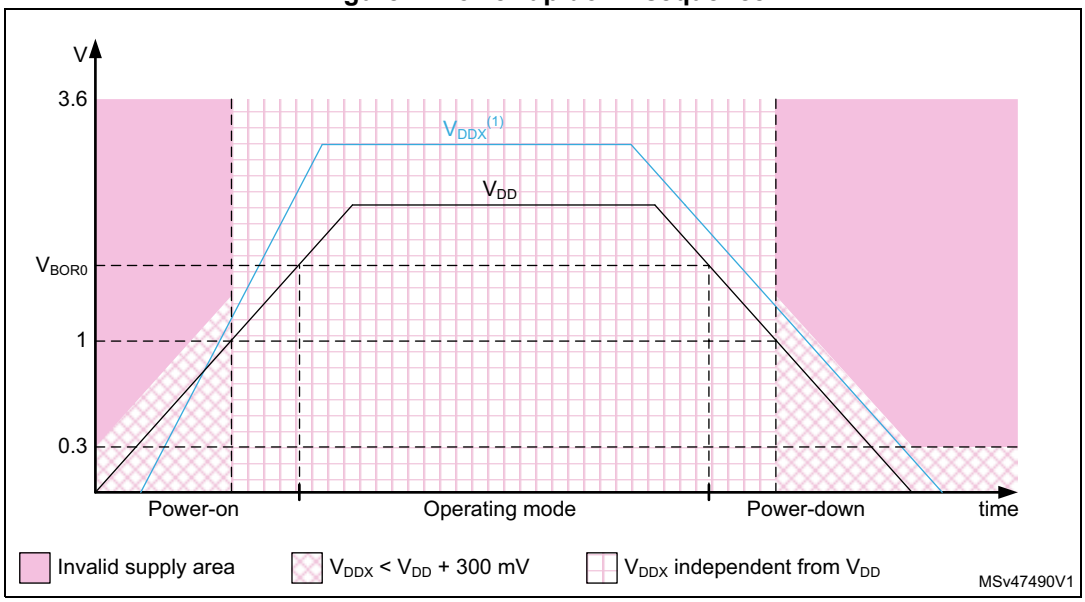
- V_{DDQ_DDR} is the DDR IO supply.
  - Voltage range is 1.425 V to 1.575 V for interfacing DDR3 memories (1.5 V typ.).
  - Voltage range is 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typ.).
  - Voltage range is 1.14 V to 1.3 V for interfacing LPDDR2 or LPDDR3 memories (1.2 V typ.).

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDCORE}, V_{DDA}, V_{DDA1V8_REG}, V_{DDA1V8_DSI}, V_{DDA1V1_REG}, $V_{DD3V3\_USBHS/FS}$, V_{DDQ_DDR}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the STM32MP157A device remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase.

Figure 2. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDCORE}, V_{DDA}, V_{DDA1V8_REG}, V_{DDA1V8_DSI}, V_{DDA1V1_REG}, $V_{DD3V3\_USBHS/FS}$, V_{DDQ_DDR}.

3.8.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

- Power-on reset V_{DDCORE} (POR_VDDCORE)

  The POR_VDDCORE supervisor monitors V_{DDCORE} power supply and compares it to a fixed threshold. The V_{DDCORE} domain remain in reset mode when V_{DDCORE} is below this threshold,

- Power-down reset V_{DDCORE} (PDR_VDDCORE)

  The PDR_VDDCORE supervisor monitors V_{DDCORE} power supply. A V_{DDCORE} domain reset is generated when V_{DDCORE} drops below a fixed threshold.

  The PDR_VDDCORE supervisor can be enabled/disabled through PDR_ON_CORE pin.

3.9 Low-power strategy

There are several ways to reduce power consumption on STM32MP157A:

- Decrease dynamic power consumption by slowing down the CPU clocks and/or the bus matrix clocks and/or controlling individual peripheral clocks.
- Save power consumption when the CPU is IDLE, by selecting among the available low-power mode according to the user application needs. This allows the best compromise between short startup time, low-power consumption, as well as available wakeup sources, to be achieved.

The CPUs feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- Stop (bus matrix clocks stalled, the oscillators can be stopped)
- CStandby (MPU sub-system clock stopped and wakeup via reset)
- Standby (system powered down)
- LP-Stop and LPLV-Stop (bus matrix clocks stalled, the oscillators can be stopped, low-power mode signaled to external regulator)

CSleep and CStop low-power modes are entered by the CPU when executing the WFI (wait for interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex-M4 core is set after returning from an interrupt service routine.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the CPUs are in CStop or CStandby mode.

Table 3. System versus domain power mode

System power mode	MPU	MCU
Run mode	CRun or CSleep	CRun or CSleep
	CStop or CStandby	
	CRun or CSleep	CStop
Stop mode LP-Stop mode LPLV-Stop mode	CStop or CStandby	CStop
Standby mode	CStandby or (CStop and MPU PDDS = 1 and MPU CSTBYDIS = 1)	CStop and MCU PDDS = 1

3.10 Reset and clock controller (RCC)

The clock and reset controller manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows application of clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

3.10.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, three internal oscillators with fast startup time and four PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1% accuracy)
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 8-48 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides four PLLs:

- The PLL1 is dedicated to the MPU clocking
- The PLL2 provides:
  - The clocks for the AXI-SS (including APB4, APB5, AHB5 and AHB6 bridges)
  - The clocks for the DDR interface
  - The clocks for the GPU
- The PLL3 provides:
  - The clocks for the MCU, and its bus matrix (including the APB1, APB2, APB3, AHB1, AHB2, AHB3 and AHB4)
  - The kernel clocks for peripherals
- The PLL4 is dedicated to the generation of the kernel clocks for various peripherals

The system starts on the HSI clock. The user application can then select the clock configuration.

3.10.2 System reset sources

The power-on reset initializes all registers while the system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

An application reset is generated from one of the following sources:

- a reset from NRST pad
- a reset from POR and PDR signal (generally called power-on reset)
- a reset from BOR (generally called brownout)
- a reset from the independent watchdogs 1
- a reset from the independent watchdogs 2
- a software reset from the Cortex-M4 (MCU)
- a software reset from the Cortex-A7 (MPU)
- a failure on HSE, when the clock security system feature is activated

A system reset is generated from one of the following sources:

- An application reset,
- A reset from POR_VDDCORE signal,
- Every time the system exits from Standby.

3.11 Hardware semaphore (HSEM)

The HW semaphore block provides 64 (32-bit) register-based semaphores.

The semaphores can be used to ensure synchronization between different processes running on a core and between different cores. The HSEM provides a non blocking mechanism to lock semaphores in an atomic way. The following functions are provided:

- Locking a semaphore can be done in 2 ways:
  - 2-step lock: by writing CoreID and ProcessID to the semaphore, followed by a read check.
  - 1-step lock: by reading the CoreID from the semaphore.
- Interrupt generation when a semaphore is freed.
  - Each semaphore may generated an interrupt on one of the interrupt lines.
- Semaphore clear protection.
  - A semaphore is only cleared when CoreID and ProcessID matches.
- Global semaphore clear per CoreID.

3.12 Inter-processor communication controller (IPCC)

The inter-processor communication controller (IPCC) is used for communicating data between two processors.

The IPCC block provides a non blocking signaling mechanism to post and retrieve communication data in an atomic way. It provides the signaling for four channels:

- two channels in the direction from processor 1 to processor 2
- two channels in the opposite direction.

It is then possible to have two different communication types in each direction.

The IPCC communication data must be located in a common memory, which is not part of the IPCC block.

3.12.1 IPCC main features

- Status signaling for the four channels
  - Channel occupied/free flag, also used as lock
- Two interrupt lines per processor
  - One for RX channel occupied (communication data posted by sending processor)
  - One for TX channel free (communication data retrieved by receiving processor)
- Interrupt masking per channel
  - Channel occupied mask
  - Channel free mask
- Two channel operation modes
  - Simplex (each channel has its own communication data memory location)
  - Half duplex (a single channel in associated to a bidirectional communication data information memory location)

3.13 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Additionally, GPIO pins on port Z can be individually set as secure, which would mean that software accesses to these GPIOs and associated peripherals defined as secure are restricted to secure software running on Cortex-A7.

3.14 TrustZone protection controller (ETZPC)

ETZPC is used to configure TrustZone security of bus masters and slaves with programmable-security attributes (securable resources) such as:

- On-chip SYSRAM with programmable secure region size
- AHB and APB peripherals to be made secure

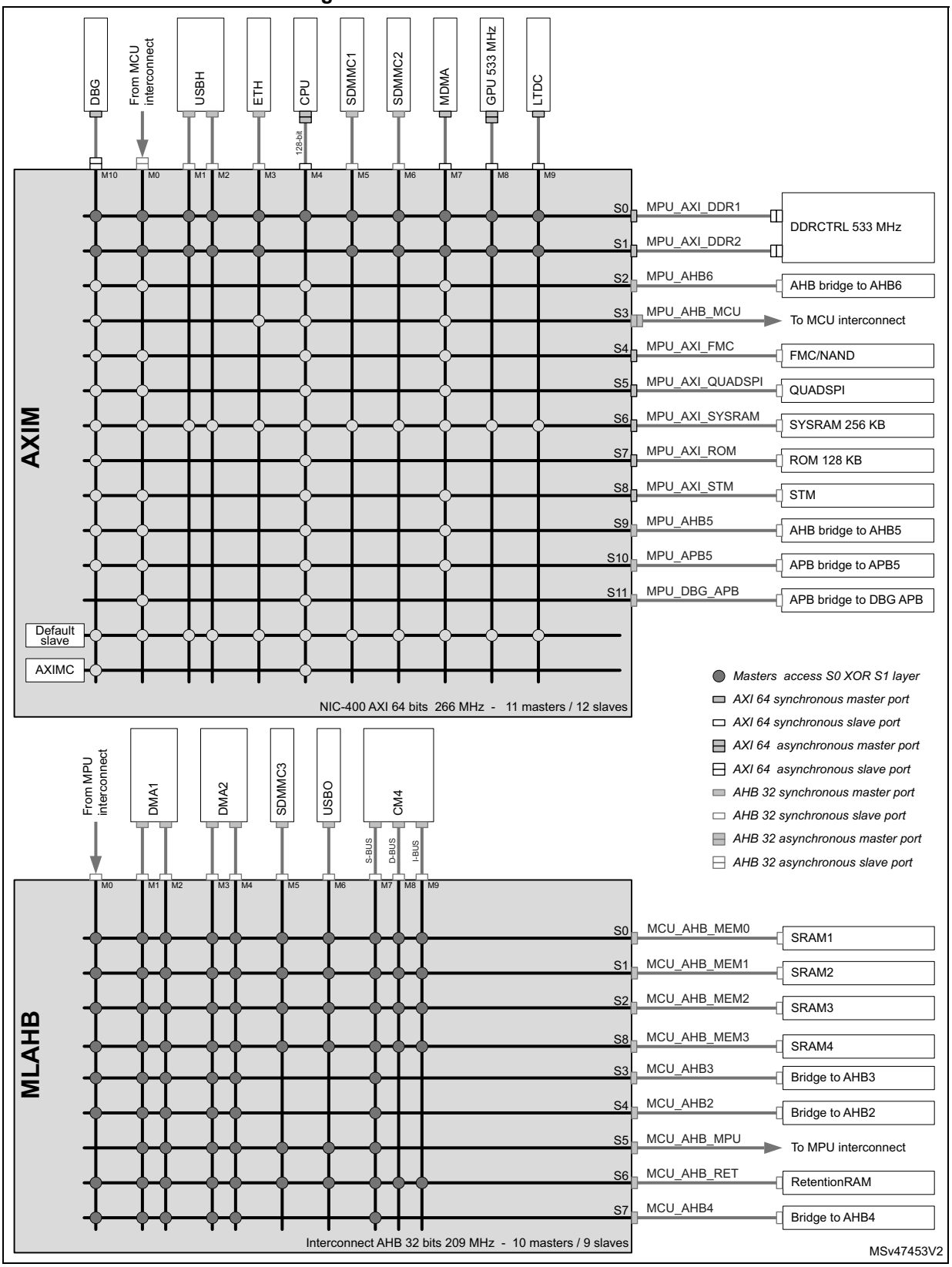
Notice that by default, SYSRAM and peripheral are set to secure access only, so, not accessible by non-secure masters such as Cortex-M4 or DMA1/DMA2.

ETZPC can also allocate peripherals and SRAM to be accessible only by the Cortex-M4 and/or DMA1/DMA2. This ensures the safe execution of the Cortex-M4 firmware, protected from other masters (e.g. Cortex-A7) unwanted accesses.

3.15 Bus-interconnect matrix

The devices feature an AXI bus matrix, one main AHB bus matrix and bus bridges that allow bus masters to be interconnected with bus slaves (see *Figure 3*, the dots represent the enabled master/slave connections).

Figure 3. STM32MP157A bus matrix



3.16 DMA controllers

The devices features three DMA modules to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface.

  The MDMA is located in MPU domain. It is able to interface with the other DMA controllers located in MCU domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 32 channels can perform block transfers, repeated block transfers and linked list transfers.

  The MDMA can be set to make secure transfers to secured memories.
- Two DMA controllers (DMA1, DMA2), located in MCU domain. Each controller is a dual-port AHB, for a total of 16 DMA channels to perform FIFO-based block transfers.

The DMAMUX is an extension of the DMA1 and DMA2 controllers. It multiplexes and routes the DMA peripheral requests to the DMA1 or DMA2 controllers, with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

3.17 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.18 Extended interrupt and event controller (EXTI)

The extended interrupt and event controller (EXTI) manages individual CPU and system wakeup through configurable and direct event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPUs NVIC or GIC and events to the CPUs event inputs. For each CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop mode, and the CPUs to be woken up from CStop and CStandby modes.

The interrupt request and event request generation can also be used in Run mode.

The block also includes the EXTI IOport selection.

Each interrupt or event can be set as secure in order to restrict access to secure software only.

3.19 Cyclic redundancy check calculation unit (CRC1, CRC2)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps computing a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.20 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - NOR Flash memory
  - Static or pseudo-static random access memory (SRAM, PSRAM)
  - NAND Flash memory with 4-bit/8-bit BCH hardware ECC
- 8-,16-bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

3.21 Dual Quad-SPI memory interface (QUADSPI)

The QUADSPI is a specialized communication interface targeting single, dual or quad SPI Flash memories. It can operate in any of the three following modes:

- indirect mode: all the operations are performed using the QUADSPI registers
- status polling mode: the external Flash memory status register is periodically read and an interrupt can be generated in case of flag setting
- memory-mapped mode: the external Flash memory is mapped to the address space and is seen by the system as if it was an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad-SPI Flash memories are accessed simultaneously.

QUADSPI is coupled with a delay block (DLYBQS) allowing the support of external data frequency above 100 MHz.

3.22 Analog-to-digital converters (ADCs)

The STM32MP157A devices embed two analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits. Each ADC shares up to 20 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- simultaneous ADC1/ADC2 conversion
- interleaved ADC1/ADC2 conversion.

The ADC can be served by the DMA controller, thus allowing the automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

In order to synchronize A/D conversion and timers, the ADCs can be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, LPTIM1, LPTIM2 and LPTIM3 timers.

3.23 Temperature sensor

The STM32MP157A devices embed a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC2_INP12. It can measure the device ambient temperature ranging from –40 to +125 °C with a precision of ±2%.

The temperature sensor has a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the OTP area, which is accessible in read-only mode.

3.24 Digital temperature sensor (DTS)

The device embeds a frequency output temperature sensor. This block counts the frequency based on the LSE or PCLK to provide the temperature information.

Following functions can be supported:

- Interrupt generation by temperature threshold.
- Wakeup signal generation by temperature threshold.

3.25 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers, the retention RAM and the backup SRAM.

In order to optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} has dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}. In the later case, VBAT mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers, the retention RAM and the backup SRAM.

Note: None of these events: external interrupts, TAMP event, or RTC alarm/events are able to directly restore the V_{DD} supply and force the STM32MP157A device out of the V_{BAT} operation. Nevertheless, TAMP events and RTC alarm/events can be used to generate a signal to an external circuitry (typically a PMIC) that can restore the STM32MP157A V_{DD} supply.

When PDR_ON pin is connected to V_{SS} (internal reset OFF), the V_{BAT} functionality is no more available and VBAT pin must be connected to V_{DD}.

3.26 Digital-to-analog converters (DAC1, DAC2)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Sample and hold mode to reduce the power consumption
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- External triggers for conversion
- input voltage reference V_{REF+} or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.27 Voltage reference buffer (VREFBUF)

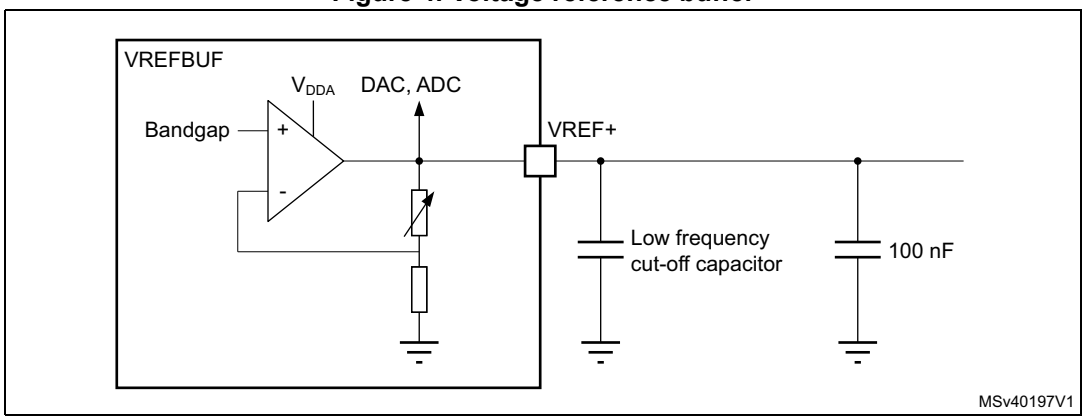
The STM32MP157A devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports four voltages:

- 1.5 V
- 1.8 V
- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

Figure 4. Voltage reference buffer



3.28 Digital filter for sigma delta modulators (DFSDM1)

The device embeds one DFSDM with support for 6 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs.

The DFSDM peripheral is dedicated to interface external ΣΔ modulators to STM32MP157A and perform digital filtering of the received data streams. ΣΔ modulators are used to convert analog signals into digital serial streams that constitute the inputs of the DFSDM. The DFSDM can also interface PDM (pulse density modulation) microphones and perform the PDM to PCM conversion and filtering (hardware accelerated). The DFSDM features optional parallel data stream inputs from internal ADC peripherals or STM32MP157A memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user-defined filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1-wire interface support
  - PDM (pulse density modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0…20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16-bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 6 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1…5), oversampling ratio (1…1024)
  - integrator: oversampling ratio (1…256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable $Sinc^x$ digital filter (order = 1…3, oversampling ratio = 1…32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1…256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "Regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

3.29 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using a 80 MHz pixel clock and 14-bit of data. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YC_bC_r 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.30 LCD-TFT display controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to WXGA (1366×768) @60 fps resolution with the following features:

- 2 display layers with dedicated FIFO
- Color look-up table (CLUT) up to 256 colors (256×24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface

3.31 Display serial interface (DSI)

The display serial interface (DSI) is part of a group of communication protocols defined by the MIPI® Alliance. The MIPI® DSI host controller is a digital core that implements all protocol functions defined in the MIPI® DSI specification.

It provides an interface between the system and the MIPI® D-PHY, allowing the communication with a DSI-compliant display.

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS
- Supports up to two D-PHY data lanes at 1 Gbps
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports ultra-low-power mode with PLL disabled
- ECC and checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for generic and DCS commands
  - Video mode interface through LTDC
  - Adapted command mode interface through LTDC
  - Independently programmable virtual channel ID in video mode, adapted command mode and APB slave
- Video mode interfaces features:
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
  - Programmable polarity of all LTDC interface signals
  - Maximum resolution is limited by available DSI physical link bandwidth
- Adapted interface features:
  - Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
- Video mode pattern generator

3.32 True random number generator (RNG1, RNG2)

All the devices embed two RNG that deliver 32-bit random numbers generated by an integrated analog circuit.

RNG1 can be defined (in ETZPC) as accessible by secure software only.

3.33 Hash processors (HASH1, HASH2)

The devices embed two processors that support the advanced algorithms usually required to ensure authentication, data integrity and non-repudiation when exchanging messages with a peer:

- Universal HASH
  - SHA-1, SHA224 and SHA256 (secure HASH algorithms)
  - MD5
  - HMAC

The accelerator supports DMA request generation.

HASH1 can be defined (in ETZPC) as accessible by secure software only.

3.34 Boot and security and OTP control (BSEC)

The BSEC (boot and security and OTP control) is intended to control an OTP (one time programmable) fuse box, used for embedded non-volatile storage for device configuration and security parameters. Some part of BSEC should be configured as accessible by secure software only.

3.35 Timers and watchdogs

The devices include two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, three watchdogs, a SysTick timer in Cortex-M4 and 4 system timers in each Cortex-A7.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose, basic and low-power timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes	100	209

Table 4. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
General purpose	TIM2, TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	100	209
	TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	100	209
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	209
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	209
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	100	209
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	100	209
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	100	209
Low-power	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	100	209

1. The maximum timer clock is up to 209 MHz depending on TIMGxPRE bit in the RCC.

3.35.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the general-purpose timers via the timer link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.35.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17)

There are ten synchronizable general-purpose timers embedded in the STM32MP157A devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the timer link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

3.35.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.35.4 Low-power timer (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the device from Stop mode.

These low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode

3.35.5 Independent watchdog (IWDG1, IWDG2)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC(LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

IWDG1 can be defined (in ETZPC) as accessible by secure software only.

3.35.6 System window watchdog (WWDG1)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.35.7 SysTick timer (Cortex-M4)

This timer is embedded inside Cortex-M4 core and dedicated to real-time operating systems, but can also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.35.8 Generic timers (Cortex-A7 CNT)

Cortex-A7 generic timers embedded inside Cortex-A7 are fed by value from system timing generation (STGEN).

The Cortex-A7 processor provides a set of four timers for each processor:

- Physical timer for use in secure and non-secure modes. The registers for the physical timer are banked to provide secure and non-secure copies.
- Virtual timer for use in non-secure modes.
- Physical timer for use in hypervisor mode.

Generic timers are not memory mapped peripherals, they are accessible only by specific Cortex-A7 coprocessor instructions (cp15).

3.36 System timer generation (STGEN)

The system timing generation (STGEN) generates a time count value that provides a consistent view of time for all Cortex-A7 generic timers.

The system timing generation has the following key features:

- 64-bit wide to avoid roll-over issues.
- Starts from zero or a programmable value.
- A control APB interface (STGENC) enables the timer to be saved and restored across powerdown events.
- Read-only APB interface (STGENR) enables the timer value to be read by non-secure software and debug tools.
- The timer value incrementing can be stopped during system debug.

STGENC can be defined (in ETZPC) as accessible by secure software only.

3.37 Real-time clock (RTC)

The RTC provides an automatic wakeup to manage all low-power modes.

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

The RTC includes also a periodic programmable wakeup flag with interrupt capability.

Two 32-bit registers contain the seconds, minutes, hours (12- or 24-hour format), day (day of week), date (day of month), month, and year, expressed in binary coded decimal format (BCD). The sub-seconds value is also available in binary format.

Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. Daylight saving time compensation can also be performed.

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

A digital calibration feature is available to compensate for any deviation in crystal oscillator accuracy.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, Low-power mode or under reset).

The RTC unit main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year.
- Daylight saving compensation programmable by software.
- Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields.
- Automatic wakeup unit generating a periodic flag that triggers an automatic wakeup interrupt.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Accurate synchronization with an external clock using the subsecond shift feature.
- Digital calibration circuit (periodic counter correction): 0.95 ppm accuracy, obtained in a calibration window of several seconds
- Timestamp function for event saving
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wakeup interrupt
  - Timestamp
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wakeup timer and timestamp individual secure or non-secure configuration

3.38 Tamper and backup registers (TAMP)

32 x 32-bit backup registers are retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. 3 tamper pins and 5 internal tampers are available for anti-tamper detection. The external tamper pins can be configured for edge detection, edge and level, level detection with filtering, or active tamper which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features

- 32 backup registers:
  - the backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on by VBAT when the V_{DD} power is switched off.
- 3 external tamper detection events.
  - Each external event can be configured to be active or passive.
  - External passive tampers with configurable filter and internal pull-up.
- 5 internal tamper events.
- Any tamper detection can generate a RTC timestamp event.
- Any tamper detection erases the backup registers.
- TrustZone support:
  - Tamper secure or non-secure configuration.
  - Backup registers configuration in 3 configurable-size areas:
    1 read/write secure area.
    1 write secure/read non-secure area.
    1 read/write non-secure area.
- Monotonic counter.

3.39 Inter-integrated circuit interface (I2C1, I2C2, I2C3, I2C4, I2C5, I2C6)

The STM32MP157A embeds six I^2C interfaces.

The I^2C bus interface handles communications between the STM32MP157A and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

I2C4 and I2C6 can be defined (in ETZPC) as accessible by secure software only.

3.40 Universal synchronous asynchronous receiver transmitter (USART1, USART2, USART3, USART6 and UART4, UART5, UART7, UART8)

The STM32MP157A devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 5* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the STM32MP157A from Stop mode using baudrates up to 200 Kbaud.The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 5. USART features

USART modes/features(1)	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	

1. X = supported.

USART1 can be defined (in ETZPC) as accessible by secure software only.

3.41 Serial peripheral interface (SPI1, SPI2, SPI3, SPI4, SPI5, SPI6)– inter- integrated sound interfaces (I2S1, I2S2, I2S3)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard I^2S interfaces (I2S1, I2S2, I2S3, multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in full-duplex and half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling

frequency. All I^2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

SPI6 can be defined (in ETZPC) as accessible by secure software only.

3.42 Serial audio interfaces (SAI1, SAI2, SAI3, SAI4)

The devices embed 4 SAIs that allow the design of many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 8 microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.43 SPDIF receiver interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX re-samples the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that is used to compute the exact sample rate for clock drift algorithms.

3.44 Management data input/output (MDIOS)

The devices embed a MDIO slave interface. It includes the following features:

- 32 MDIO register addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO register write
  - MDIO register read
  - MDIO protocol error
- Able to operate in and wake up from Stop mode

3.45 Secure digital input/output MultiMediaCard interface (SDMMC1, SDMMC2, SDMMC3)

Three secure digital input/output MultiMediaCard interfaces (SDMMC) provide an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Full compliance with *MultiMediaCard System Specification Version 4.51*.
  Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit.
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with *SD memory card specifications version 4.1*.
  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with SDIO card specification version 4.0.
  Card support for two different databus modes: 1-bit (default) and 4-bit.
  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Data transfer up to 208 Mbyte/s for the 8-bit mode.
  (depending maximum allowed I/O speed).
- Data and command output enable signals to control external bidirectional drivers.
- The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.
- IDMA linked list support

Each SDMMC is coupled with a delay block (DLYBSD) allowing support of an external data frequency above 100 MHz.

3.46 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.47 Universal serial bus high-speed host (USBH)

The devices embed one USB high-speed host (up to 480 Mbit/s) with two physical ports. USBH supports both low, full-speed (OHCI) as well as high-speed (EHCI) operations independently on each port. It integrates two transceivers which can be used for either low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) or high-speed operation (480 Mbit/s), the second high-speed transceiver is shared with OTG high-speed.

The USB HS is compliant with the USB 2.0 specification. The USB HS controllers require dedicated clocks that are generated by a PLL inside the USB high-speed PHY.

3.48 USB on-the-go high-speed (OTG)

The devices embed one USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and high-speed operation (480 Mbit/s) shared with USB Host second port.

The USB OTG HS is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL inside RCC or inside the USB high-speed PHY.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbyte with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (link power management) support
- Battery charging specification revision 1.2 support
- Internal FS or HS OTG PHY support
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.49 Gigabit Ethernet MAC interface (ETH1)

The devices provide an IEEE-802.3-2002-compliant gigabit media access controller (GMAC) for Ethernet LAN communications through an industry-standard medium-independent interface (MII), a reduced medium-independent interface (RMII), a gigabit medium-independent interface (GMII) or a reduced gigabit medium-independent interface (RGMII).

The STM32MP157A requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device port using 17 signals for MII, 7 signals for RMII, 26 signals for GMII or 13 signals for RGMII, and can be clocked using the 25 MHz (MII, RMII, GMII, RGMII) or 125 MHz (GMII, RGMII) from the STM32MP157A or from the PHY.

The devices include the following features:

- Operation modes and PHY interfaces
  - 10, 100, and 1000 Mbps data transfer rates
  - Support of both full-duplex and half-duplex operations
  - MII, RMII, GMII and RGMII PHY interfaces
- Multiple queues support and audio video bridging (AVB) management
  - Separate channels or queues for AV data transfer in 100 and 1000 Mbps modes
  - Two queues on the Rx paths and two queues on the Tx path for AV traffic
  - One DMA for Rx path and two DMA for Tx path (one per transmit channels)
  - Several arbitration algorithms between queues: weighted round robin (WRR), strict priority (SP), weighted strict priority (WSP), IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for Transmit channels
- Processing control
  - Multi-layer Packet filtering: MAC filtering on source (SA) and destination (DA) address with perfect and hash filter, VLAN tag-based filtering with perfect and

hash filter, Layer 3 filtering on IP source (SA) or destination (DA) address, Layer 4 filtering on source (SP) or destination (DP) port
  - Double VLAN processing: insertion of up to two VLAN tags in transmit path, tag filtering in receive path
  - IEEE 1588-2008/PTPv2 support
  - Supports network statistics with RMON/MIB counters (RFC2819/RFC2665)
- Hardware offload processing
  - Preamble and start-of-frame data (SFD) insertion or deletion
  - Integrity Checksum offload engine for IP header and TCP/UDP/ICMP payload: transmit checksum calculation and insertion, receive checksum calculation and comparison
  - Automatic ARP request response with the device's MAC address
  - TCP Segmentation: Automatic split of large transmit TCP packet into multiple small packets
- Low-power mode
  - Energy efficient Ethernet (Standard IEEE 802.3az-2010)
  - Remote wakeup packet and AMD Magic Packet™ detection

3.50 High-definition multimedia interface (HDMI) – Consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the consumer electronics control (CEC) protocol (supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the STM32MP157A from Stop mode on data reception.

3.51 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

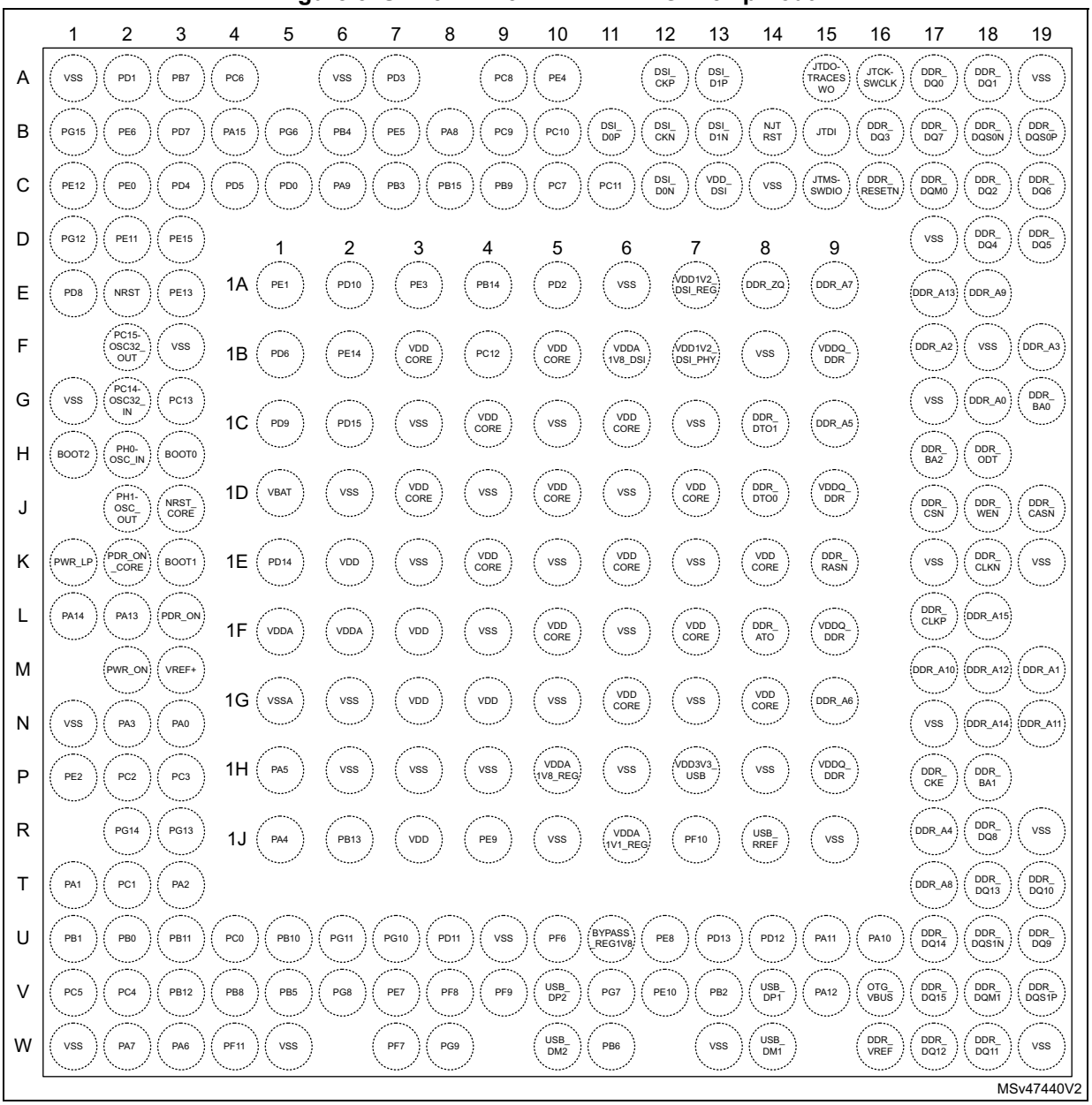
- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/serial-wire debug access port, using industry standard debugging tools.

A trace port allows data to be captured for logging and analysis.

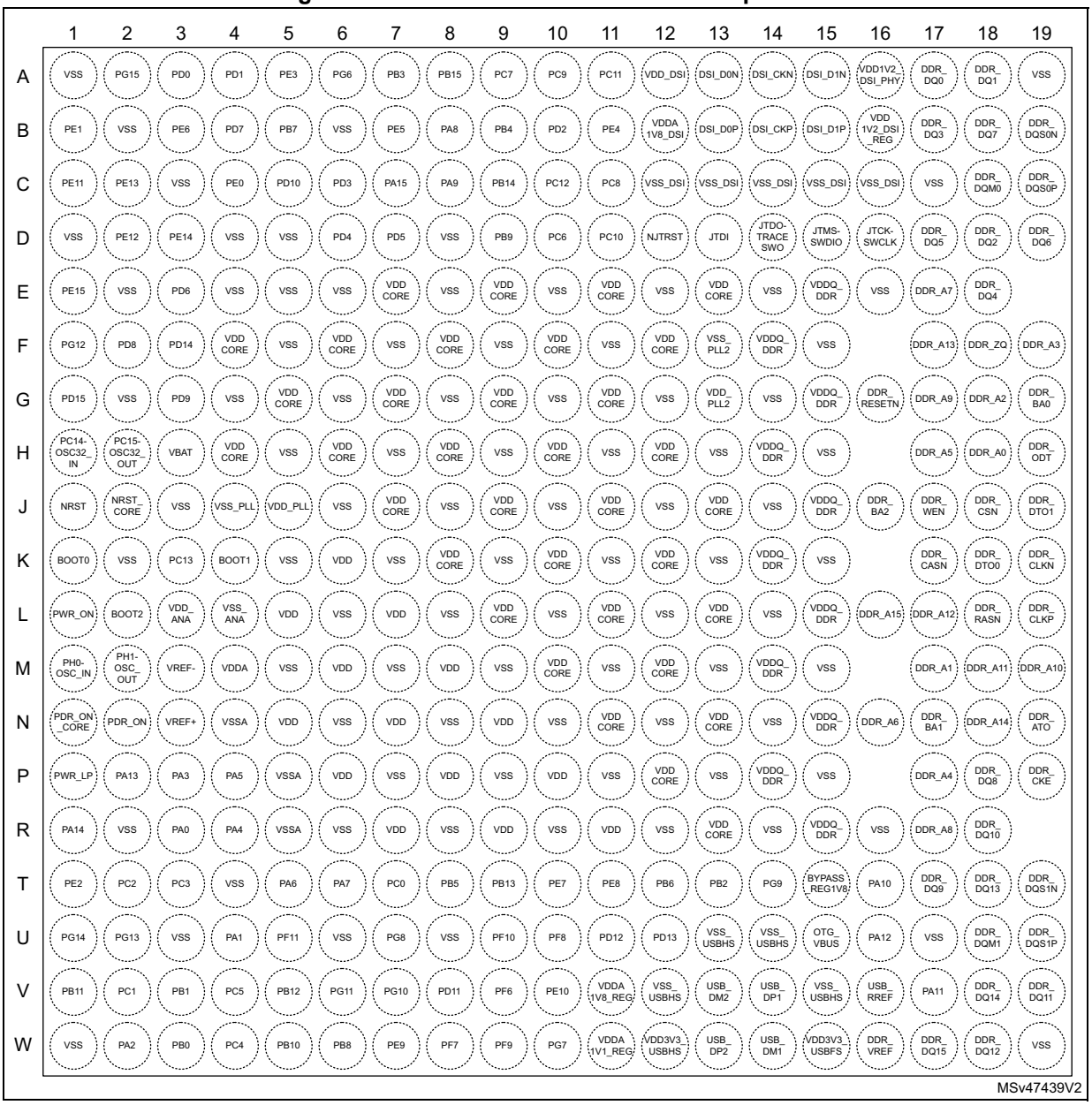
4 Pinouts, pin description and alternate functions

Figure 5. STM32MP157AADxx TFBGA257 pinout



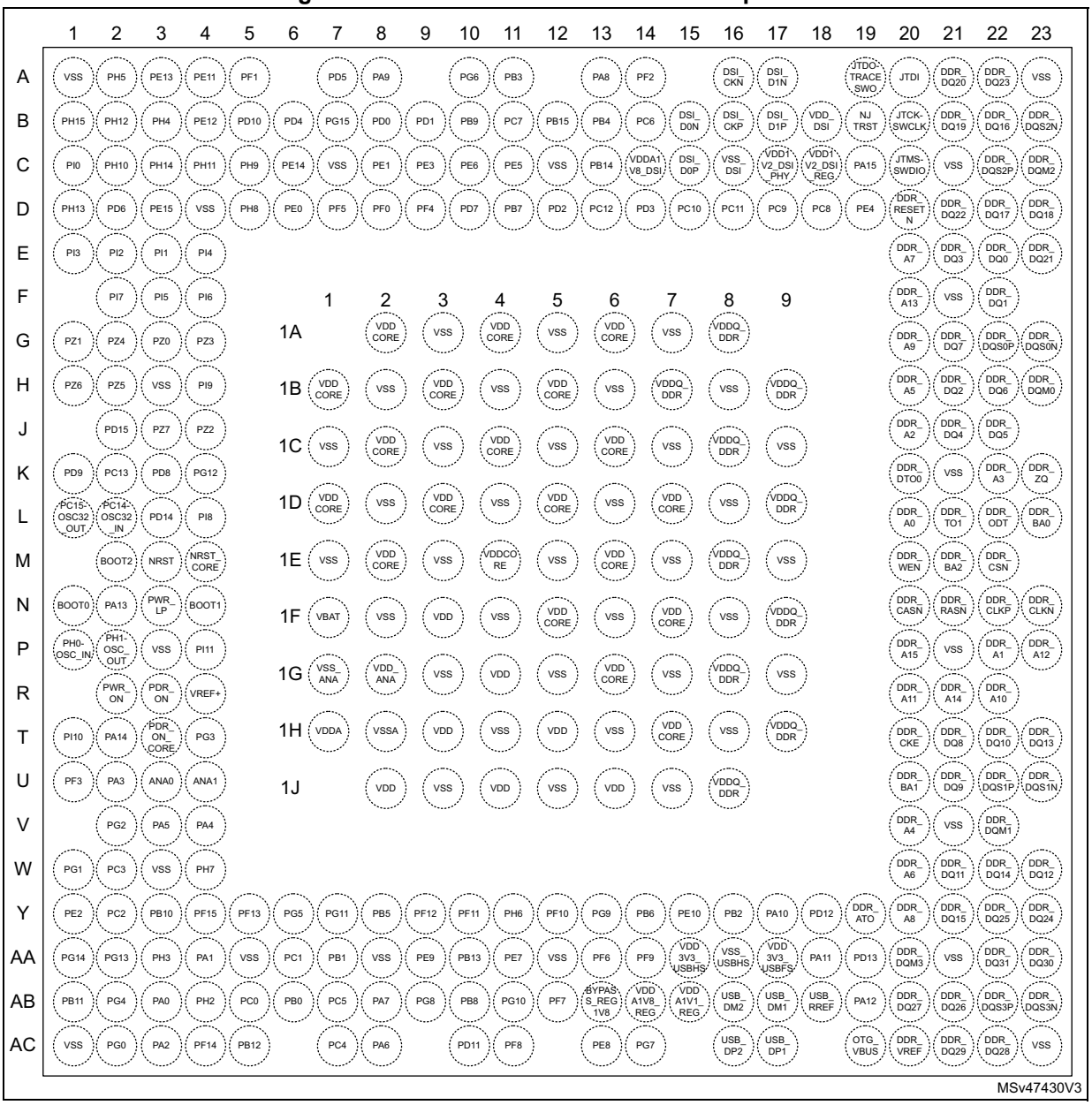
The above figure shows the package top view.

Figure 6. STM32MP157AABxx LFBGA354 pinout



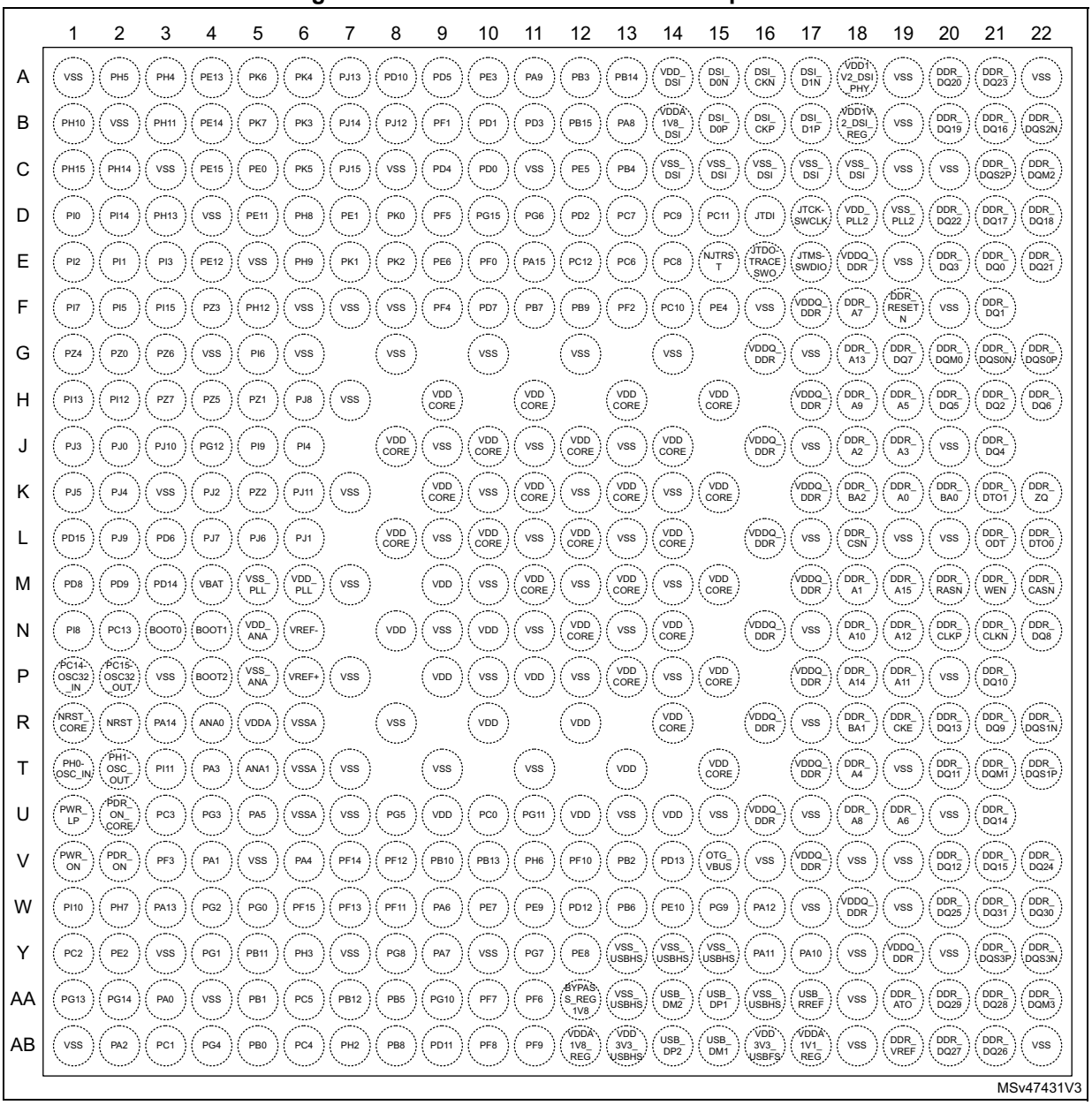
The above figure shows the package top view.

Figure 7. STM32MP157AACxx TFBGA361 pinout



The above figure shows the package top view.

Figure 8. STM32MP157AAA LFBGA448 pinout



The above figure shows the package top view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	O	Output only pin
	I/O	Input / output pin
	A	Analog or special level pin
I/O structure	FT(U/D/PD)	5 V tolerant I/O (with fixed pull-up / pull-down / programmable pull-down)
	TT	3.6 V tolerant I/O directly connected to DAC
	DDR	1.5 V, 1.35 V or 1.2 V I/O for DDR3, DDR3L, LPDDR2/LPDDR3 interface
	DSI	1.2 V I/O for DSI interface
	A	Analog signal
	RST	Reset pin with weak pull-up resistor
	Option for TT or FT I/Os	
	_f(1)	I2C FM+ option
	_a(2)	Analog option (supplied by VDDA for the analog part of the I/O)
	_u(3)	USB option (supplied by VDD3V3_USBxx for the USB part of the I/O)
	_h(4)	High-speed output for 1.8V typ. VDD (for SPI, SDMMC, QUADSPI, TRACE)
	_e(5)	Very-high-speed option for 1.8V typ. VDD (for ETH, SPI, SDMMC, QUADSPI, TRACE)
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 7* are: FT_f, FT_fae, FT_fh, FT_fha, FT_uf
2. The related I/O structures in *Table 7* are: FT_a, TT_a, FT_ae, FT_fae, FT_fha, FT_ha, TT_ha
3. The related I/O structures in *Table 7* are: FT_u, FT_uf
4. The related I/O structures in *Table 7* are: FT_h, FT_fh, FT_fha, FT_ha, TT_ha
5. The related I/O structures in *Table 7* are: FT_e, FT_ae, FT_fae

Table 7. STM32MP157A pin and ball definitions

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	A2	A2	PH5	I/O	FT_f	-	I2C2_SDA, SPI5_NSS, SAI4_SD_B, EVENTOUT	-
-	-	C2	B1	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, I2C1_SMBA, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	B2	F5	PH12	I/O	FT_f	-	HDP2, TIM5_CH3, I2C4_SDA, I2C1_SDA, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	D1	D3	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, FDCAN1_TX, LCD_G2, EVENTOUT	-
1E2	K6	1F3	M9	VDD	S	-	-	-	-
A1	A1	A1	A1	VSS	S	-	-	-	-
-	-	C3	C2	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, FDCAN1_RX, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	B1	C1	PH15	I/O	FT	-	TIM8_CH3N, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	-	H6	PJ8	I/O	FT_h	-	TRACED14, TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	D2	PI14	I/O	FT_h	-	TRACECLK, LCD_CLK, EVENTOUT	-
-	-	-	F3	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	C1	D1	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	E3	E2	PI1	I/O	FT_h	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	E2	E1	PI2	I/O	FT_h	-	TIM8_CH4, SPI2_MISO/I2S2_SDI, DCMI_D9, LCD_G7, EVENTOUT	-
1B3	E7	1A2	H9	VDDCORE	S	-	-	-	-
-	-	E1	E3	PI3	I/O	FT_h	-	TIM8_ETR, SPI2_MOSI/I2S2_SDO, DCMI_D10, EVENTOUT	-
-	-	E4	J6	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	F3	F2	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, DCMI_VSYNC, LCD_B5, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	F4	G5	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	F2	F1	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, DCMI_D7, LCD_B7, EVENTOUT	-
-	A19	A23	A19	VSS	S	-	-	-	-
-	-	G1	H5	PZ1	I/O	FT_fh	-	I2C6_SDA, I2C2_SDA, I2C5_SDA, SPI1_MISO/I2S1_SDI, I2C4_SDA, USART1_RX, SPI6_MISO, EVENTOUT	-
-	-	G4	F4	PZ3	I/O	FT_f	-	I2C6_SDA, I2C2_SDA, I2C5_SDA, SPI1_NSS/I2S1_WS, I2C4_SDA, USART1_CTS/USART1_NSS, SPI6_NSS, EVENTOUT	-
-	-	H4	J5	PI9	I/O	FT	-	HDP1, UART4_RX, FDCAN1_RX, LCD_VSYNC, EVENTOUT	-
-	-	G3	G2	PZ0	I/O	FT_fh	-	I2C6_SCL, I2C2_SCL, SPI1_SCK/I2S1_CK, USART1_CK, SPI6_SCK, EVENTOUT	-
-	-	J4	K5	PZ2	I/O	FT_fh	-	I2C6_SCL, I2C2_SCL, I2C5_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, USART1_TX, SPI6_MOSI, EVENTOUT	-
-	-	G2	G1	PZ4	I/O	FT_f	-	I2C6_SCL, I2C2_SCL, I2C5_SCL, I2C4_SCL, EVENTOUT	-
G1	B2	-	A22	VSS	S	-	-	-	-
D1	F1	K4	J4	PG12	I/O	FT_h	-	LPTIM1_IN1, SPI6_MISO, SAI4_CK2, USART6_RTS/USART6_DE, SPDIFRX_IN1, LCD_B4, SAI4_SCK_A, ETH1_PHY_INTN, FMC_NE4, LCD_B1, EVENTOUT	-
-	-	H2	H4	PZ5	I/O	FT_f	-	I2C6_SDA, I2C2_SDA, I2C5_SDA, I2C4_SDA, USART1_RTS/USART1_DE, EVENTOUT	-
-	E9	-	-	VDDCORE	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	H1	G3	PZ6	I/O	FT_f	-	I2C6_SCL, I2C2_SCL, USART1_CK, I2S1_MCK, I2C4_SMBA, USART1_RX, EVENTOUT	-
-	-	J3	H3	PZ7	I/O	FT_f	-	I2C6_SDA, I2C2_SDA, USART1_TX, EVENTOUT	-
-	-	-	H2	PI12	I/O	FT_h	-	TRACED0, HDP0, LCD_HSYNC, EVENTOUT	-
-	B6	C7	B2	VSS	S	-	-	-	-
-	-	-	H1	PI13	I/O	FT_h	-	TRACED1, HDP1, LCD_VSYNC, EVENTOUT	-
-	-	1A4	H11	VDDCORE	S	-	-	-	-
-	-	-	J3	PJ10	I/O	FT_h	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	K6	PJ11	I/O	FT_h	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	J2	PJ0	I/O	FT_h	-	TRACED8, LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	L6	PJ1	I/O	FT_h	-	TRACED9, LCD_R2, EVENTOUT	-
-	-	-	K4	PJ2	I/O	FT_h	-	TRACED10, DSI_TE, LCD_R3, EVENTOUT	-
-	L5	-	-	VDD	S	-	-	-	-
-	-	-	J1	PJ3	I/O	FT_h	-	TRACED11, LCD_R4, EVENTOUT	-
N1	C3	-	B19	VSS	S	-	-	-	-
-	-	-	K2	PJ4	I/O	FT_h	-	TRACED12, LCD_R5, EVENTOUT	-
1D3	E11	-	-	VDDCORE	S	-	-	-	-
-	-	-	K1	PJ5	I/O	FT_h	-	TRACED2, HDP2, LCD_R6, EVENTOUT	-
-	-	-	L5	PJ6	I/O	FT_h	-	TRACED3, HDP3, TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	L4	PJ7	I/O	FT_h	-	TRACED13, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	C17	C12	C3	VSS	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
1B1	E3	D2	L3	PD6	I/O	FT_ha	-	TIM16_CH1N, SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
-	E13	-	H13	VDDCORE	S	-	-	-	-
-	-	-	L2	PJ9	I/O	FT_h	-	TRACED15, TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-
-	J5	-	M6	VDD_PLL	S	-	-	-	-
-	J4	-	M5	VSS_PLL	S	-	-	-	-
1E1	F3	L3	M3	PD14	I/O	FT_a	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_AD0/FMC_D0, EVENTOUT	-
1C2	G1	J2	L1	PD15	I/O	FT_a	-	TIM4_CH4, SAI3_MCLK_A, UART8_CTS, FMC_AD1/FMC_D1, LCD_R1, EVENTOUT	-
E1	F2	K3	M1	PD8	I/O	FT_a	-	DFSDM1_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX_IN1, FMC_AD13/FMC_D13, LCD_B7, EVENTOUT	-
1C1	G3	K1	M2	PD9	I/O	FT_a	-	DFSDM1_DATIN3, SAI3_SD_B, USART3_RX, FMC_AD14/FMC_D14, DCMI_HSYNC, LCD_B0, EVENTOUT	-
-	-	-	N8	VDD	S	-	-	-	-
W1	D1	C21	C8	VSS	S	-	-	-	-
-	-	1A6	-	VDDCORE	S	-	-	-	-
1D1	H3	1F1	M4	VBAT	S	-	-	-	-
-	D4	-	C11	VSS	S	-	-	-	-
-	-	L4	N1	PI8	I/O	FT	(1)	EVENTOUT	RTC_OUT2/ RTC_LSCO, TAMP_IN2/ TAMP_OUT3, WKUP4

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
G3	K3	K2	N2	PC13	I/O	FT	(1)	EVENTOUT	RTC_OUT1/ RTC_TS/ RTC_LSCO, TAMP_IN1/ TAMP_OUT2/ TAMP_OUT3, WKUP3
F3	D5	D4	C19	VSS	S	-	-	-	-
F2	H2	L1	P2	PC15-OSC32_OUT	I/O	FT	(1)	EVENTOUT	OSC32_OUT
-	F4	-	H15	VDDCORE	S	-	-	-	-
1C4	F6	1B1	-	VDDCORE	S	-	-	-	-
G2	H1	L2	P1	PC14-OSC32_IN	I/O	FT	(1)	EVENTOUT	OSC32_IN
E2	J1	M3	R2	NRST	I/O	RST	-	-	-
J3	J2	M4	R1	NRST_CORE	I	RST	-	-	-
H3	K1	N1	N3	BOOT0	I	FTPD	-	-	-
K3	K4	N4	N4	BOOT1	I	FTPD	-	-	-
H1	L2	M2	P4	BOOT2	I	FTPD	-	-	-
H2	M1	P1	T1	PH0-OSC_IN	I/O	FT	-	EVENTOUT	OSC_IN
-	-	-	J8	VDDCORE	S	-	-	-	-
J2	M2	P2	T2	PH1-OSC_OUT	I/O	FT	-	EVENTOUT	OSC_OUT
-	D8	-	C20	VSS	S	-	-	-	-
M2	L1	R2	V1	PWR_ON	O	FT	-	-	PWR_ONLP
K1	P1	N3	U1	PWR_LP	O	FT	-	-	-
K2	N1	T3	U2	PDR_ON_CORE	I	FT	-	-	-
L3	N2	R3	V2	PDR_ON	I	FT	-	-	-
-	L3	1G2	N5	VDD_ANA	S	-	-	-	-
-	L4	1G1	P5	VSS_ANA	S	-	-	-	-
L2	P2	N2	W3	PA13	I/O	FT_a	-	DBTRGO, DBTRGI, MCO1, UART4_TX, EVENTOUT	BOOTFAILN
L1	R1	T2	R3	PA14	I/O	FT_a	-	DBTRGO, DBTRGI, MCO2, EVENTOUT	-
-	-	P4	T3	PI11	I/O	FT	-	MCO1, I2S_CKIN, LCD_G6, EVENTOUT	WKUP5

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	T1	W1	PI10	I/O	FT	-	HDP0, USART3_CTS/USART3_NSS, ETH1_GMII_RX_ER/ ETH1_MII_RX_ER, LCD_HSYNC, EVENTOUT	-
-	L7	1G4	-	VDD	S	-	-	-	-
W5	E2	F21	-	VSS	S	-	-	-	-
-	F8	-	-	VDDCORE	S	-	-	-	-
1F1	M4	1H1	R5	VDDA	S	-	-	-	-
1F2	-	-	-	VDDA	S	-	-	-	-
M3	N3	R4	P6	VREF+	S	-	-	-	-
1G1	N4	1H2	R6	VSSA	S	-	-	-	-
-	P5	-	T6	VSSA	S	-	-	-	-
-	R5	-	U6	VSSA	S	-	-	-	-
-	M3	-	N6	VREF-	S	-	-	-	-
-	-	W4	W2	PH7	I/O	FT_fh	-	I2C3_SCL, SPI5_MISO, ETH1_GMII_RXD3/ ETH1_MII_RXD3/ ETH1_RGMII_RXD3, MDIOS_MDC, DCMI_D9, EVENTOUT	-
-	-	U1	V3	PF3	I/O	FT_e	-	ETH1_GMII_TX_ER, FMC_A3, EVENTOUT	-
P3	T3	W2	U3	PC3	I/O	FT_ha	-	TRACECLK, DFSDM1_DATIN1, SPI2_MOSI/I2S2_SDO, ETH1_GMII_TX_CLK/ ETH1_MII_TX_CLK, EVENTOUT	ADC1_INP13, ADC1_INN12
-	-	T4	U4	PG3	I/O	FT_e	-	TRACED3, TIM8_BKIN2, DFSDM1_CKIN1, ETH1_GMII_TXD7, FMC_A13, EVENTOUT	-
P1	T1	Y1	Y2	PE2	I/O	FT_fae	-	TRACECLK, SAI1_CK1, I2C4_SCL, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH1_GMII_TXD3/ ETH1_MII_TXD3/ ETH1_RGMII_TXD3, FMC_A23, EVENTOUT	-
-	-	-	N10	VDD	S	-	-	-	-
-	E4	H3	D4	VSS	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
N2	P3	U2	T4	PA3	I/O	FT_a	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, ETH1_GMII_COL/ ETH1_MII_COL, LCD_B5, EVENTOUT	ADC1_INP15, PVD_IN
P2	T2	Y2	Y1	PC2	I/O	FT_ae	-	DFSDM1_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, ETH1_GMII_TXD2/ ETH1_MII_TXD2/ ETH1_RGMII_TXD2, DCMI_PIXCLK, EVENTOUT	ADC1_INP12, ADC1_INN11
-	-	V2	W4	PG2	I/O	FT_e	-	TRACED2, MCO2, TIM8_BKIN, ETH1_GMII_TXD6, FMC_A12, EVENTOUT	-
R2	U1	AA1	AA2	PG14	I/O	FT_e	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, SAI4_D1, USART6_TX, QUADSPI_BK2_IO3, SAI4_SD_A, ETH1_GMII_TXD1/ ETH1_MII_TXD1/ ETH1_RGMII_TXD1/ ETH1_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	-	W1	Y4	PG1	I/O	FT_e	-	TRACED1, ETH1_GMII_TXD5, FMC_A11, EVENTOUT	-
R3	U2	AA2	AA1	PG13	I/O	FT_e	-	TRACED0, LPTIM1_OUT, SAI1_CK2, SAI4_CK1, SPI6_SCK, SAI1_SCK_A, USART6_CTS/USART6_NSS, SAI4_MCLK_A, ETH1_GMII_TXD0/ ETH1_MII_TXD0/ ETH1_RGMII_TXD0/ ETH1_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	-	U3	R4	ANA0	A	A	-	-	ADC1_INP0, ADC1_INN1, ADC2_INP0, ADC2_INN1
N3	R3	AB3	AA3	PA0	I/O	FT_ha	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH1_GMII_CRS/ ETH1_MII_CRS, EVENTOUT	ADC1_INP16, WKUP1

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	E5	-	E5	VSS	S	-	-	-	-
-	-	U4	T5	ANA1	A	A	-	-	ADC1_INP1, ADC2_INP1
T1	U4	AA4	V4	PA1	I/O	FT_ha	-	ETH_CLK, TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS/USART2_DE, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH1_GMII_RX_CLK/ ETH1_MII_RX_CLK/ ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INP17, ADC1_INN16
1H1	P4	V3	U5	PA5	I/O	TT_ha	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SAI4_CK1, SPI1_SCK/I2S1_CK, SPI6_SCK, SAI4_MCLK_A, LCD_R4, EVENTOUT	ADC1_INP19, ADC1_INN18, ADC2_INP19, ADC2_INN18, DAC_OUT2
1J1	R4	V4	V6	PA4	I/O	TT_a	-	HDP0, TIM5_ETR, SAI4_D2, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, SAI4_FS_A, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_INP18, ADC2_INP18, DAC_OUT1
-	-	AC2	W5	PG0	I/O	FT_e	-	TRACED0, DFSDM1_DATIN0, ETH1_GMII_TXD4, FMC_A10, EVENTOUT	-
U3	V1	AB1	Y5	PB11	I/O	FT_fae	-	TIM2_CH4, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, ETH1_GMII_TX_EN/ ETH1_MII_TX_EN/ ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT	-
-	-	AB2	AB4	PG4	I/O	FT_e	-	TIM1_BKIN2, ETH1_GMII_GTX_CLK/ ETH1_RGMII_GTX_CLK, FMC_A14, EVENTOUT	-
T3	W2	AC3	AB2	PA2	I/O	FT_ha	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, SDMMC2_D0DIR, ETH1_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_INP14, WKUP2

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
1F3	M6	-	-	VDD	S	-	-	-	-
T2	V2	AA6	AB3	PC1	I/O	FT_ha	-	TRACED0, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SDMMC2_CK, ETH1_MDC, MDIOS_MDC, EVENTOUT	ADC1_INP11, ADC1_INN10, ADC2_INP11, ADC2_INN10, TAMP_IN3, WKUP6
A6	-	K21	E19	VSS	S	-	-	-	-
-	-	Y6	U8	PG5	I/O	FT	-	TIM1_ETR, ETH1_GMII_CLK125/ ETH1_RGMII_CLK125, FMC_A15, EVENTOUT	-
-	F10	1B3	J10	VDDCORE	S	-	-	-	-
-	-	AA3	Y6	PH3	I/O	FT_h	-	DFSDM1_CKIN4, QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH1_GMII_COL/ ETH1_MII_COL, LCD_R1, EVENTOUT	-
U2	W3	AB6	AB5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, ETH1_GMII_RXD2/ ETH1_MII_RXD2/ ETH1_RGMII_RXD2, MDIOS_MDIO, LCD_G1, EVENTOUT	ADC1_INP9, ADC1_INN5, ADC2_INP9, ADC2_INN5
-	-	Y4	W6	PF15	I/O	FT_fh	-	TRACED7, I2C4_SDA, I2C1_SDA, ETH1_GMII_RXD7, FMC_A9, EVENTOUT	-
U1	V3	AA7	AA5	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, ETH1_GMII_RXD3/ ETH1_MII_RXD3/ ETH1_RGMII_RXD3, MDIOS_MDC, LCD_G0, EVENTOUT	ADC1_INP5, ADC2_INP5
-	E6	-	F6	VSS	S	-	-	-	-
-	-	AC4	V7	PF14	I/O	FT_fha	-	TRACED6, DFSDM1_CKIN6, I2C4_SCL, I2C1_SCL, ETH1_GMII_RXD6, FMC_A8, EVENTOUT	ADC2_INP6, ADC2_INN2

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	Y5	W7	PF13	I/O	FT_ha	-	TRACED5, DFSDM1_DATIN6, I2C4_SMBA, I2C1_SMBA, DFSDM1_DATIN3, ETH1_GMII_RXD5, FMC_A7, EVENTOUT	ADC2_INP2
-	-	AB4	AB7	PH2	I/O	FT_h	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH1_GMII_CRS/ ETH1_MII_CRS, LCD_R0, EVENTOUT	-
V1	V4	AB7	AA6	PC5	I/O	FT_a	-	SAI1_D3, DFSDM1_DATIN2, SAI4_D4, SAI1_D4, SPDIFRX_IN3, ETH1_GMII_RXD1/ ETH1_MII_RXD1/ ETH1_RGMII_RXD1/ ETH1_RMII_RXD1, SAI4_D3, EVENTOUT	ADC1_INP8, ADC1_INN4, ADC2_INP8, ADC2_INN4
V2	W4	AC7	AB6	PC4	I/O	FT_a	-	DFSDM1_CKIN2, I2S1_MCK, SPDIFRX_IN2, ETH1_GMII_RXD0/ ETH1_MII_RXD0/ ETH1_RGMII_RXD0/ ETH1_RMII_RXD0, EVENTOUT	ADC1_INP4, ADC2_INP4
-	M8	-	P9	VDD	S	-	-	-	-
1D2	E8	P3	F7	VSS	S	-	-	-	-
1J3	R7	1J2	U9	VDD	S	-	-	-	-
-	-	Y9	V8	PF12	I/O	FT_ha	-	TRACED4, ETH1_GMII_RXD4, FMC_A6, EVENTOUT	ADC1_INP6, ADC1_INN2
1E4	-	-	-	VDDCORE	S	-	-	-	-
W4	U5	Y10	W8	PF11	I/O	FT_ha	-	SPI5_MOSI, SAI2_SD_B, DCMI_D12, LCD_G5, EVENTOUT	ADC1_INP2
-	E10	-	F8	VSS	S	-	-	-	-
W2	T6	AB8	Y9	PA7	I/O	FT_ha	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SAI4_D1, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, QUADSPI_CLK, ETH1_GMII_RX_DV/ ETH1_MII_RX_DV/ ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV, SAI4_SD_A, EVENTOUT	ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	F12	-	J12	VDDCORE	S	-	-	-	-
W3	T5	AC8	W9	PA6	I/O	FT_ha	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SAI4_CK2, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, MDIOS_MDC, SAI4_SCK_A, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_INP3, ADC2_INP3
-	-	1H3	-	VDD	S	-	-	-	-
U4	T7	AB5	U10	PC0	I/O	FT_ha	-	DFSDM1_CKIN0, LPTIM2_IN2, DFSDM1_DATIN4, SAI2_FS_B, QUADSPI_BK2_NCS, LCD_R5, EVENTOUT	ADC1_INP10, ADC2_INP10
1G2	E12	P21	F16	VSS	S	-	-	-	-
U5	W5	Y3	V9	PB10	I/O	FT_fha	-	TIM2_CH3, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, ETH1_GMII_RX_ER/ ETH1_MII_RX_ER, LCD_G4, EVENTOUT	-
-	-	1B5	-	VDDCORE	S	-	-	-	-
V3	V5	AC5	AA7	PB12	I/O	FT_ae	-	TIM1_BKIN, I2C6_SMBA, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, USART3_RX, FDCAN2_RX, ETH1_GMII_TXD0/ ETH1_MII_TXD0/ ETH1_RGMII_TXD0/ ETH1_RMII_TXD0, UART5_RX, EVENTOUT	-
-	G5	-	J14	VDDCORE	S	-	-	-	-
1J2	T9	AA10	V10	PB13	I/O	FT_e	-	TIM1_CH1N, DFSDM1_CKOUT, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, FDCAN2_TX, ETH1_GMII_TXD1/ ETH1_MII_TXD1/ ETH1_RGMII_TXD1/ ETH1_RMII_TXD1, UART5_TX, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	E14	V21	F20	VSS	S	-	-	-	-
V5	T8	Y8	AA8	PB5	I/O	FT_e	-	ETH_CLK, TIM17_BKIN, TIM3_CH2, SAI4_D1, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, FDCAN2_RX, SAI4_SD_A, ETH1_PPS_OUT, UART5_RX, DCMI_D10, LCD_G7, EVENTOUT	-
U6	V6	Y7	U11	PG11	I/O	FT_e	-	TRACED11, USART1_TX, UART4_TX, SPDIFRX_IN0, ETH1_GMII_TX_EN/ ETH1_MII_TX_EN/ ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
1B5	G7	1C2	-	VDDCORE	S	-	-	-	-
-	-	Y11	V11	PH6	I/O	FT_h	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH1_GMII_RXD2/ ETH1_MII_RXD2/ ETH1_RGMII_RXD2, MDIOS_MDIO, DCMI_D8, EVENTOUT	-
1H2	E16	-	G4	VSS	S	-	-	-	-
V4	W6	AB10	AB8	PB8	I/O	FT_fae	-	HDP6, TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, SDMMC1_CKIN, I2C4_SCL, SDMMC2_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH1_GMII_TXD3/ ETH1_MII_TXD3/ ETH1_RGMII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	-	K9	VDDCORE	S	-	-	-	-
V6	U7	AB9	Y8	PG8	I/O	FT_e	-	TRACED15, TIM2_CH1/TIM2_ETR, ETH_CLK, TIM8_ETR, SPI6_NSS, SAI4_D2, USART6_RTS/USART6_DE, USART3_RTS/USART3_DE, SPDIFRX_IN2, SAI4_FS_A, ETH1_PPS_OUT, LCD_G7, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	N5	-	P11	VDD	S	-	-	-	-
U7	V7	AB11	AA9	PG10	I/O	FT_h	-	TRACED10, UART8_CTS, LCD_G3, SAI2_SD_B, QUADSPI_BK2_IO2, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	F5	W3	-	VSS	S	-	-	-	-
1J4	W7	AA9	W11	PE9	I/O	FT_ha	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS/UART7_DE, QUADSPI_BK2_IO2, FMC_AD6/FMC_D6, EVENTOUT	-
-	G9	-	-	VDDCORE	S	-	-	-	-
V7	T10	AA11	W10	PE7	I/O	FT_h	-	TIM1_ETR, TIM3_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_AD4/FMC_D4, EVENTOUT	-
1C3	F7	-	G6	VSS	S	-	-	-	-
U8	V8	AC10	AB9	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, I2C1_SMBA, USART3_CTS/USART3_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
1D5	G11	1C4	-	VDDCORE	S	-	-	-	-
W7	W8	AB12	AA10	PF7	I/O	FT_ha	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, QUADSPI_BK1_IO2, EVENTOUT	-
V8	U10	AC11	AB10	PF8	I/O	FT_ha	-	TRACED12, TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS/UART7_DE, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	K11	VDDCORE	S	-	-	-	-
1J7	U9	Y12	V12	PF10	I/O	FT_h	-	TIM16_BKIN, SAI1_D3, SAI4_D4, SAI1_D4, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	-
-	F9	AA5	G8	VSS	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
U10	V9	AA13	AA11	PF6	I/O	FT_ha	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, SAI4_SCK_B, EVENTOUT	-
-	H4	-	-	VDDCORE	S	-	-	-	-
U14	U11	Y18	W12	PD12	I/O	FT_fha	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, I2C1_SCL, USART3_RTS/USART3_DE, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
-	F11	AA8	G10	VSS	S	-	-	-	-
V9	W9	AA14	AB11	PF9	I/O	FT_ha	-	TRACED13, TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	-
-	H6	1C6	K13	VDDCORE	S	-	-	-	-
V11	W10	AC14	Y11	PG7	I/O	FT_h	-	TRACED5, SAI1_MCLK_A, USART6_CK, UART8_RTS/UART8_DE, QUADSPI_CLK, QUADSPI_BK2_IO3, DCMI_D13, LCD_CLK, EVENTOUT	-
1E3	F15	-	G12	VSS	S	-	-	-	-
1F5	-	-	-	VDDCORE	S	-	-	-	-
W11	T12	Y14	W13	PB6	I/O	FT_fha	-	TIM16_CH1N, TIM4_CH1, I2C1_SCL, CEC, I2C4_SCL, USART1_TX, FDCAN2_TX, QUADSPI_BK1_NCS, DFSDM1_DATIN5, UART5_TX, DCMI_D5, EVENTOUT	-
U12	T11	AC13	Y12	PE8	I/O	FT_h	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_AD5/FMC_D5, EVENTOUT	-
V12	V10	Y15	W14	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_AD7/FMC_D7, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	H8	1D1	K15	VDDCORE	S	-	-	-	-
V13	T13	Y16	V13	PB2	I/O	FT_ha	-	TRACED4, RTC_OUT2, SAI1_D1, DFSDM1_CKIN1, USART1_RX, I2S_CKIN, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, UART4_RX, QUADSPI_CLK, EVENTOUT	-
-	H10	-	-	VDDCORE	S	-	-	-	-
U13	U12	AA19	V14	PD13	I/O	FT_fha	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, I2C1_SDA, I2S3_MCK, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, DSI_TE, EVENTOUT	-
-	N7	-	-	VDD	S	-	-	-	-
-	G2	AA12	G14	VSS	S	-	-	-	-
1J8	V16	AB18	AA17	USB_RREF	A	A	-	-	-
-	W12	AA15	AB13	VDD3V3_ USBHS	S	-	-	-	-
1H7	-	-	-	VDD3V3_ USB	S	-	-	-	-
V10	W13	AC16	AB14	USB_DP2	A	FT_u	-	-	USBH_HS_DP2 , OTG_HS_DP
W10	V13	AB16	AA14	USB_DM2	A	FT_u	-	-	USBH_HS_DM 2, OTG_HS_DM
-	U13	AA16	Y13	VSS_USBHS	S	-	-	-	-
-	-	-	Y14	VSS_USBHS	S	-	-	-	-
U11	T15	AB13	AA12	BYPASS_ REG1V8	I	FT	-	-	-
W8	T14	Y13	W15	PG9	I/O	FT_h	-	DBTRGO, USART6_RX, SPDIFRX_IN3, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, LCD_R1, EVENTOUT	-
1G3	-	1H5	R10	VDD	S	-	-	-	-
-	N9	-	-	VDD	S	-	-	-	-
1H5	V11	AB14	AB12	VDDA1V8_ REG	S	-	-	-	-
1H3	-	-	G17	VSS	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
1J6	W11	AB15	AB17	VDDA1V1_REG	S	-	-	-	-
-	G4	AA21	H7	VSS	S	-	-	-	-
-	-	-	R12	VDD	S	-	-	-	-
-	P6	-	-	VDD	S	-	-	-	-
-	U14	-	Y15	VSS_USBHS	S	-	-	-	-
-	V12	-	AA13	VSS_USBHS	S	-	-	-	-
1D4	G6	AC1	J9	VSS	S	-	-	-	-
-	V15	-	AA16	VSS_USBHS	S	-	-	-	-
W14	W14	AB17	AB15	USB_DM1	A	FT_u	-	-	USBH_HS_DM1
V14	V14	AC17	AA15	USB_DP1	A	FT_u	-	-	USBH_HS_DP1
V15	U16	AB19	W16	PA12	I/O	FT_uf	-	TIM1_ETR, I2C6_SDA, I2C5_SDA, UART4_TX, USART1_RTS/USART1_DE, SAI2_FS_B, FDCAN1_TX, LCD_R5, EVENTOUT	OTG_FS_DP
-	G8	-	J11	VSS	S	-	-	-	-
-	-	-	L8	VDDCORE	S	-	-	-	-
U15	V17	AA18	Y16	PA11	I/O	FT_uf	-	TIM1_CH4, I2C6_SCL, I2C5_SCL, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, LCD_R4, EVENTOUT	OTG_FS_DM
1C6	H12	1D3	-	VDDCORE	S	-	-	-	-
1F4	G10	AC23	-	VSS	S	-	-	-	-
-	W15	AA17	AB16	VDD3V3_USBFS	S	-	-	-	-
V16	U15	AC19	V15	OTG_VBUS	A	FT_u	-	-	OTG_FS_VBUS, OTG_HS_VBUS
U16	T16	Y17	Y17	PA10	I/O	FT_u	-	TIM1_CH3, SPI3_NSS/I2S3_WS, USART1_RX, MDIOS_MDIO, SAI4_FS_B, DCMI_D1, LCD_B1, EVENTOUT	OTG_FS_ID, OTG_HS_ID
-	-	AB20	AB20	DDR_DQ27	I/O	DDR	-	-	-
1B9	E15	1A8	E18	VDDQ_DDR	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	AB21	AB21	DDR_DQ26	I/O	DDR	-	-	-
-	G12	-	J13	VSS	S	-	-	-	-
-	-	AC22	AA21	DDR_DQ28	I/O	DDR	-	-	-
1H4	G14	1A3	J17	VSS	S	-	-	-	-
-	-	AC21	AA20	DDR_DQ29	I/O	DDR	-	-	-
-	-	Y22	W20	DDR_DQ25	I/O	DDR	-	-	-
-	-	AB22	Y21	DDR_DQS3P	I/O	DDR	-	-	-
-	H5	-	J20	VSS	S	-	-	-	-
-	-	AB23	Y22	DDR_DQS3N	I/O	DDR	-	-	-
-	-	-	F17	VDDQ_DDR	S	-	-	-	-
-	-	AA20	AA22	DDR_DQM3	O	DDR	-	-	-
-	F14	1B7	-	VDDQ_DDR	S	-	-	-	-
-	-	AA22	W21	DDR_DQ31	I/O	DDR	-	-	-
-	H7	1A5	K3	VSS	S	-	-	-	-
-	-	AA23	W22	DDR_DQ30	I/O	DDR	-	-	-
U9	H9	1A7	K7	VSS	S	-	-	-	-
-	-	Y23	V22	DDR_DQ24	I/O	DDR	-	-	-
-	-	-	G16	VDDQ_DDR	S	-	-	-	-
-	-	-	L10	VDDCORE	S	-	-	-	-
W16	W16	AC20	AB19	DDR_VREF	A	A	-	-	-
-	H11	-	K10	VSS	S	-	-	-	-
W17	W18	W23	V20	DDR_DQ12	I/O	DDR	-	-	-
1C5	H13	1B2	K12	VSS	S	-	-	-	-
V17	W17	Y21	V21	DDR_DQ15	I/O	DDR	-	-	-
-	H15	-	K14	VSS	S	-	-	-	-
U17	V18	W22	U21	DDR_DQ14	I/O	DDR	-	-	-
W18	V19	W21	T20	DDR_DQ11	I/O	DDR	-	-	-
-	G15	1B9	H17	VDDQ_DDR	S	-	-	-	-
V19	U19	U22	T22	DDR_DQS1P	I/O	DDR	-	-	-
1E5	-	1B4	L9	VSS	S	-	-	-	-
U18	T19	U23	R22	DDR_DQS1N	I/O	DDR	-	-	-
V18	U18	V22	T21	DDR_DQM1	O	DDR	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
1D9	-	-	J16	VDDQ_DDR	S	-	-	-	-
T18	T18	T23	R20	DDR_DQ13	I/O	DDR	-	-	-
-	J3	1B6	-	VSS	S	-	-	-	-
U19	T17	U21	R21	DDR_DQ9	I/O	DDR	-	-	-
1G5	J6	-	L11	VSS	S	-	-	-	-
T19	R18	T22	P21	DDR_DQ10	I/O	DDR	-	-	-
-	H14	-	-	VDDQ_DDR	S	-	-	-	-
R18	P18	T21	N22	DDR_DQ8	I/O	DDR	-	-	-
-	J8	1B8	L13	VSS	S	-	-	-	-
1J5	J10	-	L17	VSS	S	-	-	-	-
1F8	N19	Y19	AA19	DDR_ATO	A	A	-	-	-
-	J7	-	-	VDDCORE	S	-	-	-	-
-	-	1C8	-	VDDQ_DDR	S	-	-	-	-
1G9	N16	W20	U19	DDR_A6	O	DDR	-	-	-
-	-	-	K17	VDDQ_DDR	S	-	-	-	-
T17	R17	Y20	U18	DDR_A8	O	DDR	-	-	-
-	J12	1C1	L19	VSS	S	-	-	-	-
R17	P17	V20	T18	DDR_A4	O	DDR	-	-	-
1A6	J14	1C3	L20	VSS	S	-	-	-	-
P17	P19	T20	R19	DDR_CKE	O	DDR	-	-	-
P18	N17	U20	R18	DDR_BA1	O	DDR	-	-	-
-	J15	-	L16	VDDQ_DDR	S	-	-	-	-
N18	N18	R21	P18	DDR_A14	O	DDR	-	-	-
-	K2	-	M7	VSS	S	-	-	-	-
N19	M18	R20	P19	DDR_A11	O	DDR	-	-	-
-	K5	1C5	M10	VSS	S	-	-	-	-
1D6	K7	-	M12	VSS	S	-	-	-	-
M17	M19	R22	N18	DDR_A10	O	DDR	-	-	-
-	J9	1D5	L12	VDDCORE	S	-	-	-	-
-	-	1D9	-	VDDQ_DDR	S	-	-	-	-
M18	L17	P23	N19	DDR_A12	O	DDR	-	-	-
M19	M17	P22	M18	DDR_A1	O	DDR	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	K9	1C7	M14	VSS	S	-	-	-	-
J19	K17	N20	M22	DDR_CASN	O	DDR	-	-	-
1F6	K11	-	N9	VSS	S	-	-	-	-
J18	J17	M20	M21	DDR_WEN	O	DDR	-	-	-
-	K14	-	M17	VDDQ_DDR	S	-	-	-	-
1E9	L18	N21	M20	DDR_RASN	O	DDR	-	-	-
L17	L19	N22	N20	DDR_CLKP	O	DDR	-	-	-
-	K13	1C9	-	VSS	S	-	-	-	-
K18	K19	N23	N21	DDR_CLKN	O	DDR	-	-	-
1F9	-	1E8	N16	VDDQ_DDR	S	-	-	-	-
1D8	K18	K20	L22	DDR_DTO0	O	DDR	-	-	-
1C8	J19	L21	K21	DDR_DTO1	O	DDR	-	-	-
L18	L16	P20	M19	DDR_A15	O	DDR	-	-	-
1H6	-	1D2	N11	VSS	S	-	-	-	-
1E6	-	-	-	VDDCORE	S	-	-	-	-
-	K15	-	N13	VSS	S	-	-	-	-
J17	J18	M22	L18	DDR_CSN	O	DDR	-	-	-
H18	H19	L22	L21	DDR_ODT	O	DDR	-	-	-
H17	J16	M21	K18	DDR_BA2	O	DDR	-	-	-
1C7	L6	1D4	N17	VSS	S	-	-	-	-
G18	H18	L20	K19	DDR_A0	O	DDR	-	-	-
-	L15	-	P17	VDDQ_DDR	S	-	-	-	-
G19	G19	L23	K20	DDR_BA0	O	DDR	-	-	-
E17	F17	F20	G18	DDR_A13	O	DDR	-	-	-
-	L8	-	P3	VSS	S	-	-	-	-
F17	G18	J20	J18	DDR_A2	O	DDR	-	-	-
1E7	L10	1D6	P7	VSS	S	-	-	-	-
F19	F19	K22	J19	DDR_A3	O	DDR	-	-	-
-	-	1F9	-	VDDQ_DDR	S	-	-	-	-
C16	G16	D20	F19	DDR_ RESETN	O	DDR	-	-	-
-	M14	-	R16	VDDQ_DDR	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
1C9	H17	H20	H19	DDR_A5	O	DDR	-	-	-
-	L12	1D8	P10	VSS	S	-	-	-	-
1A9	E17	E20	F18	DDR_A7	O	DDR	-	-	-
-	L14	-	P12	VSS	S	-	-	-	-
1A8	F18	K23	K22	DDR_ZQ	A	A	-	-	-
E18	G17	G20	H18	DDR_A9	O	DDR	-	-	-
1G7	M5	1E1	P14	VSS	S	-	-	-	-
-	J11	1D7	L14	VDDCORE	S	-	-	-	-
D18	E18	J21	J21	DDR_DQ4	I/O	DDR	-	-	-
-	M7	-	P20	VSS	S	-	-	-	-
D19	D17	J22	H20	DDR_DQ5	I/O	DDR	-	-	-
W13	M9	1E3	-	VSS	S	-	-	-	-
C18	D18	H21	H21	DDR_DQ2	I/O	DDR	-	-	-
-	-	-	T17	VDDQ_DDR	S	-	-	-	-
C19	D19	H22	H22	DDR_DQ6	I/O	DDR	-	-	-
-	-	1G8	-	VDDQ_DDR	S	-	-	-	-
B19	C19	G22	G22	DDR_DQS0P	I/O	DDR	-	-	-
-	M11	-	R8	VSS	S	-	-	-	-
B18	B19	G23	G21	DDR_DQS0N	I/O	DDR	-	-	-
-	N15	-	-	VDDQ_DDR	S	-	-	-	-
C17	C18	H23	G20	DDR_DQM0	O	DDR	-	-	-
1H9	-	-	U16	VDDQ_DDR	S	-	-	-	-
B17	B18	G21	G19	DDR_DQ7	I/O	DDR	-	-	-
1B8	M13	1E5	R17	VSS	S	-	-	-	-
A18	A18	F22	F21	DDR_DQ1	I/O	DDR	-	-	-
-	M15	1E7	T7	VSS	S	-	-	-	-
A17	A17	E22	E21	DDR_DQ0	I/O	DDR	-	-	-
B16	B17	E21	E20	DDR_DQ3	I/O	DDR	-	-	-
-	P14	1H9	V17	VDDQ_DDR	S	-	-	-	-
1H8	-	-	T9	VSS	S	-	-	-	-
-	J13	-	-	VDDCORE	S	-	-	-	-
-	-	E23	E22	DDR_DQ21	I/O	DDR	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	N6	1E9	T11	VSS	S	-	-	-	-
-	-	D21	D20	DDR_DQ22	I/O	DDR	-	-	-
C14	N8	-	T19	VSS	S	-	-	-	-
-	-	D22	D21	DDR_DQ17	I/O	DDR	-	-	-
-	-	D23	D22	DDR_DQ18	I/O	DDR	-	-	-
-	-	-	W18	VDDQ_DDR	S	-	-	-	-
-	-	C22	C21	DDR_DQS2P	I/O	DDR	-	-	-
-	N10	1F2	U7	VSS	S	-	-	-	-
-	-	B23	B22	DDR_DQS2N	I/O	DDR	-	-	-
-	R15	1J8	-	VDDQ_DDR	S	-	-	-	-
-	-	C23	C22	DDR_DQM2	O	DDR	-	-	-
-	-	-	Y19	VDDQ_DDR	S	-	-	-	-
-	-	B22	B21	DDR_DQ16	I/O	DDR	-	-	-
-	N12	1F4	U13	VSS	S	-	-	-	-
-	-	A22	A21	DDR_DQ23	I/O	DDR	-	-	-
1J9	N14	-	U15	VSS	S	-	-	-	-
-	-	B21	B20	DDR_DQ19	I/O	DDR	-	-	-
-	-	A21	A20	DDR_DQ20	I/O	DDR	-	-	-
-	-	1J4	-	VDD	S	-	-	-	-
-	P7	1F6	-	VSS	S	-	-	-	-
-	-	-	M11	VDDCORE	S	-	-	-	-
C15	D15	C20	E17	JTMS-SWDIO	I/O	FTU	-	-	-
A16	D16	B20	D17	JTCK-SWCLK	I	FTD	-	-	-
A15	D14	A19	E16	JTDO-TRACESWO	O	FTU	-	-	-
B15	D13	A20	D16	JTDI	I	FTU	-	-	-
1G6	K8	1E2	-	VDDCORE	S	-	-	-	-
B14	D12	B19	E15	NJTRST	I	FTU	-	-	-
-	G13	-	D18	VDD_PLL2	S	-	-	-	-
-	F13	-	D19	VSS_PLL2	S	-	-	-	-
1B6	B12	C14	B14	VDDA1V8_DSI	S	-	-	-	-
-	C12	C16	C14	VSS_DSI	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	C13	-	C15	VSS_DSI	S	-	-	-	-
A13	B15	B17	B17	DSI_D1P	A	DSI	-	-	-
B13	A15	A17	A17	DSI_D1N	A	DSI	-	-	-
1B7	A16	C17	A18	VDD1V2_DSI_PHY	S	-	-	-	-
B12	A14	A16	A16	DSI_CKN	A	DSI	-	-	-
A12	B14	B16	B16	DSI_CKP	A	DSI	-	-	-
-	C14	-	C16	VSS_DSI	S	-	-	-	-
-	C15	-	C17	VSS_DSI	S	-	-	-	-
-	C16	-	C18	VSS_DSI	S	-	-	-	-
B11	B13	C15	B15	DSI_D0P	A	DSI	-	-	-
C12	A13	B15	A15	DSI_D0N	A	DSI	-	-	-
-	P8	-	T13	VDD	S	-	-	-	-
C13	A12	B18	A14	VDD_DSI	S	-	-	-	-
1A7	B16	C18	B18	VDD1V2_DSI_REG	S	-	-	-	-
D17	P9	-	U17	VSS	S	-	-	-	-
C11	A11	D16	D15	PC11	I/O	FT_ha	-	TRACED3, DFSDM1_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SAI4_SCK_B, SDMMC1_D3, DCMI_D4, EVENTOUT	-
-	K10	-	-	VDDCORE	S	-	-	-	-
A10	B11	D19	F15	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SDMMC2_CKIN, SDMMC1_CKIN, SDMMC2_D4, SDMMC1_D4, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
-	-	-	M13	VDDCORE	S	-	-	-	-
A9	C11	D18	E14	PC8	I/O	FT_ha	-	TRACED0, TIM3_CH3, TIM8_CH3, UART4_TX, USART6_CK, UART5_RTS/UART5_DE, SDMMC1_D0, DCMI_D2, EVENTOUT	-
-	P11	1F8	U20	VSS	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
B10	D11	D15	F14	PC10	I/O	FT_ha	-	TRACED2, DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SAI4_MCLK_B, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
1D7	K12	1E4	-	VDDCORE	S	-	-	-	-
B6	B9	B13	C13	PB4	I/O	FT_ha	-	TRACED8, TIM16_BKIN, TIM3_CH1, SAI4_CK2, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, SAI4_SCK_A, UART7_TX, EVENTOUT	-
B9	A10	D17	D14	PC9	I/O	FT_fh	-	TRACED1, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	-
G17	P13	1G3	V5	VSS	S	-	-	-	-
C10	A9	B11	D13	PC7	I/O	FT_ha	-	HDP4, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, SDMMC2_D123DIR, SDMMC2_D7, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
-	L9	-	M15	VDDCORE	S	-	-	-	-
A4	D10	B14	E13	PC6	I/O	FT_ha	-	HDP1, TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, SDMMC2_D0DIR, SDMMC2_D6, DSI_TE, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
-	-	A14	F13	PF2	I/O	FT_h	-	I2C2_SMBA, SDMMC2_D0DIR, SDMMC3_D0DIR, SDMMC1_D0DIR, FMC_A2, EVENTOUT	-
1A5	B10	D12	D12	PD2	I/O	FT_ha	-	TIM3_ETR, I2C5_SMBA, UART4_RX, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
1G4	P10	-	-	VDD	S	-	-	-	-
-	P15	-	V16	VSS	S	-	-	-	-
-	-	1E6	-	VDDCORE	S	-	-	-	-
B8	B8	A13	B13	PA8	I/O	FT_fh	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, SPI3_MOSI/I2S3_SDO, USART1_CK, SDMMC2_CKIN, SDMMC2_D4, OTG_FS_SOF/OTG_HS_SOF, SAI4_SD_B, UART7_RX, LCD_R6, EVENTOUT	-
1A4	C9	C13	A13	PB14	I/O	FT_h	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS/USART3_DE, SDMMC2_D0, EVENTOUT	-
1B4	C10	D13	E12	PC12	I/O	FT_h	-	TRACECLK, MCO2, SAI4_D3, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SAI4_SD_B, SDMMC1_CK, DCMI_D9, EVENTOUT	-
K17	R2	1G5	V18	VSS	S	-	-	-	-
C8	A8	B12	B12	PB15	I/O	FT_h	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, SDMMC2_D1, EVENTOUT	-
-	L11	-	N12	VDDCORE	S	-	-	-	-
B7	B7	C11	C12	PE5	I/O	FT_h	-	TRACED3, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SDMMC2_D0DIR, SDMMC1_D0DIR, SDMMC2_D6, SDMMC1_D6, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
-	-	-	U12	VDD	S	-	-	-	-
C7	A7	A11	A12	PB3	I/O	FT_h	-	TRACED9, TIM2_CH2, SAI4_CK1, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, SAI4_MCLK_A, UART7_RX, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	R6	-	V19	VSS	S	-	-	-	-
B5	A6	A10	D11	PG6	I/O	FT_h	-	TRACED14, TIM17_BKIN, SDMMC2_CMD, DCMI_D12, LCD_R7, EVENTOUT	-
1F7	-	-	-	VDDCORE	S	-	-	-	-
A7	C6	D14	B11	PD3	I/O	FT_h	-	HDP5, DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS/USART2_NSS, SDMMC1_D123DIR, SDMMC2_D7, SDMMC2_D123DIR, SDMMC1_D7, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
C9	D9	B10	F12	PB9	I/O	FT_fh	-	HDP7, TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC2_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, SDMMC1_CDIR, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
B4	C7	C19	E11	PA15	I/O	FT_h	-	DBTRGI, TIM2_CH1/TIM2_ETR, SAI4_D2, SDMMC1_CDIR, CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS/UART4_DE, SDMMC2_D5, SDMMC2_CDIR, SDMMC1_D5, SAI4_FS_A, UART7_TX, LCD_R1, EVENTOUT	-
N17	-	1G7	W17	VSS	S	-	-	-	-
C6	C8	A8	A11	PA9	I/O	FT_h	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, SDMMC2_CDIR, SDMMC2_D5, DCMI_D0, LCD_R5, EVENTOUT	-
A3	B5	D11	F11	PB7	I/O	FT_fh	-	TIM17_CH1N, TIM4_CH2, I2C1_SDA, I2C4_SDA, USART1_RX, SDMMC2_D1, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT	-
-	L13	1F5	N14	VDDCORE	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
A2	A4	B9	B10	PD1	I/O	FT_fh	-	I2C6_SCL, DFSDM1_DATIN6, I2C5_SCL, SAI3_SD_A, UART4_TX, FDCAN1_TX, SDMMC3_D0, DFSDM1_CKIN7, FMC_AD3/FMC_D3, EVENTOUT	-
-	R9	1J6	-	VDD	S	-	-	-	-
C5	A3	B8	C10	PD0	I/O	FT_fh	-	I2C6_SDA, DFSDM1_CKIN6, I2C5_SDA, SAI3_SCK_A, UART4_RX, FDCAN1_RX, SDMMC3_CMD, DFSDM1_DATIN7, FMC_AD2/FMC_D2, EVENTOUT	-
-	R8	-	W19	VSS	S	-	-	-	-
1A3	A5	C9	A10	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SDMMC2_CK, FMC_A19, EVENTOUT	-
C4	D7	A7	A9	PD5	I/O	FT_h	-	USART2_TX, SDMMC3_D2, FMC_NWE, EVENTOUT	-
B3	B4	D10	F10	PD7	I/O	FT_fh	-	TRACED6, DFSDM1_DATIN4, I2C2_SCL, DFSDM1_CKIN1, USART2_CK, SPDIFRX_IN0, SDMMC3_D3, FMC_NE1, EVENTOUT	-
-	M10	-	-	VDDCORE	S	-	-	-	-
B1	A2	B7	D10	PG15	I/O	FT_fh	-	TRACED7, SAI1_D2, I2C2_SDA, SAI1_FS_A, USART6_CTS/USART6_NSS, SDMMC3_CK, DCMI_D13, EVENTOUT	-
B2	B3	C10	E9	PE6	I/O	FT_h	-	TRACED2, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SDMMC2_D0, SDMMC1_D2, SAI2_MCLK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	R10	1G9	Y3	VSS	S	-	-	-	-
-	-	D8	E10	PF0	I/O	FT_fh	-	I2C2_SDA, SDMMC3_D0, SDMMC3_CKIN, FMC_A0, EVENTOUT	-
-	-	-	P13	VDDCORE	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	-	A5	B9	PF1	I/O	FT_fh	-	I2C2_SCL, SDMMC3_CMD, SDMMC3_CDIR, FMC_A1, EVENTOUT	-
F18	R12	1H4	-	VSS	S	-	-	-	-
-	-	D9	F9	PF4	I/O	FT_h	-	USART2_RX, SDMMC3_D1, SDMMC3_D123DIR, FMC_A4, EVENTOUT	-
1E8	M12	1F7	-	VDDCORE	S	-	-	-	-
C3	D6	B6	C9	PD4	I/O	FT_h	-	SAI3_FS_A, USART2_RTS/USART2_DE, SDMMC3_D1, DFSDM1_CKIN0, FMC_NOE, EVENTOUT	-
-	-	-	U14	VDD	S	-	-	-	-
-	-	D7	D9	PF5	I/O	FT_h	-	USART2_TX, SDMMC3_D2, FMC_A5, EVENTOUT	-
-	R14	-	Y7	VSS	S	-	-	-	-
1A2	C5	B5	A8	PD10	I/O	FT_h	-	RTC_REFIN, TIM16_BKIN, DFSDM1_CKOUT, I2C5_SMBA, SPI3_MISO/I2S3_SDI, SAI3_FS_B, USART3_CK, FMC_AD15/FMC_D15, LCD_B3, EVENTOUT	-
-	N11	-	P15	VDDCORE	S	-	-	-	-
-	-	-	B8	PJ12	I/O	FT	-	LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	A7	PJ13	I/O	FT	-	LCD_G4, LCD_B1, EVENTOUT	-
-	-	-	B7	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
A19	R16	1H6	Y10	VSS	S	-	-	-	-
-	-	-	C7	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	-	1G6	-	VDDCORE	S	-	-	-	-
-	-	-	D8	PK0	I/O	FT_h	-	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-
-	-	-	E7	PK1	I/O	FT_h	-	TRACED4, TIM1_CH1, HDP4, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT	-
-	-	-	E8	PK2	I/O	FT_h	-	TRACED5, TIM1_BKIN, HDP5, TIM8_BKIN, LCD_G7, EVENTOUT	-
-	R11	-	-	VDD	S	-	-	-	-
-	T4	-	Y18	VSS	S	-	-	-	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
-	N13	-	R14	VDDCORE	S	-	-	-	-
-	-	-	B6	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	A6	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	C6	PK5	I/O	FT_h	-	TRACED6, HDP6, LCD_B6, EVENTOUT	-
K19	U3	1H8	Y20	VSS	S	-	-	-	-
-	-	-	A5	PK6	I/O	FT_h	-	TRACED7, HDP7, LCD_B7, EVENTOUT	-
1G8	P12	-	-	VDDCORE	S	-	-	-	-
-	-	-	B5	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
C2	C4	D6	C5	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, LPTIM2_ETR, SPI3_SCK/I2S3_CK, SAI4_MCLK_B, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
1A1	B1	C8	D7	PE1	I/O	FT	-	LPTIM1_IN2, I2S2_MCK, SAI3_SD_B, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	U6	1J3	AA4	VSS	S	-	-	-	-
-	-	D5	D6	PH8	I/O	FT_f	-	TIM5_ETR, I2C3_SDA, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	1H7	T15	VDDCORE	S	-	-	-	-
-	-	C5	E6	PH9	I/O	FT	-	TIM12_CH2, I2C3_SMBA, DCMI_D0, LCD_R3, EVENTOUT	-
D2	C1	A4	D5	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, SPI4_NSS, USART6_CK, SAI2_SD_B, FMC_AD8/FMC_D8, DCMI_D4, LCD_G3, EVENTOUT	-
C1	D2	B4	E4	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK, SDMMC1_D0DIR, SAI2_SCK_B, FMC_AD9/FMC_D9, LCD_B4, EVENTOUT	-

Table 7. STM32MP157A pin and ball definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TFBGA257	LFBGA354	TFBGA361	LFBGA448					Alternate functions	Additional functions
E3	C2	A3	A4	PE13	I/O	FT_h	-	HDP2, TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_AD10/FMC_D10, DCMI_D6, LCD_DE, EVENTOUT	-
-	R13	-	-	VDDCORE	S	-	-	-	-
-	-	C4	B3	PH11	I/O	FT_f	-	TIM5_CH2, I2C4_SCL, I2C1_SCL, DCMI_D2, LCD_R5, EVENTOUT	-
R19	U8	-	AA18	VSS	S	-	-	-	-
-	U17	1J5	AB1	VSS	S	-	-	-	-
W19	W1	-	AB18	VSS	S	-	-	-	-
-	W19	1J7	AB22	VSS	S	-	-	-	-
1B2	D3	C6	B4	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, UART8_RTS/UART8_DE, SAI2_MCLK_B, SDMMC1_D123DIR, FMC_AD11/FMC_D11, LCD_G0, LCD_CLK, EVENTOUT	-
D3	E1	D3	C4	PE15	I/O	FT	-	HDP3, TIM1_BKIN, TIM15_BKIN, USART2_CTS/USART2_NSS, UART8_CTS, FMC_NCE2, FMC_AD12/FMC_D12, LCD_R7, EVENTOUT	-
-	-	B3	A3	PH4	I/O	FT_f	-	I2C2_SCL, LCD_G5, LCD_G4, EVENTOUT	-

1. IO supplied by VSW domain.

Table 8. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	-	-	USART2_CTS/ USART2_NSS
	PA1	ETH_CLK	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	-	USART2_RTS/ USART2_DE
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_OUT	TIM15_CH2	-	-	USART2_RX
	PA4	HDP0	-	TIM5_ETR	-	SAI4_D2	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART2_CK
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_CH1N	SAI4_CK1	SPI1_SCK/I2S1 _CK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	SAI4_CK2	SPI1_MISO/ I2S1_SDI	-	-
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	SAI4_D1	SPI1_MOSI/ I2S1_SDO	-	-
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	SPI3_MOSI/ I2S3_SDO	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/ I2S2_CK	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	SPI3_NSS/ I2S3_WS	-	USART1_RX
	PA11	-	TIM1_CH4	I2C6_SCL	-	I2C5_SCL	SPI2_NSS/ I2S2_WS	UART4_RX	USART1_CTS/ USART1_NSS
	PA12	-	TIM1_ETR	I2C6_SDA	-	I2C5_SDA	-	UART4_TX	USART1_RTS/ USART1_DE

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port A	PA13	DBTRGO	DBTRGI	MCO1	-	-	-	-	-
	PA14	DBTRGO	DBTRGI	MCO2	-	-	-	-	-
	PA15	DBTRGI	TIM2_CH1/ TIM2_ETR	SAI4_D2	SDMMC1_ CDIR	CEC	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	SPI6_NSS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM1_ CKOUT	-
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_ DATIN1	-
	PB2	TRACED4	RTC_OUT2	SAI1_D1	DFSDM1_ CKIN1	USART1_RX	I2S_CKIN	SAI1_SD_A	SPI3_MOSI/ I2S3_SDO
	PB3	TRACED9	TIM2_CH2	-	-	SAI4_CK1	SPI1_SCK/ I2S1_CK	SPI3_SCK/ I2S3_CK	-
	PB4	TRACED8	TIM16_BKIN	TIM3_CH1	-	SAI4_CK2	SPI1_MISO/ I2S1_SDI	SPI3_MISO/ I2S3_SDI	SPI2_NSS/ I2S2_WS
	PB5	ETH_CLK	TIM17_BKIN	TIM3_CH2	SAI4_D1	I2C1_SMBA	SPI1_MOSI/ I2S1_SDO	I2C4_SMBA	SPI3_MOSI/ I2S3_SDO
	PB6	-	TIM16_CH1N	TIM4_CH1	-	I2C1_SCL	CEC	I2C4_SCL	USART1_TX
	PB7	-	TIM17_CH1N	TIM4_CH2	-	I2C1_SDA	-	I2C4_SDA	USART1_RX
	PB8	HDP6	TIM16_CH1	TIM4_CH3	DFSDM1_ CKIN7	I2C1_SCL	SDMMC1_ CKIN	I2C4_SCL	SDMMC2_ CKIN
	PB9	HDP7	TIM17_CH1	TIM4_CH4	DFSDM1_ DATIN7	I2C1_SDA	SPI2_NSS/ I2S2_WS	I2C4_SDA	SDMMC2_ CDIR
	PB10	-	TIM2_CH3	-	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/ I2S2_CK	DFSDM1_ DATIN7	USART3_TX

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port B	PB11	-	TIM2_CH4	-	LPTIM2_ETR	I2C2_SDA	-	DFSDM1_ CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	I2C6_SMBA	-	I2C2_SMBA	SPI2_NSS/ I2S2_WS	DFSDM1_ DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	DFSDM1_ CKOUT	LPTIM2_OUT	SPI2_SCK/ I2S2_CK	DFSDM1_ CKIN1	USART3_CTS/ USART3_NSS
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/ I2S2_SDI	DFSDM1_ DATIN2	USART3_RTS/ USART3_DE
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/ I2S2_SDO	DFSDM1_ CKIN2	-
Port C	PC0	-	-	-	DFSDM1_ CKIN0	LPTIM2_IN2	-	DFSDM1_ DATIN4	-
	PC1	TRACED0	-	SAI1_D1	DFSDM1_ DATIN0	DFSDM1_ CKIN4	SPI2_MOSI/ I2S2_SDO	SAI1_SD_A	-
	PC2	-	-	-	DFSDM1_ CKIN1	-	SPI2_MISO/ I2S2_SDI	DFSDM1_ CKOUT	-
	PC3	TRACECLK	-	-	DFSDM1_ DATIN1	-	SPI2_MOSI/ I2S2_SDO	-	-
	PC4	-	-	-	DFSDM1_ CKIN2	-	I2S1_MCK	-	-
	PC5	-	-	SAI1_D3	DFSDM1_ DATIN2	SAI4_D4	-	SAI1_D4	-
	PC6	HDP1	-	TIM3_CH1	TIM8_CH1	DFSDM1_ CKIN3	I2S2_MCK	-	USART6_TX

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port C	PC7	HDP4	-	TIM3_CH2	TIM8_CH2	DFSDM1_ DATIN3	-	I2S3_MCK	USART6_RX
	PC8	TRACED0	-	TIM3_CH3	TIM8_CH3	-	-	UART4_TX	USART6_CK
	PC9	TRACED1	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-
	PC10	TRACED2	-	-	DFSDM1_ CKIN5	-	-	SPI3_SCK/ I2S3_CK	USART3_TX
	PC11	TRACED3	-	-	DFSDM1_ DATIN5	-	-	SPI3_MISO/ I2S3_SDI	USART3_RX
	PC12	TRACECLK	MCO2	SAI4_D3	-	-	-	SPI3_MOSI/ I2S3_SDO	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port D	PD0	-	-	I2C6_SDA	DFSDM1_ CKIN6	I2C5_SDA	-	SAI3_SCK_A	-
	PD1	-	-	I2C6_SCL	DFSDM1_ DATIN6	I2C5_SCL	-	SAI3_SD_A	-
	PD2	-	-	TIM3_ETR	-	I2C5_SMBA	-	UART4_RX	-
	PD3	HDP5	-	-	DFSDM1_ CKOUT	-	SPI2_SCK/ I2S2_CK	DFSDM1_ DATIN0	USART2_CTS/ USART2_NSS
	PD4	-	-	-	-	-	-	SAI3_FS_A	USART2_RTS/ USART2_DE
	PD5	-	-	-	-	-	-	-	USART2_TX

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port D	PD6	-	TIM16_CH1N	SAI1_D1	DFSDM1_ CKIN4	DFSDM1_ DATIN1	SPI3_MOSI/ I2S3_SDO	SAI1_SD_A	USART2_RX
	PD7	TRACED6	-	-	DFSDM1_ DATIN4	I2C2_SCL	-	DFSDM1_ CKIN1	USART2_CK
	PD8	-	-	-	DFSDM1_ CKIN3	-	-	SAI3_SCK_B	USART3_TX
	PD9	-	-	-	DFSDM1_ DATIN3	-	-	SAI3_SD_B	USART3_RX
	PD10	RTC_REFIN	TIM16_BKIN	-	DFSDM1_ CKOUT	I2C5_SMBA	SPI3_MISO/ I2S3_SDI	SAI3_FS_B	USART3_CK
	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	I2C1_SMBA	-	USART3_CTS/ USART3_NSS
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	I2C1_SCL	-	USART3_RTS/ USART3_DE
	PD13	-	LPTIM1_OUT	TIM4_CH2	-	I2C4_SDA	I2C1_SDA	I2S3_MCK	-
	PD14	-	-	TIM4_CH3	-	-	-	SAI3_MCLK_B	-
	PD15	-	-	TIM4_CH4	-	-	-	SAI3_MCLK_A	-
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	-	LPTIM2_ETR	SPI3_SCK/ I2S3_CK	SAI4_MCLK_B	-
	PE1	-	LPTIM1_IN2	-	-	-	I2S2_MCK	SAI3_SD_B	-
	PE2	TRACECLK	-	SAI1_CK1	-	I2C4_SCL	SPI4_SCK	SAI1_MCLK_A	-
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port E	PE4	TRACED1	-	SAI1_D2	DFSDM1_ DATIN3	TIM15_CH1N	SPI4_NSS	SAI1_FS_A	SDMMC2_ CKIN
	PE5	TRACED3	-	SAI1_CK2	DFSDM1_ CKIN3	TIM15_CH1	SPI4_MISO	SAI1_SCK_A	SDMMC2_ D0DIR
	PE6	TRACED2	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	SDMMC2_D0
	PE7	-	TIM1_ETR	TIM3_ETR	DFSDM1_ DATIN2	-	-	-	UART7_RX
	PE8	-	TIM1_CH1N	-	DFSDM1_ CKIN2	-	-	-	UART7_TX
	PE9	-	TIM1_CH1	-	DFSDM1_ CKOUT	-	-	-	UART7_RTS/ UART7_DE
	PE10	-	TIM1_CH2N	-	DFSDM1_ DATIN4	-	-	-	UART7_CTS
	PE11	-	TIM1_CH2	-	DFSDM1_ CKIN4	-	SPI4_NSS	-	USART6_CK
	PE12	-	TIM1_CH3N	-	DFSDM1_ DATIN5	-	SPI4_SCK	-	-
	PE13	HDP2	TIM1_CH3	-	DFSDM1_ CKIN5	-	SPI4_MISO	-	-
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-
	PE15	HDP3	TIM1_BKIN	-	-	TIM15_BKIN	-	-	USART2_CTS/ USART2_NSS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port F	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	USART2_RX
	PF5	-	-	-	-	-	-	-	USART2_TX
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	UART7_RX
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_TX
	PF8	TRACED12	TIM16_CH1N	-	-	-	SPI5_MISO	SAI1_SCK_B	UART7_RTS/ UART7_DE
	PF9	TRACED13	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	UART7_CTS
	PF10	-	TIM16_BKIN	SAI1_D3	SAI4_D4	-	-	SAI1_D4	-
	PF11	-	-	-	-	-	SPI5_MOSI	-	-
	PF12	TRACED4	-	-	-	-	-	-	-
	PF13	TRACED5	-	-	DFSDM1_ DATIN6	I2C4_SMBA	I2C1_SMBA	DFSDM1_ DATIN3	-
	PF14	TRACED6	-	-	DFSDM1_ CKIN6	I2C4_SCL	I2C1_SCL	-	-
	PF15	TRACED7	-	-	-	I2C4_SDA	I2C1_SDA	-	-
Port G	PG0	TRACED0	-	-	DFSDM1_ DATIN0	-	-	-	-
	PG1	TRACED1	-	-	-	-	-	-	-
	PG2	TRACED2	MCO2	-	TIM8_BKIN	-	-	-	-

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port G	PG3	TRACED3	-	-	TIM8_BKIN2	DFSDM1_ CKIN1	-	-	-
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-
	PG5	-	TIM1_ETR	-	-	-	-	-	-
	PG6	TRACED14	TIM17_BKIN	-	-	-	-	-	-
	PG7	TRACED5	-	-	-	-	-	SAI1_MCLK_A	USART6_CK
	PG8	TRACED15	TIM2_CH1/ TIM2_ETR	ETH_CLK	TIM8_ETR	-	SPI6_NSS	SAI4_D2	USART6_RTS/ USART6_DE
	PG9	DBTRGO	-	-	-	-	-	-	USART6_RX
	PG10	TRACED10	-	-	-	-	-	-	-
	PG11	TRACED11	-	-	-	USART1_TX	-	UART4_TX	-
	PG12	-	LPTIM1_IN1	-	-	-	SPI6_MISO	SAI4_CK2	USART6_RTS/ USART6_DE
	PG13	TRACED0	LPTIM1_OUT	SAI1_CK2	-	SAI4_CK1	SPI6_SCK	SAI1_SCK_A	USART6_CTS/ USART6_NSS
	PG14	TRACED1	LPTIM1_ETR	-	-	-	SPI6_MOSI	SAI4_D1	USART6_TX
	PG15	TRACED7	-	SAI1_D2	-	I2C2_SDA	-	SAI1_FS_A	USART6_CTS/ USART6_NSS
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	-	LPTIM1_IN2	-	-	-	-	-	-

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port H	PH3	-	-	-	DFSDM1_ CKIN4	-	-	-	-
	PH4	-	-	-	-	I2C2_SCL	-	-	-
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-
	PH6	-	-	TIM12_CH1	-	I2C2_SMBA	SPI5_SCK	-	-
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-
	PH8	-	-	TIM5_ETR	-	I2C3_SDA	-	-	-
	PH9	-	-	TIM12_CH2	-	I2C3_SMBA	-	-	-
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	I2C1_SMBA	-	-
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	I2C1_SCL	-	-
	PH12	HDP2	-	TIM5_CH3	-	I2C4_SDA	I2C1_SDA	-	-
	PH13	-	-	-	TIM8_CH1N	-	-	-	-
	PH14	-	-	-	TIM8_CH2N	-	-	-	-
	PH15	-	-	-	TIM8_CH3N	-	-	-	-
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/ I2S2_WS	-	-
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/ I2S2_CK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/ I2S2_SDI	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/ I2S2_SDO	-	-

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port I	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	-	-	-
	PI6	-	-	-	TIM8_CH2	-	-	-	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-
	PI8	-	-	-	-	-	-	-	-
	PI9	HDP1	-	-	-	-	-	-	-
	PI10	HDP0	-	-	-	-	-	-	-
	PI11	MCO1	-	-	-	-	I2S_CKIN	-	-
	PI12	TRACED0	-	HDP0	-	-	-	-	-
	PI13	TRACED1	-	HDP1	-	-	-	-	-
	PI14	TRACECLK	-	-	-	-	-	-	-
	PI15	-	-	-	-	-	-	-	-
Port J	PJ0	TRACED8	-	-	-	-	-	-	-
	PJ1	TRACED9	-	-	-	-	-	-	-
	PJ2	TRACED10	-	-	-	-	-	-	-
	PJ3	TRACED11	-	-	-	-	-	-	-
	PJ4	TRACED12	-	-	-	-	-	-	-
	PJ5	TRACED2	-	HDP2	-	-	-	-	-
	PJ6	TRACED3	-	HDP3	TIM8_CH2	-	-	-	-
	PJ7	TRACED13	-	-	TIM8_CH2N	-	-	-	-

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port J	PJ8	TRACED14	TIM1_CH3N	-	TIM8_CH1	-	-	-	-
	PJ9	TRACED15	TIM1_CH3	-	TIM8_CH1N	-	-	-	-
	PJ10	-	TIM1_CH2N	-	TIM8_CH2	-	SPI5_MOSI	-	-
	PJ11	-	TIM1_CH2	-	TIM8_CH2N	-	SPI5_MISO	-	-
	PJ12	-	-	-	-	-	-	-	-
	PJ13	-	-	-	-	-	-	-	-
	PJ14	-	-	-	-	-	-	-	-
	PJ15	-	-	-	-	-	-	-	-
Port K	PK0	-	TIM1_CH1N	-	TIM8_CH3	-	SPI5_SCK	-	-
	PK1	TRACED4	TIM1_CH1	HDP4	TIM8_CH3N	-	SPI5_NSS	-	-
	PK2	TRACED5	TIM1_BKIN	HDP5	TIM8_BKIN	-	-	-	-
	PK3	-	-	-	-	-	-	-	-
	PK4	-	-	-	-	-	-	-	-
	PK5	TRACED6	-	HDP6	-	-	-	-	-
	PK6	TRACED7	-	HDP7	-	-	-	-	-
	PK7	-	-	-	-	-	-	-	-
Port Z	PZ0	-	-	I2C6_SCL	I2C2_SCL	-	SPI1_SCK/ I2S1_CK	-	USART1_CK
	PZ1	-	-	I2C6_SDA	I2C2_SDA	I2C5_SDA	SPI1_MISO/ I2S1_SDI	I2C4_SDA	USART1_RX

Table 8. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		HDP/SYS/RTC	TIM1/2/16/17/ LPTIM1/SYS/ RTC	SAI1/4/I2C6/ TIM3/4/5/12/ HDP/SYS	SAI4/I2C2/ TIM8/ LPTIM2/3/4/5/ DFSDM1 /SDMMC1	SAI4/ I2C1/2/3/4/5/ USART1/ TIM15/LPTIM2/ DFSDM1/CEC	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5/6/I2C1/ SDMMC1/3/ CEC	SPI3/I2S3/ SAI1/3/4/ I2C4/UART4/ DFSDM1	SPI2/I2S2/ SPI3/I2S3/ SPI6/ USART1/2/3/6/ UART7/ SDMMC2
Port Z	PZ2	-	-	I2C6_SCL	I2C2_SCL	I2C5_SMBA	SPI1_MOSI/ I2S1_SDO	I2C4_SMBA	USART1_TX
	PZ3	-	-	I2C6_SDA	I2C2_SDA	I2C5_SDA	SPI1_NSS/ I2S1_WS	I2C4_SDA	USART1_CTS/ USART1_NSS
	PZ4	-	-	I2C6_SCL	I2C2_SCL	I2C5_SCL	-	I2C4_SCL	-
	PZ5	-	-	I2C6_SDA	I2C2_SDA	I2C5_SDA	-	I2C4_SDA	USART1_RTS/ USART1_DE
	PZ6	-	-	I2C6_SCL	I2C2_SCL	USART1_CK	I2S1_MCK	I2C4_SMBA	USART1_RX
	PZ7	-	-	I2C6_SDA	I2C2_SDA	-	-	-	USART1_TX

1. Refer to *Table 9* for AF8 to AF15.

Table 9. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port A	PA0	UART4_TX	SDMMC2_CMD	SAI2_SD_B	ETH1_GMII_ CRS/ ETH1_MII_CRS	-	-	-	EVENTOUT
	PA1	UART4_RX	QUADSPI_ BK1_IO3	SAI2_MCLK_B	ETH1_GMII_RX _CLK/ ETH1_MII_RX_ CLK/ ETH1_RGMII_ RX_CLK/ ETH1_RMII_ REF_CLK	-	-	LCD_R2	EVENTOUT
	PA2	SAI2_SCK_B	-	SDMMC2_ D0DIR	ETH1_MDIO	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	LCD_B2	-	ETH1_GMII_ COL/ ETH1_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	SPI6_NSS	-	-	-	SAI4_FS_A	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	SPI6_SCK	-	-	-	SAI4_MCLK_A	-	LCD_R4	EVENTOUT
	PA6	SPI6_MISO	TIM13_CH1	-	MDIOS_MDC	SAI4_SCK_A	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	SPI6_MOSI	TIM14_CH1	QUADSPI_CLK	ETH1_GMII_RX _DV/ ETH1_MII_RX_ DV/ ETH1_RGMII_ RX_CTL/ ETH1_RMII_ CRS_DV	SAI4_SD_A	-	-	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port A	PA8	SDMMC2_ CKIN	SDMMC2_D4	OTG_FS_SOF/ OTG_HS_SOF	-	SAI4_SD_B	UART7_RX	LCD_R6	EVENTOUT
	PA9	SDMMC2_ CDIR	-	SDMMC2_D5	-	-	DCMI_D0	LCD_R5	EVENTOUT
	PA10	-	-	-	MDIOS_MDIO	SAI4_FS_B	DCMI_D1	LCD_B1	EVENTOUT
	PA11	-	FDCAN1_RX	-	-	-	-	LCD_R4	EVENTOUT
	PA12	SAI2_FS_B	FDCAN1_TX	-	-	-	-	LCD_R5	EVENTOUT
	PA13	UART4_TX	-	-	-	-	-	-	EVENTOUT
	PA14	-	-	-	-	-	-	-	EVENTOUT
	PA15	UART4_RTS/ UART4_DE	SDMMC2_D5	SDMMC2_ CDIR	SDMMC1_D5	SAI4_FS_A	UART7_TX	LCD_R1	EVENTOUT
Port B	PB0	UART4_CTS	LCD_R3	-	ETH1_GMII_ RXD2/ ETH1_MII_ RXD2/ ETH1_RGMII_ RXD2	MDIOS_MDIO	-	LCD_G1	EVENTOUT
	PB1	-	LCD_R6	-	ETH1_GMII_ RXD3/ ETH1_MII_ RXD3/ ETH1_RGMII_ RXD3	MDIOS_MDC	-	LCD_G0	EVENTOUT
	PB2	UART4_RX	QUADSPI_CLK	-	-	-	-	-	EVENTOUT
	PB3	SPI6_SCK	SDMMC2_D2	-	-	SAI4_MCLK_A	UART7_RX	-	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port B	PB4	SPI6_MISO	SDMMC2_D3	-	-	SAI4_SCK_A	UART7_TX	-	EVENTOUT
	PB5	SPI6_MOSI	FDCAN2_RX	SAI4_SD_A	ETH1_PPS_ OUT	UART5_RX	DCMI_D10	LCD_G7	EVENTOUT
	PB6	-	FDCAN2_TX	QUADSPI_BK1 _NCS	DFSDM1_ DATIN5	UART5_TX	DCMI_D5	-	EVENTOUT
	PB7	-	-	SDMMC2_D1	DFSDM1_ CKIN5	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH1_GMII_ TXD3/ ETH1_MII_ TXD3/ ETH1_RGMII_ TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	UART4_TX	FDCAN1_TX	SDMMC2_D5	SDMMC1_CDI R	SDMMC1_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	QUADSPI_ BK1_NCS	-	ETH1_GMII_ RX_ER/ ETH1_MII_ RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	-	-	ETH1_GMII_ TX_EN/ ETH1_MII_ TX_EN/ ETH1_RGMII_ TX_CTL/ ETH1_RMII_ TX_EN	-	DSI_TE	LCD_G5	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port B	PB12	USART3_RX	FDCAN2_RX	-	ETH1_GMII_ TXD0/ ETH1_MII_ TXD0/ ETH1_RGMII_ TXD0/ ETH1_RMII_ TXD0	-	-	UART5_RX	EVENTOUT
	PB13	-	FDCAN2_TX	-	ETH1_GMII_ TXD1/ ETH1_MII_ TXD1/ ETH1_RGMII_ TXD1/ ETH1_RMII_ TXD1	-	-	UART5_TX	EVENTOUT
	PB14	-	SDMMC2_D0	-	-	-	-	-	EVENTOUT
	PB15	-	SDMMC2_D1	-	-	-	-	-	EVENTOUT
Port C	PC0	SAI2_FS_B	-	QUADSPI_BK2 _NCS	-	-	-	LCD_R5	EVENTOUT
	PC1	-	SDMMC2_CK	-	ETH1_MDC	MDIOS_MDC	-	-	EVENTOUT
	PC2	-	-	-	ETH1_GMII_ TXD2/ ETH1_MII_ TXD2/ ETH1_RGMII_ TXD2	-	DCMI_PIXCLK	-	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port C	PC3	-	-	-	ETH1_GMII_ TX_CLK/ ETH1_MII_ TX_CLK	-	-	-	EVENTOUT
	PC4	-	SPDIFRX_IN2	-	ETH1_GMII_ RXD0/ ETH1_MII_ RXD0/ ETH1_RGMII_ RXD0/ ETH1_RMII_ RXD0	-	-	-	EVENTOUT
	PC5	-	SPDIFRX_IN3	-	ETH1_GMII_ RXD1/ ETH1_MII_ RXD1/ ETH1_RGMII_ RXD1/ ETH1_RMII_ RXD1	SAI4_D3	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	SDMMC2_ D0DIR	SDMMC2_D6	DSI_TE	SDMMC1_D6	DCMI_D0	LCD_HSYNC	EVENTOUT
	PC7	SDMMC1_ D123DIR	SDMMC2_ D123DIR	SDMMC2_D7	-	SDMMC1_D7	DCMI_D1	LCD_G6	EVENTOUT
	PC8	UART5_RTS/ UART5_DE	-	-	-	SDMMC1_D0	DCMI_D2	-	EVENTOUT
	PC9	UART5_CTS	QUADSPI_BK1 _IO0	-	-	SDMMC1_D1	DCMI_D3	LCD_B2	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port C	PC10	UART4_TX	QUADSPI_ BK1_IO1	SAI4_MCLK_B	-	SDMMC1_D2	DCMI_D8	LCD_R2	EVENTOUT
	PC11	UART4_RX	QUADSPI_ BK2_NCS	SAI4_SCK_B	-	SDMMC1_D3	DCMI_D4	-	EVENTOUT
	PC12	UART5_TX	-	SAI4_SD_B	-	SDMMC1_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port D	PD0	UART4_RX	FDCAN1_RX	SDMMC3_CMD	DFSDM1_ DATIN7	FMC_AD2/ FMC_D2	-	-	EVENTOUT
	PD1	UART4_TX	FDCAN1_TX	SDMMC3_D0	DFSDM1_ CKIN7	FMC_AD3/ FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	-	-	-	SDMMC1_CMD	DCMI_D11	-	EVENTOUT
	PD3	SDMMC1_ D123DIR	SDMMC2_D7	SDMMC2_ D123DIR	SDMMC1_D7	FMC_CLK	DCMI_D5	LCD_G7	EVENTOUT
	PD4	-	-	SDMMC3_D1	DFSDM1_ CKIN0	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	SDMMC3_D2	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	FMC_NWAIT	DCMI_D10	LCD_B2	EVENTOUT
	PD7	-	SPDIFRX_IN0	SDMMC3_D3	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	SPDIFRX_IN1	-	-	FMC_AD13/ FMC_D13	-	LCD_B7	EVENTOUT
	PD9	-	-	-	-	FMC_AD14/ FMC_D14	DCMI_HSYNC	LCD_B0	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port D	PD10	-	-	-	-	FMC_AD15/ FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	QUADSPI_ BK1_IO0	SAI2_SD_A	-	FMC_A16/ FMC_CLE	-	-	EVENTOUT
	PD12	-	QUADSPI_ BK1_IO1	SAI2_FS_A	-	FMC_A17/FMC _ALE	-	-	EVENTOUT
	PD13	-	QUADSPI_ BK1_IO3	SAI2_SCK_A	-	FMC_A18	DSI_TE	-	EVENTOUT
	PD14	UART8_CTS	-	-	-	FMC_AD0/ FMC_D0	-	-	EVENTOUT
	PD15	UART8_CTS	-	-	-	FMC_AD1/ FMC_D1	-	LCD_R1	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port E	PE0	UART8_RX	-	SAI2_MCLK_A	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	UART8_TX	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	-	QUADSPI_ BK1_IO2	-	ETH1_GMII_ TXD3/ ETH1_MII_ TXD3/ ETH1_RGMII_ TXD3	FMC_A23	-	-	EVENTOUT
	PE3	-	SDMMC2_CK	-	-	FMC_A19	-	-	EVENTOUT
	PE4	SDMMC1_ CKIN	SDMMC2_D4	-	SDMMC1_D4	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	SDMMC1_ D0DIR	SDMMC2_D6	-	SDMMC1_D6	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	SDMMC1_D2	-	SAI2_MCLK_B	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port E	PE7	-	-	QUADSPI_ BK2_IO0	-	FMC_AD4/ FMC_D4	-	-	EVENTOUT
	PE8	-	-	QUADSPI_ BK2_IO1	-	FMC_AD5/ FMC_D5	-	-	EVENTOUT
	PE9	-	-	QUADSPI_ BK2_IO2	-	FMC_AD6/ FMC_D6	-	-	EVENTOUT
	PE10	-	-	QUADSPI_ BK2_IO3	-	FMC_AD7/ FMC_D7	-	-	EVENTOUT
	PE11	-	-	SAI2_SD_B	-	FMC_AD8/ FMC_D8	DCMI_D4	LCD_G3	EVENTOUT
	PE12	SDMMC1_ D0DIR	-	SAI2_SCK_B	-	FMC_AD9/ FMC_D9	-	LCD_B4	EVENTOUT
	PE13	-	-	SAI2_FS_B	-	FMC_AD10/ FMC_D10	DCMI_D6	LCD_DE	EVENTOUT
	PE14	UART8_RTS/ UART8_DE	-	SAI2_MCLK_B	SDMMC1_ D123DIR	FMC_AD11/ FMC_D11	LCD_G0	LCD_CLK	EVENTOUT
	PE15	UART8_CTS	-	FMC_NCE2	-	FMC_AD12/ FMC_D12	-	LCD_R7	EVENTOUT
Port F	PF0	-	SDMMC3_D0	SDMMC3_ CKIN	-	FMC_A0	-	-	EVENTOUT
	PF1	-	SDMMC3_CMD	SDMMC3_ CDIR	-	FMC_A1	-	-	EVENTOUT
	PF2	-	SDMMC2_ D0DIR	SDMMC3_ D0DIR	SDMMC1_ D0DIR	FMC_A2	-	-	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port F	PF3	-	-	-	ETH1_GMII_ TX_ER	FMC_A3	-	-	EVENTOUT
	PF4	-	SDMMC3_D1	SDMMC3_ D123DIR	-	FMC_A4	-	-	EVENTOUT
	PF5	-	SDMMC3_D2	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	QUADSPI_ BK1_IO3	-	-	SAI4_SCK_B	-	-	EVENTOUT
	PF7	-	QUADSPI_ BK1_IO2	-	-	-	-	-	EVENTOUT
	PF8	-	TIM13_CH1	QUADSPI_ BK1_IO0	-	-	-	-	EVENTOUT
	PF9	-	TIM14_CH1	QUADSPI_ BK1_IO1	-	-	-	-	EVENTOUT
	PF10	-	QUADSPI_CLK	-	-	SAI4_D3	DCMI_D11	LCD_DE	EVENTOUT
	PF11	-	-	SAI2_SD_B	-	-	DCMI_D12	LCD_G5	EVENTOUT
	PF12	-	-	-	ETH1_GMII_ RXD4	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	ETH1_GMII_ RXD5	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	ETH1_GMII_ RXD6	FMC_A8	-	-	EVENTOUT
Port F	PF15	-	-	-	ETH1_GMII_ RXD7	FMC_A9	-	-	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port G	PG0	-	-	-	ETH1_GMII_ TXD4	FMC_A10	-	-	EVENTOUT
	PG1	-	-	-	ETH1_GMII_ TXD5	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	ETH1_GMII_ TXD6	FMC_A12	-	-	EVENTOUT
	PG3	-	-	-	ETH1_GMII_ TXD7	FMC_A13	-	-	EVENTOUT
	PG4	-	-	-	ETH1_GMII_ GTX_CLK/ ETH1_RGMII_ GTX_CLK	FMC_A14	-	-	EVENTOUT
	PG5	-	-	-	ETH1_GMII_ CLK125/ ETH1_RGMII_ CLK125	FMC_A15	-	-	EVENTOUT
	PG6	-	-	SDMMC2_CMD	-	-	DCMI_D12	LCD_R7	EVENTOUT
	PG7	UART8_RTS/ UART8_DE	QUADSPI_CLK	-	QUADSPI_ BK2_IO3	-	DCMI_D13	LCD_CLK	EVENTOUT
	PG8	USART3_RTS/ USART3_DE	SPDIFRX_IN2	SAI4_FS_A	ETH1_PPS_ OUT	-	-	LCD_G7	EVENTOUT
	PG9	SPDIFRX_IN3	QUADSPI_ BK2_IO2	SAI2_FS_B	-	FMC_NE2/FMC _NCE	DCMI_VSYNC	LCD_R1	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port G	PG10	UART8_CTS	LCD_G3	SAI2_SD_B	QUADSPI_ BK2_IO2	FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT
	PG11	SPDIFRX_IN0	-	-	ETH1_GMII_ TX_EN/ ETH1_MII_ TX_EN/ ETH1_RGMII_ TX_CTL/ ETH1_RMII_ TX_EN	-	DCMI_D3	LCD_B3	EVENTOUT
	PG12	SPDIFRX_IN1	LCD_B4	SAI4_SCK_A	ETH1_PHY_ INTN	FMC_NE4	-	LCD_B1	EVENTOUT
	PG13	-	-	SAI4_MCLK_A	ETH1_GMII_ TXD0/ ETH1_MII_ TXD0/ ETH1_RGMII_ TXD0/ ETH1_RMII_ TXD0	FMC_A24	-	LCD_R0	EVENTOUT
	PG14	-	QUADSPI_ BK2_IO3	SAI4_SD_A	ETH1_GMII_ TXD1/ ETH1_MII_ TXD1/ ETH1_RGMII_ TXD1/ ETH1_RMII_ TXD1	FMC_A25	-	LCD_B0	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port G	PG15	-	-	SDMMC3_CK	-	-	DCMI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	QUADSPI_ BK2_IO0	SAI2_SCK_B	ETH1_GMII_ CRS/ ETH1_MII_CRS	-	-	LCD_R0	EVENTOUT
	PH3	-	QUADSPI_ BK2_IO1	SAI2_MCLK_B	ETH1_GMII_ COL/ ETH1_MII_COL	-	-	LCD_R1	EVENTOUT
	PH4	-	LCD_G5	-	-	-	-	LCD_G4	EVENTOUT
	PH5	-	-	-	-	SAI4_SD_B	-	-	EVENTOUT
	PH6	-	-	-	ETH1_GMII_ RXD2/ ETH1_MII_ RXD2/ ETH1_RGMII_ RXD2	MDIOS_MDIO	DCMI_D8	-	EVENTOUT
	PH7	-	-	-	ETH1_GMII_ RXD3/ ETH1_MII_ RXD3/ ETH1_RGMII_ RXD3	MDIOS_MDC	DCMI_D9	-	EVENTOUT
	PH8	-	-	-	-	-	DCMI_HSYNC	LCD_R2	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port H	PH9	-	-	-	-	-	DCMI_D0	LCD_R3	EVENTOUT
	PH10	-	-	-	-	-	DCMI_D1	LCD_R4	EVENTOUT
	PH11	-	-	-	-	-	DCMI_D2	LCD_R5	EVENTOUT
	PH12	-	-	-	-	-	DCMI_D3	LCD_R6	EVENTOUT
	PH13	UART4_TX	FDCAN1_TX	-	-	-	-	LCD_G2	EVENTOUT
	PH14	UART4_RX	FDCAN1_RX	-	-	-	DCMI_D4	LCD_G3	EVENTOUT
	PH15	-	-	-	-	-	DCMI_D11	LCD_G4	EVENTOUT
Port I	PI0	-	-	-	-	-	DCMI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	-	-	DCMI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	-	-	DCMI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	-	-	DCMI_D10	-	EVENTOUT
	PI4	-	-	SAI2_MCLK_A	-	-	DCMI_D5	LCD_B4	EVENTOUT
	PI5	-	-	SAI2_SCK_A	-	-	DCMI_VSYNC	LCD_B5	EVENTOUT
	PI6	-	-	SAI2_SD_A	-	-	DCMI_D6	LCD_B6	EVENTOUT
	PI7	-	-	SAI2_FS_A	-	-	DCMI_D7	LCD_B7	EVENTOUT
	PI8	-	-	-	-	-	-	-	EVENTOUT
	PI9	UART4_RX	FDCAN1_RX	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI10	USART3_CTS/ USART3_NSS	-	-	ETH1_GMII_ RX_ER/ ETH1_MII_ RX_ER	-	-	LCD_HSYNC	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port I	PI11	-	LCD_G6	-	-	-	-	-	EVENTOUT
	PI12	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	LCD_G2	-	-	-	-	LCD_R0	EVENTOUT
Port J	PJ0	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
	PJ1	-	-	-	-	-	-	LCD_R2	EVENTOUT
	PJ2	-	-	-	-	-	DSI_TE	LCD_R3	EVENTOUT
	PJ3	-	-	-	-	-	-	LCD_R4	EVENTOUT
	PJ4	-	-	-	-	-	-	LCD_R5	EVENTOUT
	PJ5	-	-	-	-	-	-	LCD_R6	EVENTOUT
	PJ6	-	-	-	-	-	-	LCD_R7	EVENTOUT
	PJ7	-	-	-	-	-	-	LCD_G0	EVENTOUT
	PJ8	UART8_TX	-	-	-	-	-	LCD_G1	EVENTOUT
	PJ9	UART8_RX	-	-	-	-	-	LCD_G2	EVENTOUT
	PJ10	-	-	-	-	-	-	LCD_G3	EVENTOUT
	PJ11	-	-	-	-	-	-	LCD_G4	EVENTOUT
	PJ12	-	LCD_G3	-	-	-	-	LCD_B0	EVENTOUT
	PJ13	-	LCD_G4	-	-	-	-	LCD_B1	EVENTOUT
	PJ14	-	-	-	-	-	-	LCD_B2	EVENTOUT

Table 9. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/SAI2/ USART3/ UART4/5/8/ SDMMC1/2/ SPDIFRX	FDCAN1/2/ TIM13/14/ QUADSPI/ SDMMC2/3/ LCD/SPDIFRX	SAI2/4/ QUADSPI/ FMC/ SDMMC2/3/ OTG_FS/ OTG_HS	DFSDM1/ QUADSPI/ SDMMC1/ MDIOS/ETH1/ DSI	SAI4/UART5/ FMC/SDMMC1/ MDIOS	UART7/DCMI/ LCD/DSI/RNG	UART5/LCD	SYS
Port J	PJ15	-	-	-	-	-	-	LCD_B3	EVENTOUT
Port K	PK0	-	-	-	-	-	-	LCD_G5	EVENTOUT
	PK1	-	-	-	-	-	-	LCD_G6	EVENTOUT
	PK2	-	-	-	-	-	-	LCD_G7	EVENTOUT
	PK3	-	-	-	-	-	-	LCD_B4	EVENTOUT
	PK4	-	-	-	-	-	-	LCD_B5	EVENTOUT
	PK5	-	-	-	-	-	-	LCD_B6	EVENTOUT
	PK6	-	-	-	-	-	-	LCD_B7	EVENTOUT
	PK7	-	-	-	-	-	-	LCD_DE	EVENTOUT
Port Z	PZ0	SPI6_SCK	-	-	-	-	-	-	EVENTOUT
	PZ1	SPI6_MISO	-	-	-	-	-	-	EVENTOUT
	PZ2	SPI6_MOSI	-	-	-	-	-	-	EVENTOUT
	PZ3	SPI6_NSS	-	-	-	-	-	-	EVENTOUT
	PZ4	-	-	-	-	-	-	-	EVENTOUT
	PZ5	-	-	-	-	-	-	-	EVENTOUT
	PZ6	-	-	-	-	-	-	-	EVENTOUT
	PZ7	-	-	-	-	-	-	-	EVENTOUT

1. Refer to *Table 8* for AF0 to AF7.

5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V, V_{DDCORE} = 1.2 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

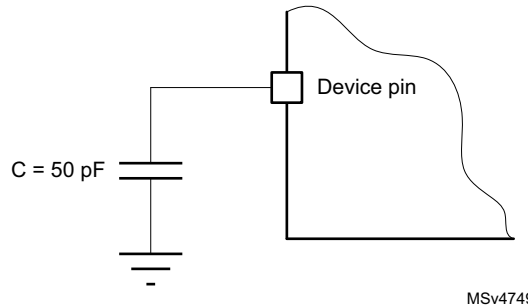
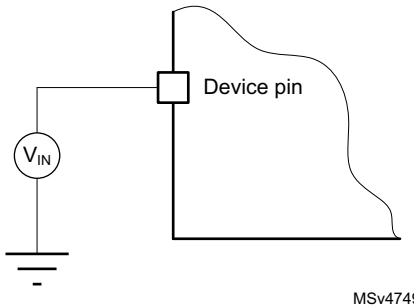
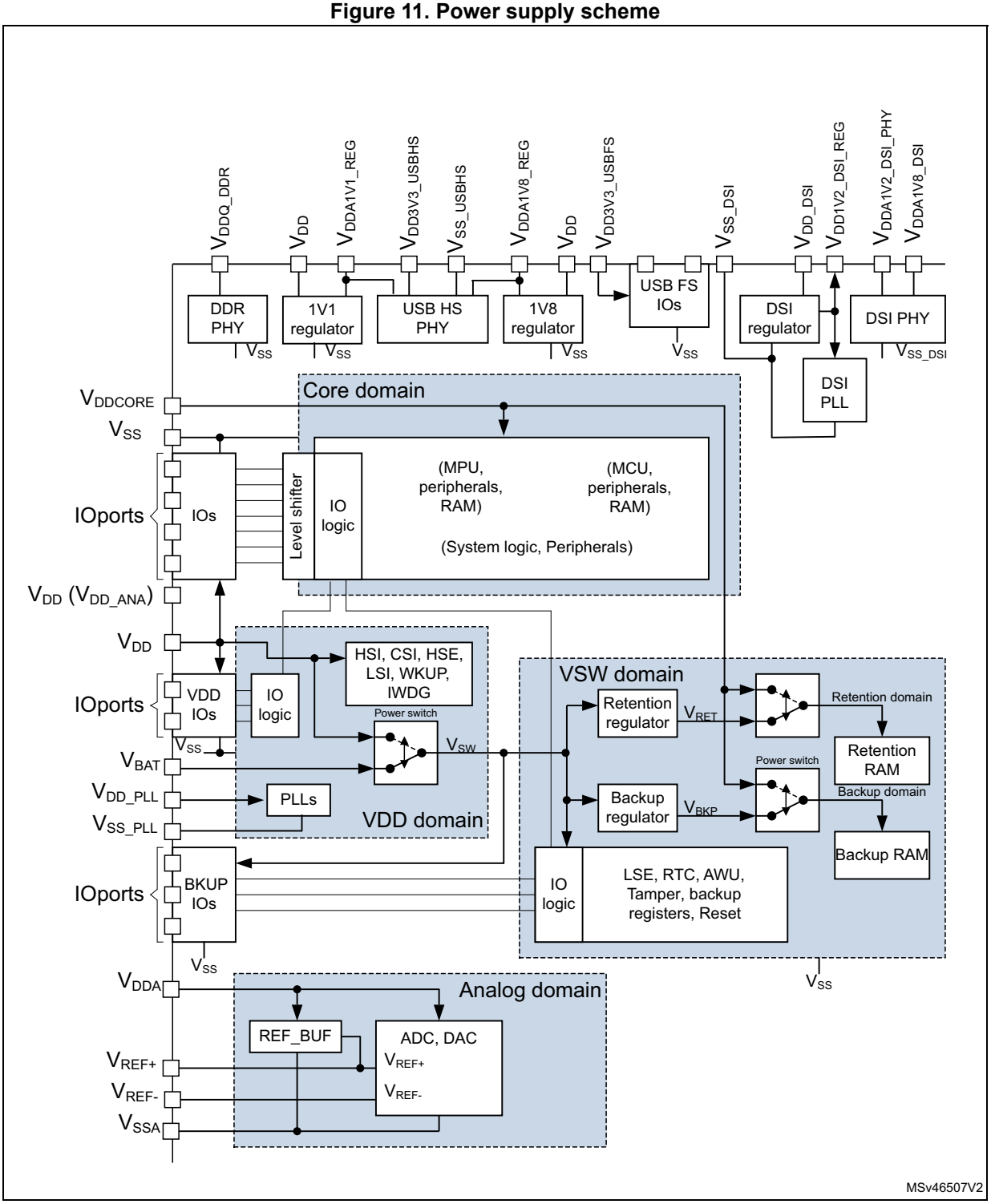


Figure 10. Pin input voltage



6.1.6 Power supply scheme

Figure 11. Power supply scheme



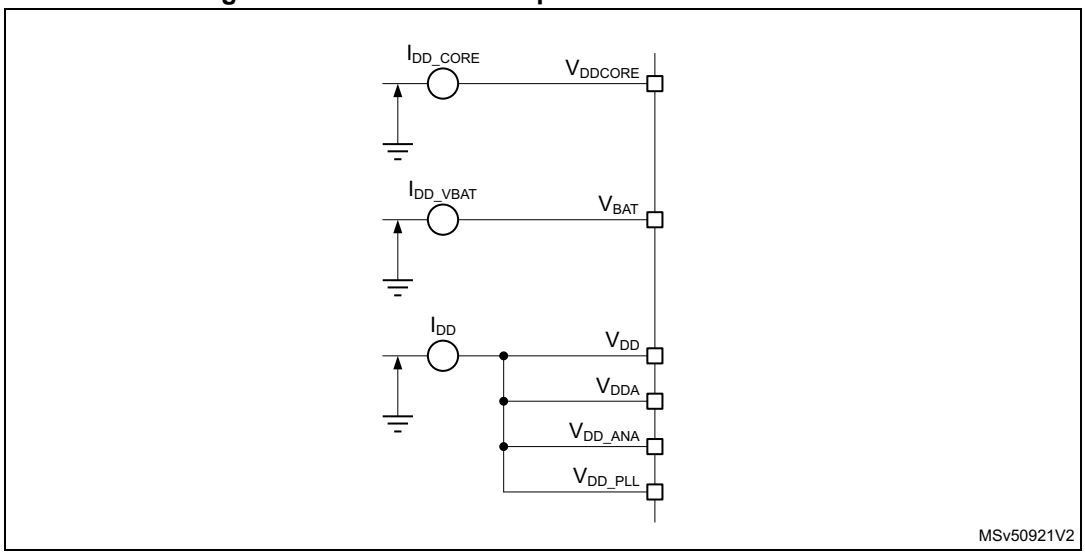
Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDCORE}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the

device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

The number of needed capacitances and their values are provided in AN5031 “Getting started with STM32MP1 Series hardware development” available from the ST website *www.st.com*.

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 10. Voltage characteristics (1)

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SSX}	External main supply voltage (including V_{DD}, V_{DD_ANA}, V_{DD_PLL}, V_{DD_DSI}, V_{DDA}, V_{DD3V3_USB}, V_{BAT})	-0.3	3.9	V
V_{DDCORE} - V_{SS}	External core supply voltage	-0.3	1.5	V
V_{DDA_DDR} - V_{SS}	DDR IO supply voltage	-0.3	1.98	V
V_{DDA1V8} - V_{SS}	1.8 V supply (including V_{DDA1V8_REG}, V_{DDA1V8_DSI})	-0.3	3.9	V

Table 10. Voltage characteristics (continued)(1)

Symbols	Ratings	Min	Max	Unit
V_{DDA1V2} - V_{SS}	1.2 V supply (including $V_{DDA1V2\_DSI\_REG}$, $V_{DDA1V2\_DSI\_PHY}$)	-0.3	1.98	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS} - 0.3	Min(V_{DD}, V_{DDA}, V_{DD3V3_USB}, V_{BAT}) +3.9(3)(4)	V
	Input voltage on TT_xx pins		3.9	V
	Input voltage on VBUS pin		6.0	V
	Input voltage on USB/OTG_HS_DP/DM pins		5.25	V
	Input voltage on OTG_FS_DP/DM pins		5.5	V
	Input voltage on any other pins		3.9	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV

1. All power (V_{DD}, V_{DDA}, V_{DD3V3_USB}, V_{DDCORE}, V_{BAT}) and ground (V_{SS}, V_{SSA}, V_{SSX}) pins must always be connected to the external/internal power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 51* for the maximum allowed injected current values.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 3.9 V the internal pull-up/pull-down resistors must be disabled.

Table 11. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	440	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	440	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, NRST pins except PA4, PA5	-5/+0	
	Injected current on PA4, PA5	-0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All power (V_{DD}, V_{DDA}, V_{DD3V3_USB}, V_{DDCORE}) and ground (V_{SS}, V_{SSA}, V_{SSX}) pins must always be connected to the external/internal power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 10: Voltage characteristics* for the maximum allowed input voltage values.

5. When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

Table 13. General operating conditions

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
F_{mpuss_ck}	Cortex-A7 subsystem	consumer mission profile	0	-	650	MHz
F_{axiss_ck}, F_{hclk5}, F_{hclk6}	Internal AXI, AHB5, AHB6 clock frequency	-	0	-	266	
F_{mcu_ck}	Internal MCU AHB clock frequency	-	0	-	209	
F_{pclk1}	Internal APB1 clock frequency	-	0	-	100	
F_{pclk2}	Internal APB2 clock frequency	-	0	-	100	
F_{pclk3}	Internal APB3 clock frequency	-	0	-	100	
F_{pclk4}	Internal APB4 clock frequency	-	0	-	133	
F_{pclk5}	Internal APB5 clock frequency	-	0	-	133	
V_{DD}	I/Os and embedded regulators (REG1V1, REG1V8) supply voltage	SYSCFG_IOCTRLSETR = 0	1.71(1)(2)	-	3.6	V
		SYSCFG_IOCTRLSETR ≠ 0	1.71	-	2.7	
V_{DD_ANA}(3)	System analog supply voltage	-	1.71	-	3.6	V
V_{DD_PLL}, V_{DD_PLL2}(4)	PLL supply voltage	-	1.71	-	3.6	V
V_{DD_DSI}(6)	DSI regulator supply voltage	-	1.71	-	3.6	V
V_{DDCORE}	Digital core domain supply voltage	Run, Stop, LP-Stop mode	1.18	1.2	1.25	V
		LPLV-Stop mode	0.85	0.9	1.25(5)	
		Standby mode	0	0	0.75	

Table 13. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
V_{DDA}	Analog operating voltage	ADC used with V_{REF} < 2 V	1.62	-	2	V
		ADC used with V_{REF} > 2 V	2	-	3.6	
		DAC used	1.8	-	3.6	
		VREFBUF with V_{REF} = 1.5 V(6)	1.8	-	3.6	
		VREFBUF with V_{REF} = 1.5 V and ADC used		-	2	
		VREFBUF with V_{REF} = 1.8 V(7)	2.1	-	3.6	
		VREFBUF with V_{REF} = 2.048 V	2.35	-	3.6	
		VREFBUF with V_{REF} = 2.5 V	2.8	-	3.6	
		ADC, DAC, V_{REF} not used	0	-	3.6	
V_{BAT}	Backup operating voltage	64 KB retention SRAM not used	1.2	-	3.6	V
		64 KB retention SRAM used	1.4			
V_{DD3V3_USBFS}(8)	USB FS I/O supply voltage	USB OTG FS used	3	3.3	3.6	V
		USB OTG FS not used	0	-	3.6	
V_{DD3V3_USBHS}(8)(9)	USB HS I/O supply voltage	USBH or USB OTG HS used	3.07	3.3	3.6	V
		USBH and USB OTG HS not used	0	-	3.6	
V_{DD3V3_USB}(8)	USB I/O supply voltage	USB used	3.07	3.3	3.6	V
		USB not used	0	-	3.6	
$V_{DD1V2\_DSI\_PHY}$(6)	1.2 V DSI PHY supply voltage	-	1.15	1.2	1.26	V
V_{DDA1V8_DSI}(6)	1.8 V DSI PHY supply voltage	-	1.65	1.8	1.95	V
V_{DDQ_DDR}(10)	DDR PHY supply voltage	DDR3 memory	1.425	1.5	1.575	V
		DDR3L memory	1.283	1.35	1.45	
		LPDDR2 or LPDDR3	1.14	1.2	1.3	
V_{DDA1V8_REG}	USB HS PHY voltage supply with 1.8 V regulator in bypass mode	BYPASS_REG1V8 = V_{DD}	1.65	1.8	1.95	V
VIN	I/O Input voltage	TTxa I/O	-0.3	-	V_{DD}+0.3	V
		VBUS I/O	-0.3	-	6	
		DDR I/O	-0.3	-	V_{DDQ_DDR}	
		USB HS I/O	-1	-	5.25	
		All I/O except TTxa	-0.3	-	See(11)	
T_J	Junction temperature range	Suffix 3 version	-40	-	125	°C

1. Once nRST is released functionality is guaranteed down to V_{BOR} falling edge max.

2. Min V_{DD} is 2.25 V when REG1V8 is used BYPASS_REG1V8 = 0.
3. Should be connected to same power supply voltage as V_{DD}.
4. It is recommended to connect V_{DD_PLL} and V_{DD_PLL2} to same power supply as V_{DD}.
5. 1.25 V is the max allowed voltage, however LPLV-Stop mode is only relevant for V_{DDCORE} up to 0.95 V. In LPLV-Stop mode, if VDDQ_DDR is not shutdown, to avoid overconsumption on VDDQ_DDR, the DDR memory must be put in SelfRefresh and DDR PHY must be set in retention mode (setting bit DDRRETEN: DDR retention enable of PWR control register 3 (PWR_CR3)).
6. DAC cannot be used with V_{REF} below 1.8 V.
7. ADC cannot be used with V_{REF} below 2 V and V_{DDA} above 2 V.
8. Depending on package selected, either V_{DD3V3_USBFS} and V_{DD3V3_USBHS} or only V_{DD3V3_USB} are available.
9. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DD3V3_USBFS}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
10. Independent from any other supply.
11. Min(V_{DD}, V_{DDA}, V_{DD3V3_USBFS}) +3.6 V < 5.5 V. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.

6.3.1 General operating conditions

6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions.

Table 14. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDD3V3_USB}(2) t_{VDD3V3_USBHS} t_{VDD3V3_USBFS}	V_{DD3V3_USBxx} rise time rate	0	∞	
	V_{DD3V3_USBxx} fall time rate	10	∞	
$t_{VDDCORE}$	V_{DDCORE} rise time rate (from reset to RUN mode)	-	2000(3)	
	V_{DDCORE} rise time rate (from LPLV-Stop to RUN mode)	-	1000(4)	
	V_{DDCORE} fall time rate	7.33	∞	

1. V_{DD} must be present before V_{DDCORE} .
2. V_{DDA1V8_REG} must be present before V_{DD3V3_USBHS}.
3. In case V_{DDCORE} rise time is larger than 2 ms/V, user should control the NRST_CORE signal with a Power Good (PG) control signal from the external regulator to avoid dysfunction of the device due to V_{DDCORE} potentially not yet established when internal reset signal is de-activated after $t_{VDDCORETEMPO}$ (cf. *Table 14* and *Figure 13*).
4. In case V_{DDCORE} rise time at exit of LPLV-Stop is larger than 1 ms/V, there is a risk of unwanted reset due to V_{DDCORE} potentially not yet established after $t_{SEL\_VDDCORETEMPO}$ (cf. *Table 14* and *Figure 14*). In such a case, the V_{DDCORE} supply should not be decreased during LPLV-Stop mode.

Figure 13. V_{DDCORE} rise time from reset

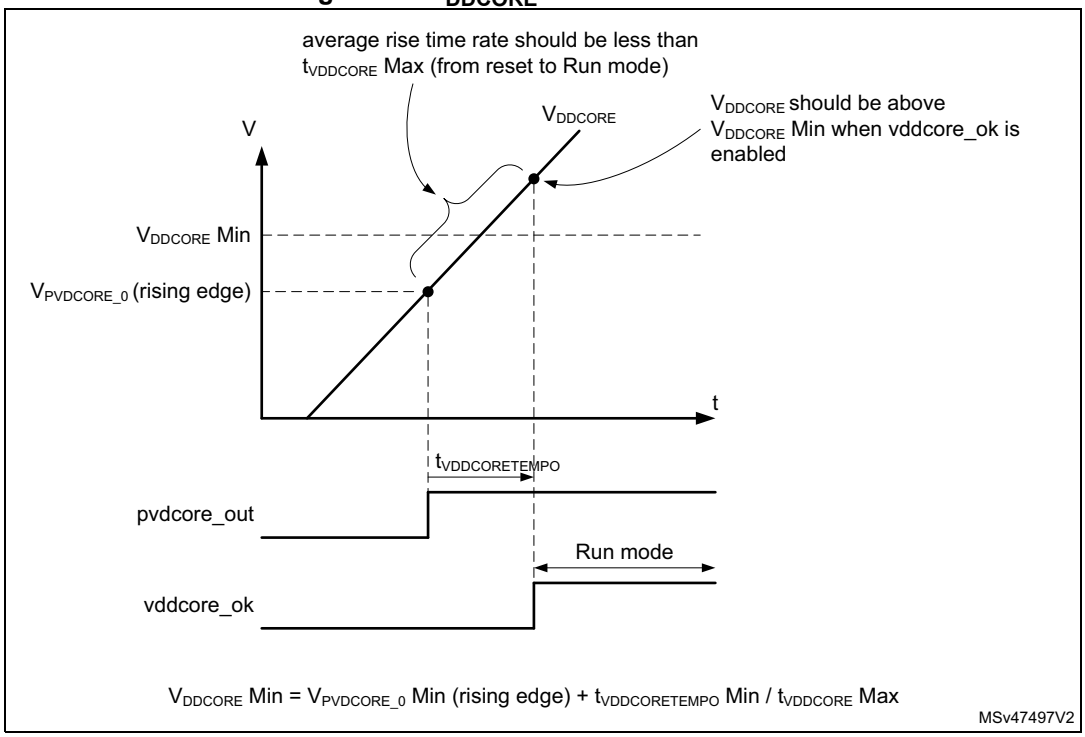
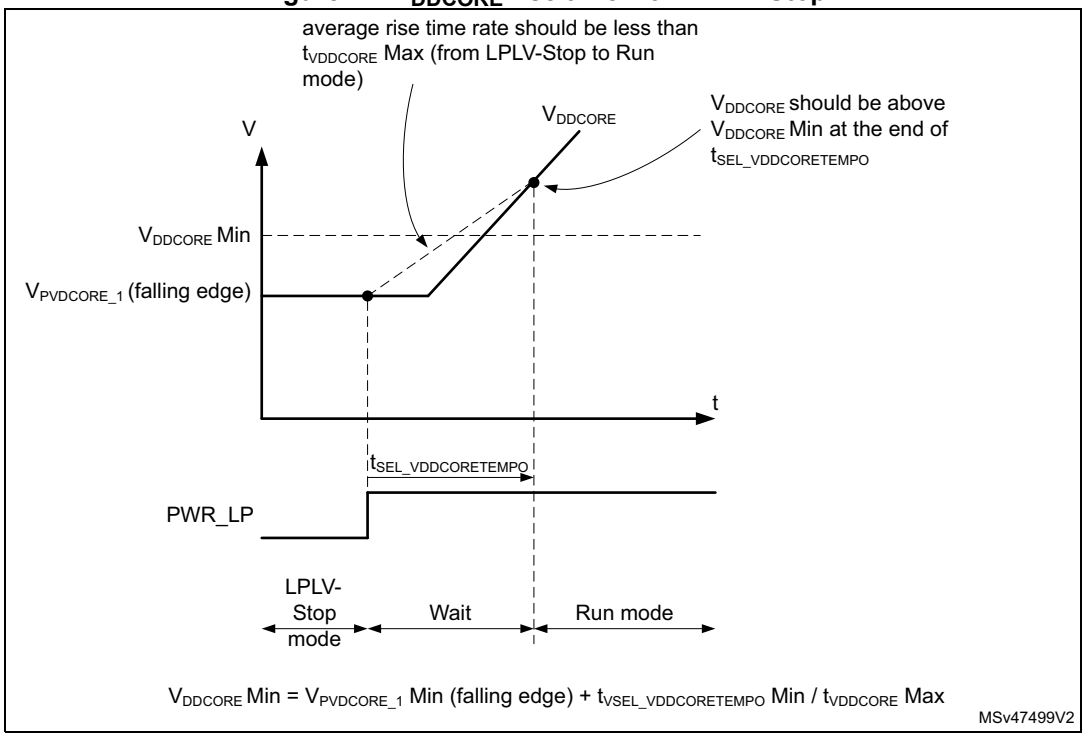


Figure 14. V_{DDCORE} rise time from LPLV-Stop



6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization. after BOR0 released	-	-	377	550	µs
V_{BOR0}(1)	Brown-out reset threshold 0	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.63	1.67	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.055	2.1	2.145	V
		Falling edge	1.955	2	2.045	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.355	2.4	2.445	V
		Falling edge	2.255	2.3	2.345	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.655	2.7	2.745	V
		Falling edge	2.555	2.6	2.645	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.905	1.95	1.995	V
		Falling edge	1.805	1.85	1.895	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.055	2.1	2.145	V
		Falling edge	1.955	2	2.045	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.205	2.25	2.295	V
		Falling edge	2.105	2.15	2.195	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.355	2.4	2.445	V
		Falling edge	2.255	2.3	2.345	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.505	2.55	2.595	V
		Falling edge	2.405	2.45	2.495	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.655	2.7	2.745	V
		Falling edge	2.555	2.6	2.645	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.805	2.85	2.895	V
		Falling edge in RUN mode	2.705	2.75	2.795	
V_{hyst_BOR0}	Hysteresis voltage of BOR0	Hysteresis in RUN mode	-	40	-	mV
V_{hyst_BOR}	Hysteresis voltage of BOR	Unless BOR0	-	100	-	mV
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD(2)	Hysteresis in RUN mode	-	100	-	mV
$I_{DD\_BOR\_PVD}$(1)(3)	BOR (unless BOR0) and PVD consumption from V_{DD}	-	0.246	-	0.626	µA

Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVM_0}	Analog voltage (V_{DDA}) detector threshold 0	Rising edge	1.655	1.7	1.745	V
		Falling edge	1.555	1.6	1.645	
V_{AVM_1}	Analog voltage (V_{DDA}) detector threshold 1	Rising edge	2.055	2.1	2.145	V
		Falling edge	1.955	2	2.045	
V_{AVM_2}	Analog voltage (V_{DDA}) detector threshold 2	Rising edge	2.455	2.5	2.545	V
		Falling edge	2.355	2.4	2.445	
V_{AVM_3}	Analog voltage (V_{DDA}) detector threshold 3	Rising edge	2.755	2.8	2.845	V
		Falling edge	2.655	2.7	2.745	
V_{hyst_VDDA}	Hysteresis of analog voltage (V_{DDA}) detector	-	-	100	-	mV
I_{VDD_AVM}(1)	Analog Voltage Monitoring (V_{DDA}) consumption on V_{DD}	-	-	-	0.248	µA
I_{VDDA_AVM}(1)	Analog Voltage Monitoring (V_{DDA}) consumption on V_{DDA}	Resistor bridge	-	2.12	-	µA
$V_{PVDCORE\_0}$(4)	Digital core domain supply voltage (V_{DDCORE}) detector threshold 0 (Run)	Rising edge	0.95	0.995	1.04	V
		Falling edge	0.91	0.955	1	
$V_{PVDCORE\_1}$(5)	Digital core domain supply voltage (V_{DDCORE}) detector threshold 1 (LPLV_Stop)	Falling edge	0.71	0.755	0.8	V
$V_{hyst\_VDDCORE}$	Hysteresis of Digital core domain supply voltage (V_{DDCORE}) detector	-	-	40	-	mV
$t_{VDDCORETEMPO}$	Tempo on VPVDCORE_0 at rising edge of V_{DDCORE} to ensure that V_{DDCORE} is fully established	-	200	340	550	µs
$t_{SEL\_VDDCORETEMPO}$	Tempo on $V_{PVDCORE\_1}$ at rising edge of V_{DDCORE} to ensure that V_{DDCORE} is fully established on exit of LPLV-Stop mode	-	234	380	606	µs
$I_{VDD\_VDDCOREVM}$(1)	V_{DDCORE} Voltage Monitoring consumption on V_{DD}	-	1.7	2.6	4.2	µA
USB_VTH	USB Threshold voltage	-	-	1.21	-	V

1. Guaranteed by design.
2. No hysteresis when using PVD_IN pin.
3. BOR0 is enabled in all modes and its consumption is therefore included in the supply current characteristics tables.
4. During the first rising edge of V_{DDCORE}, the slope should be less than 2 ms/V to ensure V_{DDCORE} is fully established before the end of the $t_{VDDCORETEMPO}$.
5. When exiting from LPLV-STOP mode to RUN mode the rising slope for V_{DDCORE} should be less than 1 ms/V to ensure V_{DDCORE} is fully established before the end of the $t_{VDDCORETEMPO}$.

6.3.4 Embedded reference voltage

The parameters given in *Table 16*, *Table 17* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 16. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40 °C < TJ < 125 °C	1.175	1.210	1.241	V
$t_{S\_vrefint}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(1)	V_{BAT} sampling time when reading the internal V_{BAT} reference voltage	-	9.8	-	-	
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	0.8	-	4.6	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DDA} = 3.3 V	9.1	13.6	27.7	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40 °C < T_J < 125 °C	-	4.3	15	mV
$T_{coeff\_VREFINT}$	Average temperature coefficient	Average temperature coefficient	-	19	67	ppm/°C
$V_{DDcoeff}$	Average Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

Table 17. Embedded reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = V_{REF+} = 3.3 V	0x5C00 5250[31:16](1)(2)

1. Mandatory to read in 32-bits word and do relevant mask and shift to isolate required bits.
2. These address is inside BSEC which should be enabled in RCC to allow access.

6.3.5 Embedded regulators characteristics

The parameters given in *Table 18*, *Table 19*, *Table 20* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

REG1V1 embedded regulator (USB_PHY)

Table 18. REG1V1 embedded regulator (USB_PHY) characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA1V1_REG}	Regulated output voltage	-	1.045	1.1	1.155	V
C_L	Load Capacitor	-	1.1	2.2(2)	3.3	µF
esr	Equivalent Serial Resistor of Cload	-	0.1	25	600	mΩ
I_{load}	Static load current(3)	-	0	-	30	mA
t_{START}	Start-up time. from PWR_CR3.REG11EN = 1 to PWR_CR3.REG11RDY = 1	C_L=2.2uF	-	93	-	µs
		C_L=3.3uF	-	-	180	
I_{INRUSH}	V_{DD} Inrush Current to load external capacitor at start	-	-	50	60	mA
I_{VDD}	Regulator Current consumption on V_{DD}	Regulator Enabled and I_{load} = 0 mA	-	150	205	µA
		Regulator Enabled and I_{load} = 30 mA	-	176	242	

1. Guaranteed by design.
2. For better dynamic performances a 2.2 µF typical value external capacitor is recommended.
3. Load is for internal STM32MP157A analog blocks, no additional external load is accepted unless mentioned.

REG_1V2 embedded regulator (DSI)

Table 19. REG1V2 embedded regulator (DSI) characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD1V2\_DSI\_REG}$	Regulated output voltage	-	1.15	1.2	1.26	V
C_L	Load Capacitor	-	0.5	2.2(2)	3.3	µF
esr	Equivalent Serial Resistor of Cload	-	0.1	25	600	mΩ
I_{load}	Static load current(3)	-	-	-	50	mA
t_{START}	Start-up time. from DSI_WRPCR.REGEN = 1 to DSI_WISR.RRS = 1	C_L=2.2uF	-	84	-	µs
		C_L=3.3uF	-	-	164	
I_{INRUSH}	V_{DD} Inrush Current to load external capacitor at start	-	-	45	60	mA

Table 19. REG1V2 embedded regulator (DSI) characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VDD}	Regulator Current consumption on V_{DD}	Regulator Enabled and I_{load} = 0 mA	-	150	203	µA
		Regulator Enabled and I_{load} = 50 mA	-	178	243	

1. Guaranteed by design.
2. For better dynamic performances a 2.2 µF typical value external capacitor is recommended.
3. Load is for internal STM32MP157A analog blocks, no additional external load is accepted unless mentioned.

REG1V8 embedded regulator (USB+DSI)

Table 20. REG1V8 embedded regulator (USB+DSI) characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Regulator input voltage	-	2.25	3.3	3.6	V
V_{DDA1V8_REG}	Regulated output voltage	after trimming	1.7	1.8	1.9	V
C_L	Load Capacitor	-	0.5	2.2(2)	3.3	µF
esr	Equivalent Serial Resistor of Cload	-	0.1	25	600	mΩ
I_{load}	Static load current(3)	-	-	-	70	mA
t_{START}	Start-up time. from PWR_CR3.REG11EN = 1 to PWR_CR3.REG11RDY = 1	C_L=2.2uF	-	81	-	µs
		C_L=3.3uF	-	-	150	
I_{INRUSH}	V_{DD} Inrush Current to load external capacitor at start	-	-	80	100	mA
I_{VDD}	Regulator Current consumption on V_{DD}	Regulator Enabled and I_{load} = 0 mA	-	130	181	µA
		Regulator Enabled and I_{load} = 70 mA	-	170	231	

1. Guaranteed by design.
2. For better dynamic performances a 2.2 µF typical value external capacitor is recommended.
3. Load is for internal STM32MP157A analog blocks, no additional external load is accepted unless mentioned.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.

All the Run mode current consumption measurements given in this section are performed with a CoreMark code unless otherwise specified.

Typical and maximum current consumption

The device is placed under the following conditions:

- All I/O pins are in analog input mode except when explicitly mentioned.
- All peripherals are disabled except when explicitly mentioned.
- The maximum values are obtained for V_{DD}/V_{BAT} = 3.6 V and V_{DDCORE} = 1.25 V, and the typical values for V_{DD}/V_{BAT} = 3.3 V and V_{DDCORE} = 1.2 V unless otherwise specified.

The parameters given in *Table 22* to *Table 26* are derived from tests performed under supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 21. Current consumption (I_{DDCORE}) in Run mode(1)

Symbol	Parameter	Conditions						Typ	Max				Unit
		-	MPU SS mode	MCU SS mode	Oscillator	MPU clk (MHz)	MCU clk (MHz)	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals enabled	CRun (P0Run, P1Run)	CRun	HSE+HSI+LSI+PLL	648	209	400	560	-	-	1500	mA
						600		385	545	-	-	-	
						400		340	490	-	-	-	
I_{DDCORE}	Supply current in Run mode	All peripherals enabled	CRun (P0Run, P1Run)	CStop	HSE+HSI+LSI+PLL	648	209	385	550	-	-	-	mA
						600		375	535	-	-	-	
						400		325	475	-	-	-	
I_{DDCORE}	Supply current in Run mode	All peripherals disabled	CRun (P0Run, P1Run)	CStop	HSE+HSI+LSI+PLL	648	209	245	365	-	-	-	mA
						600		240	355	-	-	-	
						400		190	295	-	-	-	
I_{DDCORE}	Supply current in Run mode	All peripherals disabled	CRun (P0Run, P1Stop)	CStop	HSE+HSI+PLL	648	-	180	285	-	-	-	mA
					HSE+HSI+PLL	600	-	175	280	-	-	-	
					HSE+HSI+PLL	300	-	135	230	-	-	-	
					HSE+HSI+PLL	150	-	92	175	-	-	-	
					HSE+HSI+PLL	64	-	65	140	-	-	-	
					HSE+HSI+PLL	24	-	51	125	-	-	-	
					HSE+HSI	24	-	35.5	105	-	-	-	
					HSI+PLL	64	-	65	140	-	-	-	
					HSI+PLL	24	-	51	120	-	-	-	
					HSI	64	-	49	120	-	-	-	

Table 21. Current consumption (I_{DDCORE}) in Run mode[1] (continued)

Symbol	Parameter	Conditions						Typ	Max				Unit
		-	MPU SS mode	MCU SS mode	Oscillator	MPU clk (MHz)	MCU clk (MHz)	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDCORE}	Supply current in Run mode	MPU in CSleep with WFI (CLK OFF). All peripherals disabled	CSleep (P0Stop, P1Stop)	CStop	HSE+HSI+PLL	648	-	110	200	-	-	-	mA
					HSE+HSI+PLL	600	-	110	195	-	-	-	
					HSE+HSI+PLL	300	-	100	190	-	-	-	
					HSE+HSI+PLL	150	-	74	150	-	-	-	
					HSE+HSI+PLL	64	-	57	130	-	-	-	
					HSE+HSI+PLL	24	-	48.5	120	-	-	-	
					HSE+HSI	24	-	32.5	97	-	-	-	
					HSI+PLL	64	-	57	130	-	-	-	
					HSI+PLL	24	-	48	115	-	-	-	
					HSI	64	-	41	110	-	-	-	

Table 21. Current consumption (I_{DDCORE}) in Run mode[1] (continued)

Symbol	Parameter	Conditions						Typ	Max				Unit
		-	MPU SS mode	MCU SS mode	Oscillator	MPU clk (MHz)	MCU clk (MHz)	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals disabled	CStop (P0Stop, P1Stop)	CRun	HSE+HSI+PLL	-	209	71.0	150	-	-	-	mA
					HSE+HSI+PLL	-	100	53	125	-	-	-	
					HSE+HSI+PLL	-	64	59.5	130	-	-	-	
					HSE+HSI+PLL	-	24	53	125	-	-	-	
					HSE+HSI+PLL	-	10	38.5	105	-	-	-	
					HSE+HSI+PLL	-	4	37.5	105	-	-	-	
					HSE+HSI	-	24	27.5	90	-	-	-	
					HSI+PLL	-	64	59	130	-	-	-	
					HSI+PLL	-	24	53	125	-	-	-	
					HSI	-	64	33.5	98	-	-	-	
					CSI+HSI+PLL	-	64	59.5	130	-	-	-	
					CSI+HSI+PLL	-	24	53	125	-	-	-	
					CSI+HSI+PLL	-	4	37	105	-	-	-	
					CSI+HSI	-	4	24	86	-	-	-	

Table 21. Current consumption (I_{DDCORE}) in Run mode(1) (continued)

Symbol	Parameter	Conditions						Typ	Max				Unit
		-	MPU SS mode	MCU SS mode	Oscillator	MPU clk (MHz)	MCU clk (MHz)	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDCORE}	Supply current in Run mode	MCU in CSleep with WFI (CLK OFF). All peripherals disabled	CStop (P0Stop, P1Stop)	CSleep	HSE+HSI+PLL	-	209	59.5	130	-	-	-	mA
					HSE+HSI+PLL	-	100	47.5	115	-	-	-	
					HSE+HSI+PLL	-	64	56	125	-	-	-	
					HSE+HSI+PLL	-	24	52	120	-	-	-	
					HSE+HSI+PLL	-	10	38	105	-	-	-	
					HSE+HSI+PLL	-	4	37	105	-	-	-	
					HSE+HSI	-	24	26	88	-	-	-	
					HSI+PLL	-	64	55.5	125	-	-	-	
					HSI+PLL	-	24	51.5	120	-	-	-	
					HSI	-	64	30	93	-	-	-	
					CSI+HSI+PLL	-	64	56	125	-	-	-	
					CSI+HSI+PLL	-	24	51.5	120	-	-	-	
					CSI+HSI+PLL	-	4	37	105	-	-	-	
					CSI+HSI	-	4	23.5	85	-	-	-	

1. HSE = 24 MHz, AXI clk (F_{axiss_ck}) = Max(F_{mpuss_ck}, 264).

Table 22. Current consumption (I_{DD}) in Run mode(1)

Symbol	Parameter	Conditions			Typ	Max				Unit
		MPU SS mode	MCU SS mode	Oscillator	Tj = 25 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in Run mode	CRun (P0Run, P1Run)	CRun	HSE+HSI+LSI+PLL1,2,3,4	3.95	6.14	-	-	6.6	mA
I_{DD}	Supply current in Run mode	CRun (P0Run, P1Stop)	CStop	HSI+PLL1,2	3.00	4.67	-	-	5.1	mA
				HSE+HSI	1.75	3.45	-	-	3.5	
				HSI	1.25	2.46	-	-	2.5	

1. HSE = 24 MHz.

Table 23. Current consumption in Stop mode(1)

Symbol	Parameter	Conditions			Typ				Max				Unit
		-	MPU SS mode	MCU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in Stop mode	All peripherals disabled	CStop (P0Stop, P1Stop)	CStop	980	985	985	995	1500	-	-	1600	µA
		All peripherals disabled	CStandby (P0Stop, P1Stop)	CStop	980	985	985	995	1500	-	-	1100	
I_{DDCORE}		All peripherals disabled	CStop (P0Stop, P1Stop)	CStop	19000	90500	150000	230000	80000	-	-	1100000	
		All peripherals disabled	CStandby (P0Stop, P1Stop)	CStop	19000	90000	150000	225000	79000	-	-	1100000	

1. HSE = 24 MHz.

Table 24. Current consumption in LPLV-Stop mode(1)

Symbol	Parameter	Conditions			Typ(2)				Max(3)				Unit
		-	MPU SS mode	MCU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DD}	Supply current in LPLV-Stop mode	All Peripheral disabled	CStop (P0Stop, P1Stop)	CStop	980	985	985	995	1200	-	-	1300	µA
		All Peripheral disabled	CStandby (P0Stop, P1Stop)	CStop	980	985	985	995	1200	-	-	1300	
I_{DDCORE}		All Peripheral disabled	CStop (P0Stop, P1Stop)	CStop	7150	39000	67500	105000	30000	-	-	520000	
		All Peripheral disabled	CStandby (P0Stop, P1Stop)	CStop	7150	39000	67500	105000	30000	-	-	500000	

1. HSE = 24 MHz.
2. V_{DDCORE} = 0.9 V.
3. V_{DDCORE} = 0.95 V.

Table 25. Current consumption in Standby mode(1)

Symbol	Parameter	Conditions				Typ				Max				Unit
		-		MPU SS mode	MCU SS mode	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj= 125 °C	
I_{DD}	Supply current in Standby mode	Backup SRAM OFF, RTC OFF, LSE OFF	Retention RAM OFF	CStandby (P0Stop, P1Stop)	CStop	1.95	4.00	7.60	16.5	-	-	-	-	µA
		Backup SRAM ON, RTC ON, LSE ON, medium_high drive		CStandby (P0Stop, P1Stop)	CStop	9.6	38.5	64.5	105	-	-	-	-	
			Retention RAM ON	CStandby (P0Stop, P1Stop)	CStop	74	460	800	1300	-	-	-	-	

1. IWDG OFF, LSI OFF, V_{DDCORE} = 0 V.

Table 26. Current consumption in V_{BAT} mode

Symbol	Parameter	Conditions			Typ				Max				Unit
		-		V_{BAT} (V)	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDVBAT}	Supply current in V_{BAT} mode	Backup SRAM OFF, RTC OFF, LSE OFF	Retention RAM OFF	1.6	0.007	0.13	0.39	1.1	-	-	-	-	µA
				2.4	0.008	0.14	0.415	1.15	-	-	-	-	
				3	0.012	0.175	0.495	1.35	-	-	-	-	
				3.3	0.041	0.52	1.45	3.9	-	-	-	-	
				3.6	0.073	0.62	1.65	4.25	-	-	-	6	
		Backup SRAM OFF, RTC ON, LSE ON, medium_high drive		1.6	0.84	1.05	1.35	2.1	-	-	-	-	
				2.4	1.05	1.3	1.6	2.45	-	-	-	-	
				3	1.25	1.5	1.9	2.8	-	-	-	-	
				3.3	1.4	2	3.05	5.7	-	-	-	-	
				3.6	1.55	2.25	3.35	6.25	-	-	-	-	
		Backup SRAM ON, RTC ON,. LSE ON, medium_high drive		1.6	7.75	31	54	87.5	-	-	-	-	
				2.4	8.25	31.5	55	88.5	-	-	-	-	
				3	8.45	33	57	91.5	-	-	-	-	
				3.3	9.5	34	59	95.5	-	-	-	-	
				3.6	9.55	35	60.5	98	18	-	-	195	
		Backup SRAM ON, RTC ON,. LSE ON, high drive		1.6	7.9	31.5	55	89	-	-	-	-	
				2.4	8.4	32.5	56	90	-	-	-	-	
				3	8.6	33.5	58	93	-	-	-	-	
				3.3	9.2	35	60.5	97.5	-	-	-	-	
				3.6	9.85	36	62.5	100	18	-	-	195	

Table 26. Current consumption in V_{BAT} mode (continued)

Symbol	Parameter	Conditions			Typ				Max				Unit
		-		V_{BAT} (V)	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	Tj = 25 °C	Tj = 85 °C	Tj = 105 °C	Tj = 125 °C	
I_{DDVBAT}	Supply current in V_{BAT} mode	Backup SRAM ON, RTC ON,. LSE ON, medium_high drive	Retention RAM ON	1.6	74	405	760	1250	-	-	-	-	µA
				2.4	76	410	765	1250	-	-	-	-	
				3	81	420	785	1300	-	-	-	-	
				3.3	79	430	795	1300	-	-	-	-	
				3.6	84.5	435	815	1350	212	-	-	2500	
		Backup SRAM ON, RTC ON, LSE ON, high drive		1.6	75.5	405	770	1250	-	-	-	-	
				2.4	75.5	410	770	1250	-	-	-	-	
				3	76	425	790	1300	-	-	-	-	
				3.3	78	435	805	1300	-	-	-	-	
				3.6	84.5	440	820	1350	212	-	-	2500	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

The I/Os used by an application contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

The theoretical formula is provided below:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: C = CINT+ CEXT

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 27* are measured starting from the wakeup event trigger up to the first instruction executed by the MPU or MCU:

- For SLEEP modes:
  - the MPU or MCU goes in low-power mode after WFE (Wait For Event) instruction.
- For STOP modes:
  - MCU goes in low-power mode after WFE (Wait For Event) instruction.
  - MPU goes in low-power mode after WFI (Wait For Interrupt) instruction.
- WKUPx pin is used to wakeup from STANDBY, STOP and SLEEP modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Conditions (after wakeup)	Typ(1)	Max(1)	Unit
$t_{WUCSLEEP\_MPU}$	MPU wakeup from CSleep, MCU in CSleep	HSE 24 MHz, SYSRAM	31	TBD	CPU clock cycles
$t_{WUCSTOP\_MPU}$	MPU wakeup from CStop, MCU in CStop	HSI 64 MHz, SYSRAM	5.7	TBD	µs
		HSE + PLL 648 MHz, SYSRAM	112	TBD	
	MPU wakeup from CStop, MCU in CRun	HSI 64 MHz, SYSRAM	0.54	TBD	
		HSE + PLL 648 MHz, SYSRAM	0.083	TBD	
$t_{WULPLV-STOP\_MPU}$	MPU wakeup from CStop with system in LPLV-Stop (LVDS=1), MCU in CStop	HSI 64 MHz, SYSRAM	410	TBD	
$t_{WUCSLEEP\_MCU}$	MCU wakeup from CSleep, MPU in CSleep	HSE 24 MHz, SRAM	6	TBD	CPU clock cycles
$t_{WULPLV-STOP\_MCU}$	MCU wakeup from CStop with system in LPLV-Stop (LVDS=1), MPU in CStop	HSI 64 MHz, SRAM, MCTMPSKP = 1	5.3	TBD	µs
		HSI 64 MHz, SRAM, MCTMPSKP = 0, PWR_LP delay = 1 ms	1.4	TBD	
$t_{WUCSTOP\_MCU}$	MCU wakeup from CStop, MPU in CStop	HSI 64 MHz, SRAM	5.3	TBD	
$t_{WUCSTOP\_MCU2}$	MCU wakeup from CStop, HSI active (HSIKERON=1), MPU in CStop	HSI 64 MHz, SRAM	0.33	TBD	
$t_{WUCSTOP\_MCU3}$	MCU wakeup from CStop, MPU in CRun	HSI 64 MHz, SRAM	0.12	TBD	
$t_{WUSTANDBY\_MCU}$	MCU wakeup from STANDBY	HSI 64 MHz, RETRAM	2550	TBD	

1. Guaranteed by characterization results unless otherwise specified.

Table 28. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
tWUUSART tWULPUART	Wakeup time needed to calculate the maximum USART/LPUART baud rate allowing the wakeup from stop mode when USART/LPUART clock source is HSI.	Stop	-	6.7	µs
		LPLV-Stop	-	240.7(2)	µs

1. Guaranteed by design.
2. Including the $t_{SEL\_VDDCORETEMPO}$ = 234 µs.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

Digital and analog bypass modes are available.

The external clock signal has to respect the *Table 52: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 15* for digital bypass mode and in *Figure 16* for analog bypass mode. In analog bypass mode the clock can be a sinusoidal waveform.

Table 29. High-speed external user clock characteristics (digital bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	8	24	48	MHz
V_{SW} (V_{HSEH} -V_{HSEL})	OSC_IN amplitude	0.7×V_{DD}	-	V_{DD}	V
V_{DC}	OSC_IN input voltage	V_{SS}	-	0.3×V_{SS}	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram (digital bypass)

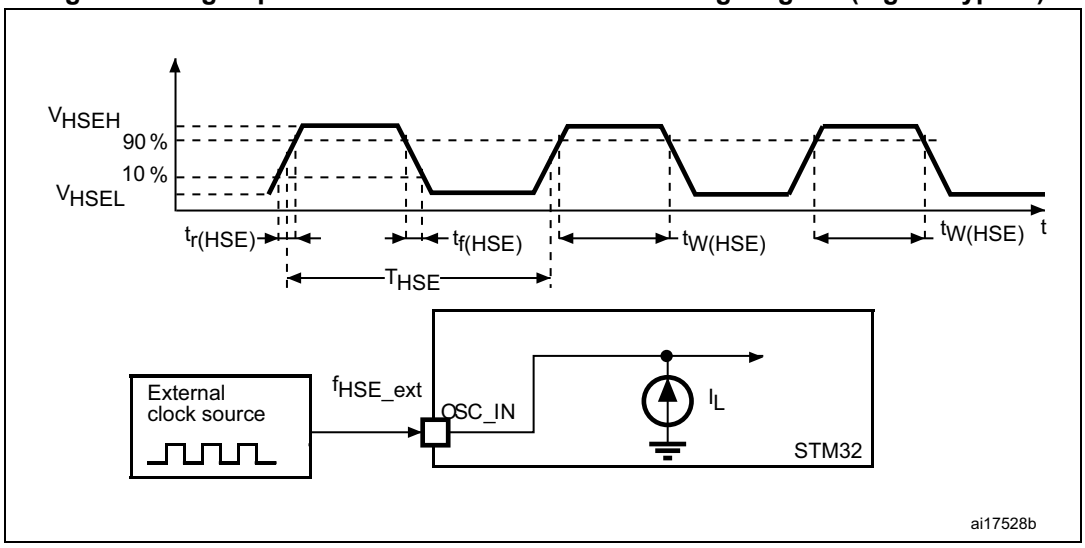


Table 30. High-speed external user clock characteristics (analog bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	8	24	48	MHz
	duty cycle (Square wave)	45	50	55	%
	duty cycle deterioration	0	±10(2)	±20(3)	%
V_{HSE}	Absolute input range	0	-	V_{DD}	-
V_{PP}	OSC_IN peak-to-peak amplitude	0.2(4)	-	0.67×V_{DD}	V

Table 30. High-speed external user clock characteristics (analog bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SU}(5)	Time to start	-	1	10(6)	µs
$tr/tf_{(HSE)}$	Rise and Fall time (10% to 90% threshold levels of the input peak-to-peak amplitude)	0.05 ×T_{HSE}	-	0.3 ×T_{HSE}	ns
$I_{(HSE)}$	Power consumption	-	150(7)	500(8)	µA

1. Guaranteed by design.
2. Guaranteed by design with a square wave signal (@25 °C, V_{DD}=3.3 V /V_{PP} = 400 mV / V_{DC}=1 V) where V_{DC} is the DC component of the input signal.
3. Guaranteed by design with a square wave signal (@25 °C, V_{DD}=1.71 V /V_{PP} = 200 mV / V_{DC}=0.8 V) where V_{DC} is the DC component of the input signal.
4. minimum peak-to-peak amplitude (@25 °C, 0.1<V_{DC}<V_{DD}-0.1 V) where V_{DC} is the DC component of the input signal.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized analog bypass clock interface is reached. This value is measured with 200 mV peak-to-peak amplitude.
6. Maximum start-up time is obtained with 200 mV peak-to-peak amplitude.
7. with a sine wave signal (V_{PP} = 400 mV / V_{DC}=0.4 V) where V_{DC} is the DC component of the input signal.
8. with a sine wave signal (V_{DD} = 3.6 V / V_{PP} = 800 mV / V_{DC} = 1.8 V) where V_{DC} is the DC component of the input signal.

Figure 16. High-speed external clock source AC timing diagram (analog bypass)

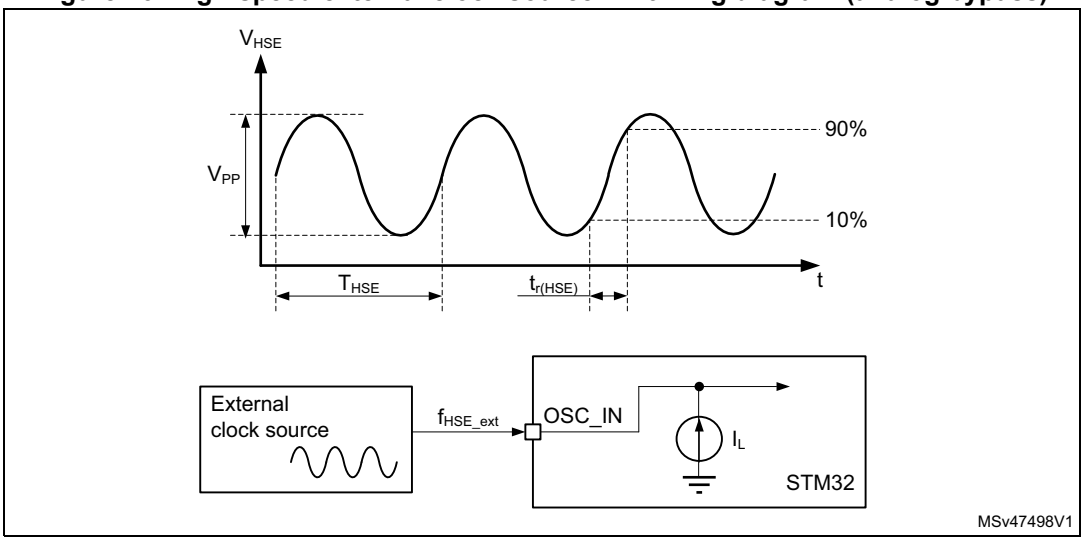


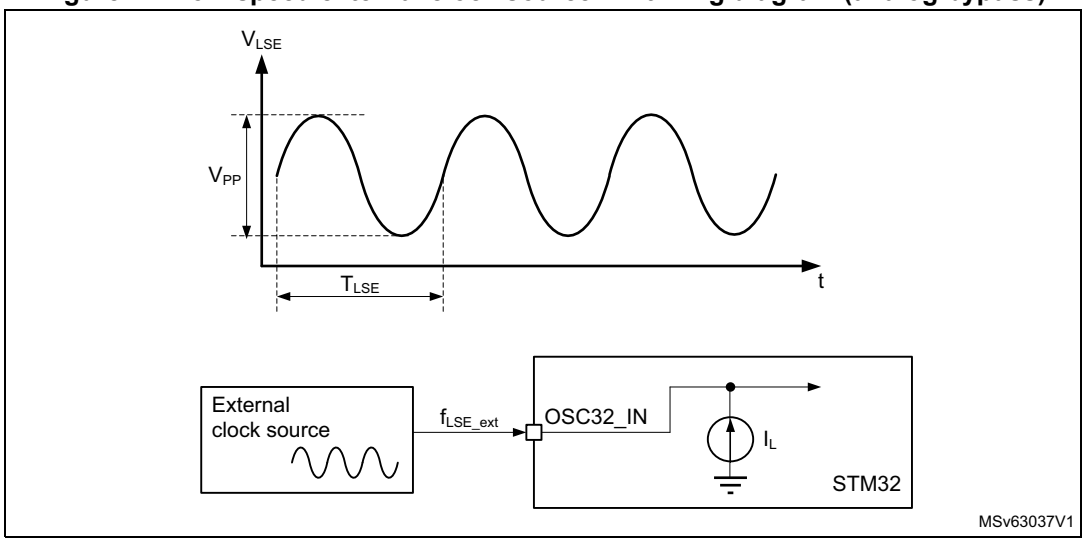
Table 31. Low-speed external user clock characteristics (analog bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	-	kHz
V_{LSE}	Absolute input range	0	-	V_{SW}(2)	-
V_{PP}	OSC32_IN peak-to-peak amplitude	0.2(3)	1	-	V
$I_{(LSE)}$	Power consumption	-	120	-	nA

1. Guaranteed by design.
2. V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise

3. Minimum peak-to-peak amplitude (@25 °C, 0.1 < V_{DC} < V_{SW} - 0.1 V) where V_{DC} is the DC component of the input signal.

Figure 17. Low-speed external clock source AC timing diagram (analog bypass)



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 52: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 18* for digital bypass and *Figure 17* for analog bypass.

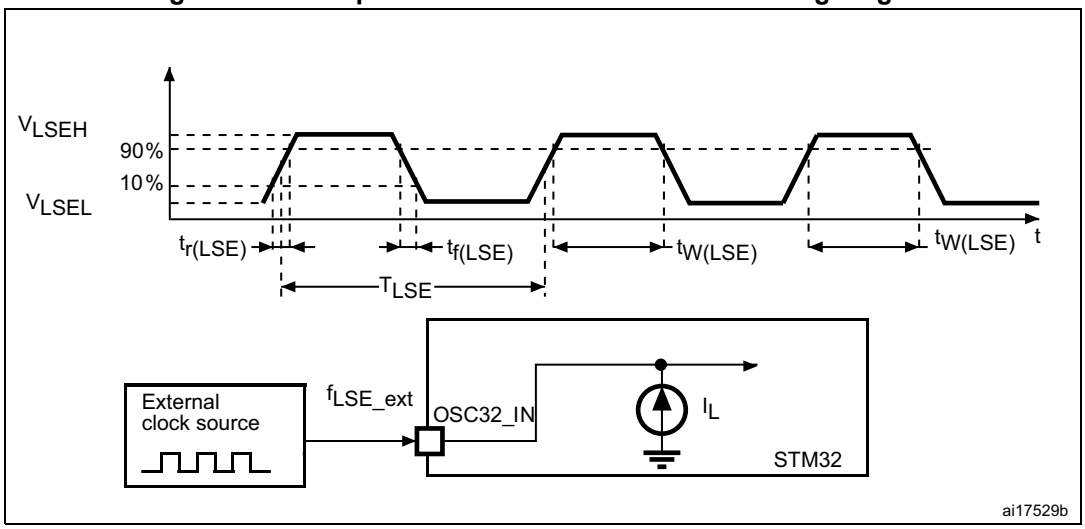
Table 32. Low-speed external user clock characteristics (digital bypass)(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	250	-	-	ns

1. Guaranteed by design.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 8 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 33*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 33. 8-48 MHz HSE oscillator characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	8	24	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD} = 3 V, Rm = 150 Ω C_L = 12 pF at 4 MHz	-	0.35	-	
		V_{DD} = 3 V, Rm = 120 Ω C_L = 12 pF at 16 MHz	-	0.40	-	
		V_{DD} = 3 V, Rm = 100 Ω C_L = 10 pF at 24 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 80 Ω C_L = 8 pF at 32 MHz	-	0.65	-	
		V_{DD} = 3 V, Rm = 80 Ω C_L = 8 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

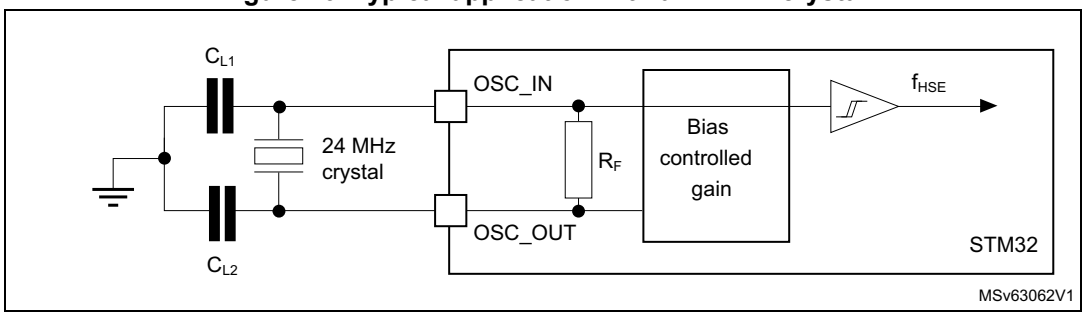
1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 19*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 19. Typical application with a 24 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 34*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

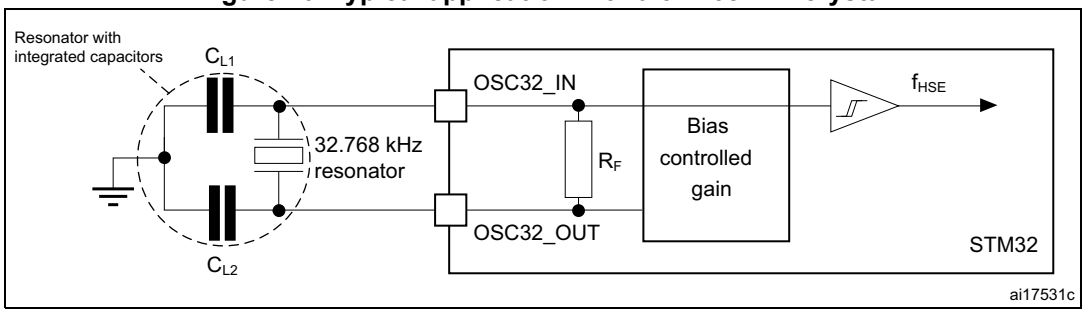
Table 34. Low-speed external user clock characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 20. Typical application with a 32.768 kHz crystal



1. Adding an external resistor between OSC32_IN and OSC32_OUT is forbidden.

6.3.9 External clock source security characteristics

Table 35. High-speed external user clock security system (HSE CSS)(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DCM(HSE\_CSS)}$	Time to detect clock missing	-	2	-	µs
$t_{DCP(HSE\_CSS)}$	Time to detect clock presence	-	-	250	ns
$I_{VDD(HSE\_CSS)}$	Power consumption (f_{HSE} = 48 MHz)	-	-	50	µA

1. Guaranteed by design.

6.3.10 Internal clock source characteristics

The parameters given in *Table 36*, *Table 37* and *Table 38* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

64 MHz high-speed internal RC oscillator (HSI)

Table 36. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}(2)	HSI frequency	V_{DD} = 3.3 V, T_J = 30 °C	63.7	64	64.3	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.33	%
		Trimming is 128, 256 and 384	-	-2.43	-	
		Trimming is 64, 192, 320 and 448	-	-0.70	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	-	-0.30	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD} = 1.71 to 3.6 V	-0.12	-	0.03	%
$\Delta_{TEMP\ (HSI)}$(3)	HSI oscillator frequency drift over temperature after factory calibration	T_J = -20 to 110 °C	-1.25	-	0.75	%
		T_J = -40 to 125 °C	-1.75	-	0.95	
t_{su}(HSI)	HSI oscillator start-up time (Time between Enable rising and First output clock edge.)	-	-	1.47	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	3	-	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

4 MHz low-power internal RC oscillator (CSI)

Table 37. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}(2)	CSI frequency	V_{DD} = 3.3 V, T_J = 30 °C	3.98	4	4.02	MHz
TRIM	Trimming step	Trimming code is not a multiple of 16	-	0.85	1	%
		Trimming code is a multiple of 16	-	-1.65	-	-
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{VDD} (CSI) + Δ_{TEMP} (CSI)(3)	CSI oscillator frequency drift over V_{DD} & drift over temperature	V_{DD} = 1.71 to 3.6 V T_J = 0 to 85 °C	-	±1.43	-	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1.5	2.4	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ±5% of f_{CSI})	T_J = 0 to 85 °C	-	5	-	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	30	-	µA

1. Guaranteed by design.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

32 kHz low-speed internal (LSI) RC oscillator

Table 38. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_J = 30 °C,(2) V_{DD} = 3.3 V	31.4	32	32.6	kHz
		T_J = -40 to 125 °C, V_{DD} = 1.71 to 3.6 V	29	32	33.6	
$t_{su(LSI)}$	LSI oscillator startup time (Time between Enable rising and First output clock edge.)	-	-	64	125	µs
$t_{stab(LSI)}$	LSI oscillator stabilization time (5% of final value)	-	-	110	170	
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	120	230	nA

1. Guaranteed by design.
2. Guaranteed by test in production.

6.3.11 PLL characteristics

The parameters given in *Table 39*, *Table 40*, *Table 41*, *Table 42* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

PLL1_1600, PLL2_1600 characteristics

Table 39. PLL1_1600, PLL2_1600 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode and Sigma delta mode	8	-	16	MHz
	PLL input clock duty cycle	-	10	-	90	%
$f_{PLL\_P\_Q\_R\_OUT}$	PLL P,Q,R multiplier output clock	-	3.125	-	800(2)	MHz
	PLL P,Q,R clock duty cycle	Division by 1	45	50	55	%
		Even divisions (N multiple of 2)	45	50	55	
		Odd divisions (N not multiple of 2)	[100, (N+1)/2N] - 5	[100, (N+1)/2N]	[100, (N+1)/2N] + 5	
f_{VCO_OUT}	PLL VCO output	-	800	-	1600	MHz
t_{LOCK}	PLL lock time	Normal mode	-	50	150	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)	-	65	170	
A_{LOCK}	Lock Accuracy (Ratio VCO frequency versus target frequency at lock)	-	-	-	±2	%

Table 39. PLL1_1600, PLL2_1600 characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter	RMS cycle-to-cycle jitter	$f_{PLL\_P\_Q\_R\_OUT}$ division = 1 to 16 Without Fractional mode	VCO = 400 MHz	-	18(3)	-	±ps
			VCO = 533 MHz	-	14(3)	-	
			VCO = 800 MHz	-	12(3)	-	
		$f_{PLL\_P\_Q\_R\_OUT}$ division = 1 to 16 With Fractional mode	VCO = 533 MHz	-	20(3)	-	
			VCO = 800 MHz	-	18(3)	-	
	RMS period jitter	$f_{PLL\_P\_Q\_R\_OUT}$ division = 1 to 16 Without Fractional mode	VCO = 400 MHz	-	16(3)	-	±ps
			VCO = 533 MHz	-	12(3)	-	
			VCO = 800 MHz	-	10(3)	-	
		$f_{PLL\_P\_Q\_R\_OUT}$ division = 1 to 16 With Fractional mode	VCO = 533 MHz	-	16(3)	-	
			VCO = 800 MHz	-	15(3)	-	
	Long term jitter	$f_{PLL\_P\_Q\_R\_OUT}$ division = 1 to 16 f_{PLL_IN} = 8 MHz Without Fractional mode	VCO = 400 MHz	-	225(4)	-	ps
			VCO = 533 MHz	-	200(4)	-	
			VCO = 800 MHz	-	100(4)	-	
		$f_{PLL\_P\_Q\_R\_OUT}$ division = 1 to 16 f_{PLL_IN} = 8 MHz With Fractional mode	VCO = 400 MHz	-	350(4)	-	
			VCO = 533 MHz	-	250(4)	-	
			VCO = 800 MHz	-	150(4)	-	
I_{VDD_PLL}(2)	PLL power consumption on $V_{DD\_PLL\ (Analog)}$	VCO freq = 800 MHz		-	930	-	µA
		VCO freq = 400 MHz		-	560	-	
$I_{VDDCORE}$(2)	PLL power consumption on $V_{DDCORE\ (Digital)}$	VCO freq = 800 MHz		-	4200	-	µA
		VCO freq = 400 MHz		-	2100	-	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Measured on DDR high speed IO.
4. Measured on DDR high speed IO for 10000 output clock cycles.

PLL3_800, PLL4_800 characteristics

Table 40. PLL3_800, PLL4_800 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode	4	-	16	MHz
	-	Sigma delta mode	8	-	16	
	PLL input clock duty cycle	-	10	-	90	%

Table 40. PLL3_800, PLL4_800 characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{PLL\_P\_Q\_R\_OUT}$	PLL P,Q,R multiplier output clock	-		3.125	-	800(2)	MHz
	PLL P,Q,R clock duty cycle	Even divisions (N multiple of 2)		45	50	55	%
		Odd divisions (N not multiple of 2)		[100, (N+1)/2N] - 5	[100, (N+1)/2N]	[100, (N+1)/2N] + 5	
f_{VCO_OUT}	PLL VCO output	-		400	-	800	MHz
t_{LOCK}	PLL lock time	Normal mode		15	50	150	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		25	65	170	
A_{LOCK}	Lock accuracy (Ratio VCO frequency versus target frequency at lock)	-		-	-	±2	%
Jitter	RMS cycle-to-cycle jitter	$f_{PLL\_P\_Q\_R\_OUT}$ division = 25 to 100 Without Fractional mode	VCO = 400 MHz	-	80(3)	-	±ps
			VCO = 600 MHz	-	50(3)	-	
			VCO = 800 MHz	-	45(3)	-	
		$f_{PLL\_P\_Q\_R\_OUT}$ division = 25 to 100 With Fractional mode	VCO = 600 MHz	-	65(3)	-	
			VCO = 800 MHz	-	60(3)	-	
	RMS period jitter	$f_{PLL\_P\_Q\_R\_OUT}$ division = 25 to 100 Without Fractional mode	VCO = 400 MHz	-	75(3)	-	±ps
			VCO = 600 MHz	-	38(3)	-	
			VCO = 800 MHz	-	30(3)	-	
		$f_{PLL\_P\_Q\_R\_OUT}$ division = 25 to 100 With Fractional mode	VCO = 600 MHz	-	55(3)	-	
			VCO = 800 MHz	-	50(3)	-	
	Long term jitter	$f_{PLL\_P\_Q\_R\_OUT}$ division = 25 to 100 f_{PLL_IN} = 8 MHz Without Fractional mode	VCO = 400 MHz	-	225(4)	-	ps
			VCO = 600 MHz	-	150(4)	-	
			VCO = 800 MHz	-	125(4)	-	
		$f_{PLL\_P\_Q\_R\_OUT}$ division = 25 to 100 f_{PLL_IN} = 8 MHz With Fractional mode	VCO = 400 MHz	-	300(4)	-	
			VCO = 600 MHz	-	200(4)	-	
			VCO = 800 MHz	-	150(4)	-	
I_{VDD_PLL}	PLL power consumption on $V_{DD\_PLL\ (Analog)}$	VCO freq = 800 MHz		-	600	610	µA
		VCO freq = 400 MHz		-	320	350	

Table 40. PLL3_800, PLL4_800 characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDCORE}$	PLL power consumption on V_{DDCORE} (Digital)	VCO freq = 800 MHz	-	2200	5250	µA
		VCO freq = 400 MHz	-	1130	4550	

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Measured on GPIO.
4. Measured on GPIO for 10000 output clock cycles.

PLL_USB (2880 MHz) characteristics

Table 41. USB_PLL characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock		19.2	24	38.4	MHz
f_{PLL_INFIN}	PFD input clock		19.2	24	38.4	MHz
f_{PLL_OUT}	PLL multiplier output clock		-	480	-	MHz
f_{VCO_OUT}	PLL VCO output		-	2880	-	MHz
t_{LOCK}	PLL lock time		-	-	100	µs
t_{PDN}	PLL power down time		10	-	-	µs
$I_{DDA1V1\_REG(PLL)}$	PLL power consumption on V_{DDA1V1_REG} (internal connection)	PLL in power down	-	5	425	µA
		f_{VCO_OUT} = 2880 MHz	-	4.4	5.6	mA
$I_{DDA1V8\_REG(PLL)}$	PLL power consumption on V_{DDA1V8_REG} (internal connection)	PLL in power down	-	-	2	µA
		f_{VCO_OUT} = 2880 MHz	-	2	2.5	mA

1. Guaranteed by design unless otherwise specified.

PLL_DSI (2000 MHz) characteristics

Table 42. DSI_PLL characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock		8	-	200	MHz
f_{PLL_INFIN}	PFD input clock		8	-	50	MHz
f_{PLL_OUT}	PLL multiplier output clock		62.5	-	1000	MHz
f_{VCO_OUT}	PLL VCO output		1000	-	2000	MHz
t_{LOCK}	PLL lock time		-	-	100	µs
t_{PDN}	PLL power down time		5	-	-	µs
$I_{DD1V2\_DSI\_REG(PLL)}$	PLL power consumption on $V_{DD1V2\_DSI\_REG}$ (internal connection)	PLL in power down	-	2.5	20	µA
		f_{VCO_OUT} = 2000 MHz	-	400	500	

1. Guaranteed by design unless otherwise specified.

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows the reduction of electromagnetic interferences (see *Table 48: EMI characteristics*). It is available only on the PLL1_1600, PLL2_1600, PLL3_800 and PLL4_800.

Table 43. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	20	-	60	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	2^{15}-1	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and fMod must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows the increment step (INCSTEP) calculation:

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2% (4% peak-to-peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

Figure 21 and *Figure 22* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 21. PLL output clock waveforms in center spread mode

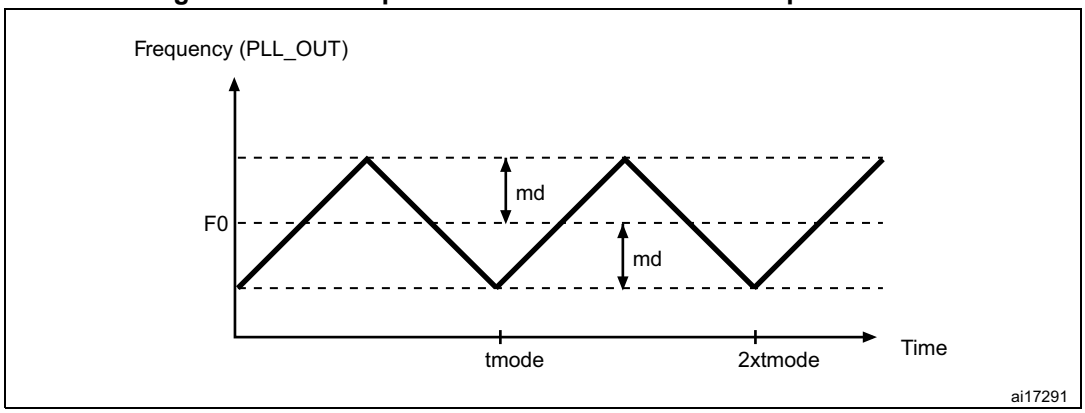
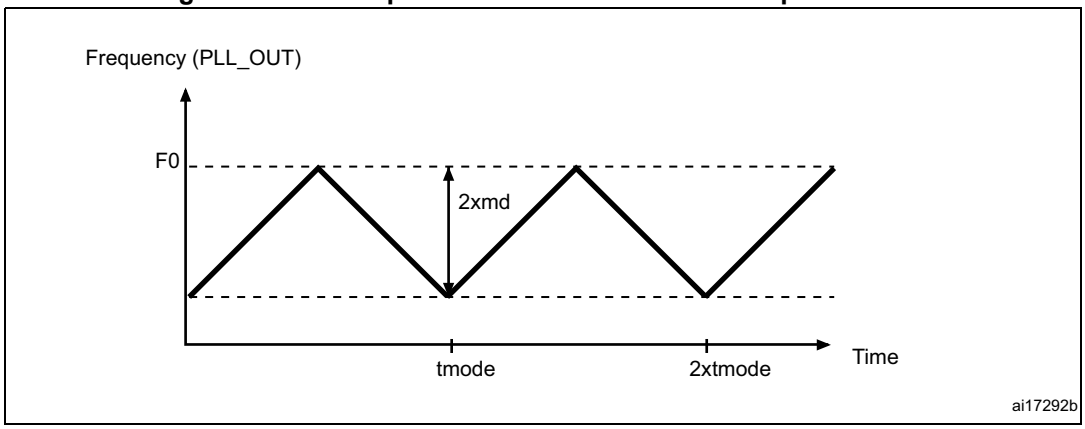


Figure 22. PLL output clock waveforms in down spread mode



6.3.13 Memory characteristics

OTP characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 44. OTP characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{VDDCORE}$	OTP consumption on V_{DDCORE}	Programming	-	450	µA
		Reading	-	490	µA
		PowerDown	-	4.2	µA

Table 44. OTP characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
I_{VDD}	OTP consumption on V_{DD}	Programming	-	10000	µA
		Reading	-	2200	µA
		PowerDown	-	1	µA
F_{OTP} (1)	OTP operating Frequency	-	-	67	MHz
NB_CYCLE (2)	Maximum number of reading cycles	-	-	500	Million

1. Guaranteed by design.
2. Guaranteed by characterization results.

DDR characteristics

DDR3, DDR3L I/O DC specifications

The following table provides input and output DC threshold values and on-die-termination (ODT) recommended values. The conditions for the output threshold values are un-terminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Table 45. DC specifications – DDR3 or DDR3L mode(1)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IH(DC)}$	DC input voltage high	V_{REF} + 0.09	-	V_{DDQ}	V
$V_{IL(DC)}$	DC input voltage low	V_{SSQ} - 0.3	-	V_{REF} - 0.09	V
V_{OH}	DC output logic high	0.8 × V_{DDQ}	-	-	V
V_{OL}	DC output logic low	-	-	0.2 × V_{DDQ}	V
R_{TT}	Input termination resistance (ODT) to $V_{DDQ}/2$	100 54 36	120 60 40	140 66 44	Ω
I_{LS}	Input leakage current, SSTL mode, unterminated	-	0.01	4.8	µA

1. Guaranteed by design.

LPDDR2, LPDDR3 I/O DC specifications

The following table provides input and output DC threshold values. The conditions for the output threshold values are un-terminated outputs loaded with 1 pF capacitor load.

Table 46. DC specifications – LPDDR2 or LPDDR3 mode(1)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IH(DC)}$	DC input voltage high	V_{REF} + 0.13	-	V_{DDQ}	V
$V_{IL(DC)}$	DC input voltage low	V_{SSQ}	-	V_{REF} - 0.13	V
V_{OH}	DC output logic high	0.9 × V_{DDQ}	-	-	V
V_{OL}	DC output logic low	-	-	0.1 × V_{DDQ}	V
ILEAK	Input leakage current	-	0.01	4.51	µA

1. Guaranteed by design.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: a burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709 available from the ST website *www.st.com*.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, V_{DDCORE} = 1.2 V, T_A = +25 °C, LFBGA448, F_{mpuss_ck} = 648 MHz, F_{mcu_ck} = 209 MHz, M4 core not running, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 available from the ST website *www.st.com*.).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/400 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, V_{DDCORE} = 1.2 V, T_A = 25 °C, LFBGA448 package, F_{mpuss_ck} = 648 MHz, F_{mcu_ck} = 209 MHz, M4 core not running, conforming to IEC61967-2	0.1 to 30 MHz	19	dBµV
			30 to 130 MHz	-2	
			130 MHz to 1 GHz	19	
			1 GHz to 2 GHz	9	
			EMI Level	3.5	-

6.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on three parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

6.3.16 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the device in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 51. I/O current injection susceptibility(1)

Symbol	Description	Negative injection	Positive injection	Unit
I_{INJ}	ANA0, ANA1, DSI_D0_P, DSI_D0_N, DSI_CK_P, DSI_CK_N, DSI_D1_P, DSI_D1_N, PA4, PA5	0	0	mA
	PG2, PG3, PG4, PH2	0	N/A	
	All other FTxx I/Os	5	N/A	

1. Guaranteed by characterization.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 52: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 13: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics

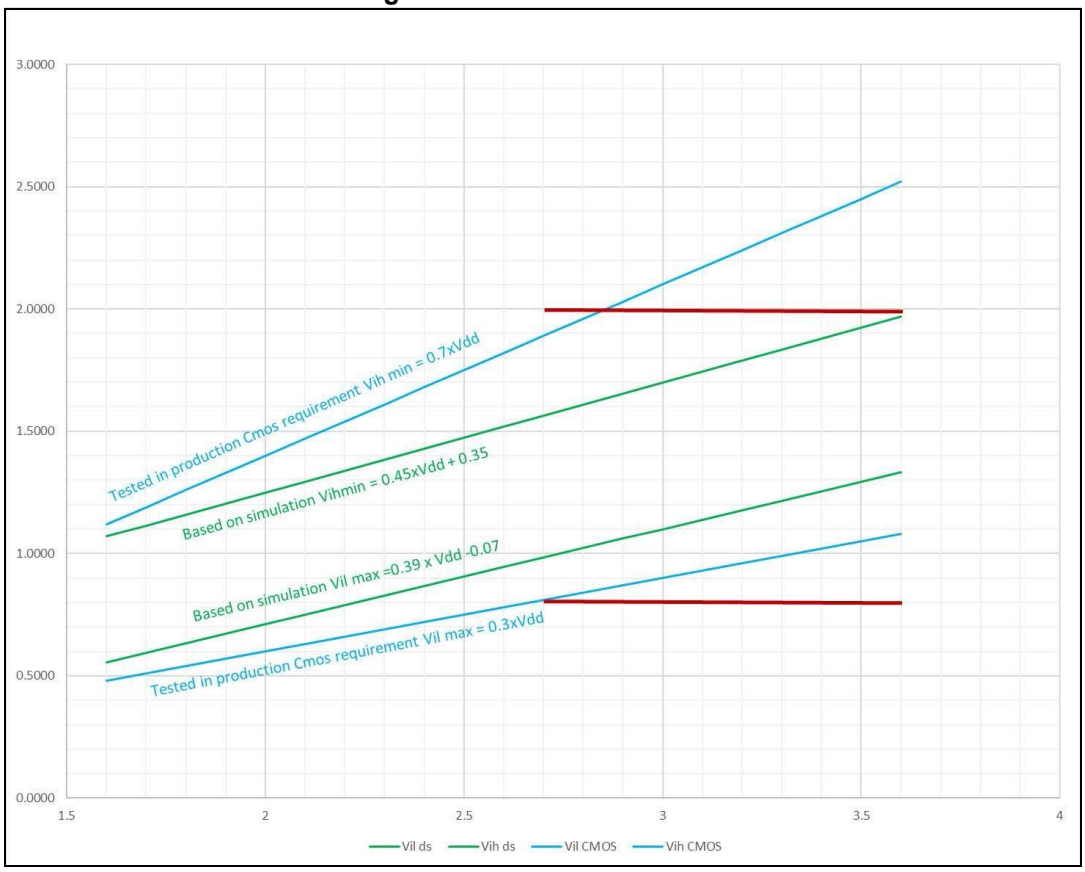
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	1.71 V < V_{DD} < 2.7 V	-	-	0.35 × V_{DD}	V
		2.7 V < V_{DD} < 3.6 V	-	-	0.3 × V_{DD}	
		1.71 V < V_{DD} < 3.6 V	-	-	0.45 × V_{DD} + 0.35	
V_{IH}(1)	I/O input high level voltage	1.71 V < V_{DD} < 3.6 V	0.7 × V_{DD}	-	-	V
V_{HYS}(1)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.71 V < V_{DD} < 3.6 V	-	0.1 × V_{DD}	-	mV
I_{leak}	FT_xx input leakage current(1)	0 < V_{IN} ≤ Max(V_{DD})(6)	-	-	250	nA
		Max(V_{DD}) < V_{IN} ≤ 5.5 V (6)(2)(3)	-	-	3500	
	FT_u, IO	0 < V_{IN} ≤ Max(V_{DD})(6)	-	-	500	
		Max(V_{DD}) < V_{IN} ≤ 5.5 V (6)(3)	-	-	5000(4)	
	TT_xx input leakage current	0 < V_{IN} ≤ Max(V_{DD}) (6)	-	-	100	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN}=V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN}=V_{DD}(6)	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by design.
2. All FT_xx IO except FT_uf, FT_u.
3. V_{IN} must be less than Max(V_{DD}) + 3.6 V.
4. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DD3V3_USBxxx}) +0.3 V, the internal pull-up and pull-down resistors must be disabled.

5. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
6. Max(V_{DD}) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 23*.

Figure 23. VIL/VIH for FT I/Os



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run mode consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $\sum I_{VDD}$ (see *Table 11*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run mode consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $\sum I_{VSS}$ (see *Table 11*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 53. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -8 mA 2.0 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 4 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.45	
V_{OH} (3)	Output high level voltage	I_{IO} = -4 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT_f IO pin in FM+ mode	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 10 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 10: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ∑IIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Table 54. Output voltage characteristics for PC13, PC14, PC15 and PI8(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage	TTL port(2) I_{IO} = -3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(2)	Output low level voltage	I_{IO} = 1.5 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage	I_{IO} = -1.5 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 10: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Output buffer timing characteristics (HSLV option disabled)

Table 55. Output timing characteristics (HSLV OFF)(1)(2)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	20	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	24	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	26	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	30	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	10	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	11	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	12	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	13	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	13.3	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11.4	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10.2	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	8.8	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	23	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	20	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	18.3	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	16	
01	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	68	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	83	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	88	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	103	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	25	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	28	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	30	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	36	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.9	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.9	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.7	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	8.1	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	6.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5.7	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	4.6	

Table 55. Output timing characteristics (HSLV OFF)(1)(2) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	94	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	124	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	144	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	166	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	53	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	66	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	72	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	81	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	3.5	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.7	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.2	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	1.7	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	6.3	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	4.8	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	4	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	3.2	
11	F_{max}(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	110	MHz
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	150	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	185	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	210	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	62	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	70	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	79	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	94	
	t_r/t_f(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	3	ns
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	2.2	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	1.8	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V(5)	-	1.3	
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	5.3	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	4	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	3.3	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(5)	-	2.5	

1. Guaranteed by design.
2. GPIO under VSW domain (PC13, PC14, PC15, PI8) are frequency limited. The maximum frequency is 2 MHz with a maximum load of 30 pF. Only one I/O at a time can be used as GPIO output and these I/Os must not be used as a current source (e.g to drive a LED). For theses IOs, the speed value must be kept to (default) 00.

3. The maximum frequency is defined with the following conditions: (t_r+t_f) ≤ 2/3, skew ≤ 1/20 T and 45% < duty cycle < 55%.
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. Compensation system enabled.

Output buffer timing characteristics (IO structure with _h, HSLV option enabled)

The HSLVEN_xx bits of SYSCFG_IOCTRLSETR register (together with OTP bit PRODUCT_BELOW_2V5) can be used to optimize the I/O speed when the product voltage is below 2.5 V typ. (2.7 V max.).

Table 56. Output timing characteristics (HSLV ON, _h IO structure)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	20	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	22	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	24	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	28	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	9.9	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	8.1	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	7.1	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5.8	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	58	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	79	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	90	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	100	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5.7	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	4.2	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	3.5	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	2.7	
10	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	71	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	101	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	126	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	162	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	4.7	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3.3	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.7	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	1.9	

Table 56. Output timing characteristics (HSLV ON, _h IO structure)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
11	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	77	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	111	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	145	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	172	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	4.3	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.3	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	1.6	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions: (t_r+t_f) ≤ 2/3, skew ≤ 1/20 T and 45% < duty cycle < 55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Output buffer timing characteristics (IO structure with _e, HSLV option enabled)

The HSLVEN_xx bits of SYSCFG_IOCTRLSETR register (together with OTP bit PRODUCT_BELOW_2V5) can be used to optimize the I/O speed when the product voltage is below 2.5 V typ. (2.7 V max.).

Table 57. Output timing characteristics (HSLV ON, _e IO structure)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	36	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	41	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	46	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	55	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	9.2	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	7.4	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	6.5	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	5.2	

Table 57. Output timing characteristics (HSLV ON, _e IO structure)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	55	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	71	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	85	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	100	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	6.1	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	4.7	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	3.9	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	68	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	95	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	118	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	162	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	4.9	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	3.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.8	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.1	
11	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	80	MHz
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	121	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	162	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	245	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	4.2	ns
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.8	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	2.1	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2.7 V(4)	-	1.4	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3, skew ≤ 1/20 T and 45% < Duty cycle < 55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

6.3.18 NRST and NRST_CORE pin characteristics

The NRST and NRST_CORE pins input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 52: I/O static characteristics*).

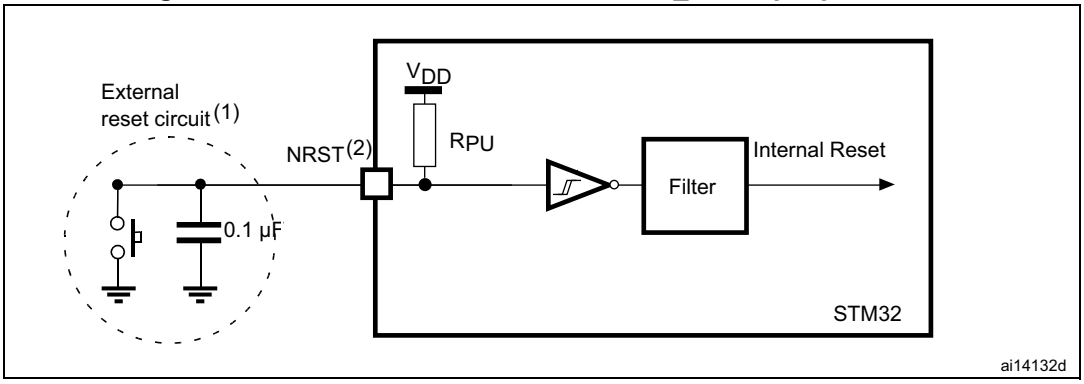
Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 58. NRST and NRST_CORE pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST/NRST_CORE Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST/NRST_CORE Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 24. Recommended NRST and NRST_CORE pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST/NRST_CORE pin can go below the $V_{IL(NRST)}$ max level specified in *Table 58*. Otherwise the reset is not taken into account by the device.

6.3.19 FMC characteristics

Unless otherwise specified, the parameters given in *Table 59* to *Table 72* for the FMC interface are derived from tests performed under the ambient temperature, F_{mc_hclk} (F_{hclk6}) frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5×V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

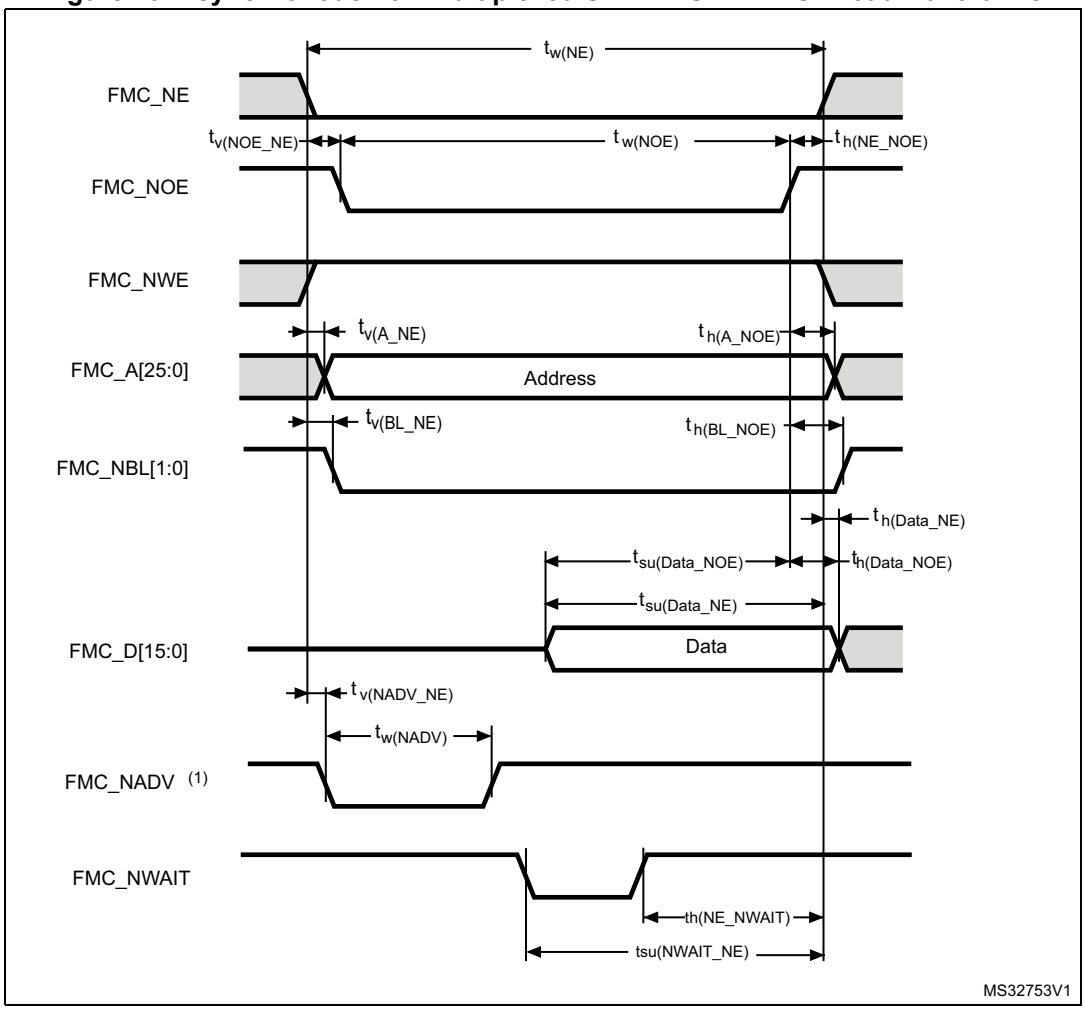
Asynchronous waveforms and timings

Figure 25 through *Figure 28* represent asynchronous waveforms and *Table 59* through *Table 66* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime = 0x1 ($1\times T_{fmc\_ker\_ck}$ for read operations and $2\times T_{fmc\_ker\_ck}$ for write operations)
- ByteLaneSetup = 0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period.

Figure 25. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck}-1$	$3T_{fmc\_ker\_ck}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc\_ker\_ck}-1$	$2T_{fmc\_ker\_ck}+1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}-1$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc\_ker\_ck}-1$	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{fmc\_ker\_ck}+15$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	16	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck}+1$	

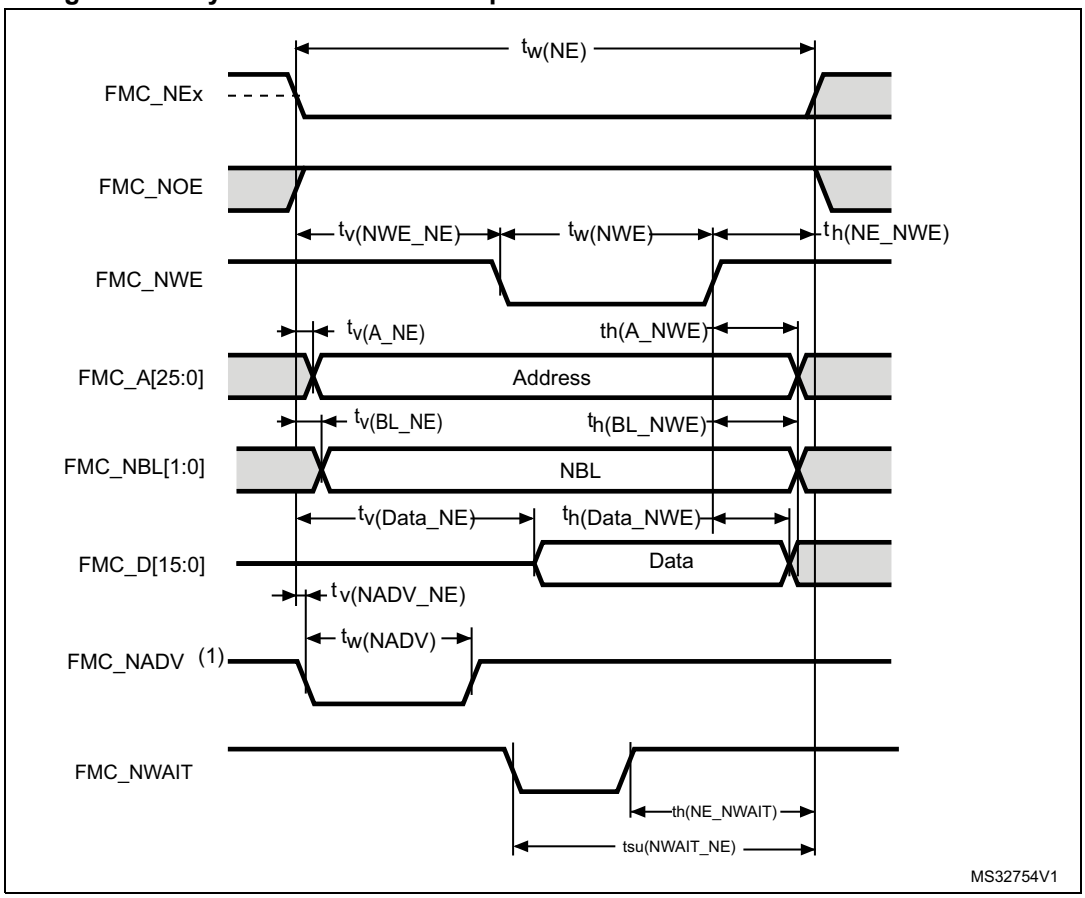
1. Guaranteed by characterization results.

Table 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc\_ker\_ck}-0.5$	$7T_{fmc\_ker\_ck}+1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{fmc\_ker\_ck}-0.5$	$6T_{fmc\_ker\_ck}+1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc\_ker\_ck}$	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{fmc\_ker\_ck}+2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 26. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 61. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck}$-0.5	$4T_{fmc\_ker\_ck}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck}$-0.5	$T_{fmc\_ker\_ck}$+1	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc\_ker\_ck}$-0.5	$T_{fmc\_ker\_ck}$+0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{fmc\_ker\_ck}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$3T_{fmc\_ker\_ck}$-1	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc\_ker\_ck}$-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	2.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$3T_{fmc\_ker\_ck}$-1	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck}$+0.5	

1. Guaranteed by characterization results.

Table 62. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck}$-0.5	$8T_{fmc\_ker\_ck}$+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck}$-0.5	$5T_{fmc\_ker\_ck}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$8T_{fmc\_ker\_ck}$+4	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$6T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 AHB cycle.

Figure 27. Asynchronous multiplexed PSRAM/NOR read waveforms

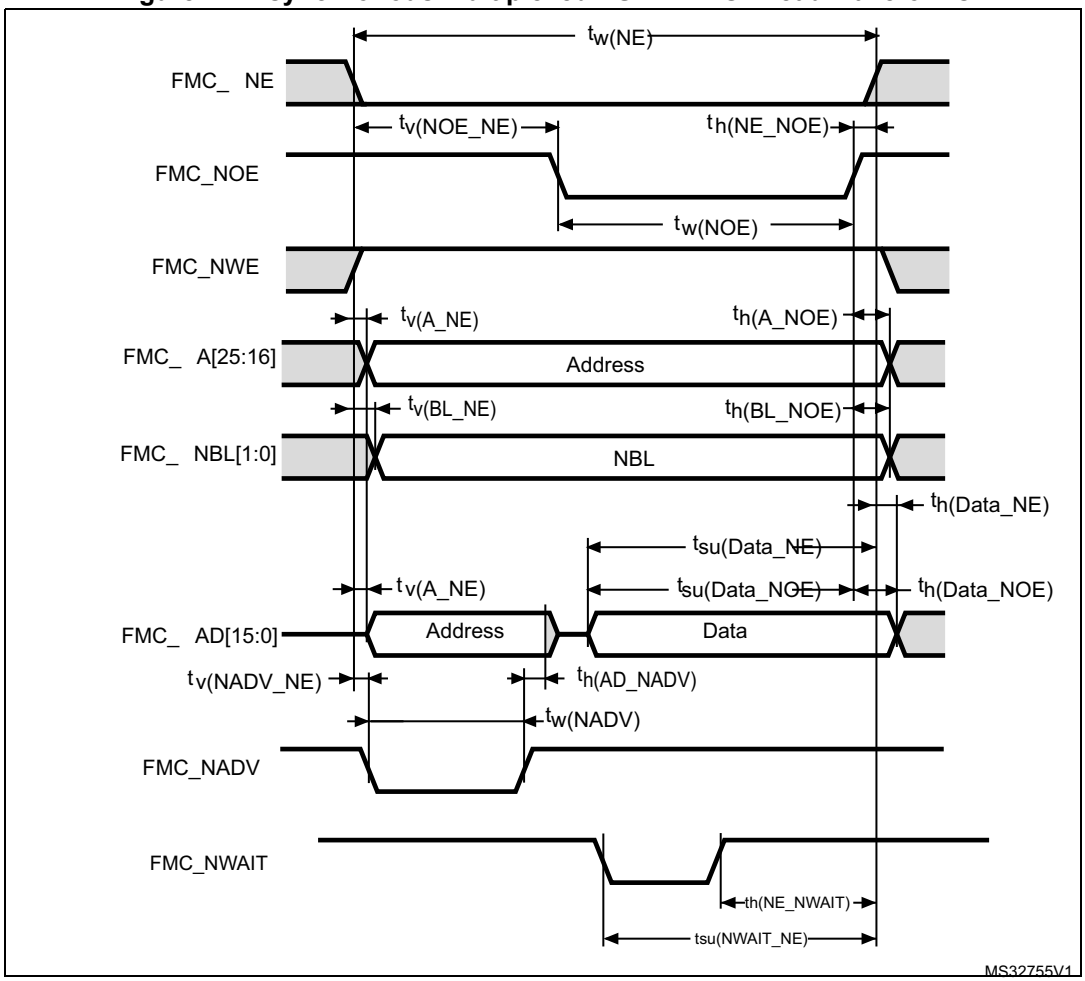


Table 63. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck}$-0.5	$4T_{fmc\_ker\_ck}$+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc\_ker\_ck}$-0.5	$2T_{fmc\_ker\_ck}$+1	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc\_ker\_ck}$-0.5	$T_{fmc\_ker\_ck}$+0.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$-1	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck}$+1	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck}$-3	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{fmc\_ker\_ck}$+15	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	16	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 64. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc\_ker\_ck}$-0.5	$8T_{fmc\_ker\_ck}$+1	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck}$-0.5	$6T_{fmc\_ker\_ck}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{fmc\_ker\_ck}$+2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.

Figure 28. Asynchronous multiplexed PSRAM/NOR write waveforms

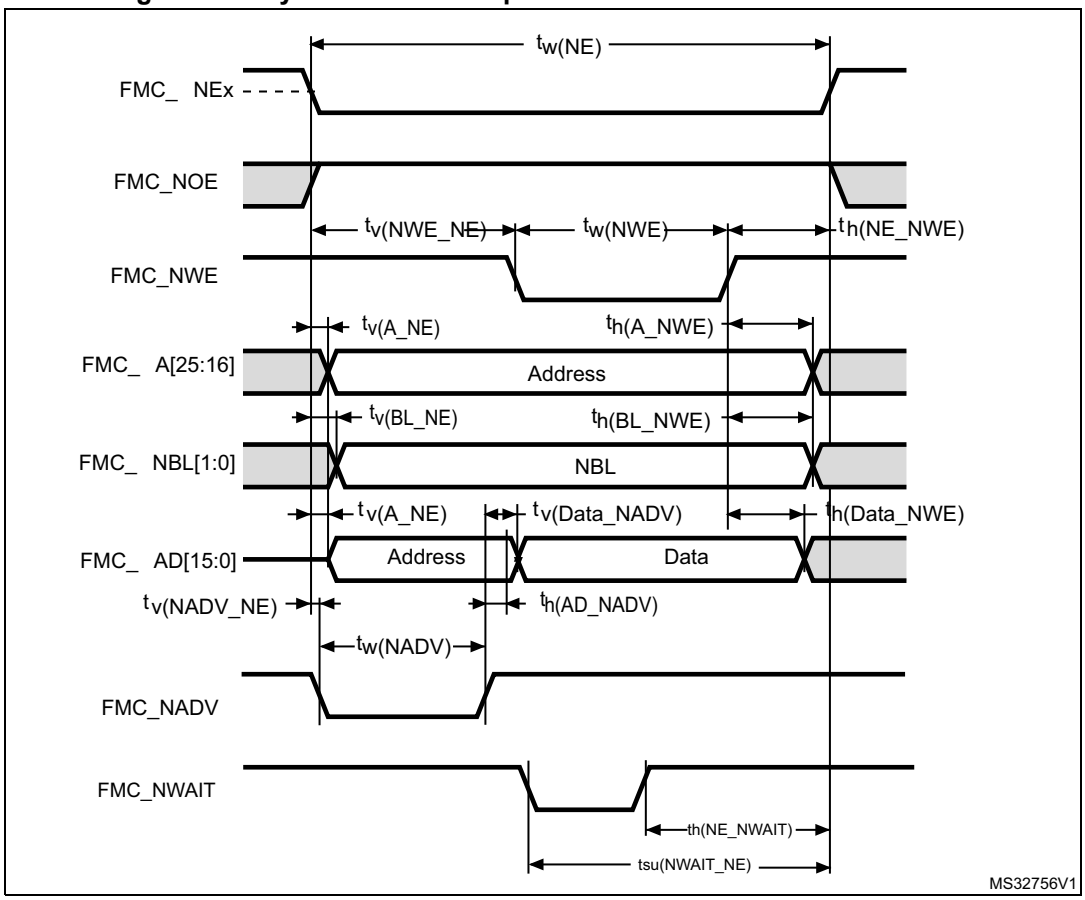


Table 65. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$5T_{fmc\_ker\_ck}$-0.5	$5T_{fmc\_ker\_ck}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck}$-0.5	$T_{fmc\_ker\_ck}$+1	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc\_ker\_ck}$-1	$2T_{fmc\_ker\_ck}$+0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{fmc\_ker\_ck}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$+0.5	$T_{fmc\_ker\_ck}$+1	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck}$+0.5	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	Address held until next write operation	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc\_ker\_ck}$+0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck}$+4	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$3T_{fmc\_ker\_ck}$+0.5	-	

1. Guaranteed by characterization results.

Table 66. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc\_ker\_ck}$-0.5	$9T_{fmc\_ker\_ck}$+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc\_ker\_ck}$-0.5	$6T_{fmc\_ker\_ck}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$8T_{fmc\_ker\_ck}$+4	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$6T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 29 through *Figure 32* represent synchronous waveforms and *Table 67* through *Table 70* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 2.7 V < V_{DD} < 3.6 V, FMC_CLK = 130 MHz at 20 pF
- For 1.71 V < V_{DD} < 1.9 V, FMC_CLK = 95 MHz at 20 pF

Figure 29. Synchronous multiplexed NOR/PSRAM read timings

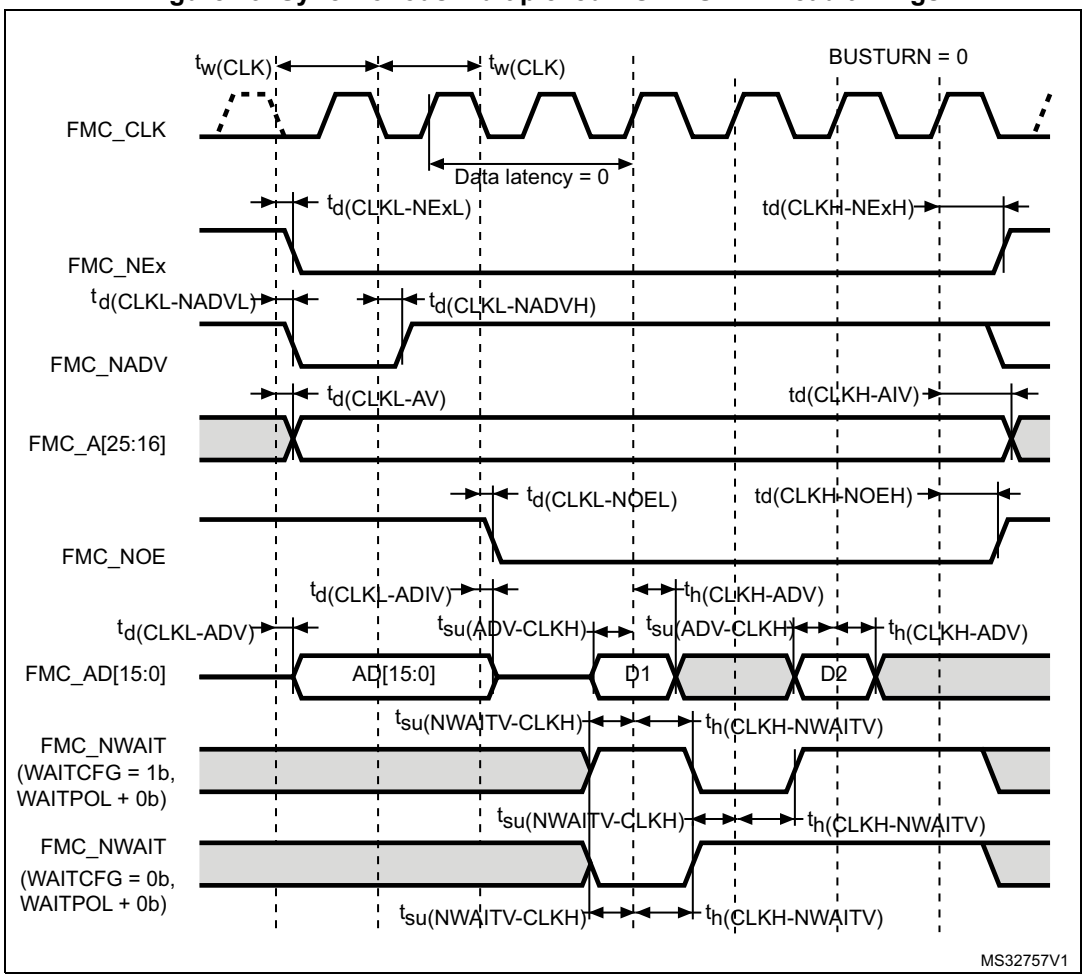


Table 67. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc\_ker\_ck} - 1$(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R \times T_{fmc\_ker\_ck}/2+0.5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R \times T_{fmc\_ker\_ck}/2+1.5$(2)	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc\_ker\_ck}/2+0.5$(2)	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	1.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Guaranteed by characterization results.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 30. Synchronous multiplexed PSRAM write timings

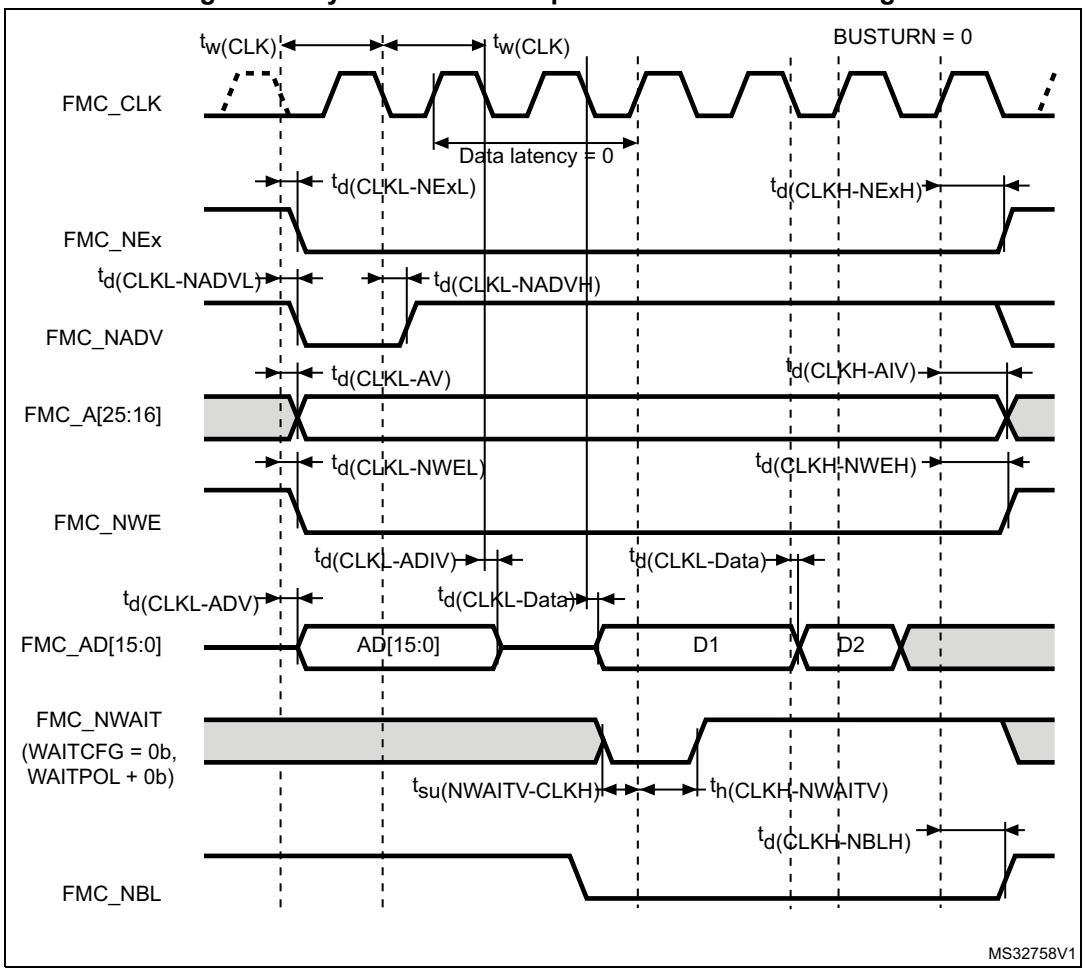


Table 68. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} range = 2.7 to 3.6 V	$R \times T_{fmc\_ker\_ck} - 1^{(2)}$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R \times T_{fmc\_ker\_ck}/2 + 0.5^{(2)}$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R \times T_{fmc\_ker\_ck}/2 + 1.5^{(2)}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc\_ker\_ck}/2 + 0.5^{(2)}$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	1.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc\_ker\_ck}/2 + 0.5^{(2)}$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Guaranteed by characterization results.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 31. Synchronous non-multiplexed NOR/PSRAM read timings

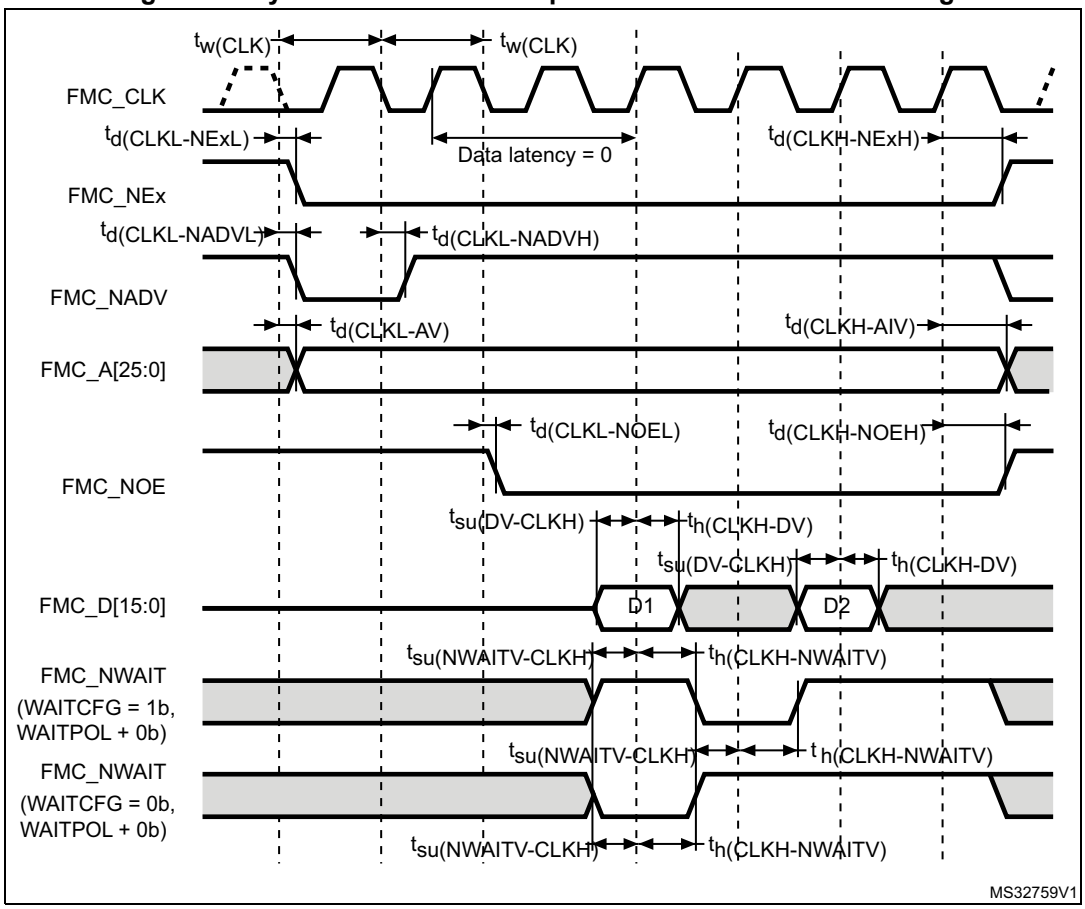


Table 69. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc\_ker\_ck} - 1^{(2)}$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R \times T_{fmc\_ker\_ck}/2+0.5^{(2)}$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R \times T_{fmc\_ker\_ck}/2+1.5^{(2)}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc\_ker\_ck}/2+1.5^{(2)}$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Guaranteed by characterization results.

2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 32. Synchronous non-multiplexed PSRAM write timings

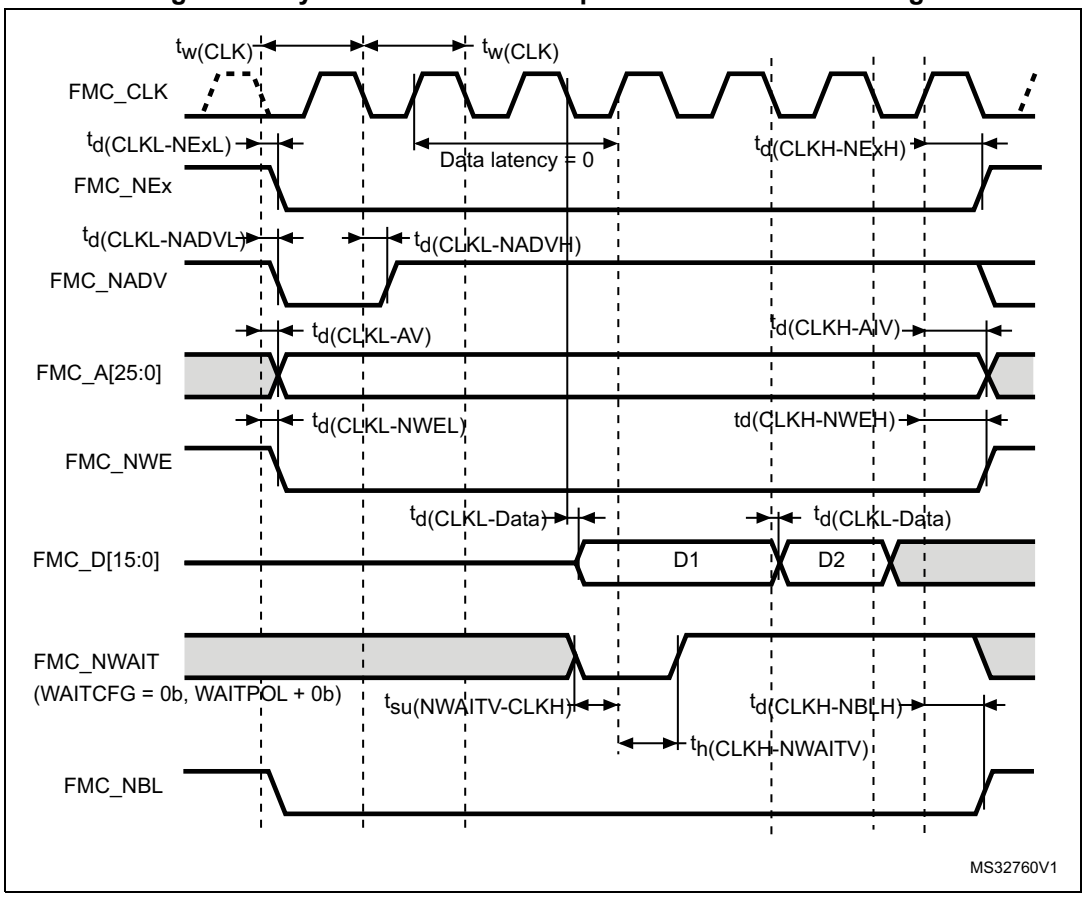


Table 70. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$R \times T_{fmc\_ker\_ck}$ -1(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R \times T_{fmc\_ker\_ck}/2+0.5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R \times T_{fmc\_ker\_ck}/2+1.5$(2)	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc\_ker\_ck}/2+0.5$(2)	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc\_ker\_ck}/2+0.5$(2)	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Guaranteed by characterization results.
2. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

NAND controller waveforms and timings

Figure 33 through *Figure 36* represent synchronous waveforms, and *Table 71* and *Table 72* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- FMC_SetupTime = 0x01
- FMC_WaitSetupTime = 0x03
- FMC_HoldSetupTime = 0x02
- FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30 pF

In all timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period.

Figure 33. NAND controller waveforms for read access

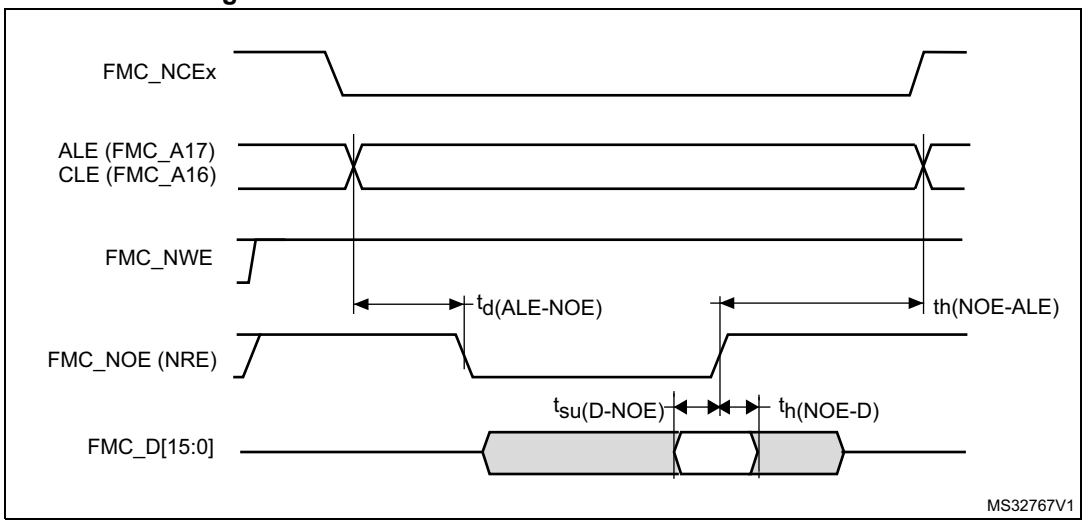


Figure 34. NAND controller waveforms for write access

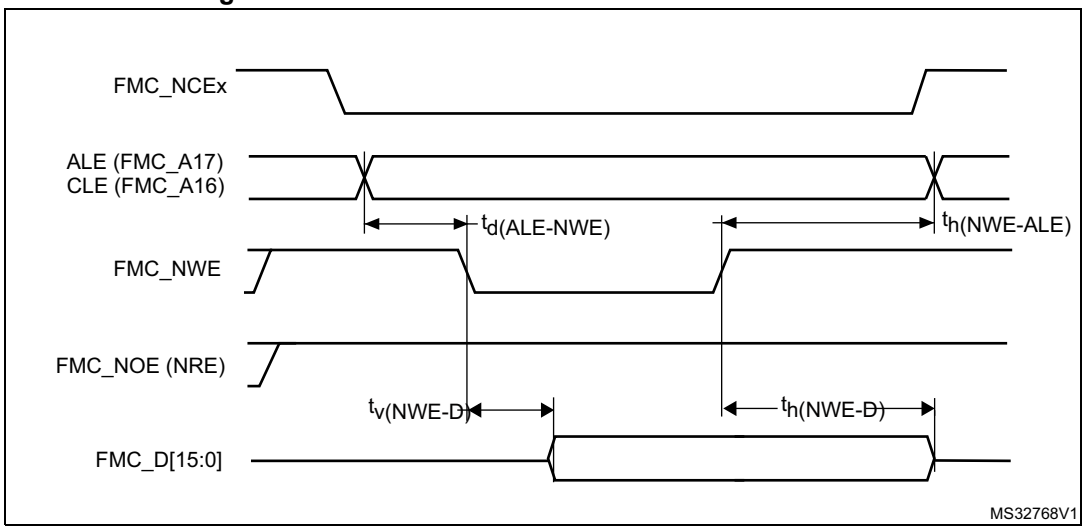


Figure 35. NAND controller waveforms for common memory read access

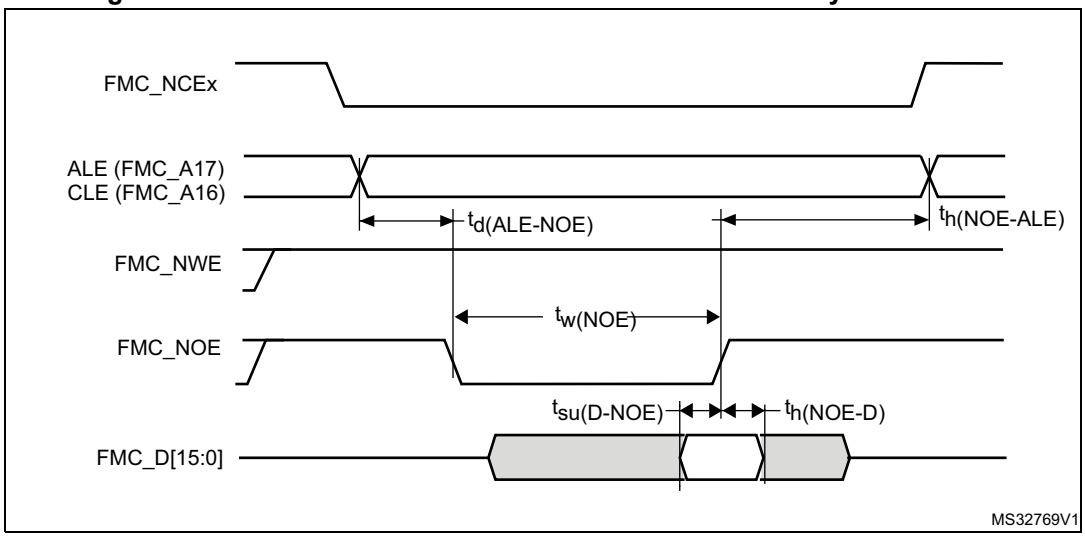


Figure 36. NAND controller waveforms for common memory write access

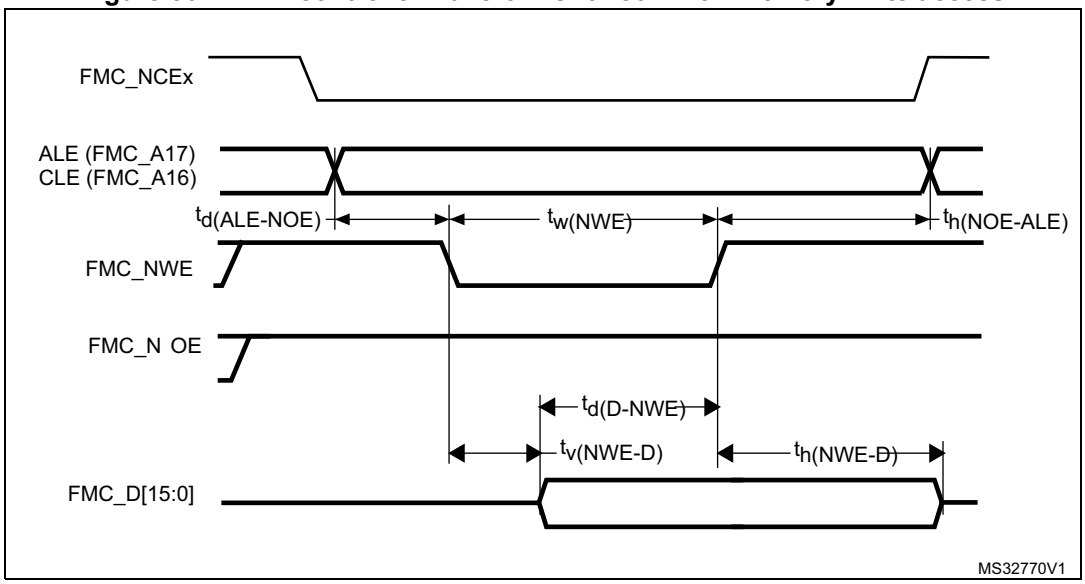


Table 71. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc\_ker\_ck}-1$	$4T_{fmc\_ker\_ck}+1$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$2T_{fmc\_ker\_ck}+1$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc\_ker\_ck}+0.5$	-	

1. Guaranteed by characterization results.

Table 72. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc\_ker\_ck}$-1	$4T_{fmc\_ker\_ck}$+1	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$3T_{fmc\_ker\_ck}$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$4T_{fmc\_ker\_ck}$-3	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$2T_{fmc\_ker\_ck}$+1	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc\_ker\_ck}$+0.5	-	

1. Guaranteed by characterization results.

6.3.20 QUADSPI interface characteristics

Unless otherwise specified, the parameters given in *Table 73* and *Table 74* for QUADSPI are derived from tests performed under the ambient temperature, F_{axiss_ck} frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 73. QUADSPI characteristics in SDR mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CLK)}$	QUADSPI clock frequency	2.7 V ≤ V_{DD} < 3.6 V C_L = 20 pF	-	-	166	MHz
		1.71 V < V_{DD} <3.6 V C_L = 15 pF	-	-	90	
$t_{w(CLKH)}$	QUADSPI clock high and low time	-	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	
$t_{s(IN)}$	Data input setup time	-	1.25	-	-	
$t_{h(IN)}$	Data input hold time	-	2.75	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

Table 74. QUADSPI characteristics in DDR mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CLK)}$	QUADSPI clock frequency	2.7 V < V_{DD} < 3.6 V CL=20 pF	-	-	90	MHz
		1.71 V < V_{DD} < 3.6 V CL=15 pF	-	-	90	
$t_{w(CLKH)}$	QUADSPI clock high and low time	-	$t_{(CLK)}$/2 - 0.5	-	$t_{(CLK)}$/2 + 0.5	ns
$t_{w(CLKL)}$		-	$t_{(CLK)}$/2 - 0.5	-	$t_{(CLK)}$/2 + 0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	0.5	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	2.75	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHHC = 0	-	1	1.5	
		DHHC = 1 Pres = 1, 2...	-	$t_{(CLK)}$/4+1	$t_{(CLK)}$/4+1.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHHC = 0	0	-	-	
		DHHC = 1 Pres = 1, 2...	$t_{(CLK)}$/4	-	-	

Figure 37. QUADSPI timing diagram - SDR mode

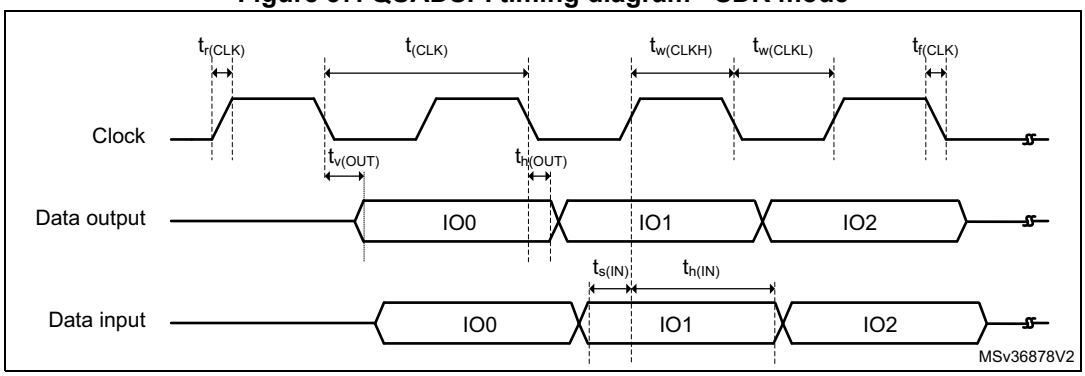
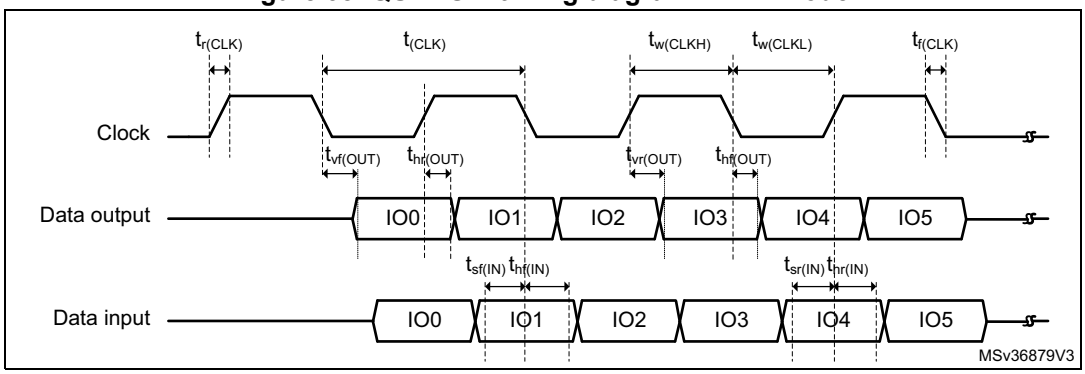


Figure 38. QUADSPI timing diagram - DDR mode



6.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 75* for the delay block are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*.

Table 75. Dynamics characteristics: Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	900	1200	1500	ps
t_{Δ}	Unit Delay	-	42	46	50	

6.3.22 16-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 76* are derived from tests performed under the ambient temperature, f_{pclk2} frequency and V_{DDA} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 76. ADC characteristics(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog power supply	-		1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V		2	-	V_{DDA}	
		$V_{DDA} < 2$ V		V_{DDA}			
V_{REF-}	Negative reference voltage	-		V_{SSA}			
f_{ADC}	ADC clock frequency	2 V ≤ V_{DDA} ≤3.3 V	BOOST = 1	-	-	36	MHz
			BOOST = 0	-	-	20	

Table 76. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S	Sampling rate for Fast channels, BOOST = 1, f_{ADC} = 36 MHz, sampling time = 1.5 cycles	16-bit resolution	-	-	3.60	MSPS
		14-bit resolution	-	-	4.00	
		12-bit resolution	-	-	4.50	
		10-bit resolution	-	-	5.00	
		8-bit resolution	-	-	6.00	
	Sampling rate for Fast channels, BOOST = 0, f_{ADC} = 20 MHz, sampling time = 1.5 cycles	16-bit resolution	-	-	2.00	
		14-bit resolution	-	-	2.20	
		12-bit resolution	-	-	2.50	
		10-bit resolution	-	-	2.80	
		8-bit resolution	-	-	3.30	
	Sampling rate for Slow channels, BOOST = 1, f_{ADC} = 28 MHz, sampling time = 2.5 cycles	16-bit resolution	-	-	2.55	
		14-bit resolution	-	-	2.80	
		12-bit resolution	-	-	3.11	
		10-bit resolution	-	-	3.50	
		8-bit resolution	-	-	4.00	
	Sampling rate for Slow channels, BOOST = 0, f_{ADC} = 20 MHz, sampling time = 2.5 cycles	16-bit resolution	-	-	1.82	
		14-bit resolution	-	-	2.00	
		12-bit resolution	-	-	2.22	
		10-bit resolution	-	-	2.50	
		8-bit resolution	-	-	2.86	
f_{TRIG}	External trigger frequency	f_{ADC} = 36 MHz	-	-	3.6	MHz
		16-bit resolution	-	-	10	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-	V_{REF}/2-10%	V_{REF}/2	V_{REF}/2+10%	
C_{ADC}	Internal sample and hold capacitor	-	-	4	-	pF
t_{ADCREG_STUP}	ADC LDO startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started	1			$1/f_{ADC}$

Table 76. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CAL}	Offset and linearity calibration time	-	16384			$1/f_{ADC}$
t_{OFF_CAL}	Offset calibration time	-	1280			
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2.5	
		CKMODE = 10	-	-	2.5	
		CKMODE = 11	-	-	2.25	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time	-	1.5	-	810.5	
t_{CONV}	Total conversion time (including sampling time)	N-bit resolution	t_s + N/2(4)			
$I_{DDA(ADC)}$	ADC consumption from V_{DDA} supply (differential)	F_S = 3.6 Msps, BOOST = 1	-	1900	-	µA
		F_S = 1 Msps, BOOST = 0	-	460	-	
$I_{DDA(REF)}$	ADC consumption from V_{REF+} (differential)	F_S = 3.6 Msps, BOOST = 1	-	260	-	
		F_S = 1 Msps, BOOST = 0	-	140	-	
$I_{DDA(ADC)}$	ADC consumption from V_{DDA} supply (single-ended)	F_S = 3.6 Msps, BOOST = 1	-	1700	-	
		F_S = 1 Msps, BOOST = 0	-	445	-	
$I_{DDA(REF)}$	ADC consumption from V_{REF+} supply (single-ended)	F_S = 3.6 Msps, BOOST = 1	-	160	-	
		F_S = 1 Msps, BOOST = 0	-	75	-	

1. Guaranteed by design.
2. Voltage BOOSTER on ADC switches must be used for V_{DDA} < 2.4 V (switches inside IO).
3. Depending on the package, V_{REF-} can be internally connected to V_{SSA}.
4. 9 to 818 cycles @ 14-bit mode.

Table 77. Minimum sampling time versus RAIN with 47 pF PCB capacitor up to 125 °C and V_{DDA} = 1.6 V(1)

Resolution(2)	RAIN (Ω)	Fast channels(3) (ns)	Slow channels(4) (ns)
16 bits	47(5)	107	166
14 bits	47	90.8	144
	68	967	151
	100	108	157
	150	128	171
	220(5)	161	192
12 bits	47	76.7	125
	68	81.5	127
	100	89.8	134
	150	107	146
	220	132	169
	330	177	205
	470	2.36	264
	680	329	345
	1000(5)	462	488
10 bits	47	62.5	103
	68	66.2	106
	100	72.7	112
	150	85.4	121
	220	106	137
	330	140	168
	470	187	209
	680	258	279
	1000	367	381
	1500	537	552
	2200	776	786
	3300	1130	1140
	4700(5)	1600	1600

Table 77. Minimum sampling time versus RAIN with 47 pF PCB capacitor up to 125 °C and V_{DDA} = 1.6 V(1) (continued)

Resolution(2)	RAIN (Ω)	Fast channels(3) (ns)	Slow channels(4) (ns)
8 bits	47	48.7	82.4
	68	51.4	84.6
	100	56.4	88.7
	150	65.8	95.7
	220	80.4	108
	330	106	130
	470	139	160
	680	189	208
	1000	269	284
	1500	390	405
	2200	562	572
	3300	827	840
	4700	1170	1170
	6800	1670	1670
	10000	2440	2430
	15000	3660	3630
	2200(5)	5360	5310

1. Guaranteed by design.
2. The tolerance is 8 LSB for 16-bit, 4 LSB for 14-bit, 2 LSB for 12-bit, 10-bit and 8-bit conversions.
3. On ADC1, fast channels are PA6, PA7, PB0, PB1, PC4, PC5, PF11, PF12.
   On ADC2, fast channels are PA6, PA7, PB0, PB1, PC4, PC5, PF13, PF14.
4. Slow channels are all ADC inputs except the fast channels.
5. Maximum external input impedance value authorized for the given resolution.

Table 78. ADC accuracy(1)(2)(3)(4)(5)(6)(7)

Symbol	Parameter	Conditions(8)		Min	Typ(9)	Max	Unit
ET(10)	Total unadjusted error	Single ended	BOOST = 1	-	±5	-	±LSB
			BOOST = 0	-	±7	-	
		Differential	BOOST = 1	-	±6	-	
			BOOST = 0	-	±5	-	
ED	Differential linearity error	Single ended	BOOST = 1	-	3	-	
			BOOST = 0	-	1	-	
		Differential	BOOST = 1	-	8	-	
			BOOST = 0	-	2	-	
EL	Integral linearity error	Single ended	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
		Differential	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
ENOB(11)	Effective number of bits (2 MSPS)	Single ended	BOOST = 1	-	12.5	-	bits
			BOOST = 0	-	12.75	-	
		Differential	BOOST = 1	-	13.3	-	
			BOOST = 0	-	13.7	-	
SINAD(11)	Signal-to-noise and distortion ratio (2 MSPS)	Single ended	BOOST = 1	-	77.5	-	dB
			BOOST = 0	-	78.75	-	
		Differential	BOOST = 1	-	82	-	
			BOOST = 0	-	84.2	-	
SNR(11)	Signal-to-noise ratio (2 MSPS)	Single ended	BOOST = 1	-	77.6	-	
			BOOST = 0	-	79	-	
		Differential	BOOST = 1	-	82.4	-	
			BOOST = 0	-	84.3	-	
THD(11)	Total harmonic distortion	Single ended	BOOST = 1	-	-85	-	
			BOOST = 0	-	-88	-	
		Differential	BOOST = 1	-	-90	-	
			BOOST = 0	-	-93	-	

1. Guaranteed by characterization.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy versus negative injection current: injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The above table gives the ADC performance in 16-bit mode.
5. Dual Simultaneous mode is limited to 12-bit.
6. Dual mode consisting in an injected conversion (reset) occurring during another (regular) conversion is forbidden.
7. Dual Interleaved 16-bit/14-bit/12-bit modes can work if the delay between the 2 ADCs is as specified in *Table 79*.

8. ADC clock frequency ≤36 MHz, 2 V ≤ V_{DDA} ≤ 3.3 V, 1.6 V ≤ V_{REF+} ≤ V_{DDA}, BOOSTEN (for I/O) = 1.
9. V_{DDA} = V_{REF+} = 3.3 V, 25 °C.
10. ET, ED, EL are specified for [2 V ≤ V_{DDA} ≤ 3.3 V with 2 V ≤ V_{REF+} ≤ V_{DDA}] and [1.6V ≤ V_{DDA} ≤ 2 V with 1.6V ≤ V_{REF+} ≤ V_{DDA}].
11. ENOB, SINAD, SNR and THD are specified for V_{DDA} = V_{REF+} = 3.3 V.

Table 79. Minimum delay for interleaved conversion versus resolution

		16-bit Mode		14-bit mode		12-bit Mode	
Boost	**Fclk (MHz)**	**Delay ADC1/ADC2 (clock cycles)**	**Data rate (MSPS)**	**Delay ADC1/ADC2 (clock cycles)**	**Data rate (MSPS)**	**Delay ADC1/ADC2 (clock cycles)**	**Data rate (MSPS)**
0	1	1.5	1.0	1.5	1.0	1.5	1.0
0	2	1.5	2.0	1.5	2.0	1.5	2.0
0	3	1.5	1.5	1.5	1.5	1.5	1.5
0	4	1.5	2.0	1.5	2.0	1.5	2.0
0	5	1.5	1.7	1.5	1.7	1.5	2.5
0	6	1.5	2.0	1.5	2.0	1.5	2.0
0	7	2.5	1.8	1.5	2.3	1.5	2.3
0	8	2.5	2.0	2.5	2.0	1.5	2.7
0	9	3.5	1.8	2.5	2.3	2.5	2.3
0	10	3.5	2.0	3.5	2.0	2.5	2.5
0	11	4.5	1.8	3.5	2.2	2.5	2.8
0	12	4.5	2.0	4.5	2.0	3.5	2.4
0	13	4.5	2.2	4.5	2.2	3.5	2.6
0	14	4.5	2.3	4.5	2.3	3.5	2.8
0	15	5.5	2.1	4.5	2.5	3.5	3.0
0	16	5.5	2.3	4.5	2.7	3.5	3.2
0	17	5.5	2.4	4.5	2.8	3.5	3.4
0	18	5.5	2.6	4.5	3.0	3.5	3.6
0	19	5.5	2.7	4.5	3.2	3.5	3.8
0	20	5.5	2.9	4.5	3.3	3.5	4.0
1	21	4.5	3.5	3.5	4.2	3.5	4.2
1	22	4.5	3.7	3.5	4.4	3.5	4.4
1	23	4.5	3.8	3.5	4.6	3.5	4.6
1	24	4.5	4.0	4.5	4.0	3.5	4.8
1	25	4.5	4.2	4.5	4.2	3.5	5.0
1	26	4.5	4.3	4.5	4.3	3.5	5.2
1	27	5.5	3.9	4.5	4.5	3.5	5.4

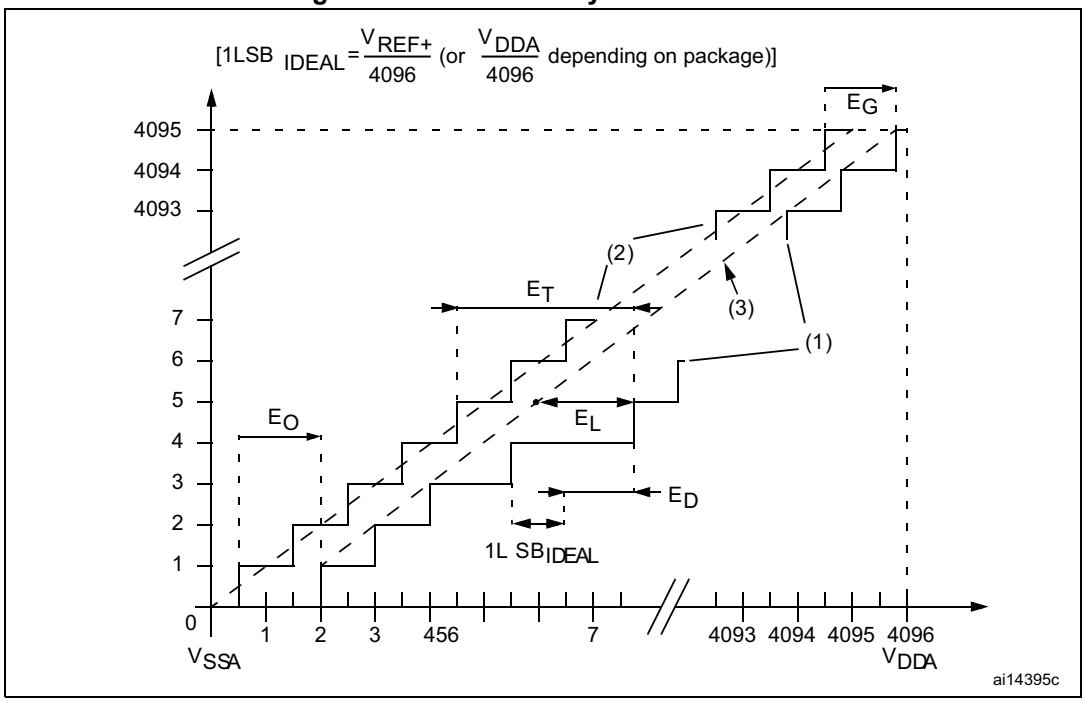
Table 79. Minimum delay for interleaved conversion versus resolution (continued)

		16-bit Mode		14-bit mode		12-bit Mode	
Boost	**Fclk (MHz)**	**Delay ADC1/ADC2 (clock cycles)**	**Data rate (MSPS)**	**Delay ADC1/ADC2 (clock cycles)**	**Data rate (MSPS)**	**Delay ADC1/ADC2 (clock cycles)**	**Data rate (MSPS)**
1	28	5.5	4.0	4.5	4.7	3.5	5.6
1	29	5.5	4.1	4.5	4.8	3.5	5.8
1	30	5.5	4.3	4.5	5.0	3.5	6.0
1	31	5.5	4.4	4.5	5.2	3.5	6.2
1	32	5.5	4.6	4.5	5.3	3.5	6.4
1	33	5.5	4.7	4.5	5.5	3.5	6.6
1	34	5.5	4.9	4.5	5.7	3.5	6.8
1	35	5.5	5.0	4.5	5.8	3.5	7.0
1	36	5.5	5.1	4.5	6.0	3.5	7.2

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

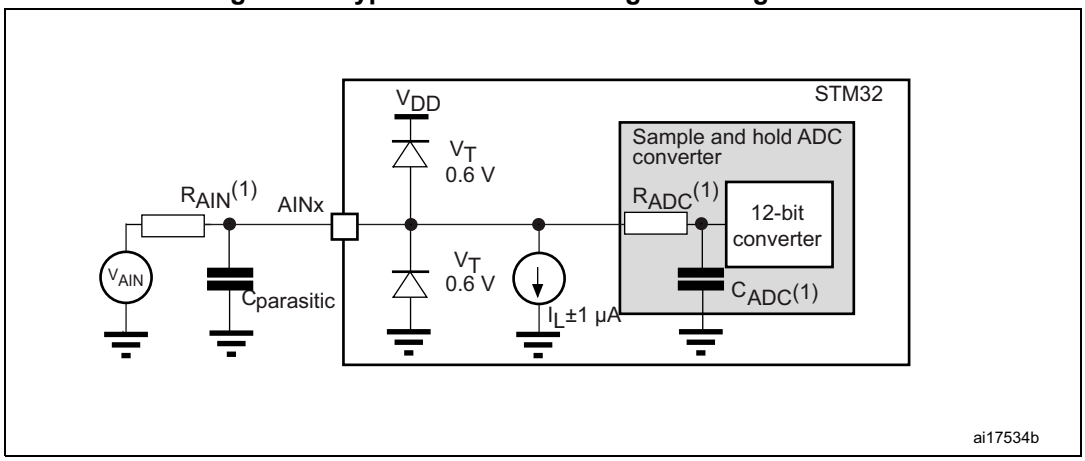
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\sum I_{INJ(PIN)}$ in *Section 6.2* does not affect the ADC accuracy.

Figure 39. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 40. Typical connection diagram using the ADC



1. Refer to *Table 76* for the values of RAIN, RADC and CADC.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

PCB design guidelines are provided in AN5031 “Getting started with STM32MP1 Series hardware development.” available from the ST website *www.st.com*.

6.3.23 DAC electrical characteristics

Table 80. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	V
R_L	Resistive Load	DAC output buffer ON, Not valid in Sample & Hold mode	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	kΩ
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	kΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	kΩ
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} -0.2(2)	V
		DAC output buffer OFF		0	-	V_{REF+}	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±1LSB)	Normal mode, DAC output buffer ON, $C_L \le 50$ pF $R_L \ge 5$ kΩ	±1 LSB	-	2	-	µs
		Normal mode, DAC output buffer OFF, +/-1LSB, Cload ≤ 10 pF		-	2	-	µs
t_{WAKEUP}(3)	Wakeup time from off state (setting the Enx bit in the DAC Control register) until the ±1LSB final value	Normal mode, DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	5	-	µs
		Normal mode, DAC output buffer OFF, $C_L \le 10$ pF		-	2	-	µs
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON $C_L \le 50$ pF, R_L = 5 kΩ DC		-	-80	-	dB

Table 80. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SAMP}	Sampling time in Sample and Hold mode C_{SH}=100nF (Code transition between the lowest input code and the highest input code when DAC_OUT reaches final value ± 1LSB)	DACMCR.MODEx[2:0] = 100/101 (BUFFER ON)		-	0.7	-	ms
		DACMCR.MODEx[2:0] = 110 (BUFFER OFF)		-	11.5	-	
		DACMCR.MODEx[2:0] = 111 (INTERNAL BUFFER OFF)		-	0.3	-	
CI_{int}	Internal sample and hold capacitor	-		-	2.2	-	pF
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	450	-	µV
		V_{REF+} = 1.8 V		-	213	-	
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	TBD	-	µA
			No load, worst code (0xF1C)	-	TBD	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	TBD	-	
		Sample and Hold mode, C_{SH} = 100 nF		-	TBD	-	
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	TBD	-	
			No load, worst code (0xF1C)	-	TBD	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	TBD	-	
		Sample and Hold mode, Buffer ON, C_{SH} = 100 nF (worst code)		-	TBD	-	
		Sample and Hold mode, Buffer OFF, C_{SH} = 100 nF (worst code)		-	TBD	-	

1. Guaranteed by design.
2. Since V_{REF+} must always be ≤ VDDA, maximum V_{DAC_OUT} = minimum value between Max(V_{REF+}) and Max(V_{DDA}-0.2)
3. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).

Table 81. DAC accuracy

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON	-	±2	TBD	LSB
		DAC output buffer OFF	-	±2	TBD	

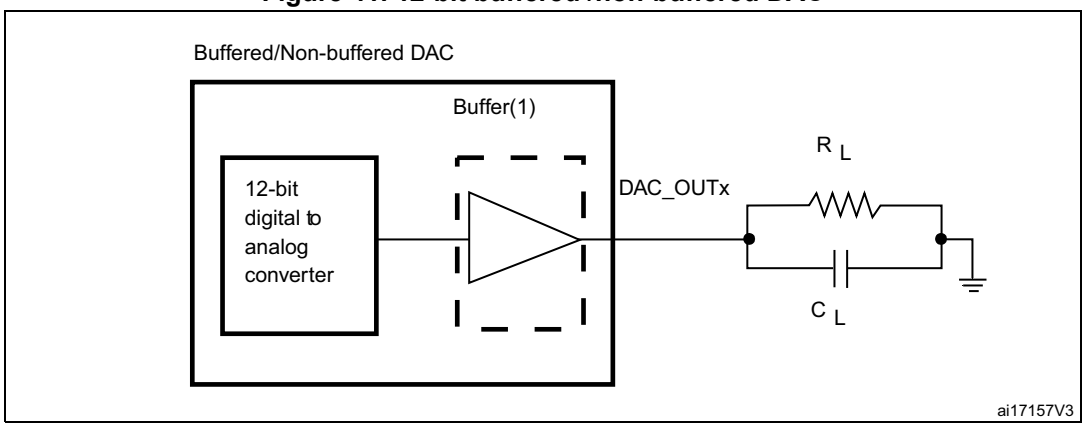
Table 81. DAC accuracy (continued)

Symbol	Parameter	Conditions		Min	Typ(1)	Max	Unit
INL	Integral non linearity(3)	DAC output buffer ON, C_L≤50 pF, R_L≥5 kΩ		-	±4	TBD	LSB
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	±4	TBD	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ	V_{REF+} = 3.6 V	-	±12	TBD	LSB
			V_{REF+} = 1.8 V	-	±25	TBD	
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	±8	TBD	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	±5	TBD	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ	V_{REF+} = 3.6 V	-	±5	TBD	LSB
			V_{REF+} = 1.8 V	-	±7	TBD	
Gain	Gain error(5)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ		-	±1	TBD	%
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	±1	TBD	
TUE	Total unadjusted error	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ		-	±30	TBD	LSB
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	±12	TBD	
TUECal	Total unadjusted error after calibration	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ	V_{REF+}=3.6 V	-	±10	TBD	LSB
			V_{REF+}=1.8 V	-	±8	TBD	
SNR	Signal-to-noise ratio(6)	DAC output buffer ON,C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz, BW = 500 kHz		-	67.8	-	dB
THD	Total harmonic distorsion(6)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1kHz		-	-78.6	-	dB
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz		-	67.5	-	dB
ENOB	Effective number of bits	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz		-	10.9	-	bits

1. Guaranteed by characterization.
2. Difference between two consecutive codes minus 1 LSB.

3. Difference between measured the value at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is -0.5dBFS with $F_{sampling}$=1 MHz.

Figure 41. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.24 Voltage reference buffer characteristics

Table 82. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode(2)	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode	VSCALE = 000	-	2.5	-	
			VSCALE = 001	-	2.048	-	
			VSCALE = 010	-	1.8	-	
			VSCALE = 011	-	1.5	-	
		Degraded mode(2)	VSCALE = 000	V_{DDA}- 220 mV	-	2.5	
			VSCALE = 001	V_{DDA}- 220 mV	-	2.048	
			VSCALE = 010	V_{DDA}- 220 mV	-	1.8	
			VSCALE = 011	V_{DDA}- 220 mV	-	1.5	
TRIM	Trim step resolution	-	-	-	±0.05	-	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +125 °C	-	-	$T_{coeff\_VREFINT}$ +75	-	ppm/ °C
		0 °C < T_J < +50 °C	-	-	TBD	-	
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100 kHz	-	-	40	-	

Table 82. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{START}	Start-up time	C_L = 0.5 µF	-	-	300	-	µs
		C_L = 1 µF	-	-	500	-	
		C_L = 1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	-	µA
		I_{LOAD} = 500 µA	-	-	16	-	
		I_{LOAD} = 4 mA	-	-	32	-	

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}-drop voltage).
3. To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

6.3.25 Temperature sensor characteristics

Table 83. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	VSENSE linearity with temperature (from Vsensor voltage)	-	-	3	°C
	VSENSE linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from Vsensor voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30 °C ± 5 °C	-	0.62	-	V
t_{start_run}(1)	Startup time in Run mode (buffer startup)	5.3	-	40.5	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9.8	-	-	
I_{sens}(1)	Sensor consumption	0.11	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	2.3	3.8	6.1	

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 84. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ±5 °C V_{DDA} = V_{REF+} = 3.3 V ±10 mV	0x5C00 525C[15:0](1)(2)
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C ±2 °C V_{DDA} = V_{REF+} = 3.3 V ±10 mV	0x5C00 525C[31:16](1)(2)

1. It is mandatory to read a 32-bit word and to do relevant masking and shifting to isolate the required bits.
2. This address is located inside the BSEC and the access is allowed after being enabled in the RCC.

6.3.26 DTS characteristics

Table 85. DTS characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}	Output Clock frequency (PTAT clock)	-	-	500	-	kHz
T_{SLOPE}	Average slope	-	-	1600	-	Hz/°C
T_L	Linearity with temperature (from Output clock frequency).	V_{DDCORE} = 1.2 V	-	-	3.8	°C
T_{TOTAL_ERROR}	Temperature measurement error	V_{DDCORE} = 1.2 V Temperature: -40 to 125 °C	-5	-	+5	°C
$T_{VDD\ CORE}$	Additional error due to V_{DDCORE} variation	-	-	10	-	°C/V
t_{TRIM}	Calibration time	-	2	-	-	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready signal = 1	-	-	50	-	µs
I_{DDCORE_DTS}	DTS consumption on V_{DDCORE}	-	-	20	-	µA

1. Guaranteed by design.

6.3.27 V_{BAT} ADC monitoring characteristics and charging characteristics

Table 86. V_{BAT} ADC monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	kΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9.8	-	-	µs

1. Guaranteed by design.

Table 87. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	kΩ
		VBRS in PWR_CR3= 1	-	1.5	-	

6.3.28 Temperature and V_{BAT} monitoring characteristics for tamper detection

Table 88. Temperature and V_{BAT} monitoring characteristics for temper detection

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	105	116	126	°C
$TEMP_{low}$	Low temperature monitoring	-42	-31	-20	
$V_{BAThigh}$(1)	High supply monitoring	3.47	3.59	3.73	V
V_{BATlow}(1)	Low supply monitoring	1.3	1.34	1.43	

1. Monitored supply is V_{SW} (i.e. V_{DD} if V_{DD} is present, V_{BAT} otherwise)

6.3.29 V_{DDCORE} monitoring characteristics

Table 89. V_{DDCORE} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{S\_vddcore}$(1)	ADC sampling time when reading V_{DDCORE} input	100	-	-	ns

1. Guaranteed by design.

6.3.30 Voltage booster for analog switch

Table 90. Voltage booster for analog switch characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.71	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

6.3.31 Compensation cell

Table 91. Compensation cell characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{COMPCELL}$	V_{DD} current consumption during code calculation	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	3.5	mA
		2.7 V < V_{DD} < 3.6 V	-	-	10	
T_{READY}	Time needed for code calculation	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	300	µs
		2.7 V < V_{DD} < 3.6 V	-	-	250	

6.3.32 Digital filter for sigma-delta modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 92* for DFSDM are derived from tests performed under the ambient temperature, f_{pclkx} frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5×V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDMx_CKINx, DFSDMx_DATINx, DFSDMx_CKOUT for DFSDMx).

Table 92. DFSDM measured timing

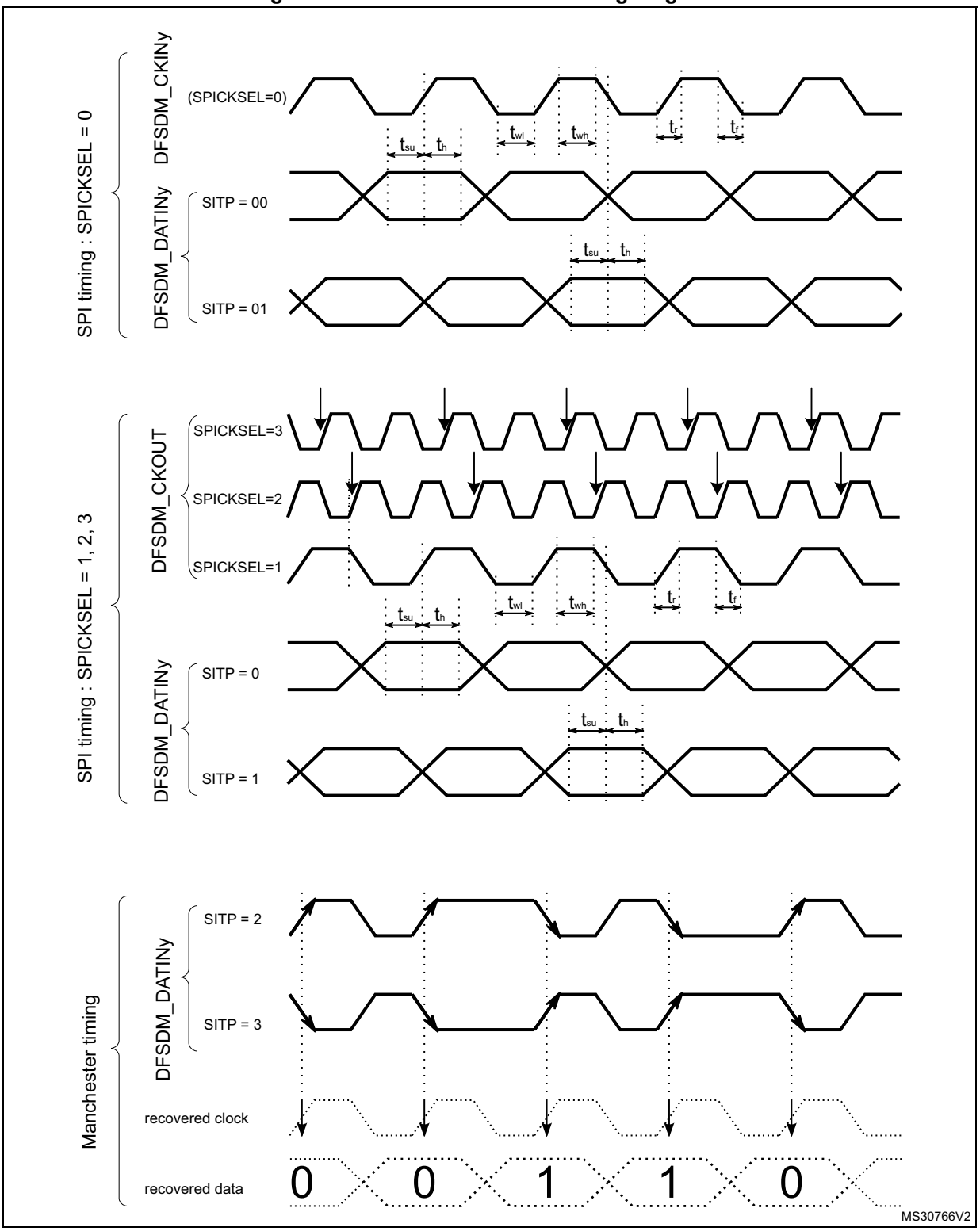
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 V < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 V < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%

Table 92. DFSDM measured timing (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	$T_{CKIN}/2$ - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	1	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]10), 1.71 < V_{DD} < 3.6 V	(CKOUTDIV+1) ×$T_{DFSDMCLK}$(1)	-	(2×CKOUTDIV) × $T_{DFSDMCLK}$(1)	

1. See DFSDM section in RM0436 reference manual for definition of CKOUTDIV.

Figure 42. Channel transceiver timing diagrams



6.3.33 Camera interface (DCMI) characteristics

Unless otherwise specified, the parameters given in *Table 93* for DCMI are derived from tests performed under the ambient temperature, F_{mcu_ck} frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*, with the following configuration:

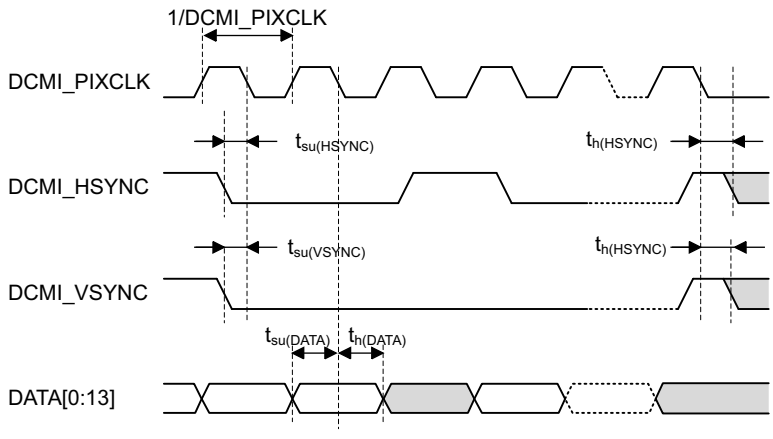
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Table 93. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/F_{mcu_ck}	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	80	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data input hold time	0.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	

1. Guaranteed by characterization results.

Figure 43. DCMI timing diagram



6.3.34 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 94* for LCD-TFT are derived from tests performed under the ambient temperature, F_{pclk4} frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled

Table 94. LTDC characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V OSPEEDR[1:0] = 11, 10	-	90	MHz
		1.71 V < V_{DD} < 3.6 V OSPEEDR[1:0] = 11	-	45	
		1.71 V < V_{DD} < 3.6 V OSPEEDR[1:0] = 10	-	38	
D_{CLK}	LTDC clock output duty cycle	-	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time	-	$t_{w(CLK)}/2$ - 0.5	$t_{w(CLK)}/2$ + 0.5	ns
$t_{v(DATA)}$	Data output valid time	OSPEEDR[1:0] = 11	-	3	
		OSPEEDR[1:0] = 10	-	4	
$t_{h(DATA)}$	Data output hold time	-	0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	OSPEEDR[1:0] = 11	-	2.5	
		OSPEEDR[1:0] = 10	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time	-	0	-	

1. Guaranteed by characterization results.

Figure 44. LCD-TFT horizontal timing diagram

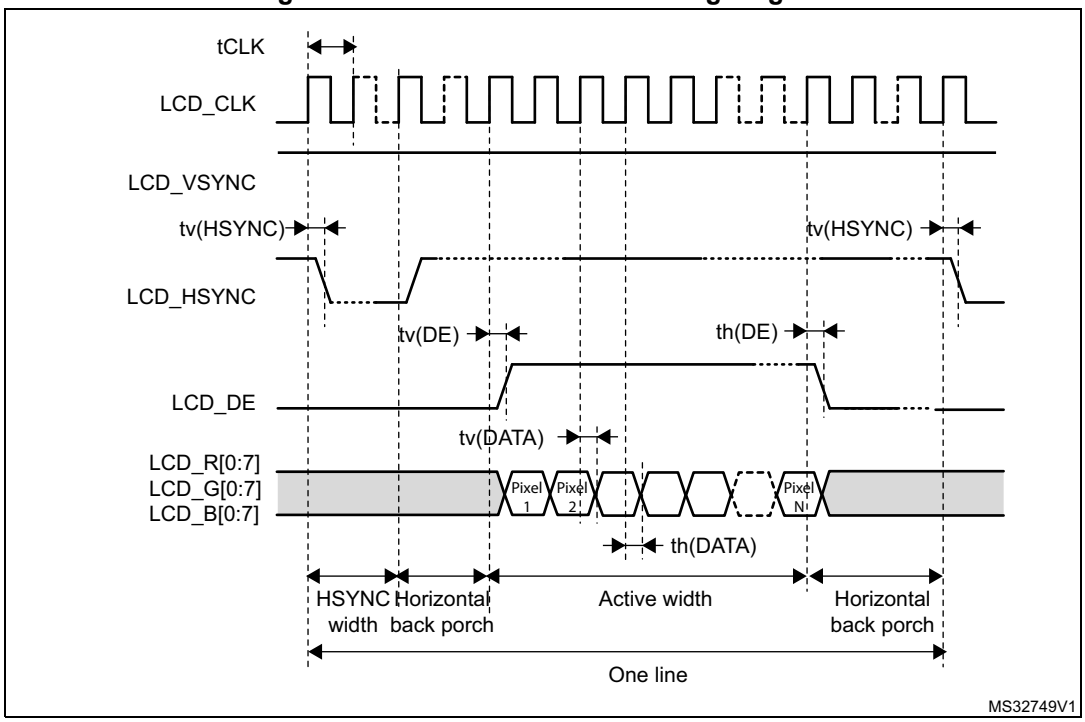
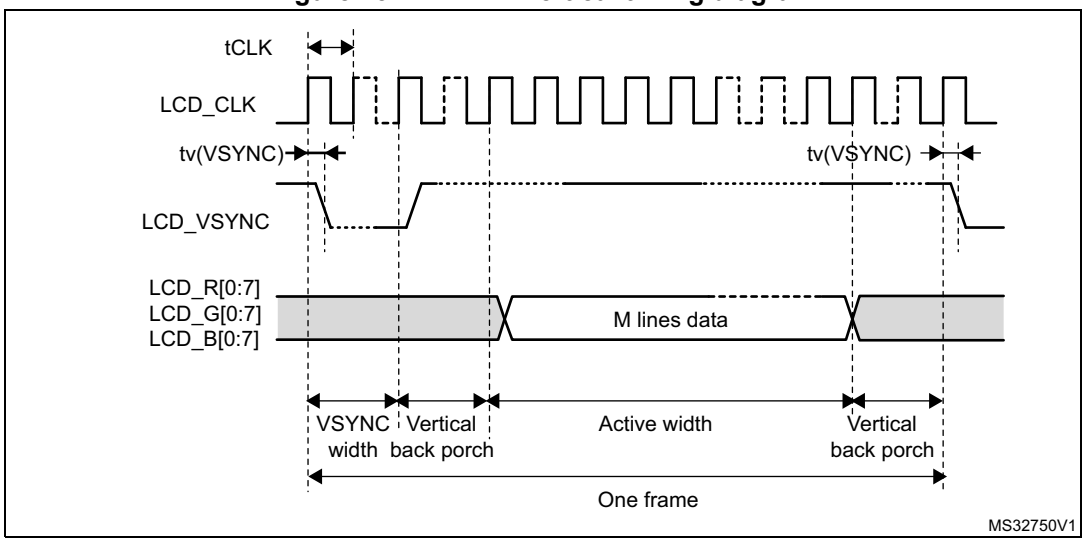


Figure 45. LCD-TFT vertical timing diagram



6.3.35 Timer characteristics

The parameters given in *Table 95* are guaranteed by design.

Refer to *Section 6.3.17: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 95. TIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{TIMxCLK}$	Timer kernel clock	0	209	MHz
f_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 16-bit counters	-	65536	$t_{TIMxCLK}$
	Maximum possible count with 32-bit counter (TIM2, TIM5)		65536 × 65536	

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.

Table 96. LPTIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	104.5	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	$f_{LPTIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

1. LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
2. Guaranteed by design.

6.3.36 Communications interfaces

I2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2C peripheral is properly configured and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 97. Minimum i2c_ker_ck frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON DNF=0	8	
			Analog filter OFF DNF=1	9	
		Fast-mode Plus	Analog filter ON DNF=0	19	
			Analog filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

$t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$

$R_{p(min)} = (V_{DD}-V_{OL(max)})/I_{OL(max)}$

Where R_p is the I2C lines pull-up. Refer to *Section 6.3.17: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 98* for the analog filter characteristics:

Table 98. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	40(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

The I2C pins can be set in FM+ mode in SYSCFG_PMCR register.

Unless otherwise specified, the parameters given in Table 55 are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*.

Table 99. I2C FM+ pin characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
F_{max}(1)	Maximum frequency	C = 50 pF 1.71 ≤ V_{DD} ≤ 3.6 V	-	1	MHz
T_f(2)	Output high to low level fall time		-	5	ns

1. The maximum frequency is defined with the following conditions:
   - (Tr + Tf) ≤ ⅔T
   - 45% < duty cycle < 55%.
2. The fall time is defined between 70% and 30% of the output waveform accordingl to I^2C specification NXP UM10204 rev- Oct 2012.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 100* for the SPI interface are derived from tests performed under the ambient temperature, f_{pclkx} frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5×V_{DD}
- I/O compensation cell enabled
- HSLV activated when V_{DD} ≤ 2.7 V

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 100. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI1	-	-	70	MHz
		Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V SPI1			80	
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI2, SPI3			80	
		Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V SPI2, SPI3			100	
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI4, SPI5, SPI6			66	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI1, SPI2, SPI3			100	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V SPI4, SPI5, SPI6			66	
		Slave mode transmitter/full duplex 2.7 V ≤ V_{DD} ≤ 3.6 V			38(2)	
		Slave mode transmitter/full duplex 1.71 V ≤ V_{DD} ≤ 3.6 V			35(2)	
$t_{su(NSS)}$	NSS setup time	Slave mode	2	-	-	ns
$t_{h(NSS)}$	NSS hold time		1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{pclk} - 1	T_{pclk}	T_{pclk} + 1	

Table 100. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	11	16	
$t_{dis(SO)}$	Data output disable time	Slave mode	3	5	7.5	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	13	
		Slave mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	11	14	
$t_{v(MO)}$		Master mode	-	1.5	2.5	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V ≤ V_{DD} ≤ 3.6 V	8	-	-	
$t_{h(MO)}$		Master mode	1	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.

Figure 46. SPI timing diagram - slave mode and CPHA = 0

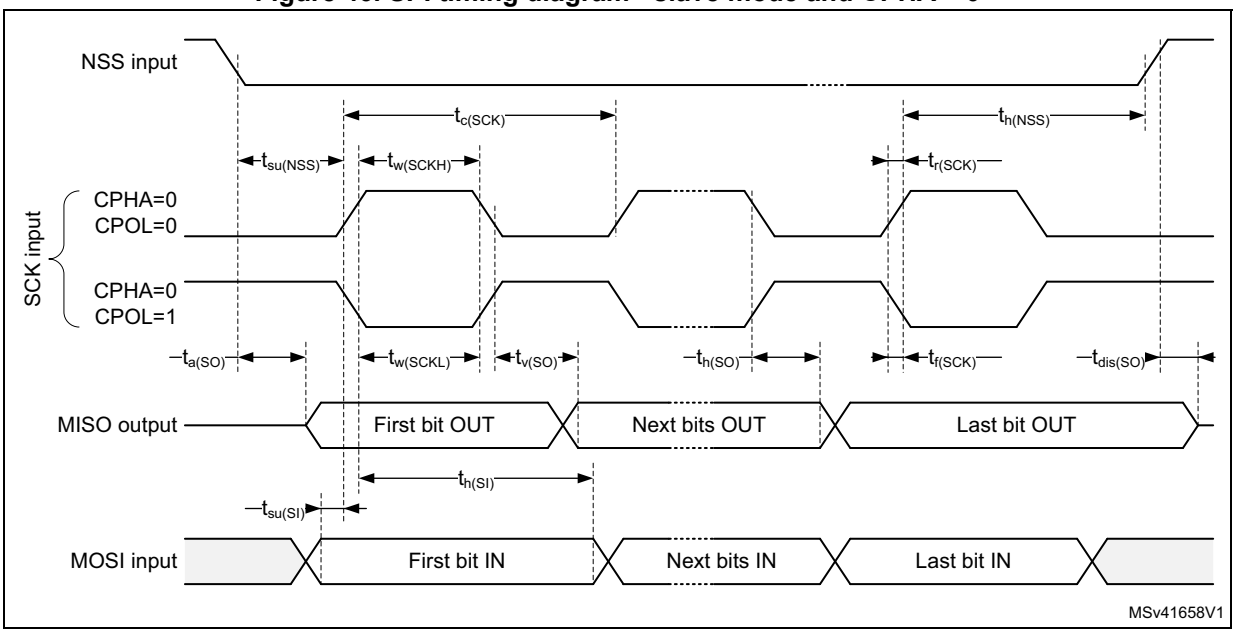
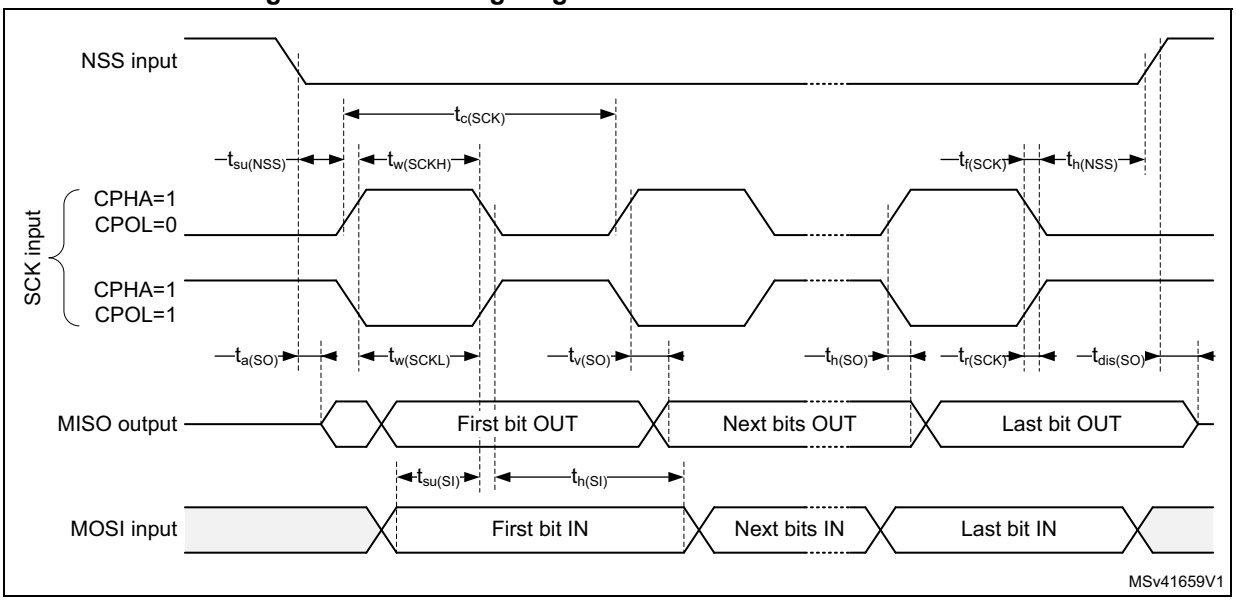
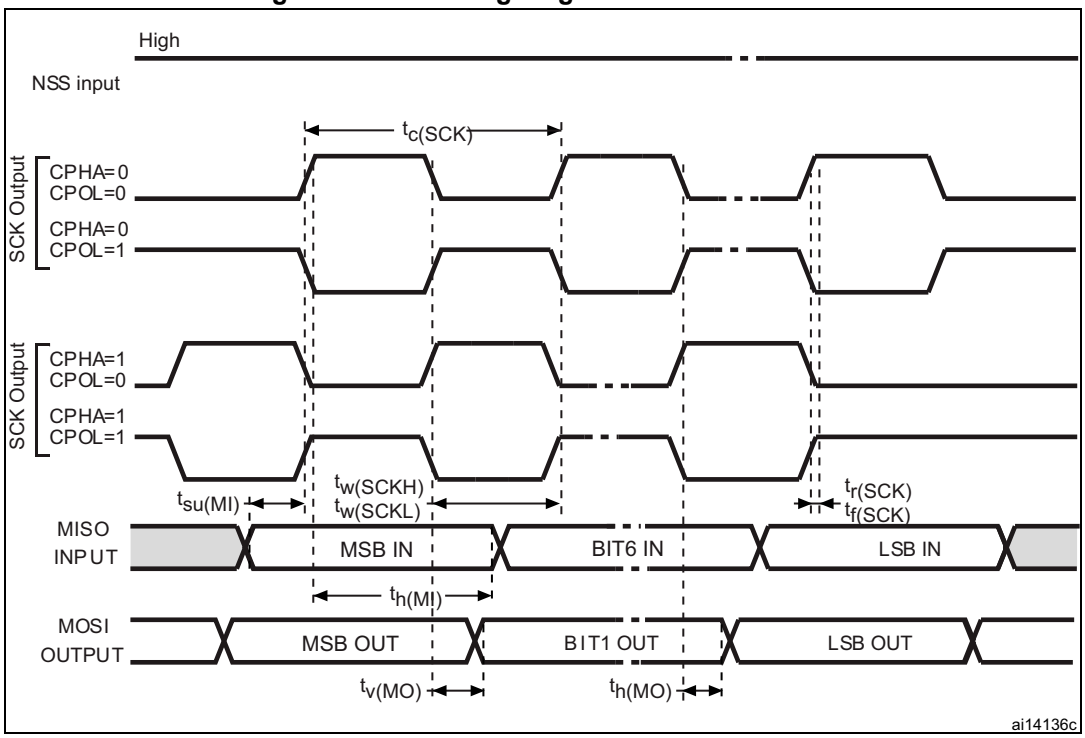


Figure 47. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at 0.5×V_{DD} and with external C_L = 30 pF.

Figure 48. SPI timing diagram - master mode(1)



1. Measurement points are done at 0.5×V_{DD} and with external C_L = 30 pF.

I2S interface characteristics

Unless otherwise specified, the parameters given in *Table 101* for the I2S interface are derived from tests performed under the ambient temperature, f_{pclkx} frequency and V_{DD}

supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled

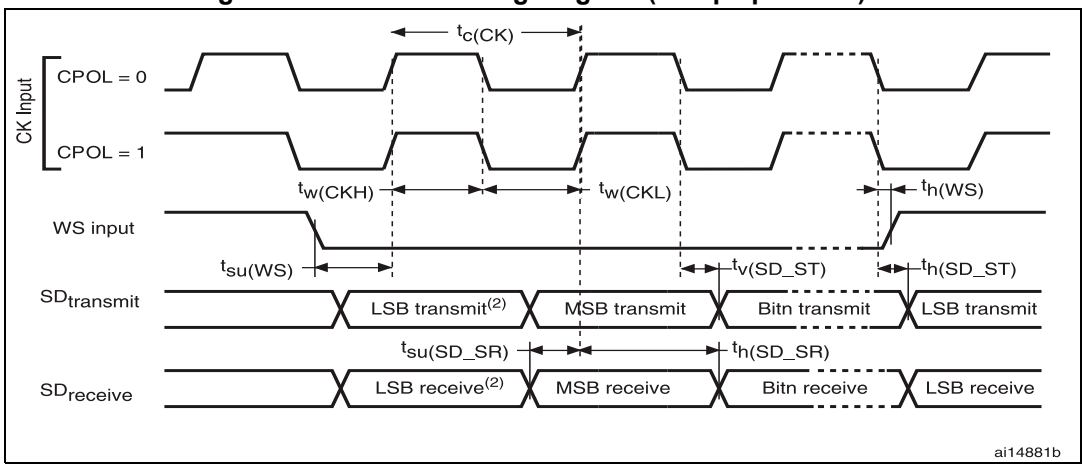
Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 101. I2S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	256×8K	256×Fs	MHz
f_{CK}	I2S clock frequency	Master data	-	64×Fs	MHz
		Slave data	-	64×Fs	
$t_{v(WS)}$	WS valid time	Master mode	-	6.5	ns
$t_{h(WS)}$	WS hold time	Master mode	0.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2	-	
$t_{su(SD\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	2	-	
$t_{h(SD\_SR)}$		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	1	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8.5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

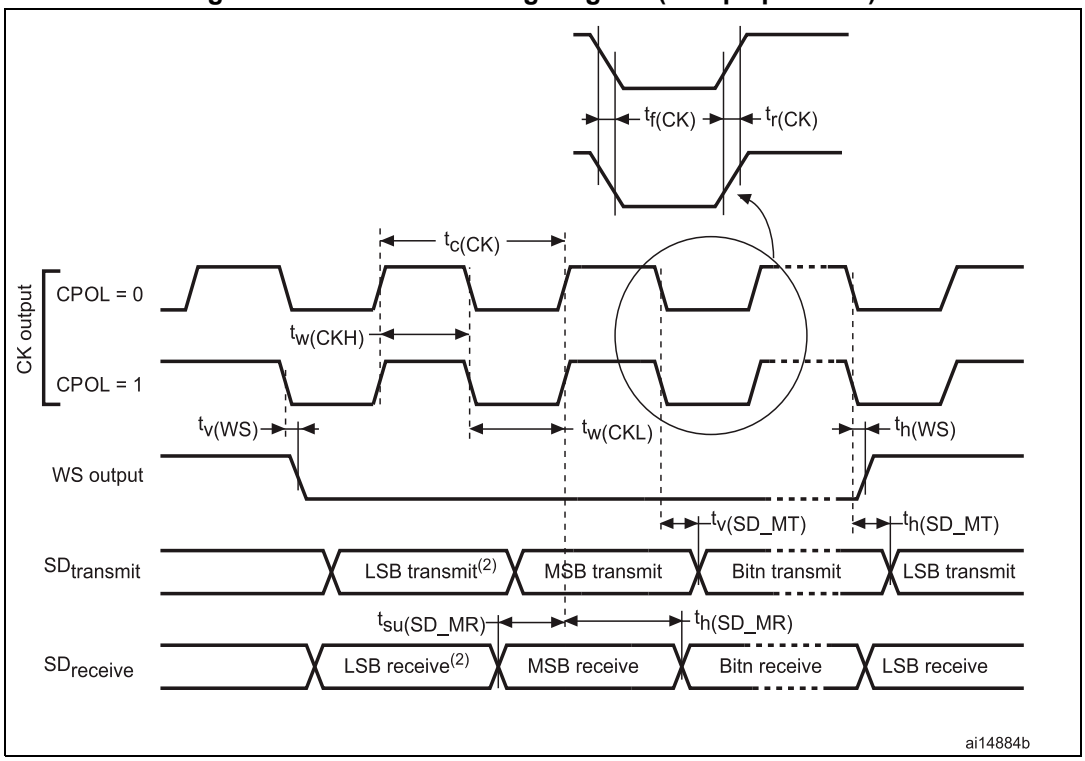
1. Guaranteed by characterization results.

Figure 49. I2S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I2S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 102* for SAI are derived from tests performed under the ambient temperature, F_{pclk2} frequency and V_{DD} supply voltage

conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are performed at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 102. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	-	50	MHz
F_{CK}	SAI bit clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V	-	27	
		Master receiver 1.71 V ≤ V_{DD} ≤ 3.6 V	-	27	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V	-	31	
		Slave receiver 1.71 ≤ V_{DD} ≤ 3.6 V	-	50	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	18	
$t_{su(FS)}$	FS setup time	Slave mode	7	-	
$t_{h(FS)}$	FS hold time	Master mode	2	-	
		Slave mode	2.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	3	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	0.5	-	

Table 102. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	16	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8.5	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	18	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	7	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 51. SAI master timing waveforms

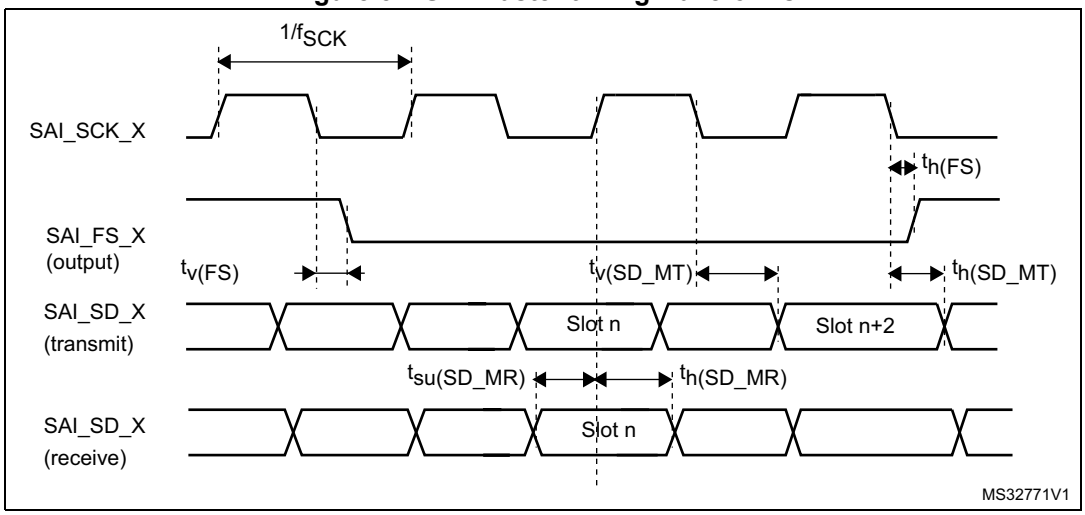
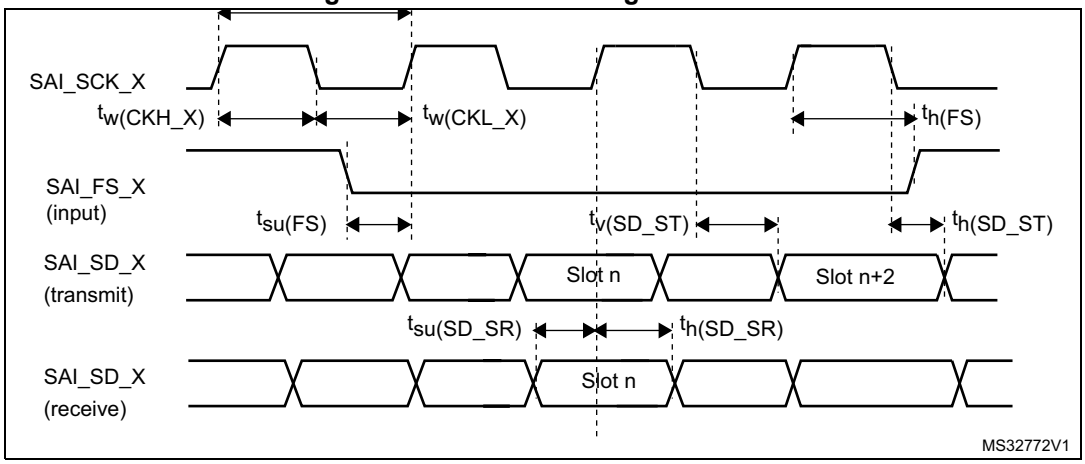


Figure 52. SAI slave timing waveforms



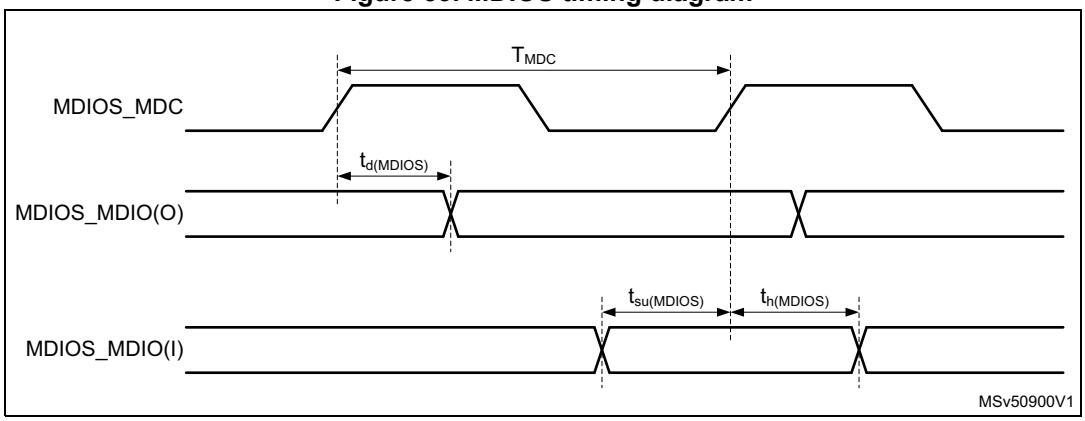
MDIOS characteristics

Table 103. MDIOS timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
F_{MDC}	Management data clock	-	-	30	MHz
$t_{d(MDIOS)}$	Management data input/output **output valid time**	6.5	8	19	ns
$t_{su(MDIOS)}$	Management data input/output **setup time**	1	-	-	
$t_{h(MDIOS)}$	Management data input/output **hold time**	0.5	-	-	

The MDIOS controller is mapped on APB1 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{pclk1} \geq 1.5 * F_{MDC}$.

Figure 53. MDIOS timing diagram



SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 104* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, F_{hclk6} frequency and V_{DD} supply voltage conditions summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- HSLV activated when $V_{DD} \leq 2.7$ V
- Delay block disabled

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 104. Dynamic characteristics: SD / MMC / *e*•MMC characteristics, V_{DD} = 2.7 V to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	130	MHz
-	SDIO_CK/f_{pclk2} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS/SDR(3)/DDR(3) mode						
t_{ISU}	Input setup time HS	-	1.5	-	-	ns
t_{IH}	Input hold time HS		1.5	-	-	
t_{IDW}(4)	Input valid window (variable window)		2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS/SDR(3)/DDR(3) mode						
t_{OV}	Output valid time HS	-	-	5	6.5	ns
t_{OH}	Output hold time HS		2.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	1.5	-	-	ns
t_{IHD}	Input hold time SD		1.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	1.5	ns
t_{OHD}	Output hold default time SD		0	-	-	

1. Guaranteed by characterization results.
2. Above 100 MHz, C_L = 20 pF.
3. For SD 1.8 V support, an external voltage converter is required.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 105. Dynamic characteristics: SD / MMC / *e*•MMC characteristics V_{DD} = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	105	MHz
-	SDIO_CK/f_{pclk2} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in *e*•MMC mode						
t_{ISU}	Input setup time HS	-	1.5	-	-	ns
t_{IH}	Input hold time HS		2.5	-	-	
t_{IDW}(3)	Input valid window (variable window)		3	-	-	
CMD, D outputs (referenced to CK) in *e*•MMC mode						

Table 105. Dynamic characteristics: SD / MMC / *e*•MMC characteristics V_{DD} = 1.71 V to 1.9 V(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{OV}	Output valid time HS	-	-	5	6	ns
t_{OH}	Output hold time HS		4	-	-	

1. Guaranteed by characterization results.
2. C_L = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 54. SDIO high-speed mode

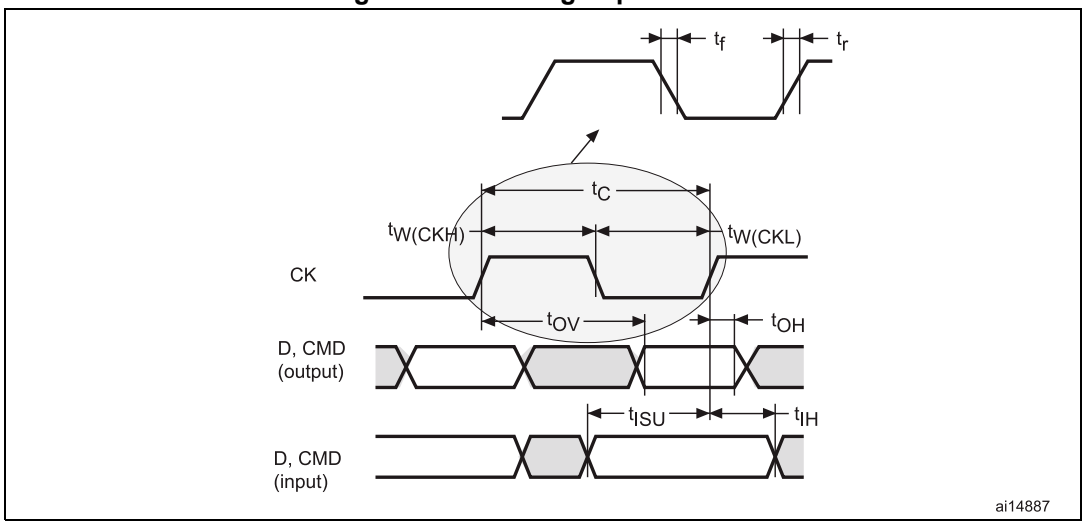


Figure 55. SD default mode

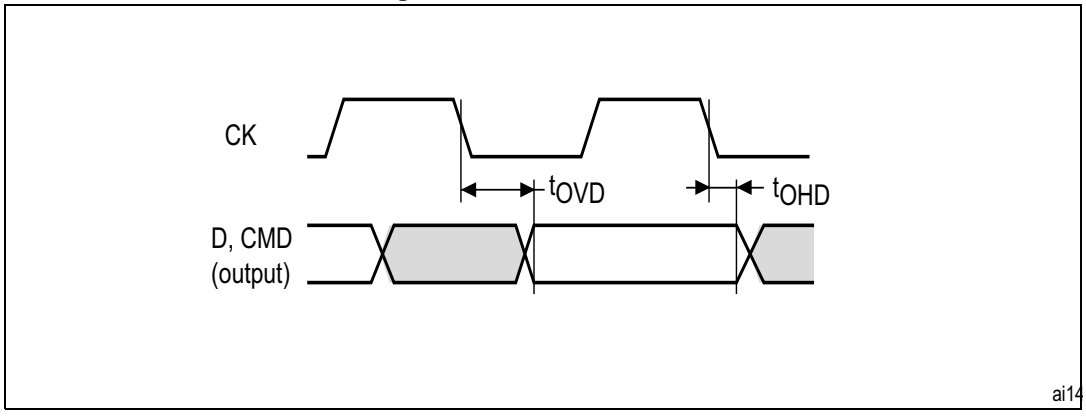
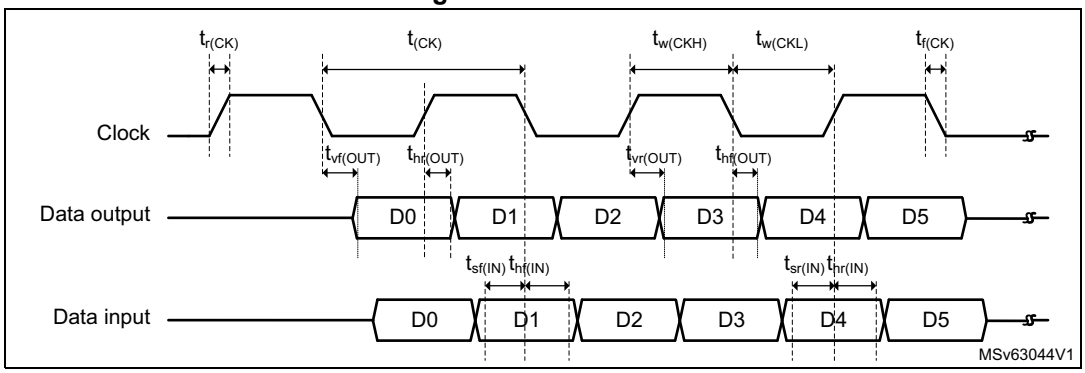


Figure 56. DDR mode



FDCAN (controller area network) interface

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

USB OTG_FS characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 106. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance(2)	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

Ethernet (ETH) characteristics

Unless otherwise specified, the parameters given in *Table 107*, *Table 108*, *Table 109*, *Table 110* and *Table 111* for MDIO/SMA, RMII, GMII, RGMII and MII are derived from tests performed under the ambient temperature, F_{axiss_ck} frequency summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$.

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 107 gives the list of Ethernet MAC timings for the MDIO/SMA and *Figure 57* shows the corresponding timing diagram.

Table 107. Dynamics characteristics: Ethernet MAC timings for MDIO/SMA(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	399	400	401	ns
$T_{d(MDIO)}$	Write data valid time	0.5	1	3	
$t_{su(MDIO)}$	Read data setup time	13.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

Figure 57. Ethernet MDIO/SMA timing diagram

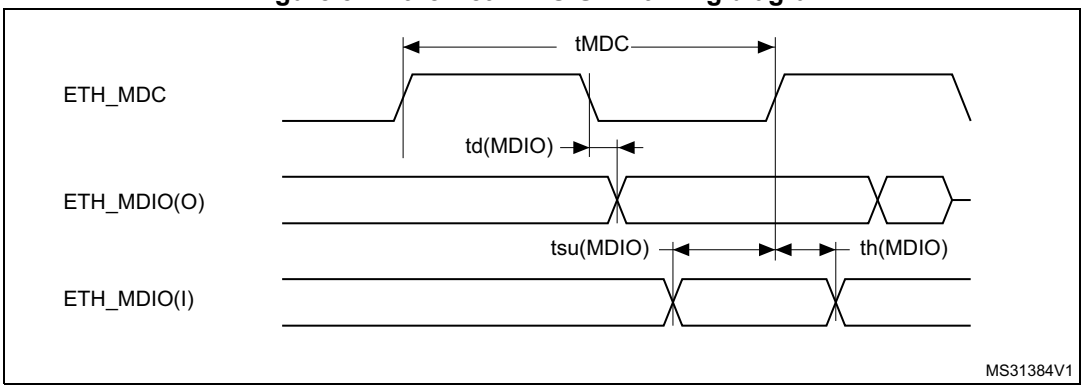


Table 108 gives the list of Ethernet MAC timings for the RMII and *Figure 58* shows the corresponding timing diagram.

Table 108. Dynamics characteristics: Ethernet MAC timings for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(CRS)}$	Carrier sense setup time	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	5.5	6.5	9.5	
$t_{d(TXD)}$	Transmit data valid delay time	6	6.5	10	

1. Guaranteed by characterization results.

Figure 58. Ethernet RMII timing diagram

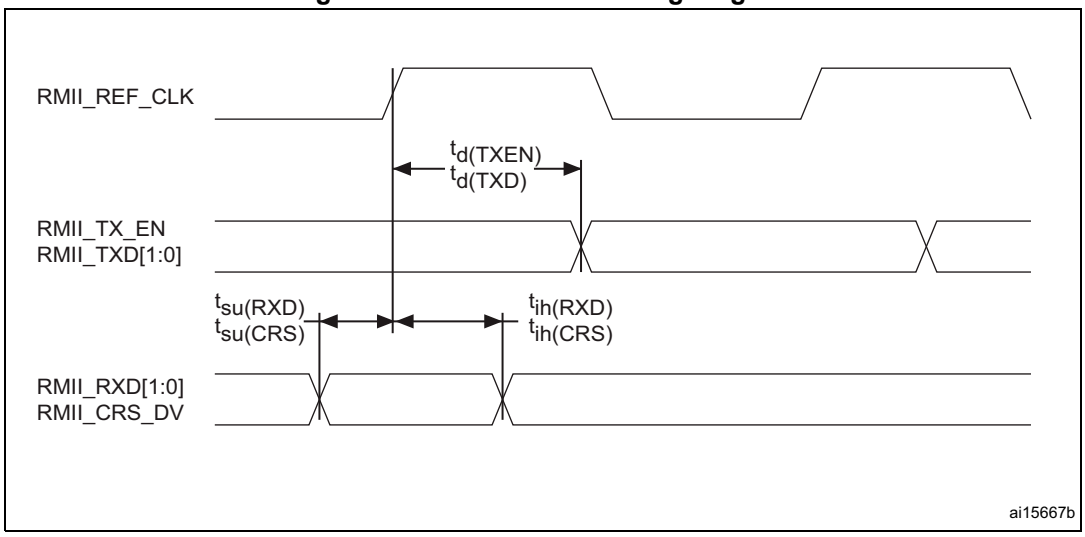


Table 109 gives the list of Ethernet MAC timings for MII and *Figure 59* shows the corresponding timing diagram.

Table 109. Dynamics characteristics: Ethernet MAC timings for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	
$t_{su(DV)}$	Data valid setup time	1	-	-	
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	
$t_{su(ER)}$	Error setup time	1	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	6	7.5	10.5	
$t_{d(TXD)}$	Transmit data valid delay time	7	8	11	

1. Guaranteed by characterization results.

Figure 59. Ethernet MII timing diagram

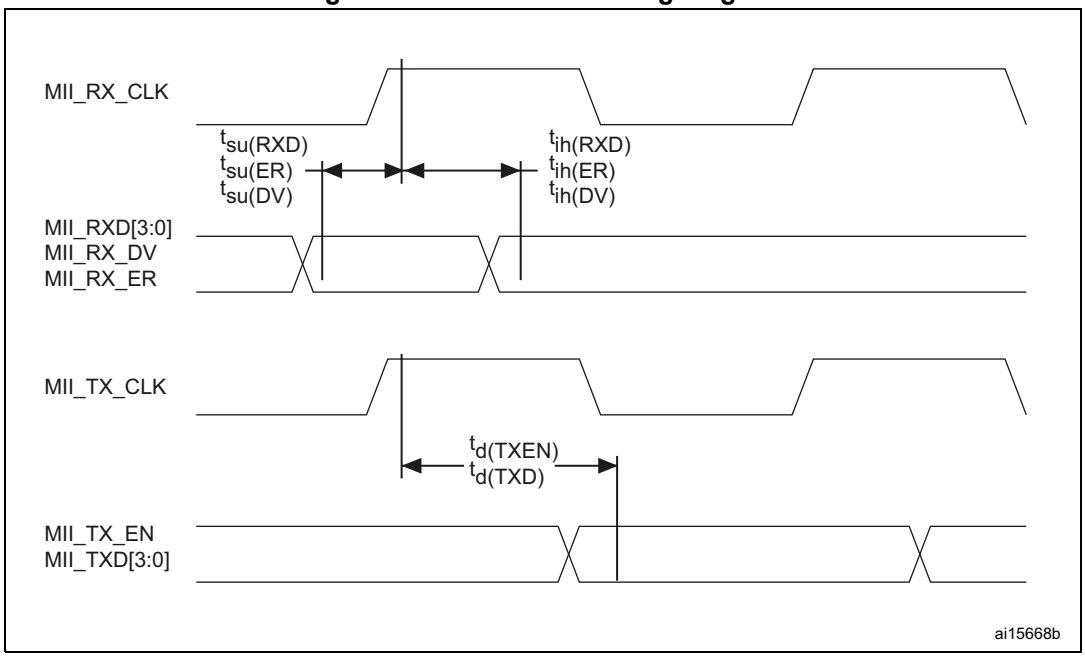


Table 110. Dynamics characteristics: Ethernet MAC signals for GMII (1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	0.5	-	-	
$t_{su(DV)}$	Data valid setup time	1	-	-	
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	
$t_{su(ER)}$	Error setup time	1	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	1	1.5	2	
$t_{d(TXD)}$	Transmit data valid delay time	1	2	3	

1. Guaranteed by characterization results.

Figure 60. Ethernet GMII timing diagram

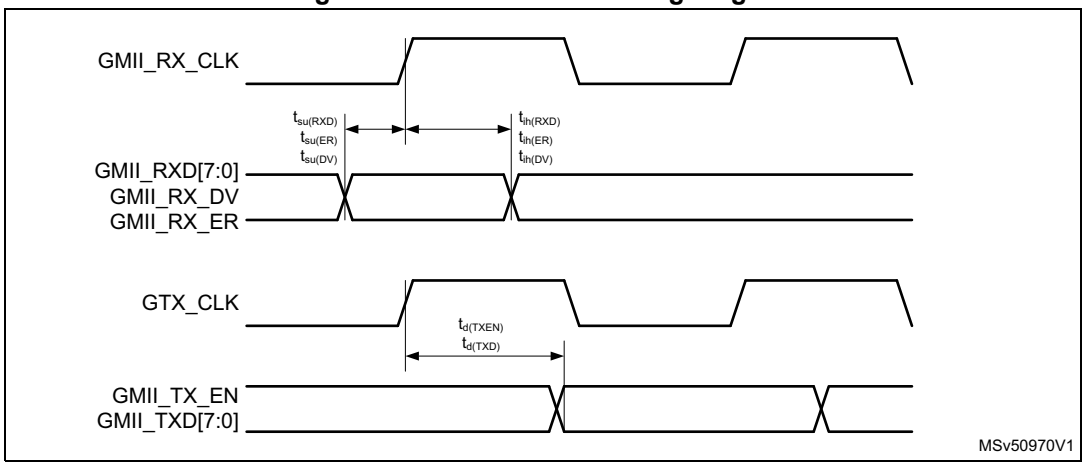
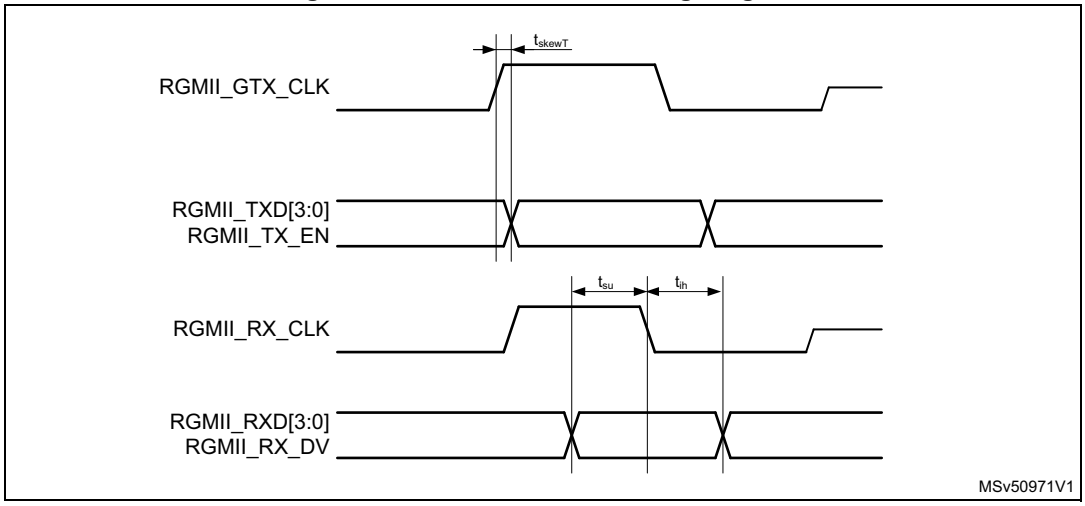


Table 111. Dynamics characteristics: Ethernet MAC signals for RGMII (1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1.12(2)	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	0.83(2)	-	-	
$t_{su(DV)}$	Data valid setup time	1.12(2)	-	-	
$t_{ih(DV)}$	Data valid hold time	0.83(2)	-	-	
$T_{skewT(TXEN)}$	Transmit enable valid delay time	-0.25	0.25	0.5	
$T_{skewT(TXD)}$	Transmit data valid delay time	-0.25	2	0.5	

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 61. Ethernet RGMII timing diagram



6.3.37 USART interface characteristics

Unless otherwise specified, the parameters given in *Table 112* for USART are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 112*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 112. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode USART2,3,6	-	-	12.5	MHz
		Master mode USART1			16.5	
		Slave mode	-	-	27	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}+2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	ns
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	Master mode	$1/f_{CK}/2$ - 1	1/fck/2	$1/f_{CK}/2$ + 1	ns
$t_{su(RX)}$	Data input setup time	Master mode	t_{ker}+3	-	-	ns
		Slave mode	2	-	-	
$t_{hRX)}$	Data input hold time	Master mode	1	-	-	ns
		Slave mode	1	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode	-	10	18	ns
		Master mode	-	0.5	1	
th(TX)	Data output hold time	Slave mode	8	-	-	ns
		Master mode	0	-	-	

1. 1.Guaranteed by characterization results.

6.3.38 USB High-Speed PHY characteristics

Table 113. USB High-Speed PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA1V1\_REG(PHY)}$	High-Speed TX(2)	One USB port	-	1.4	-	mA
		Two USB ports	-	2.4	-	
	High-Speed RX(3) / Idle	One USB port	-	5.4	-	
		Two USB ports	-	10.4	-	
	Ful-Speed and Low-Speed mode (Suspend, TX or RX)		-	0	-	

Table 113. USB High-Speed PHY characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA1V8\_REG(PHY)}$	High-Speed TX(2)	One USB port	-	25.5	-	mA
		Two USB ports	-	50.5	-	
	High-Speed RX(3) / Idle	One USB port	-	2.5	-	
		Two USB ports	-	5.5	-	
	Ful-Speed and Low-Speed mode (Suspend, TX or RX)		-	0	-	
$I_{DDA3V3\_USBHS(PHY)}$	High-Speed TX(2)	One USB port	-	5	-	mA
		Two USB ports	-	7	-	
	High-Speed RX(3) / Idle	One USB port	-	6	-	
		Two USB ports	-	10	-	
	Full-Speed Suspend (host mode)	One USB port	-	0	-	
		Two USB ports	-	0	-	
	Full-Speed Suspend (peripheral mode)	One USB port	-	0.2	-	
		Two USB ports	-	0.4	-	
	Full-Speed TX(2)	One USB port	-	6.5	-	
		Two USB ports	-	10.5	-	
	Full-Speed RX(3)	One USB port	-	6.5	-	
		Two USB ports	-	11.5	-	
	Low-Speed TX(2)	One USB port	-	7	-	
		Two USB ports	-	11.5	-	
	Low-Speed RX(3)	One USB port	-	4.3	-	
		Two USB ports	-	6.1	-	

1. Guaranteed by design unless otherwise specified.
2. USB link 100% of the time in transmission
3. USB link 100% of the time in reception

6.3.39 DSI PHY characteristics

Table 114. DSI PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA1V2\_DSI\_PHY(PHY)}$	Power down	-	-	185	-	µA
	High-Speed TX	2 lanes in High-Speed mode	-	17.35	-	mA
	LPDT transmit	All data lanes in LPDT mode	-	3.35	-	
	LPDT receive	All data lanes in LPDT mode	-	0.8	-	

Table 114. DSI PHY characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA1V8\_DSI(PHY)}$	Power down	-	-	1	-	µA
	High-Speed TX	2 lanes in High-Speed mode	-	400	-	
	LPDT transmit	All data lanes in LPDT mode	-	1	-	
	LPDT receive	All data lanes in LPDT mode	-	1	-	

1. Guaranteed by design unless otherwise specified.

6.3.40 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 115* and *Table 116* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 13: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 115. Dynamics characteristics: JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	35	MHz
$1/t_{c(TCK)}$		1.71 V < V_{DD}< 3.6 V	-	-	27	
$ti_{su(TMS)}$	TMS input setup time	-	2.5	-	-	
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	2	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	2.7 V <V_{DD}< 3.6 V	-	8	14	
		1.71 V <V_{DD}< 3.6 V	-	8	18	
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

Table 116. Dynamics characteristics: SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.71 V < V_{DD}< 3.6 V	-	-	55	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	2.7 V <V_{DD}< 3.6 V	-	8.5	14	
		1.71 V <V_{DD}< 3.6 V	-	8.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

Figure 62. JTAG timing diagram

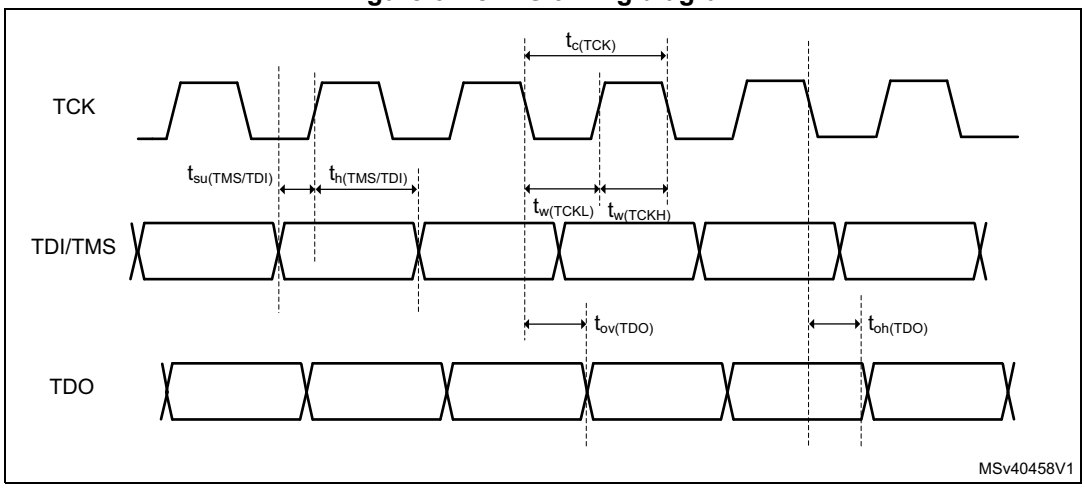
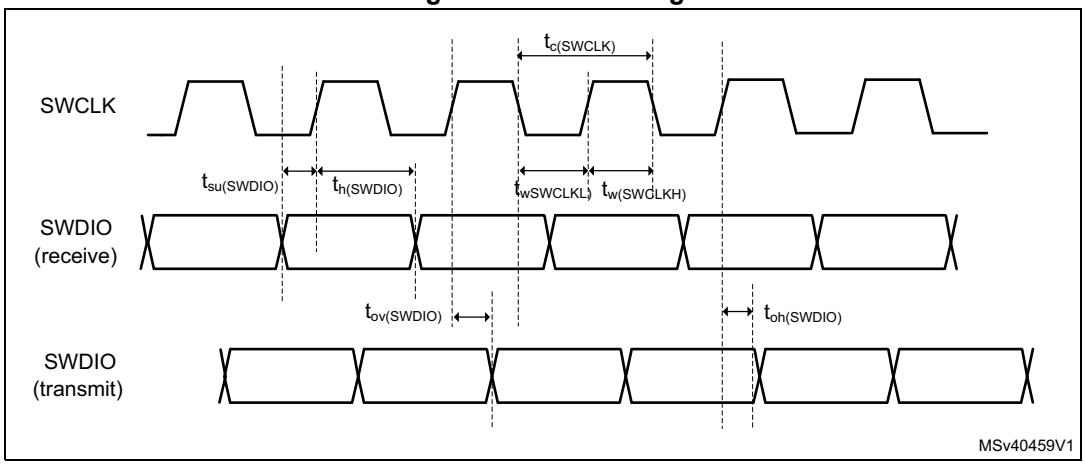


Figure 63. SWD timing

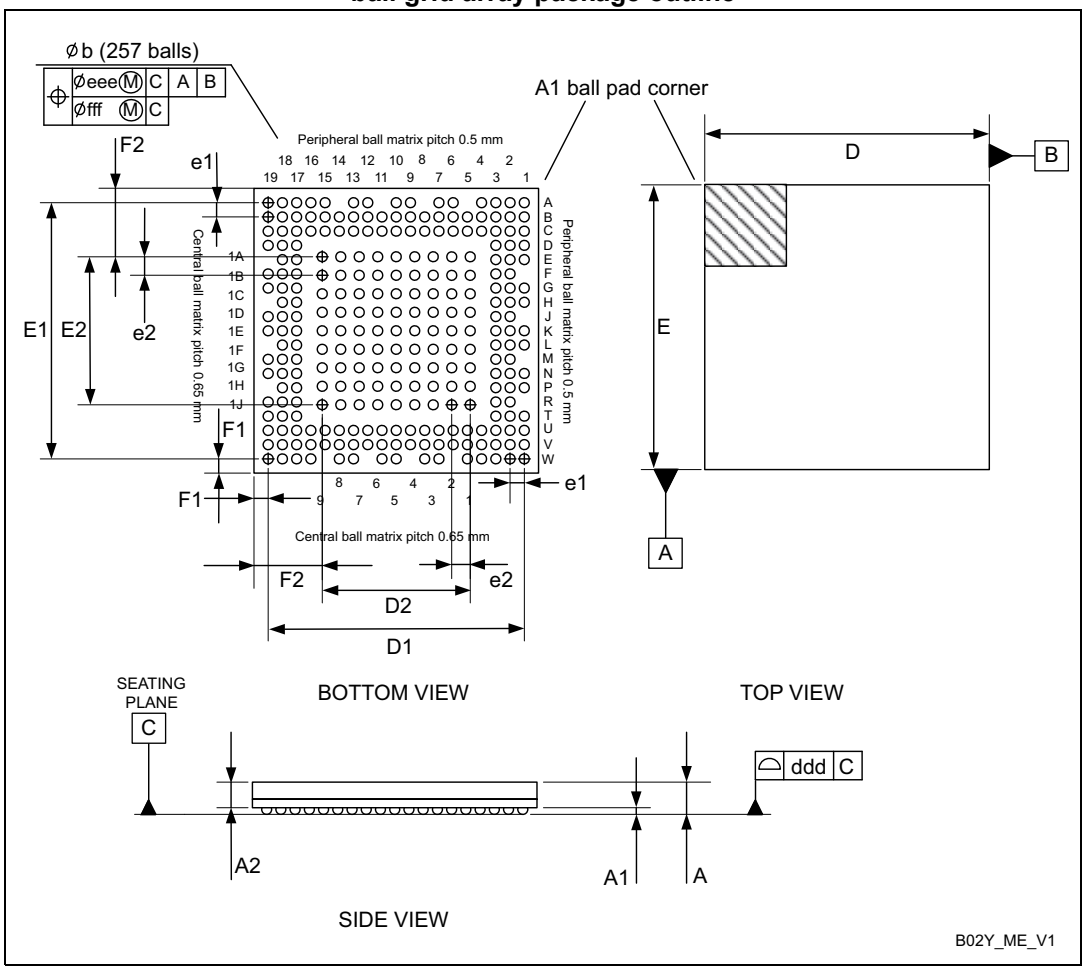


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 TFBGA 257 package information

Figure 64. TFBGA - 257 balls, 10x10 mm, 0.5/0.65 mm pitch, low profile fine pitch ball grid array package outline



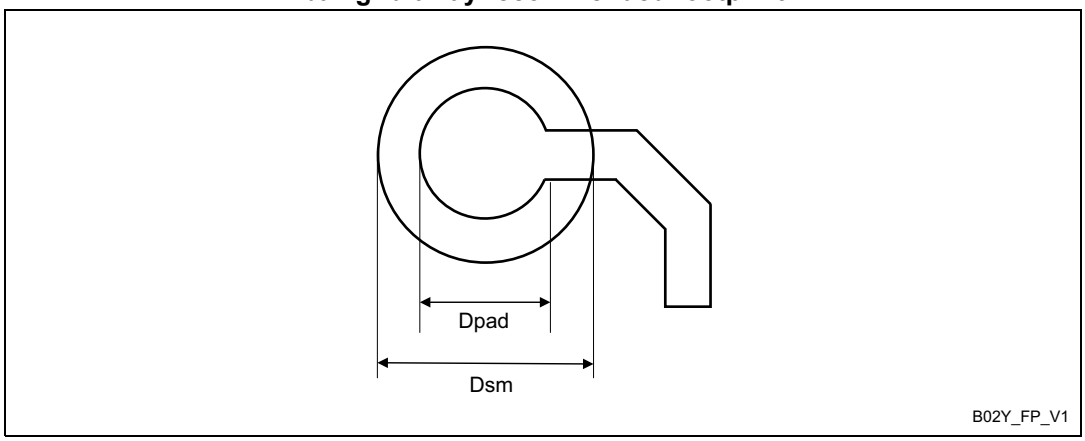
1. Drawing is not to scale.

Table 117. TFBGA - 257 balls, 10x10 mm, 0.5/0.65 mm pitch, low profile fine pitch ball grid array mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1[2]	0.150	-	-	0.0059	-	-
A2	-	0.810	-	-	0.0319	-
b[3]	0.300	0.350	0.400	0.0118	0.0138	0.0157
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.000	-	-	0.3543	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.000	-	-	0.3543	-
D2	-	5.200	-	-	0.2047	-
E2	-	5.200	-	-	0.2047	-
e1	-	0.500	-	-	0.0197	-
e2	-	0.650	-	-	0.0256	-
F1	-	0.500	-	-	0.0197	-
F2	-	2.400	-	-	0.0945	-
ddd	-	-	0.100	-	-	0.0039
eee[4]	-	-	0.150	-	-	0.0059
fff[5]	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
3. Initial ball equal 0.300 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

Figure 65. TFBGA - 257 balls, 10x10 mm, 0.5/0.65 mm pitch, low profile fine pitch ball grid array recommended footprint



1. Dimensions are expressed in millimeters.

Table 118. TFBGA - 257 balls, recommended PCB design rules (0.5/0.65 mm pitch, BGA)

Dimension	Recommended values
Pitch	0.5/0.65 mm
Dpad	0.350 mm
Dsm	0.480 mm typ.
Stencil opening	0.350 mm
Stencil thickness	0.125 mm to 0.100 mm

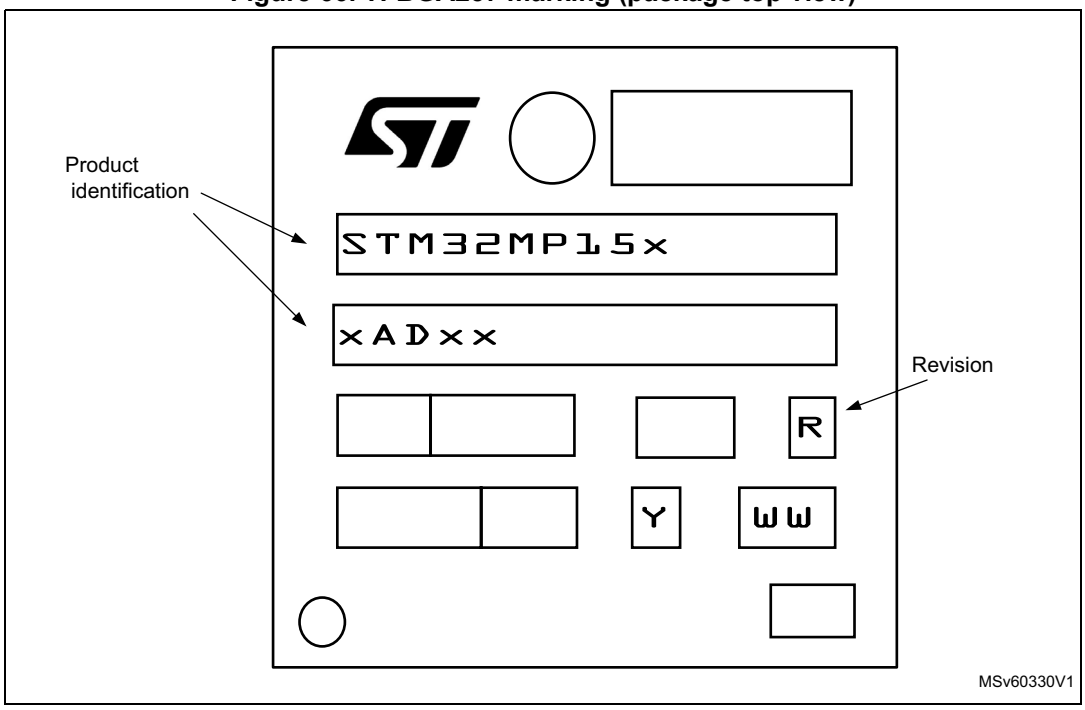
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

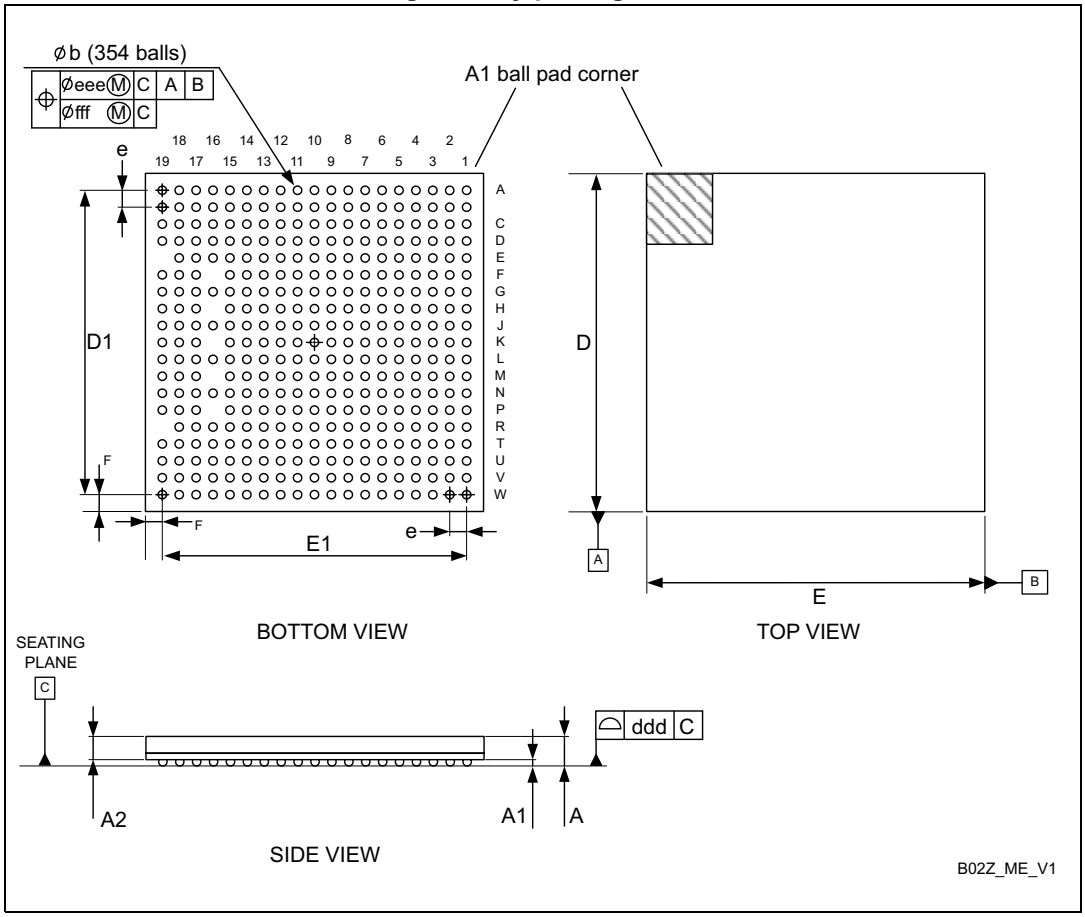
Figure 66. TFBGA257 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 LFBGA354 package information

Figure 67. LFBGA - 354balls, 16x16 mm, 0.8 mm pitch, low profile fine pitch ball grid array package outline



1. Drawing is not to scale.
2. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Table 119. LFBGA - 354balls, 16x16 mm, 0.8 mm pitch, low profile fine pitch ball grid array mechanical data

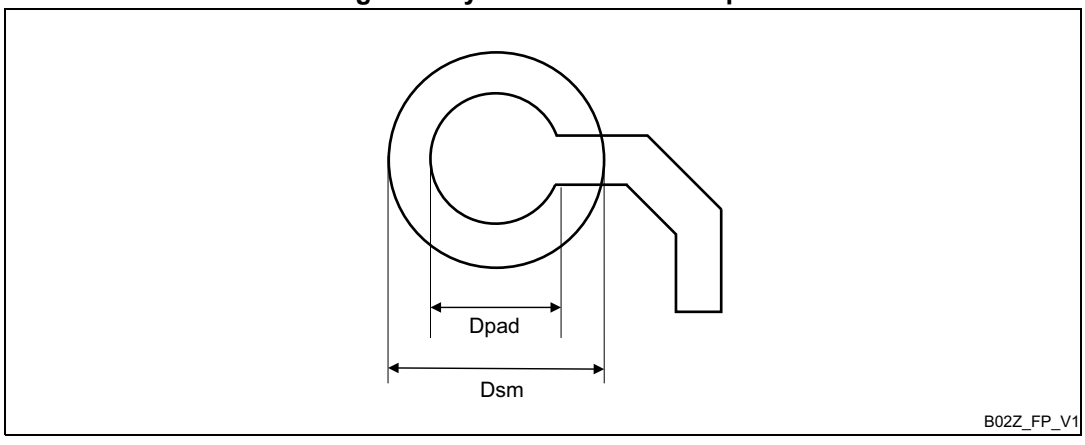
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.290	-	-	0.0508
A1[3]	0.250	-	-	0.0098	-	-
A2	-	0.900	-	-	0.0354	-
b[4]	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	15.850	16.000	16.150	0.6240	0.6299	0.6358
D1	-	14.400	-	-	0.5669	-

Table 119. LFBGA - 354balls, 16x16 mm, 0.8 mm pitch, low profile fine pitch ball grid array mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	15.850	16.000	16.150	0.6240	0.6299	0.6358
E1	-	14.400	-	-	0.5669	-
e	-	0.800	-	-	0.0315	-
F	-	0.800	-	-	0.0315	-
ddd	-	-	0.100	-	-	0.0039
eee[5]	-	-	0.150	-	-	0.0059
fff[6]	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. LFBGA stands for Low profile Fine pitch Ball Grid Array package.
   Low profile: 1.20mm < A ≤ 1.70mm / Fine pitch: e < 1.00mm pitch. The total profile height (Dim A) is measured from the seating plane to the top of the component The maximum total package height is calculated by the RSS method (Root Sum Square).
   A Max = A1 Typ + A2 Typ + A4 Typ + $\sqrt{(A1^2 + A2^2 + A4^2}$ tolerance values).
3. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
4. Initial ball equal 0.400 mm.
5. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

Figure 68. LFBGA - 354balls, 16x16 mm, 0.8 mm pitch, low profile fine pitch ball grid array recommended footprint



1. Dimensions are expressed in millimeters.

Table 120. LFBGA - 354 balls, recommended PCB design rules (0.8 mm pitch, BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	0.125 mm to 0.100 mm

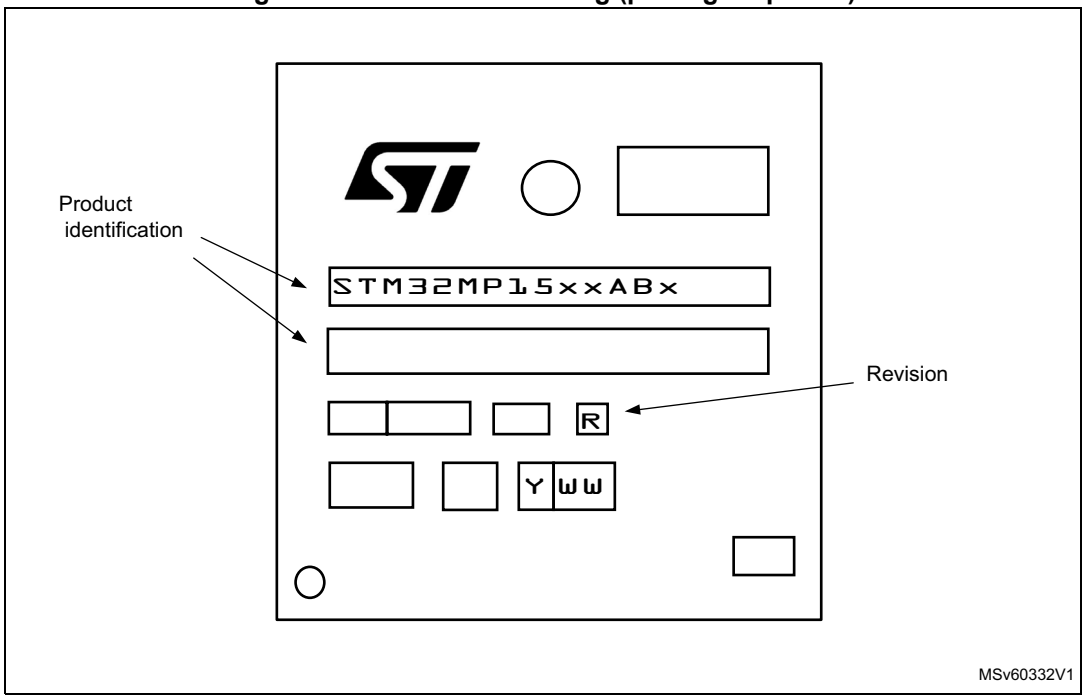
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

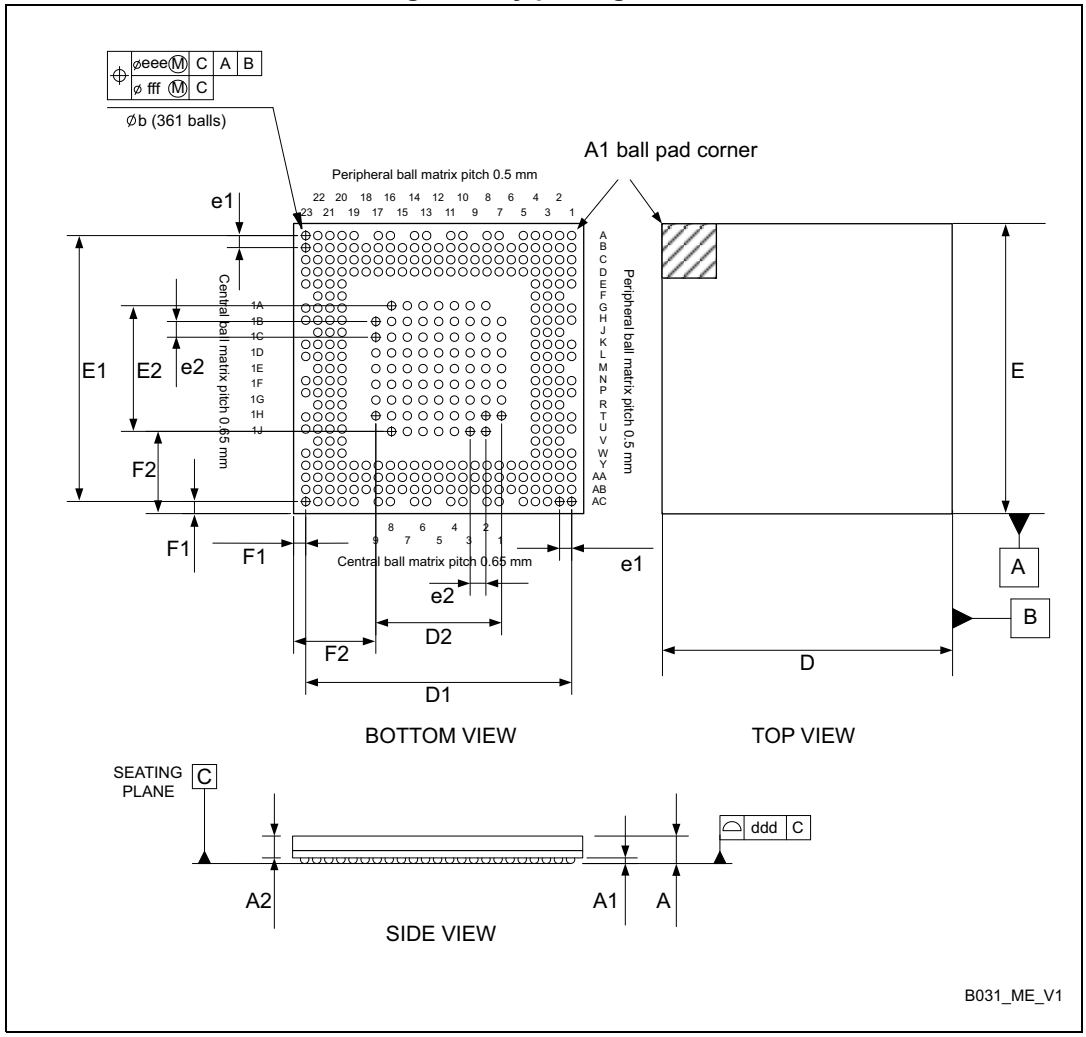
Figure 69. LFBGA354 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 TFBA361 package information

Figure 70. TFBGA - 361 ball, 12x12 mm, 0.5/0.65 mm pitch, thin profile fine pitch ball grid array package outline



1. Drawing is not to scale.
2. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 121. TFBGA - 361 ball, 12x12 mm, 0.5/0.65 mm pitch, thin profile fine pitch ball grid array mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.810	-	-	0.0319	-
b[3]	0.300	0.350	0.400	0.0118	0.0138	0.0157
D	11.850	12.000	12.150	0.4665	0.4724	0.4783
D1	-	11.000	-	-	0.4331	-
E	11.850	12.000	12.150	0.4665	0.4724	0.4783
E1	-	11.000	-	-	0.4331	-
D2	-	5.200	-	-	0.2047	-
E2	-	5.200	-	-	0.2047	-
e1	-	0.500	-	-	0.0197	-
e2	-	0.650	-	-	0.0256	-
F1	-	0.500	-	-	0.0197	-
F2	-	3.400	-	-	0.1339	-
ddd	-	-	0.080	-	-	0.0031
eee[4]	-	-	0.150	-	-	0.0059
fff[5]	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. TFBGA stands for Thin Profile Fine Pitch Ball Grid Array. The total profile height (dim A) is measured from the seating plane to the top of the component.
3. Initial ball equal to 0.300 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

Figure 71. TFBGA - 361 ball, 12x12 mm, 0.5/0.65 mm pitch, thin profile fine pitch ball grid array recommended footprint

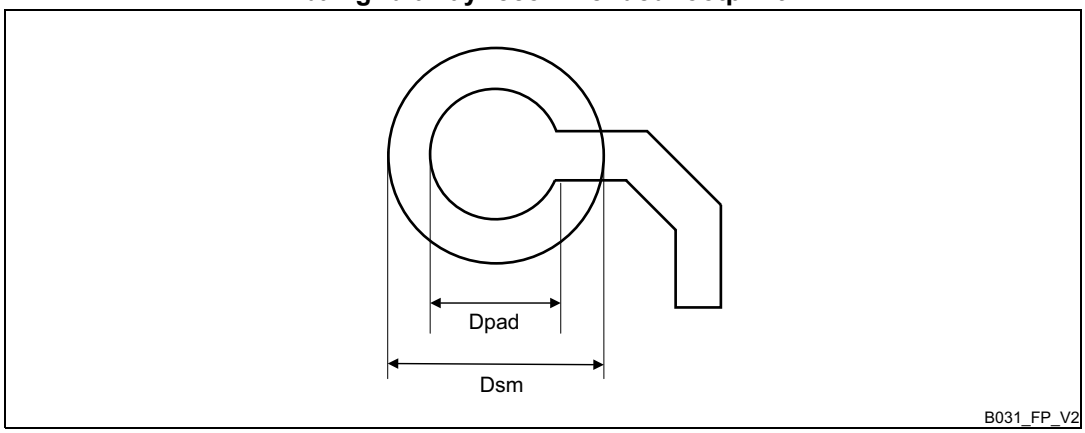


Table 122. TFBGA - 361 ball, recommended PCB design rules (0.5/0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5/0.65 mm
Dpad	0.350 mm
Dsm	0.480 mm typ.
Stencil opening	0.350 mm
Stencil thickness	0.125 mm to 0.100 mm

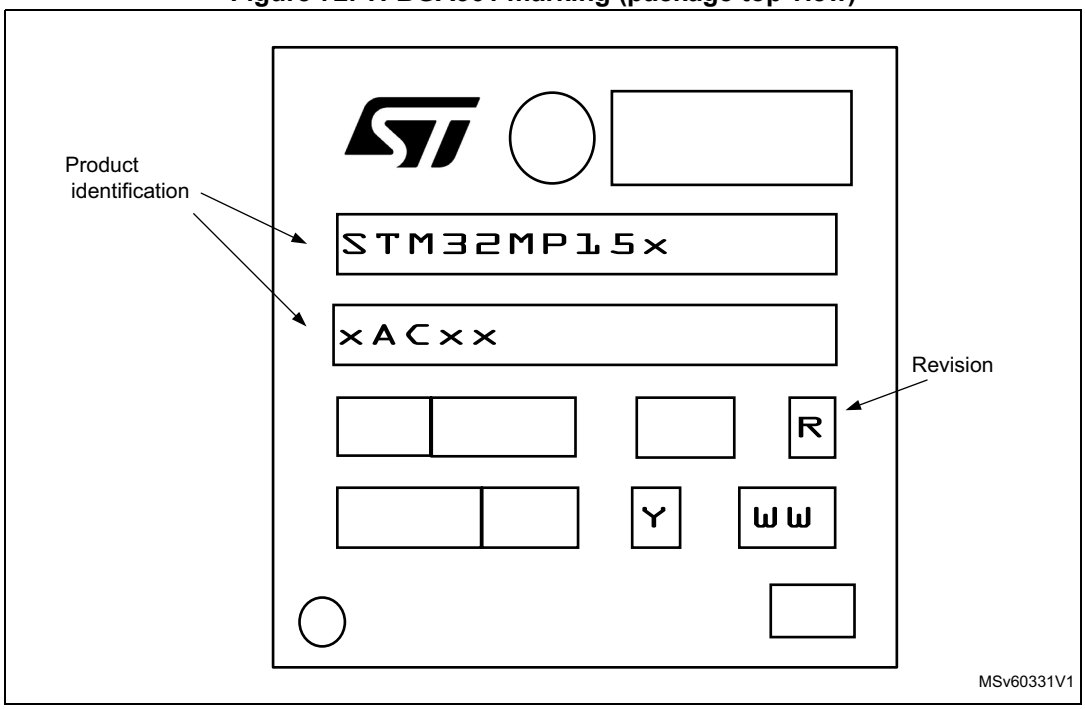
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

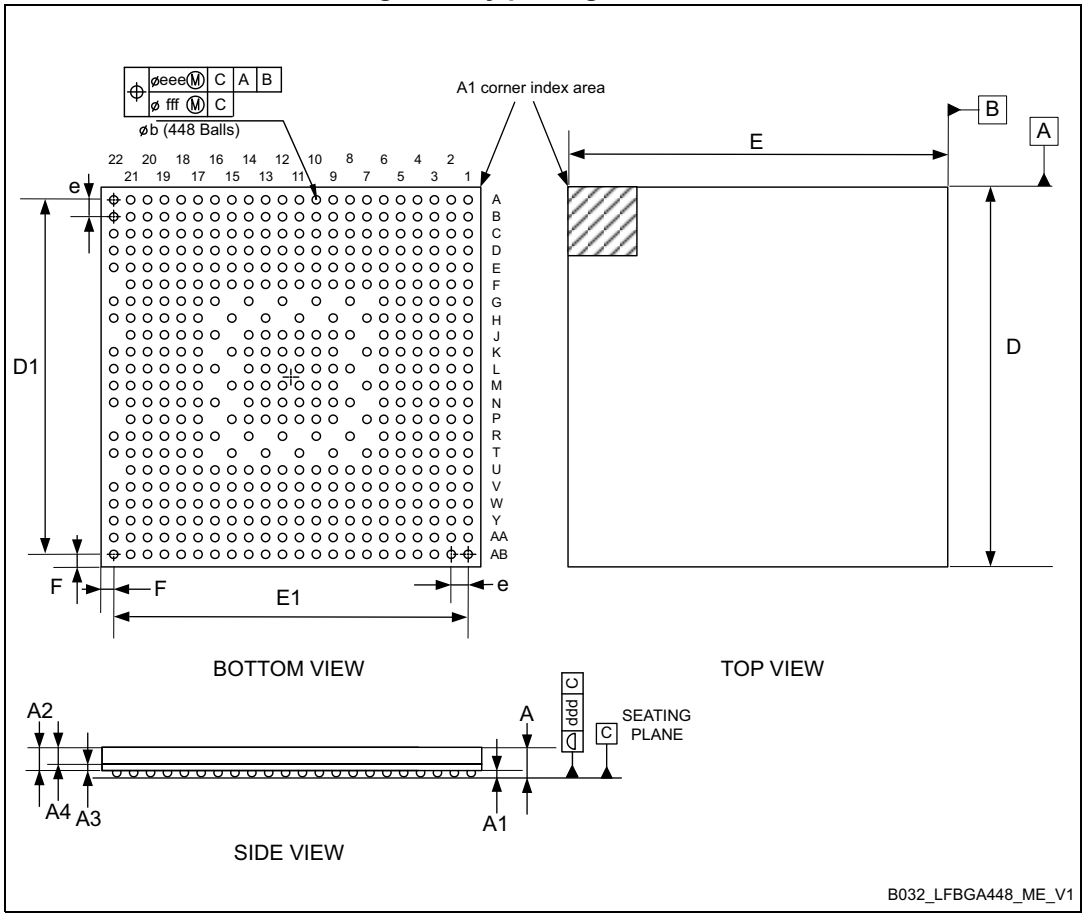
Figure 72. TFBGA361 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 LFBGA448 package information

Figure 73. LFBGA - 448 balls, 18x18 mm, 0.8 mm pitch, low profile fine pitch ball grid array package outline



1. Drawing is not to scale.
2. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Table 123. LFBGA - 448 balls, 18x18 mm, 0.8 mm pitch, low profile fine pitch ball grid array mechanical data

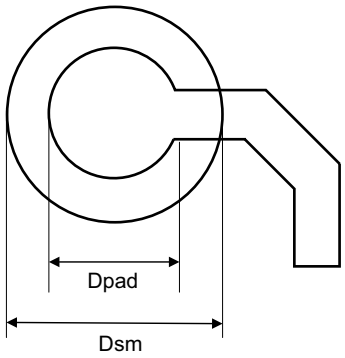
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.270	-	-	0.0500
A1	0.250	0.290	0.330	0.0098	0.0114	0.0130
A2	0.790	0.880	0.970	0.0311	0.0346	0.0382
A3	0.240	0.28	0.320	0.0094	0.0110	0.0126
A4	0.550	0.600	0.650	0.0217	0.0236	0.0256
b[2]	0.350	0.400	0.450	0.0138	0.0157	0.0177

Table 123. LFBGA - 448 balls, 18x18 mm, 0.8 mm pitch, low profile fine pitch ball grid array mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	17.900	18.000	18.100	0.7047	0.7087	0.7126
D1	-	16.800	-	-	0.6614	-
E	17.900	18.000	18.100	0.7047	0.7087	0.7126
E1	-	16.800	-	-	0.6614	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	-	0.120	-	-	0.0047	-
eee[3]	-	0.150	-	-	0.0059	-
fff[4]	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Low profile: 1.20 mm < A ≤ 1.70 mm / Fine pitch: e < 1.00 mm pitch.
   The total profile height (Dim.A) is measured from the seating plane “C” to the top of the component. The maximum total package height is calculated by the RSS method (Root Sum Square).
   A Max = A1 Typ + A2 Typ + A4 Typ + √(A1² + A2² + A4² tolerance values).
3. The typical ball diameter before mounting is 0.40 mm
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

Figure 74. LFBGA - 448 balls, 18x18 mm, 0.8 mm pitch, low profile fine pitch ball grid array recommended footprint



B032_LFBGA448_FP_V1

1. Dimensions are expressed in millimeters.

Table 124. LFBGA - 448 balls, recommended PCB design rules (0.8 mm pitch, BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm

Table 124. LFBGA - 448 balls, recommended PCB design rules (0.8 mm pitch, BGA)

Dimension	Recommended values
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	0.125 mm to 0.100 mm

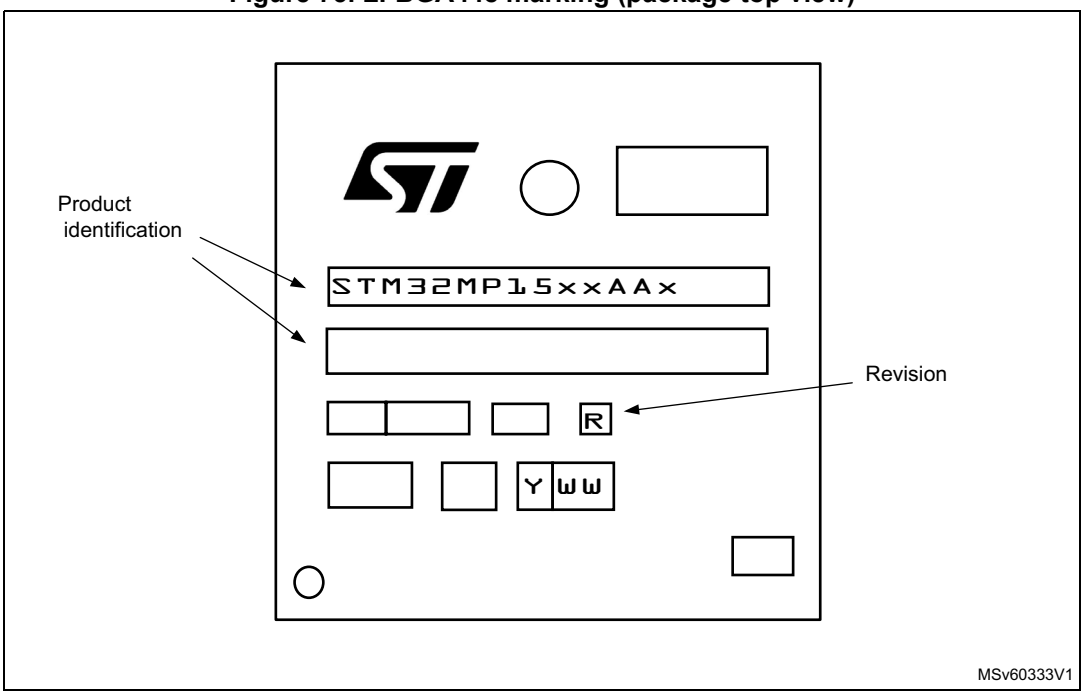
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 75. LFBGA448 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 Thermal characteristics

Package thermal characteristics in *Table 125* are specified with conditions as per JEDEC JESD51-6, JESD51-8, JESD51-9, and JESD51-12. These typical values will vary in function of board thermal characteristics and other components on the board.

Θ_{JA} : Thermal resistance junction-ambient.
Θ_{JB}: Thermal resistance junction-board.
Θ_{JC}: Thermal resistance junction-top-case.
Θjb: Thermal parameter junction-board.
Ψjt: Thermal parameter junction-top-case.
Motherboard type: four layers, JEDEC 2S2P

Table 125. Thermal characteristics

Symbol	Parameter	Value		Unit
		Natural convection	1m/s (200 ft/mn)	
Θ_{JA}(1)	TFBGA257 - 257-ball 10x10 mm 0.50/0.65 mm pitch	36.079	31.79	°C/W
	TFBGA361 - 361-ball 12x12 mm 0.50/0.65 mm pitch	35.151	30.953	
	LFBGA354 - 354-ball 16x16 mm 0.80 mm pitch	34.145	30.121	
	LFBGA448 - 448-ball 18x18 mm 0.80 mm pitch	28.545	24.797	
Θ_{JB}(2)	TFBGA257 - 257-ball 10x10 mm 0.50/0.65 mm pitch	19.487		°C/W
	TFBGA361 - 361-ball 12x12 mm 0.50/0.65 mm pitch	20.555		
	LFBGA354 - 354-ball 16x16 mm 0.80 mm pitch	22.038		
	LFBGA448 - 448-ball 18x18 mm 0.80 mm pitch	17.409		
Θ_{JC}(3)	TFBGA257 - 257-ball 10x10 mm 0.50/0.65 mm pitch	10.768		°C/W
	TFBGA361 - 361-ball 12x12 mm 0.50/0.65 mm pitch	10.049		
	LFBGA354 - 354-ball 16x16 mm 0.80 mm pitch	9.675		
	TLFBGA448 - 448-ball 18x18 mm 0.80 mm pitch	8.439		
Ψjb (4)	TFBGA257 - 257-ball 10x10 mm 0.50/0.65 mm pitch	18.949	18.332	°C/W
	TFBGA361 - 361-ball 12x12 mm 0.50/0.65 mm pitch	20.002	19.398	
	LFBGA354 - 354-ball 16x16 mm 0.80 mm pitch	21.456	20.894	
	LFBGA448 - 448-ball 18x18 mm 0.80 mm pitch	16.946	16.574	
Ψjt (5)	TFBGA257 - 257-ball 10x10 mm 0.50/0.65 mm pitch	0.383	0.812	°C/W
	TFBGA361 - 361-ball 12x12 mm 0.50/0.65 mm pitch	0.354	0.735	
	LFBGA354 - 354-ball 16x16 mm 0.80 mm pitch	0.339	0.658	
	LFBGA448 - 448-ball 18x18 mm 0.80 mm pitch	0.297	0.542	

1. Per JEDEC JESD51-9
2. Per JEDEC JESD51-8
3. Per JEDEC JESD51-12 best practice guidelines
4. Per JEDEC JESD51-12.
5. Per JEDEC JESD51-12.

7.5.1 Reference documents

JESD51-6 Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air). Available from www.jedec.org.

JESD51-8 Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board. Available from www.jedec.org.

JESD51-9 Test Boards for Area Array Surface. Mount Package Thermal. Measurements. Available from www.jedec.org.

JESD51-12 Guidelines for Reporting and Using Electronic Package Thermal Information. Available from www.jedec.org.

8 Ordering information

Table 126. STM32MP157A ordering information scheme

Example: STM32 MP 157 A AA 3 T

Device family

STM32 = Arm-based 32-bit processor

Product type

MP = MPU product

Device subfamily

157 = STM32MP157 Line

Security option

A = Basic security

Package and pin count

AD = TFBGA257 10x10, 257 balls pitch 0.5 mm

AB = LFBGA354 16x16, 354 balls pitch 0.8 mm

AC = TFBGA361 12x12, 361 balls pitch 0.5 mm

AA = LFBGA448 18x18, 448 balls pitch 0.8 mm

Junction temperature range

3 = -40°C < T_J < +125°C

Packing

T = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 127. Document revision history

Date	Revision	Changes
08-Feb-2019	1	Initial release.
01-Aug-2019	2	Updated ADC characteristics on cover page. Updated *Table 1: STM32MP157A features and peripheral counts* Updated *Section 3.8.1: Power supply scheme*. Updated *Table 7: STM32MP157A pin and ball definitions*. Updated *Table 8: Alternate function AF0 to AF7*. Updated *Table 10: Voltage characteristics*. Updated *Table 13: General operating conditions*. Updated *Table 14: Operating conditions at power-up / power-down*. Updated *Table 15: Embedded reset and power control block characteristics*. Updated *Figure 13: VDDCORE rise time from reset*. Updated *Table 15: Embedded reset and power control block characteristics*. Updated *Table 16: Embedded reference voltage*. Updated *Table 18: REG1V1 embedded regulator (USB_PHY) characteristics*. Updated *Table 19: REG1V2 embedded regulator (DSI) characteristics*. Updated *Table 20: REG1V8 embedded regulator (USB+DSI) characteristics*. Updated *Table 21: Current consumption (IDDCORE) in Run mode*. Updated *Table 22: Current consumption (IDD) in Run mode*. Updated *Table 23: Current consumption in Stop mode*. Updated *Table 24: Current consumption in LPLV-Stop mode*. Updated *Table 26: Current consumption in VBAT mode*. Updated *Table 29: High-speed external user clock characteristics (digital bypass)*. Updated *Table 30: High-speed external user clock characteristics (analog bypass)*. Added *Table 31: Low-speed external user clock characteristics (analog bypass)*. Added *Figure 17: Low-speed external clock source AC timing diagram (analog bypass)*. Updated *Table 33: 8-48 MHz HSE oscillator characteristics*. Updated *Figure 19: Typical application with a 24 MHz crystal*.

Table 127. Document revision history

Date	Revision	Changes
01-Aug-2019	2 (continued)	Updated *Figure 20: Typical application with a 32.768 kHz crystal*. Updated *Table 36: HSI oscillator characteristics*. Updated *Table 37: CSI oscillator characteristics*. Updated *Table 38: LSI oscillator characteristics*. Updated *Table 39: PLL1_1600, PLL2_1600 characteristics*. Updated *Table 36: HSI oscillator characteristics*. Updated *Table 37: CSI oscillator characteristics*. Updated *Table 38: LSI oscillator characteristics*. Updated *Table 39: PLL1_1600, PLL2_1600 characteristics*. Updated *Table 40: PLL3_800, PLL4_800 characteristics*. Updated *Table 41: USB_PLL characteristics*. Updated *Table 42: DSI_PLL characteristics*. Updated *Table 48: EMI characteristics*. Updated *Table 49: ESD absolute maximum ratings*. Updated *Section : Static latchup* Updated *Table 51: I/O current injection susceptibility*. Updated *Table 52: I/O static characteristics*. Updated *Table 53: Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8*. Added *Table 54: Output voltage characteristics for PC13, PC14, PC15 and PI8*. Updated *Table 55: Output timing characteristics (HSLV OFF)*. Added *Figure 23: VIL/VIH for FT I/Os*. Updated *Table 76: ADC characteristics*. Updated *Table 77: Minimum sampling time versus RAIN with 47 pF PCB capacitor up to 125 °C and VDDA = 1.6 V*. Updated *Table 80: DAC characteristics*. Updated *Table 85: DTS characteristics*. Updated *Table 86: V_{BAT} ADC monitoring characteristics*. Updated *Table 88: Temperature and VBAT monitoring characteristics for temper detection*. Added *Section 6.3.31: Compensation cell*. Updated *Table 98: I2C analog filter characteristics*. Added *Section 6.3.38: USB High-Speed PHY characteristics*. Added *Section 6.3.39: DSI PHY characteristics*. Added *Section 7.5: Thermal characteristics*.