Nhóm 06-07-08CLC - Kiến trúc máy tính và hợp ngữ

Started on	Tuesday, 14 March 2017, 10:46 AM
State	Finished
Completed on	Tuesday, 14 March 2017, 11:25 AM
Time taken	38 mins 36 secs

Question 1
Complete
Marked out of 1.20

What is the correct sequence of instruction cycle?

Step 5: Calculate operand address
Step 2: Decode
Step 4: Execution
Step 3: Fetch operand
Step 1: Fetch opcode
Step 6: Store result

Your answer is partially correct.
You have correctly selected 3.

Question 2
Complete
Marked out of 1.00

Which one best describe cache hit and cache miss?

Cache miss ratio: the number of memory accesses that CPU must retrieve from the main memory per the total number of memory accesses
Cache hit ratio: the number of memory accesses that the CPU can retrieve from the cache per the total number of memory accesses

Your answer is correct.

Question 3
Complete
Marked out of 1.00

For cache write policies, which are often used for write-hit and write-miss

Write-hit: Write-back
Write-miss: Write-allocate

Your answer is correct.

Question 4
Complete
Marked out of 1.00

Choose correct features for SRAM and DRAM

DRAM: Slower access time, cheaper cost per bit, can manufacture with larger size
SRAM: Faster access time, cost more per bit, smaller size

Your answer is correct.

Question 5
Complete
Marked out of 1.00

Identify the correct sequence to update a page onto a flash memory?

Step 3: the entire block is being read from flash into RAM then request data in page is update

Step 1: the entire block of flash memory are erased

Step 2: The entire block from RAM then is written back to the flash memory

Your answer is incorrect.

Question 6
Complete
Marked out of 1.00

Choose correct set of registers for x86 processor

Data pointer to source memory in extra segment ES: SI

Pointer to variable in stack SS: BP

Instruction pointer CS: IP

Data pointer in data segment DS: BX

Your answer is correct.

Question 7
Complete
Marked out of 1.00

Match the definition of flag bits in PSW

contains the carry of 0 or 1 from the leftmost bit after an arithmetic operation: CF

determine the direction for moving or comparing data between memory areas: DF

determine whether an external interrupts are to be ignored or processed: IF

the processor switches to single-step mode: TF

Your answer is correct.

Question 8
Complete
Marked out of 1.00

What are components of Von Neumann, namely IAS computer?

Select one or more:

- [ ] Monitor
- [x] Memory
- [ ] Punched card reader
- [x] CPU
- [x] Bus
- [x] I/O Equipments

Your answer is correct.

Question 9
Complete
Marked out of 1.00

Which is not correct about MOORE law?

Select one or more:

- [ ] The number of transistors that could be put on a single chip was doubling every year
- [x] The number of transistors that could be put on a single chip was triple every year nowadays.
- [x] Likely triple after 2000
- [ ] The number of transistors that could be put on a single chip was doubling every year except 1970s

Your answer is correct.

Question 10
Complete
Marked out of 1.00

For better speed, in CPU design, engineers make use of the following techniques:

Select one or more:
- [x] Branch prediction
- [x] Pipelining
- [x] Speculative execution
- [ ] Faster CPU internal bus

Your answer is correct.

Question 11
Complete
Marked out of 1.00

To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design?

Select one or more:
- [ ] To move data directly by DMA
- [x] Make wider data bus path
- [x] Make use of both on-chip and off-chip cache memory
- [x] Using higher-speed bus and us hierarchy

Your answer is correct.

Question 12
Complete
Marked out of 1.00

What is the meaning of Amdahl's law in processor performance evaluation?

Select one:
- the cost reduce when moving from single-core to multicore processor
- the potential speedup of a program using multiple processor compared to a single processor
- the speedup of a multicore processor when increasing system bus speed
- the maximum speedup of a multicore processor

Your answer is correct.

Question 13
Complete
Marked out of 1.00

What are the processor's instruction categories

Select one or more:
- [x] Data processing
- [x] Control
- [ ] Processor - Cache memory
- [x] Processor - I/O
- [x] Processor - Memory
- [ ] Memory - Memory (DMA)

Your answer is correct.

Question 14
Complete
Marked out of 1.00

In computer, how does the processor serve multiple interrupt request from devices?

Select one:
- The processor can not process multiple interrupt requests
- Each device are assigned an interrupt priority, the device with higher priority will be served.
- Device with higher priority will use interrupt enable flag
- Each device are assigned an interrupt priority, the device with lower priority will be served.

Your answer is incorrect.

Question 15
Complete
Marked out of 1.00

Bus is a shared transmission medium, multiple devices connect to it but only one at a time can successfully transmit. Which component in computer facilitates this operation?

Select one:
- Bus Arbiter
- Programmed I/O
- Direct Memory Access (DMA)
- Bus master

Your answer is correct.

Question 16
Complete
Marked out of 1.00

When many devices of different transmission speed connect to the same bus, the overall system performance suffers. How did the design engineers resolved this:

Select one:
- PCI Express bus
- PCI bus
- Split system bus into local bus and memory bus
- Multiple-Bus hierarchies

Your answer is correct.

Question 17
Complete
Marked out of 1.00

What are the features of direct-mapping cache organization?

Select one or more:
- Thrash --> low hit ratio
- faster
- Simple and inexpensive
- small cache memory

Your answer is correct.

Question 18
Complete
Marked out of 1.00

Which ones are not correct for static RAM?

Select one or more:
- Cost per bit is higher than dynamic RAM
- faster than dynamic RAM because they are made from capacitor
- Cheaper than dynamic RAM because simpler chip controller
- Cost per bit is lower than dynamic RAM

Your answer is partially correct.
You have correctly selected 2.

Question 19
Complete
Marked out of 1.00

Which one is not correct?

Select one or more:
- EEPROM is erasable by exposing under UV
- PROM is non-volatile memory
- EPROM is erasable electrically
- Flash memory can only be erased electrically byte by byte

Your answer is correct.

Question 20
Complete
Marked out of 1.00

Which statements are correct for HDDs?

Select one or more:
- [x] a. Bits are stored on tracks
- [x] b. Head, Track, Sector are key parameters for access data on hard disk
- [ ] c. Bits are store randomly on disk surfaces
- [ ] d. Head, Track, Cylinder are key parameters for access data on hard disk

Your answer is correct.

Question 21
Complete
Marked out of 1.00

What is correct about the function of TRIM command in SSD?

Select one:
- ( ) Allow SSD to allocate memory pages in blocks properly for faster access
- ( ) Allow SSD to defragment scattered data stored in separate pages
- (•) Allow OS to notify SSD the presence of occupied blocks of data which are no longer in use and can be erased internally
- ( ) Allow SSD to manage occupied pages and remove them automatically for later use

Your answer is correct.

Question 22
Complete
Marked out of 1.00

Which set of registers are valid for addressing a memory location?

Select one or more:
- [x] DS:SI
- [x] DS:BX
- [ ] SS:DI
- [x] CS:IP

Your answer is correct.

Question 23
Complete
Marked out of 1.00

Which are valid based index addressing?

Select one or more:
- [x] [BX+SI]
- [ ] [SP+DI]
- [ ] [DX+SI]
- [x] [BX+DI]

Your answer is correct.

Question 24
Complete
Marked out of 1.00

Which are valid index addressing?

Select one or more:
- [x] [SI]
- [ ] [DX]
- [ ] [BX]
- [ ] [BP]

Your answer is partially correct.
You have correctly selected 1.

Question 25

Complete

Marked out of 1.00

8088 is 16 bit processor, the maximum addressable memory is:

Select one:

- 64M
- 1024K
- 640K
- 640M

Your answer is correct.

Question 26

Complete

Marked out of 1.00

Which are correct about the data registers of IA-32 processors:

Select one or more:

- Lower halves of the 16-registers an be used as 8-bit data registers: AH,AL,BH,BL,CH,CL,DH,DL
- complete 32-bit registers: EAX, EBX, ECX, EDX
- Lower halves of the 32-registers an be used as 4 16-bit data registers: AX,BX,CX,DX
- Higher halves of the 32-bit registers can be used as 16-bit registers: EAH,EAL,EBH,EBL,ECH,ECL,EDH,EDL

Your answer is correct.

Question 27

Complete

Marked out of 1.50

Which are correct about 32 bit index registers of IA-32 processors:

Select one or more:

- EDI: 32 bit pointer to destination memory in data movement instructions
- ESH,EDH: 16 bit pointers to higher memory above 1M
- DI: 16 bit pointer to destination memory in data movement instructions
- SI: 16 bit pointer to source memory in data movement instructions
- ESI: 32 bit pointer to source memory in data movement instructions

Your answer is correct.

Question 28

Complete

Marked out of 1.00

Which statement is correct about interrupt vector table?

Select one or more:

- Store in the ending area of 1024K of the main memory
- Take up 1024 bytes in the main memory
- Store on disk
- Store in the beginning area of the main memory

Your answer is correct.

Question 29

Complete

Marked out of 1.00

Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of DX register follows the execution of MOV DX, [1D4D] is 127B. What is the endian type of this computer system

Select one:

- little-endian
- level-endian
- big-endian
- non-endian

Your answer is correct.

Question 30
Complete
Marked out of 1.00

Part of memory as shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of BX register follows the execution of MOV BX, [1D49] is F57F. What is the endian type of this computer system

Select one:

- level-endian
- big-endian
- little-endian
- non-endian

Your answer is correct.

Question 31
Complete
Marked out of 0.50

The value in CS is 1FD0h what is the location of next instruction from 00000h if Instruction pointer is 3CD4h

Answer: 3CD5H

Question 32
Complete
Marked out of 1.00

Select correct items to describe best about CISC

Number of clocks per instruction	multi-clock
code size of program	small code size
Assembly code	simpler
Instruction set	Complex
Bytes per instruction	different for variety of instructions

Your answer is correct.

Question 33
Complete
Marked out of 1.00

What best describe the Spatial and Temporal Locality?

Temporal locality	be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy
Spatial locality	be exploited by using larger cache blocks and by incorporating prefetching mechanisms into the cache control logic

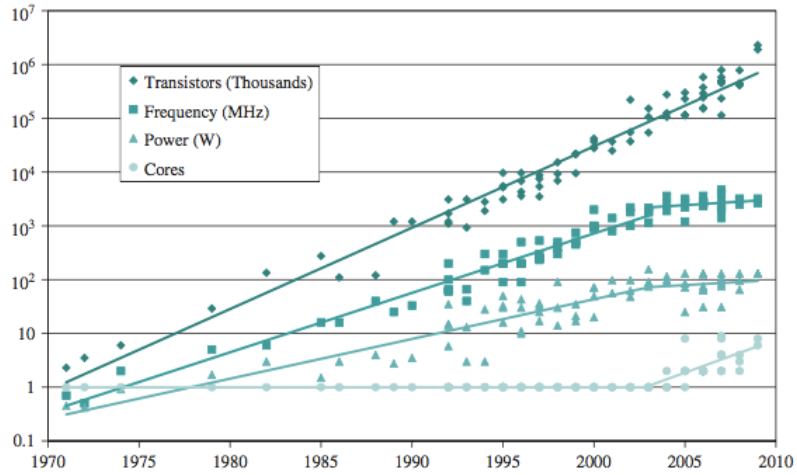
Your answer is correct.

Question 34

Complete

Marked out of 1.00

What can be concluded from the following chart of processor trends:



Select one:

- The multi-core processors and level off clock speed help to make heat dissipation of CPU chip less
- The number of transistors in chips produce more heat dissipation
- Heat dissipation in processor chip is increasing year after year since 1970
- The processor speed keeps increasing after 2003

Your answer is correct.

Question 35

Complete

Marked out of 1.00

To evaluate processor performance, the following indicators and formulas are used:

Cycles per instruction $CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$

Time to execute a program $T = I_c \times CPI \times \tau$

Or $T = I_c \times [p + (m \times k)] \times \tau$

In which:
p: the number of processor cycles needed to decode and execute the instruction
m: the number of memory references needed
k: the ratio between memory cycle time and processor cycle time
τ: cycle time = *1/f*

Which of the following system attributes affects I_c (the number of instructions of a program)

Select one or more:

- Cache and memory hierarchy
- Processor implementation
- Instruction set architecture
- Compiler technology

Your answer is correct.

Question 36

Complete

Marked out of 1.00

To evaluate processor performance, the following indicators and formulas are used:

Which of the following system attributes affects cycle time τ

Select one or more:

- Processor implementation
- Compiler technology
- Instruction set architecture
- Cache and memory hierarchy

Your answer is correct.

Question 37
Complete
Marked out of 1.00

Key parameters to consider when evaluating processor hardware include:

Select one or more:

- [x] reliability
- [x] performance
- [x] power consumption
- [ ] databus size
- [x] size
- [ ] Address bus size
- [x] cost

Your answer is correct.

Question 38
Complete
Marked out of 1.00

A memory chip has 12 address pins, determine the maximum memory words of this chip?

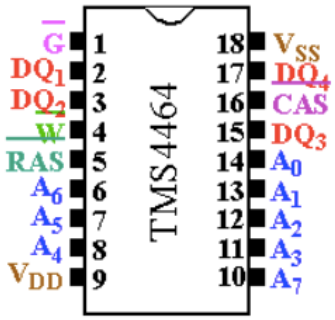
Select one:

- 2048K
- 2048
- 4000
- 4096

Your answer is correct.

Question 39
Complete
Marked out of 1.00

Which of the following best describe the memory chip with pinout as shown below:



DQ: Data pinout

Select one:

- DRAM 64Kx4-bit
- SRAM 256Kx1-bit
- DRAM 16Kx4-bit
- SDRAM 64Kx4-bit

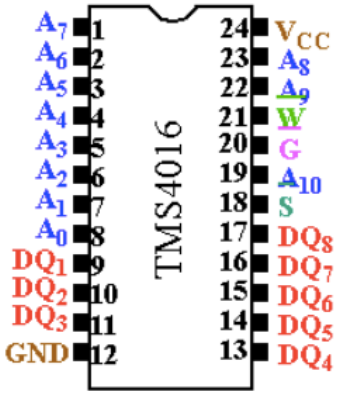
Your answer is correct.

Question 40

Complete

Marked out of 1.00

Choose the correct structure of memory chip as shown below



Note:

DQ: Data pinout

Select one:

- DRAM 2Kx8-bit
- SRAM 1Kx16-bit
- SRAM 2Kx8-bit
- DRAM 1Kx16-bit

Your answer is correct.

Question 41

Complete

Marked out of 1.00

The three key characteristics of memory are: capacity, access time and cost. Which of the following relationships hold for a variety of memory technologies?

Select one or more:

- [x] Faster access time, greater cost per bit
- [ ] Higher capacity, higher access time
- [x] Greater capacity, smaller cost per bit
- [x] Greater capacity, slower access time

Your answer is correct.

Question 42

Complete

Marked out of 1.00

A SRAM memory chip labeled 32x8bit. Which of the following is correct pinout regarding address and data lines?

Select one:

- 32 address pins, 3 data pins
- 32 address pins, 4 data pins
- 5 address pins, 3 data pins
- 15 address pins, 8 data pins

Your answer is correct.

Question 43

Complete

Marked out of 1.00

In the interconnection system, the number of address lines are governs by

Select one:

- I/O Module
- CPU
- data bus line
- Memory size

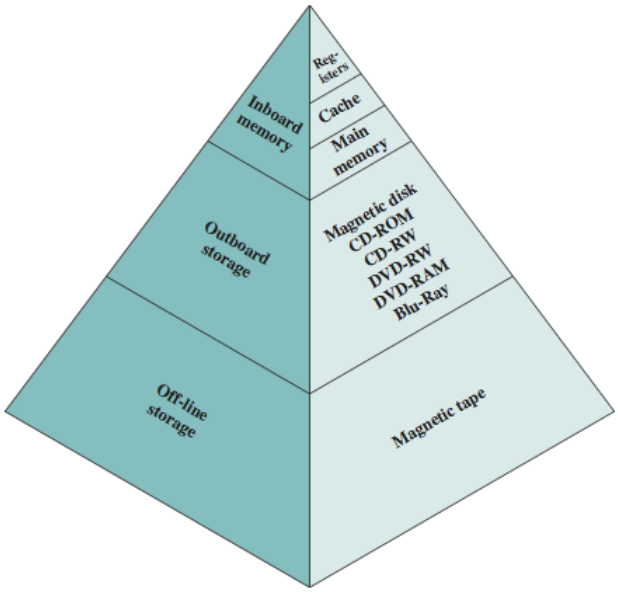
Your answer is correct.

Question 44

Complete

Marked out of 1.00

For memory hierarchy below, which relationship hold when moving downward



Select one or more:

- [x] Increasing access time
- [x] Decreasing cost per bit
- [x] Decreasing frequency of access by the processor
- [ ] the processor accesses more often
- [x] Increasing capacity

Your answer is correct.

Question 45

Complete

Marked out of 1.50

Identified correct addressing mode of the following instructions?

MOV AX, BX	Register
MOV BP, [BX+SI]	Base relative plus index
MOV AX, ARRAY [BX+SI]	Base plus index
MOV AX, [BX]	Register indirect
MOV AX,[1234h]	Direct
MOV AX, 3540h	Immediate

Your answer is partially correct.

You have correctly selected 4.

Question 46

Complete

Marked out of 1.00

Part of computer memory is shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction **MOV AX, [1D4B]** executed

Answer: 5A2D

Question 47
Complete
Marked out of 1.00

Part of memory shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of EAX follow the execution of this code

MOV BX, 1D4C

MOV EAX, [BX]

Answer: 125A

Question 48
Complete
Marked out of 1.00

the memory stack area of a program shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of SP register is 1D48. What is the value of SI follows the execution of **POP SI**

Answer: 1D48

Question 49
Complete
Marked out of 1.00

the memory stack area of a program shown in figure

Address	1D50	1D51	1D52	1D53
Value	AF	90	71	DA

The value of SP register is 1D50. What is the value of SP follows the execution of **PUSH SI**

Answer: 1D4F

Question 50
Complete
Marked out of 3.00

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs

Instruction Type	Instruction Count (millions)	Cycles Per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine A		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

Determine the effective, CPI, MIPS rate and execution time for each machine.

CPI_b 1.92 ▼

CPU Time_a 0.2 ▼

CPU Time_b 0.23 ▼

CPI_a 2.22 ▼

MIPs_b 104 ▼

MIPs_a 90 ▼

Your answer is correct.

Question 51
Complete
Marked out of 2.00

Choose correct RAID volume definitions for a request 2T storage.

RAID 1 - Mirror volume	2 x 2T HDDs are needed, no data lost when the primary storage fails
Spanned Volume	2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails
RAID 0 - Striped volume	2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails
RAID5 Volume	At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time

Your answer is correct.

Question 52
Complete
Marked out of 1.00

Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 30% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 30% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor?

Select one:

- 10%
- 15%
- 17%
- 23%

Your answer is correct.

Question 53
Complete
Marked out of 1.00

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB, the average seek time is 10.2 ms and the drive rotates at 3600 rpm. What is average access time. Given: Rotational delay = 1/(2r), where r is the rotational speed in revolutions per second

Answer: 16.3 ms

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