Computer Organization – HW3
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1. Consider a system with 2 levels of cache memory. CPU has 20 address lines (A0-A19) and 8 data lines(D0-D7). Main memory is 1M8 and cache memories in both levels are 4K8. Main memory has an access time of 120ns. L1 cache memory access time is 20ns and it has a hit rate of 95%. L2 cache memory access time is 30ns and has a hit rate of 85%. Memory controller has a delay of 50ns.
   - Draw the schematic (including memory controller)
   - Calculate effective Time.
   - The L1 memory is swapped with another cache memory (still 4K8) which has an access time of 1ns with 90% hit rate. But we also change main memory to a new one with 110ns access time. Calculate new access time. Will it be faster or slower?

2. Consider a system including a CPU with 20 lines of address (A0-A19) and 8 lines of data (D0-D7). Draw schematics for memory mapping and CPU connections in "Fully-Decoding" method with given memory chips below.
   - 512K8 (all of memory)
   - 128K4 (all of memory)
   - First half 128K8 – Second half 256K8

3. For the following code snippet, identify all of the RAW, WAW, and WAR hazards. Provide a list for each hazard. (Hint, remember that you have to check more than neighbor instructions.)

```
ADD R1, R2, R3
SUB R3, R4, R6
MUL R5, R4, R7
ADDIU R5, R5, 1
SUB R6, R3, R9
ANDI R2, R1, R9
```

4. Consider two different machines, with two different instruction sets, both of which have a clock rate of 500 MHz. Determine the effective CPI, MIPS rate, and execution time for each machine. (Million instructions per second = MIPS: an approximate measure of a computer's raw processing power)

The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Inst. Count (millions)	CPI
Machine A		
Arithmetic and Logic	8	1
Load and Store	4	3
Branch	2	4
Others	4	3
Machine B		
Arithmetic and Logic	10	1
Load and Store	8	2
Branch	2	4
Others	4	3

5. Compute the Clocks Per Instruction (CPI) of a machine which has an average CPI for ALU operations of 1.1, a CPI for branches/jumps of 3.0, and a hit rate of 50% in the cache. A hit in the cache takes 1 cycle pipelined and a cache miss takes 100 cycles. Assume 25% of instructions are loads, 15% are stores, 20% are branches/jumps and the balance are ALU operations.

6. Let's compare a CISC machine versus a RISC machine on a benchmark. Assume the following characteristics of the two machines:

   • CISC: CPI of 4 for load/store, 3 for ALU/branch and 10 for call/return, CPU clock rate of 3.5 GHz.

   • RISC: CPI of 1.3 (the machine is pipelined, the ideal CPI is 1.0, but overhead and stalls make it 1.3) and a CPU clock rate of 1.75 GHz.

   Since the CISC machine has more complex instructions, the IC for the CISC machine is 30% smaller than the IC for the RISC machine. The benchmark has a breakdown of 38% loads, 10% stores, 35% ALU operations, 3% calls, 3% returns and 11% branches.

Which machine will run the benchmark in less time and by how much? (Hint: CPU time = IC × CPI × Clock cycle time)

7. In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

alu	beq	lw	sw
45%	20%	20%	15%

   - What is the clock cycle time in a pipelined and non-pipelined processor?
   - What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
   - Assuming there are no stalls or hazards, what is the utilization of the data memory?

8. Assume a program with 820,000,000 instructions is needed for spell checking of a very large file. There are 4 types of instructions in this program and each type needs N clock cycle for execution.

Instruction Class	Clock cycles per Instructions	Number of Instructions
Branch	3	160,000,000
Store	4	200,000,000
Load	5	250,000,000
ALU/R-type	4	210,000,000

Duration of complete run of the program is 1.57 seconds. Find out clock cycles time of execution in this computer

Please submit your homeworks in the following format:

Name_StudentNumber_HW3 (BillGates_12345678_HW3)   Good Luck!