	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	|router_top	428 (0)	534 (0)	0	0	43	0	|router_top	router_top	work
1	|router_fifo:FIFO1|	145 (145)	202 (202)	0	0	0	0	|router_top| router_fifo:FIFO1	router_fifo	work
2	|router_fifo:FIFO2|	53 (53)	45 (45)	0	0	0	0	|router_top| router_fifo:FIFO2	router_fifo	work
3	|router_fifo:FIFO3|	137 (137)	202 (202)	0	0	0	0	|router_top| router_fifo:FIFO3	router_fifo	work
4	|router_fsm:FSM|	30 (30)	24 (24)	0	0	0	0	|router_top|router_fsm:FSM	router_fsm	work
5	|router_reg:REGISTER|	22 (22)	43 (43)	0	0	0	0	|router_top| router_reg:REGISTER	router_reg	work
6	| router_sync:SYNCRONIZER|	41 (41)	18 (18)	0	0	0	0	|router_top| router_sync:SYNCRONIZER	router_sync	work