

Design a 4-bit ALU

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Abstract—This project presents the design and implementation of a 4-bit Arithmetic Logic Unit (ALU). The ALU performs arithmetic and logical operations on two 4-bit inputs and produces a 4-bit output. The design is implemented using Verilog hardware description language and simulated using timing function. The ALU supports basic arithmetic operations such as addition and subtraction, as well as logical operations such as ADD, NAND, and XNOR as per requirements of the project. Overall, this project demonstrates the design and implementation of a simple but functional sequential ALU using Verilog HDL.

Index Terms—ALU, Verilog, arithmetic, logic, simulation

I. INTRODUCTION

This report presents the design and implementation of a 4-bit ALU using Verilog HDL and Quartus II software. The ALU was designed to perform various arithmetic and logical operations such as addition, subtraction, bitwise AND, bitwise OR, and bitwise XOR. The design consists of various modules such as the Adder, Subtractor, and logic gates which were generated based on the verilog code. In this report, we provide a detailed description of the design and implementation process, including the Verilog code for each module and the timing diagram for verification. We also discuss the challenges encountered during the design process and how they were overcome. Finally, we present the results of the hardware testing, demonstrating that the ALU is capable of performing the desired operations accurately and efficiently. The design of a 4-bit ALU is an essential component in digital circuit design, and it is a fundamental building block in many larger circuits and VLSI design.

II. FINITE STATE MACHINE DESIGN AND IMPLEMENTATION

Finite State Machine (FSM) is a model for designing sequential logic circuits, where the circuit's behavior is determined by a finite number of states, inputs, and outputs. In

this case, the FSM is designed to implement four different operations, namely RESET, XNOR, SUB, and ADD on two 4-bit inputs A and B. The way we coded the Verilog code represents the implementation of the FSM, which is designed to perform the above mentioned arithmetic and logical operations on the given input values. The FSM has four states, which are encoded as 2-bit values, as follows: State 0 (2'b00): In this state, the circuit performs the selected operation on the first bit of the input values and transitions to the next state. State 1 (2'b01): In this state, the circuit performs the selected operation on the second bit of the input values and transitions to the next state. State 2 (2'b10): In this state, the circuit performs the selected operation on the third bit of the input values and transitions to the next state. State 3 (2'b11): In this state, the circuit performs the selected operation on the fourth and most significant bit of the input values and transitions back to the initial state. Before transition it also sets the values of zero flag, sign flag and carry flag. Things are checked and done slightly different based on the opcode brown. The four different operations are implemented using a case statement with opcode as the selector. Each operation case statement contains the logic required to perform the operation on the given input values, and update the output values of the circuit accordingly. For example, for the ADD operation, the code first calculates the sum of the LSBs of the input values, adds the carry value to it (initially 0), and assigns the sum and the carry value to the output register C. Then, it updates the zero flag, which is set to 1 if the output is 0, and transitions to the next state. The outputs of the circuit include C, which stores the result of the operation, carr, which is the carry bit generated during addition or subtraction, sign, which is the sign bit of the output value, and zero, which is set to 1 if the output is zero. Overall, the FSM implementation allows the circuit to perform different arithmetic and logical operations on the given input values, and update the output values based on the operation performed.

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Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Abbreviations such as IEEE, SI, MKS, CGS, ac, dc, and rms do not have to be defined. Do not use abbreviations in the title or heads unless they are unavoidable.

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$$a + b = \gamma \quad (1)$$

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- The subscript for the permeability of vacuum μ_0 , and other common scientific constants, is zero with subscript formatting, not a lowercase letter “o”.
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- There is no period after the “et” in the Latin abbreviation “et al.”.
- The abbreviation “i.e.” means “that is”, and the abbreviation “e.g.” means “for example”.

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TABLE I
TABLE TYPE STYLES

Table Head	Table Column Head		
	Table column subhead	Subhead	Subhead
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^aSample of a Table footnote.

Figure Labels: Use 8 point Times New Roman for Figure labels. Use words rather than symbols or abbreviations when



Fig. 1. Example of a figure caption.

writing Figure axis labels to avoid confusing the reader. As an example, write the quantity “Magnetization”, or “Magnetization, M”, not just “M”. If including units in the label, present them within parentheses. Do not label axes only with units. In the example, write “Magnetization (A/m)” or “Magnetization {A[m(1)]}”, not just “A/m”. Do not label axes with a ratio of quantities and units. For example, write “Temperature (K)”, not “Temperature/K”.

ACKNOWLEDGMENT

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REFERENCES

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