
Getting started with STM32F3 series hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, clock management, reset control, boot mode settings and debug management. It explains how to use the STM32F3xx product lines and describes the minimum hardware resources required to develop an application based on STM32F3 series.

The STM32F3x8 line devices with their disabled embedded regulator share many features/peripherals with the STM32F301, STM32F302, STM32F303 and STM32F334 line devices, which embedded regulator is enabled, with some differences.

A summary of the differences between the product lines is provided in [Section 6](#).

A detailed reference design schematic is also contained in this document with descriptions of the main components, interfaces and modes.

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1 Power supplies

1.1 Power supply schemes

There are a variety of power supply schemes:

- $V_{DD} = 2.0$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- $V_{DDA} = 2.0$ to 3.6 V: external analog power supply for ADC/DAC, Comparators, Reset blocks, RCs and PLL (in all STM32F3 series devices except STM32F373 line, the minimum voltage to be applied to V_{DDA} is 2.4 V when the OPAMP and DAC are used. In STM32F373, minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC and DAC are used).
The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- $V_{DDSD12} = 2.2$ to 3.6 V: external power supply for SDADC1/2, PB2, PB10, and PE7 to PE15 I/O pins (I/O pin ground is internally connected to VSS). V_{DDSD12} must always be kept lower or equal to V_{DDA} . If V_{DDSD12} is not used, it must be connected to V_{DDA} .
- $V_{DDSD3} = 2.2$ to 3.6 V: external power supply for SDADC3, PB14 to PB15 and PD8 to PD15 I/O pins (I/O pin ground is internally connected to VSS). V_{DDSD3} must always be kept lower or equal to V_{DDA} . If V_{DDSD3} is not used, it must be connected to V_{DDA} .

Note: V_{DDSD12} and V_{DDSD3} are available on STM32F373 only.

Figure 1. STM32F303/302xB/C power supply scheme

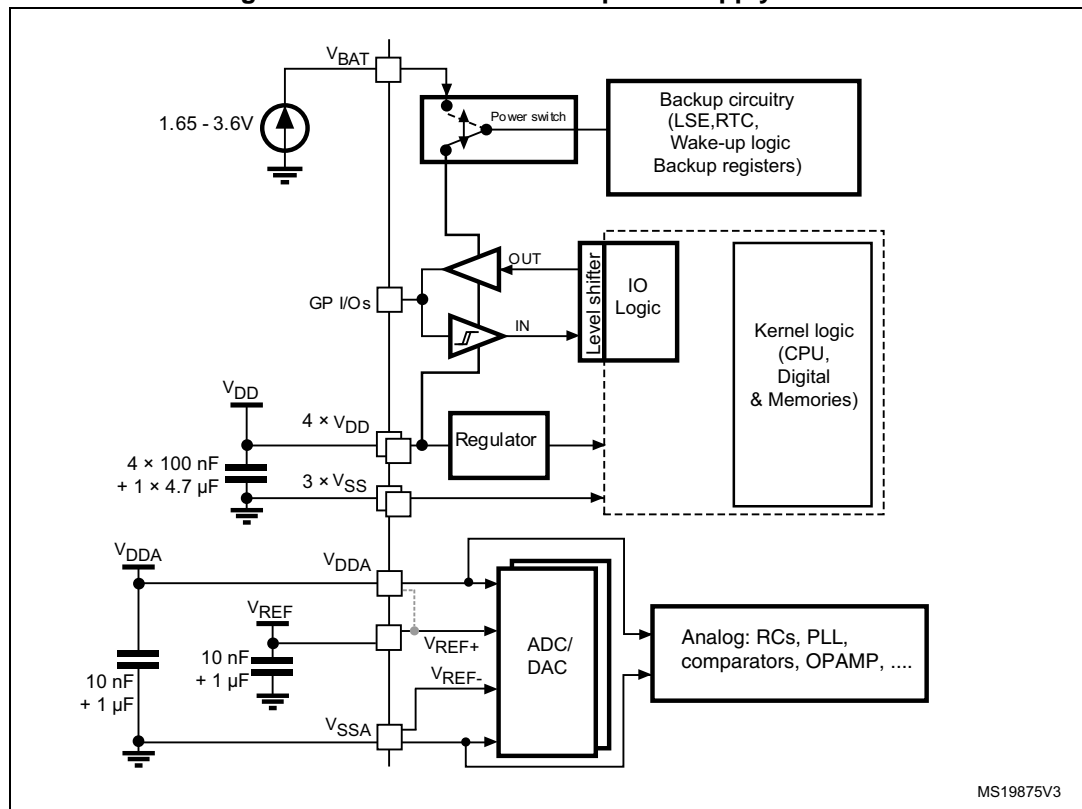


Figure 2. STM32F302xD/E/STM32F303xD/E power supply scheme

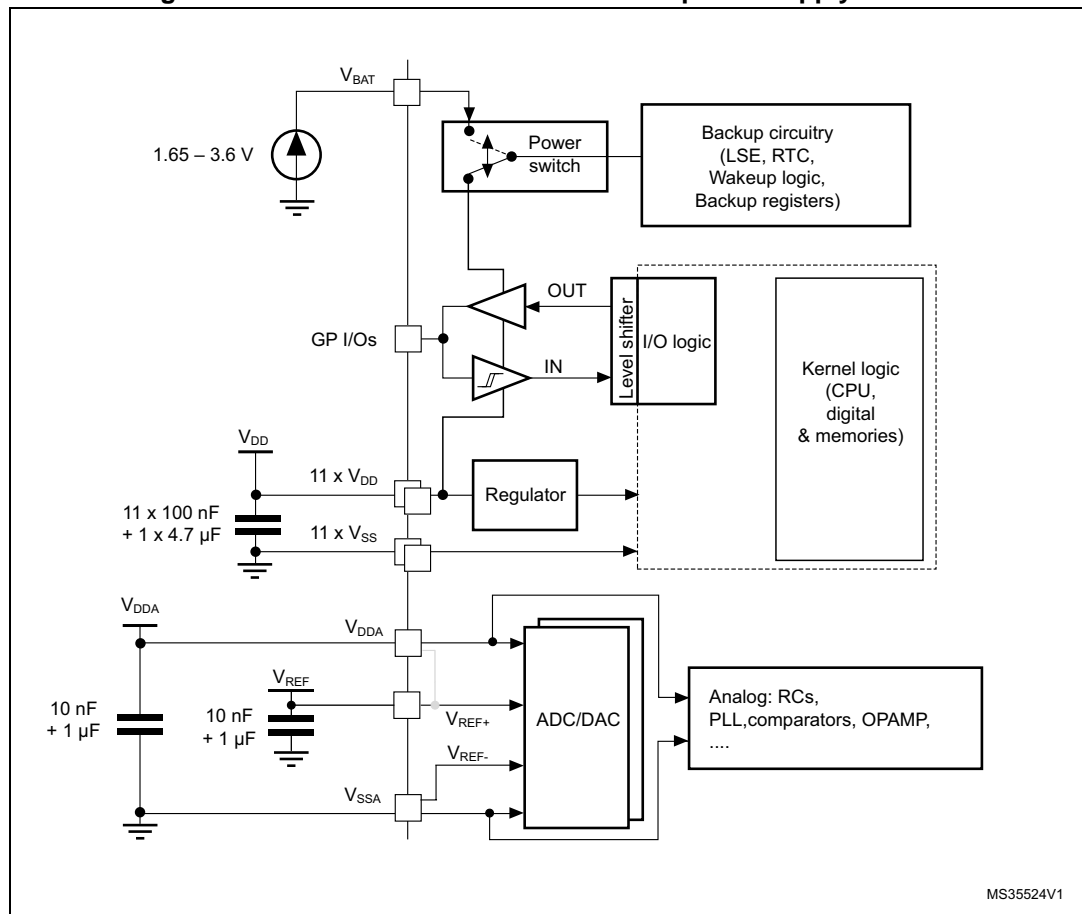
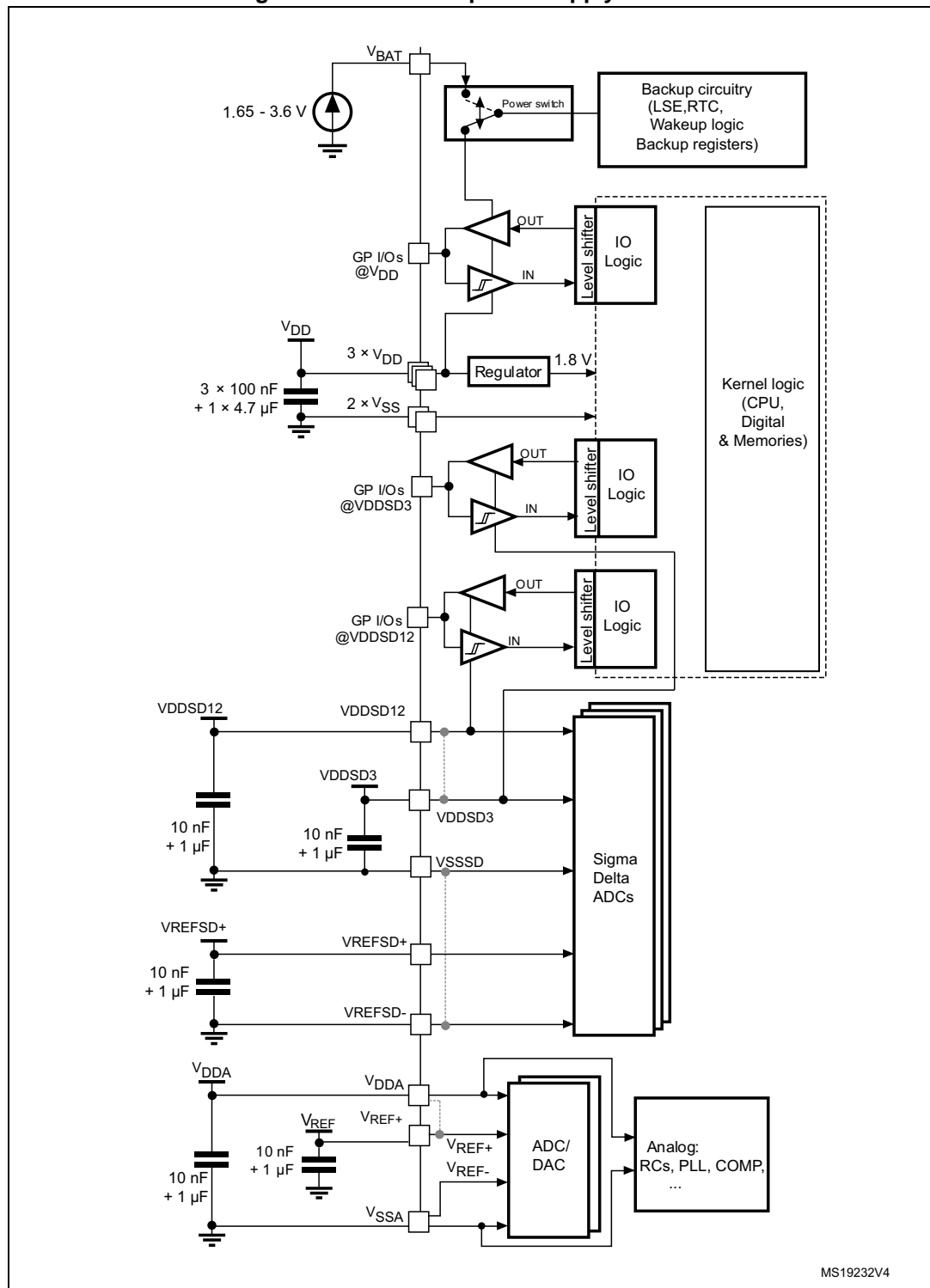


Figure 3. STM32F373 power supply scheme



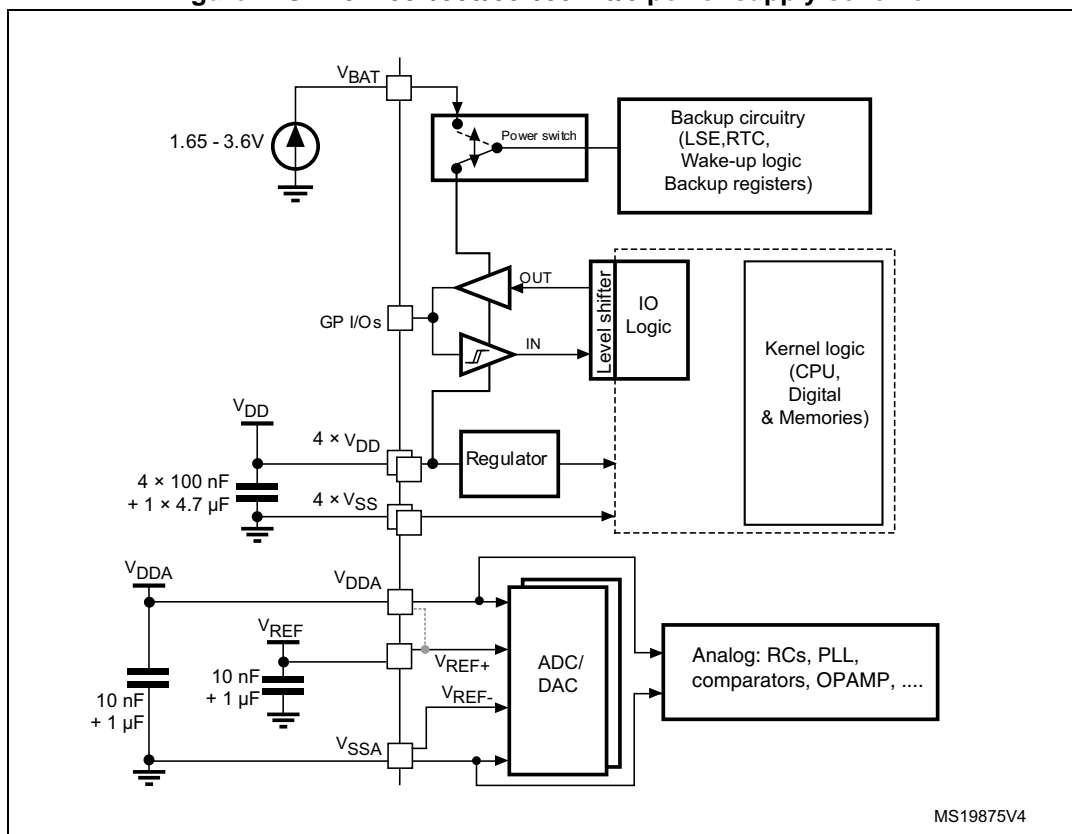
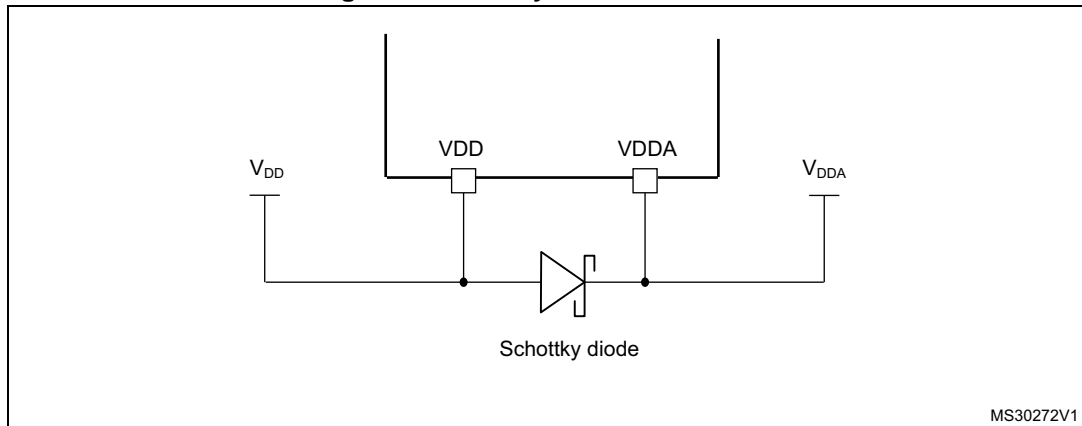


Figure 5. Schottky diode connection



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1.1.2 Sigma Delta supply voltages (only on F37x)

To improve Sigma delta ADC (SDADC) peripherals performance the device implements two independent power supplies used to power SDADC peripherals. There are two power supply pins with common ground pin (V_{DDSD12} , V_{DDSD3} , V_{SSSD}).

Those power supply sources also defines voltage levels on digital GPIO pins which are sharing SDADC analog inputs for given SDADC peripheral. Refer to device datasheet which GPIO pins are powered from V_{DDSD12} and which from V_{DDSD3} .

Sigma delta power supplies must be always less or equal to the analog supply: $V_{DDSDx} < V_{DDA}$ but they can be lower or higher than V_{DD} .

If no SDADC is used in application then V_{DDSDx} must be connected externally to V_{DD} .

V_{SSSD} must be always connected to V_{SS} .

There are some next important restrictions to V_{DDSD12} and V_{DDSD3} with relation to the reference voltage used for the SDADCs:

- If the V_{REFSD+} pin is selected as the external reference voltage for the SDADCs:
 - If SDADC1 or SDADC2 are enabled in the PWR controller (ENSD1, ENSD2 bits) then: $V_{DDSD12} > V_{REFSD+}$, $V_{DDSD3} > V_{REFSD+}$
 - If SDADC1 and SDADC2 are disabled in the PWR controller then: $V_{DDSD3} > V_{REFSD+}$
- If the V_{DDSDx} power supply is selected as the reference voltage for the SDADCs:
 - If SDADC1 or SDADC2 are enabled in PWR controller (ENSD1, ENSD2 bits) then: $V_{DDSD12} = V_{DDSD3}$
- If SDADC1 and SDADC2 are disabled and SDADC3 is enabled in the PWR controller (ENSD1, ENSD2, ENSD3 bits) then: $V_{DDSD12} \leq V_{DDSD3}$.

1.1.3 Battery backup

To retain the content of the Backup registers when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or another source.

The V_{BAT} pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply (V_{DD}) is turned off.

The switch to the V_{BAT} supply is controlled by the power down reset (PDR) circuitry embedded in the Reset block.

If no external battery is used in the application, it is highly recommended to connect V_{BAT} externally to V_{DD} .

1.1.4 Voltage regulator

The voltage regulator is always enabled after reset.

It works in three different modes depending on the application modes:

- Run mode: the regulator supplies full power to the 1.8 V domain (core, memories and digital peripherals)
- Stop mode: the regulator supplies low power to the 1.8 V domain, preserving the contents of the registers and SRAM. In Stop mode, the voltage regulator can be configured in low power mode in order to further reduce the consumption.
- Standby mode: the regulator is powered off. The contents of the registers and SRAM are lost except for the Standby circuitry and the Backup domain. This includes the following features which can be selected by programming individual control bits:
 - Independent watchdog (IWDG): the IWDG is started by writing to its Key register or by a hardware option. Once started it cannot be stopped except by a reset.
 - Real-time clock (RTC): configured by the RTCEN bit in the Backup domain control register (RCC_BDCR).
 - Internal RC oscillator (LSI): configured by the LSION bit in the Control/status register (RCC_CSR).
 - External 32.768 kHz oscillator (LSE): configured by the LSEON bit in the Backup domain control register (RCC_BDCR).

1.2 Reset and power supply supervisor

1.2.1 Reset

There are three types of reset, defined as: system reset, power reset and backup domain reset.

System reset

A system reset sets all registers to their reset values, except the reset flags in the clock controller CSR register and the registers in the Backup domain. A system reset is generated when one of the following events occurs:

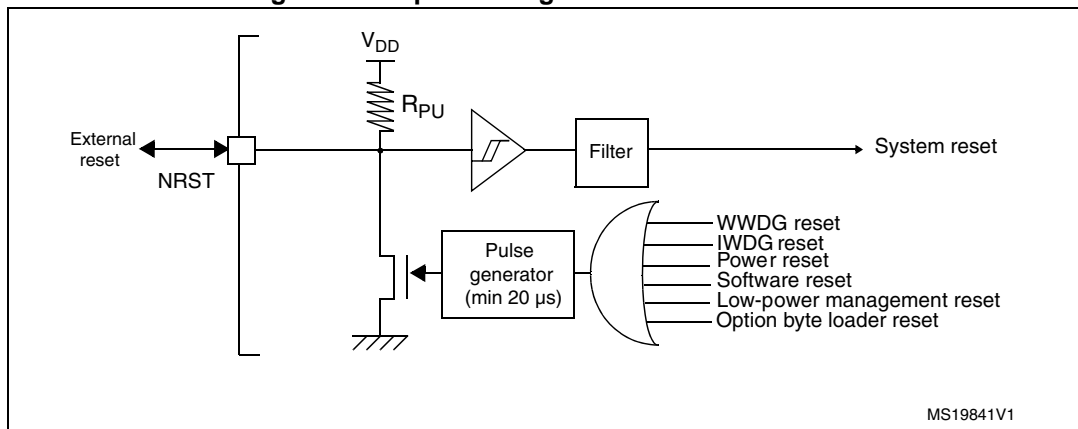
1. A low level on the NRST pin (external reset).
2. System window watchdog event (WWDG reset).
3. Independent watchdog event (IWDG reset).
4. A software reset (SW reset).
5. Low-power management reset.
6. Option byte loader reset.
7. Power reset

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR).

The RESET service routine vector is fixed at address 0x0000_0004 in the memory map.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 μ s for each internal reset source. In the case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

Figure 6. Simplified diagram of the reset circuit



For more details, please refer to the STM32F3xx reference manuals (RM0316, RM0313, RM0365 and RM0366).

Power reset

A power reset is generated when one of the following events occurs:

1. Power-on/power-down reset (POR/PDR reset)
2. When exiting Standby mode

Backup domain reset

The backup domain has two specific resets that affect only the backup domain. A backup domain reset is generated when one of the following events occurs:

1. Software reset, triggered by setting the BDRST bit in the Backup domain control register (RCC_BDCR).
2. V_{DD} or V_{BAT} power on, if both supplies have previously been powered off.

1.2.2 Power on reset (POR) / power down reset (PDR)

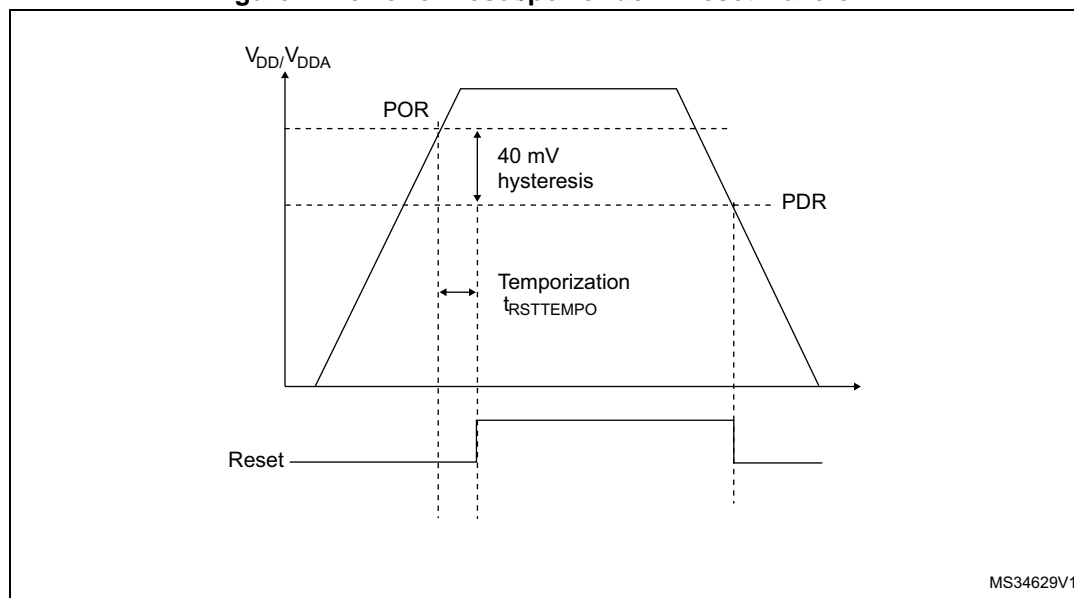
The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits which are always active and ensure proper operation above a threshold of 2 V.

The device remains in Reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase V_{DDA} must arrive first and be greater than or equal to V_{DD} .
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages. However, the V_{DDA} power supply supervisor can be disabled (by programming a dedicated option bit $V_{DDA_MONITOR}$) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD} .

For more details on the power on / power down reset threshold, refer to the electrical characteristics section in the datasheet.

Figure 7. Power on reset/power down reset waveform



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1.2.3 Programmable voltage detector (PVD)

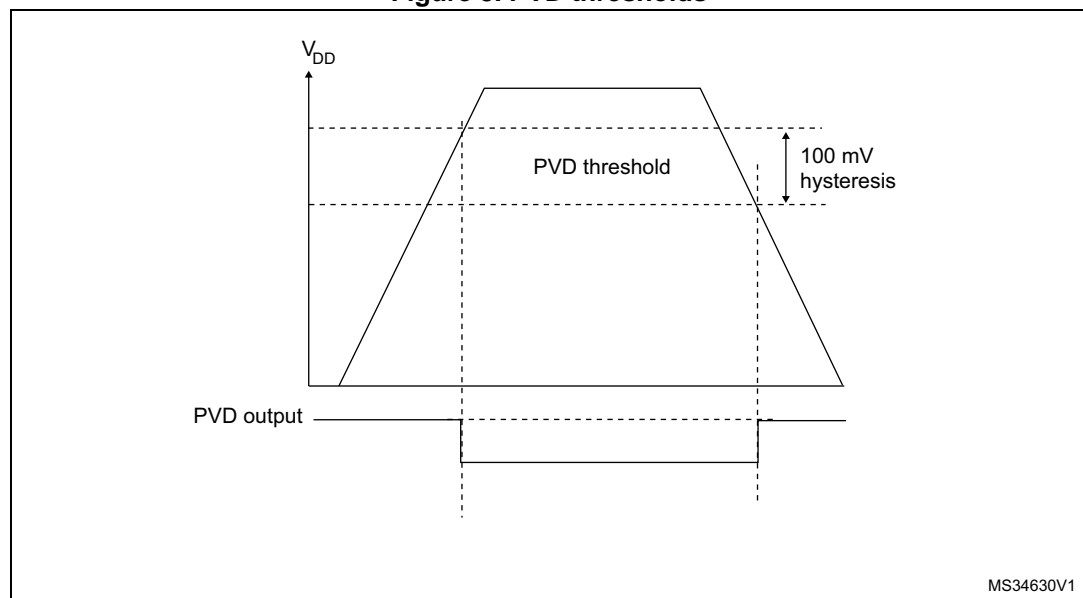
You can use the PVD to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the Power control register (PWR_CR).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the Power control/status register (PWR_CSR), to indicate if V_{DD} is higher or lower than the PVD threshold.

- This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers.
- The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example the service routine could perform emergency shutdown tasks.

Figure 8. PVD thresholds



2 Clocks

Three different clock sources can be used to drive the system clock (SYSCLK):

- HSI 8 MHz RC oscillator clock (high-speed internal clock signal)
- HSE oscillator clock (high-speed external clock signal)
- PLL clock

The devices have other secondary clock sources:

- 40 kHz low-speed internal RC (LSI RC) that drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption. Refer to the STM32F3xx reference manuals (RM0316, RM0313, RM0364, RM0365 and RM0366) for a description of the clock tree.

2.1 High speed external clock signal (HSE) OSC clock

The high speed external clock signal can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Figure 9. HSE/ LSE clock sources

| Clock source | Hardware configuration |
|----------------------------|------------------------|
| External clock | |
| Crystal/Ceramic resonators | |

External crystal/ceramic resonator (HSE crystal)

The 4 to 32 MHz external oscillator has the advantage of producing a very accurate rate on the main clock. Refer to the electrical characteristics section of the datasheet for more details about the associated hardware configuration.

The HSERDY flag in the Clock control register (RCC_CR) indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock interrupt register (RCC_CIR).

The HSE Crystal can be switched on and off using the HSEON bit in the Clock control register (RCC_CR).

External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 32 MHz. You select this mode by setting the HSEBYP and HSEON bits in the [Clock control register \(RCC_CR\)](#). The external clock signal (square, sinus or triangle) with ~40-60% duty cycle depending on the frequency (refer to the datasheet) has to drive the OSC_IN pin while the OSC_OUT pin can be used as a GPIO. See [Figure 9](#).

2.2 LSE clock

The LSE crystal is a 32.768 kHz Low Speed External crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in Backup domain control register (RCC_BDCR). The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in the Backup domain control register (RCC_BDCR) to obtain the best compromise between robustness and short start-up time on the one hand and low power consumption on the other.

The LSECRDY flag in the Backup domain control register (RCC_BDCR) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt register (RCC_CIR).

External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. You select this mode by setting the LSEBYP and LSEON bits in the Backup domain control register (RCC_BDCR). The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO. See [Figure 9](#).

2.3 HSI clock

The HSI clock signal is generated from an internal 8 MHz RC oscillator and can be used directly as a system clock or divided by 2 to be used as PLL input. The HSI RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration, the frequency is less accurate than an external crystal oscillator or ceramic resonator.

Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations. This is why each device is factory calibrated by ST for 1% accuracy at $T_A = 25\text{ }^{\circ}\text{C}$.

Furthermore, it is possible to route the HSI clock to the MCO multiplexer. The clock can then be the input to Timer 16 in all STM32F3 series devices (except the STM32F373 line where the clock is the input to Timer 14) to allow the user to calibrate the oscillator.

2.4 LSI clock

The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and RTC. The clock frequency is around 40 kHz (between 30 kHz and 60 kHz). For more details, refer to the electrical characteristics section of the datasheets.

2.5 Clock security system (CSS)

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the HSE oscillator clock, the oscillator is automatically disabled.
 - A clock failure event is sent to the break inputs of:
 - TIM1/8/15/16/17 in the STM32F303xB/C and STM32F358 devices.
 - TIM1/8/20/15/16/17 in the STM32F303xD/E and STM32F398 devices.
 - TIM1/15/16/17 in the STM32F301/302/303x6/8, STM32F302xB/C/D/E, STM32F334, STM323F318 and STM32F328 devices.
 - An interrupt is generated to inform the software about the failure (clock security system interrupt CSSI), allowing the MCU to perform recovery operations.
 - CSSI is linked to the Cortex[®]-M4 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator is used directly or indirectly as the system clock (indirectly means that it is used as the PLL input clock, and the PLL clock is used as the system clock), a detected failure causes a switch of the system clock to the HSI oscillator and the disabling of the external HSE oscillator. If the HSE oscillator clock (divided or not) is the clock entry of the PLL that is being used as a system clock when the failure occurs, the PLL is disabled too.

For details, see the STM32F3 reference manuals (RM0316, RM0313, RM0364, RM0365 and RM0366) available from STMicroelectronics website www.st.com.

3 Boot configuration

In the STM32F3xx, three different boot modes can be selected through the BOOT0 pin and nBOOT1 option bit, as shown in [Table 1](#).

Table 1. Boot modes

| Boot mode selection | | Boot mode | Aliasing |
|----------------------|-------|-------------------|---|
| BOOT1 ⁽¹⁾ | BOOT0 | | |
| x | 0 | Main Flash memory | Main Flash memory is selected as boot space |
| 0 | 1 | System memory | System memory is selected as boot space |
| 1 | 1 | Embedded SRAM | Embedded SRAM is selected as boot space |

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

The values on both BOOT0 pin and nBOOT1 bit are latched on the 4th rising edge of SYSCLK after a reset. The user must set nBOOT1 and BOOT0 to select the required boot mode.

The BOOT0 pin and nBOOT1 bit are also re-sampled when exiting from Standby mode. Consequently they must be kept in the required Boot mode configuration in Standby mode. After the startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main Flash memory, system memory or SRAM is accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from System memory: the system memory is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x1FFF EC00).
- Boot from embedded SRAM: the SRAM is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x2000 0000).

Note: In the STM32F3 series devices embedding a CCM RAM is not possible to boot from the CCM SRAM mapped at 0x1000 0000.

The embedded boot loader is located in the System memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following interfaces:

- USART1(PA9/PA10), USART2(PD5/PD6) or USB(PA11/PA12) on STM32F302/303xB/C devices,
- USART1(PA9/PA10), USART2(PA2/PA3) or USB(PA11/PA12) on STM32F301/302x6/8 and STM32F302/303xD/E devices,
- USART1 (PA9/PA10), USART2 (PA2/PA3), I2C1 (PB6/PB7) on STM32F303x6/8 and STM32F334 devices.
- USART1 (PA9/PA10), USART2 (PA2/PA3), I2C1 (PB6/PB7), I2C3 (PA8/PB5) on STM32F398 and F318 devices.

For additional information, refer to application note AN2606.

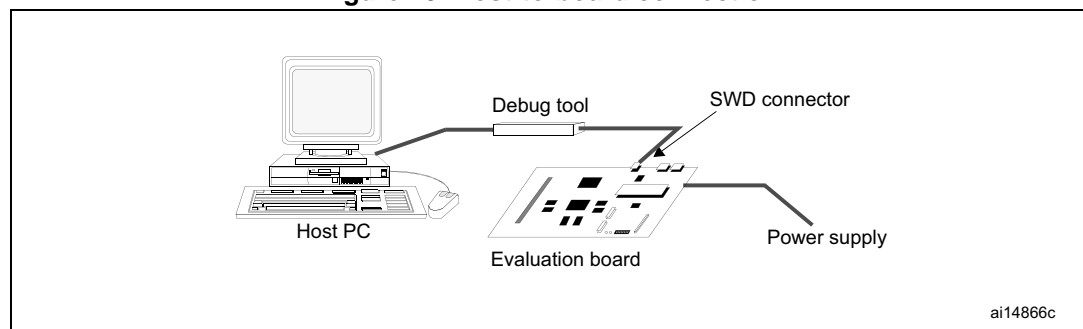
4 Debug management

4.1 Introduction

The Host/Target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SWD connector and a cable connecting the host to the debug tool.

Figure 10 shows the connection of the host to the STM32F3xx evaluation board.

Figure 10. Host-to-board connection



4.2 SWJ debug port (serial wire and JTAG)

The STM32F3 series core integrates the serial wire / JTAG debug port (SWJ-DP). It is an ARM® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

4.3 Pinout and debug port pins

The STM32F3 series MCU is offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

4.3.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as *alternate functions* of general-purpose I/Os (GPIOs). These pins, shown in [Table 2](#), are available on all packages.

Table 2. Debug port pin assignment

| SWJ-DP pin name | JTAG debug port | | SW debug port | | Pin assignment |
|-----------------|-----------------|--------------------------|---------------|------------------------------------|----------------|
| | Type | Description | Type | Debug assignment | |
| JTMS/SWDIO | I | JTAG test mode selection | I/O | Serial wire data input/output | PA13 |
| JTCK/SWCLK | I | JTAG test clock | I | Serial wire clock | PA14 |
| JTDI | I | JTAG test data input | - | - | PA15 |
| JTDO/TRACESWO | O | JTAG test data output | - | TRACESWO if async trace is enabled | PB3 |
| JNTRST | I | JTAG test nReset | - | - | PB4 |

4.3.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, some of the JTAG pins shown in [Table 3](#) can be configured to an alternate function through the GPIOx_AFRx registers.

Table 3. SWJ I/O pin availability

| Available Debug ports | SWJ I/O pin assigned | | | | |
|---|--|---------------------|-------------|------------|--------------|
| | PA13 / JTMS / SWDIO | PA14 / JTCK / SWCLK | PA15 / JTDI | PB3 / JTDO | PB4 / JNTRST |
| Full SWJ (JTAG-DP + SW-DP) - reset state | X | X | X | X | X |
| Full SWJ (JTAG-DP + SW-DP) but without JNTRST | X | X | X | X | |
| JTAG-DP disabled and SW-DP enabled | X | X | | | |
| JTAG-DP disabled and SW-DP disabled | Free to be configured as alternate functions | | | | |

[Table 3](#) shows the different possibilities to free some pins to be configured alternate functions.

For more details, see the corresponding STM32F3xx reference manual (RM0316, RM0313, RM0365 and RM0366) available from the STMicroelectronics website www.st.com.

4.3.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must *not* be floating since they are directly connected to flip-flops to control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32F3xx embeds internal pull-up and pull-down resistors on JTAG input pins:

- JNTRST: Internal pull-up
- JTDI: Internal pull-up
- JTMS/SWDIO: Internal pull-up
- TCK/SWCLK: Internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the equivalent state:

- JNTRST: Input pull-up
- JTDI: Input pull-up
- JTMS/SWDIO: Input pull-up
- JTCK/SWCLK: Input pull-down
- JTDO: Input floating

The software can then use these I/Os as standard GPIOs.

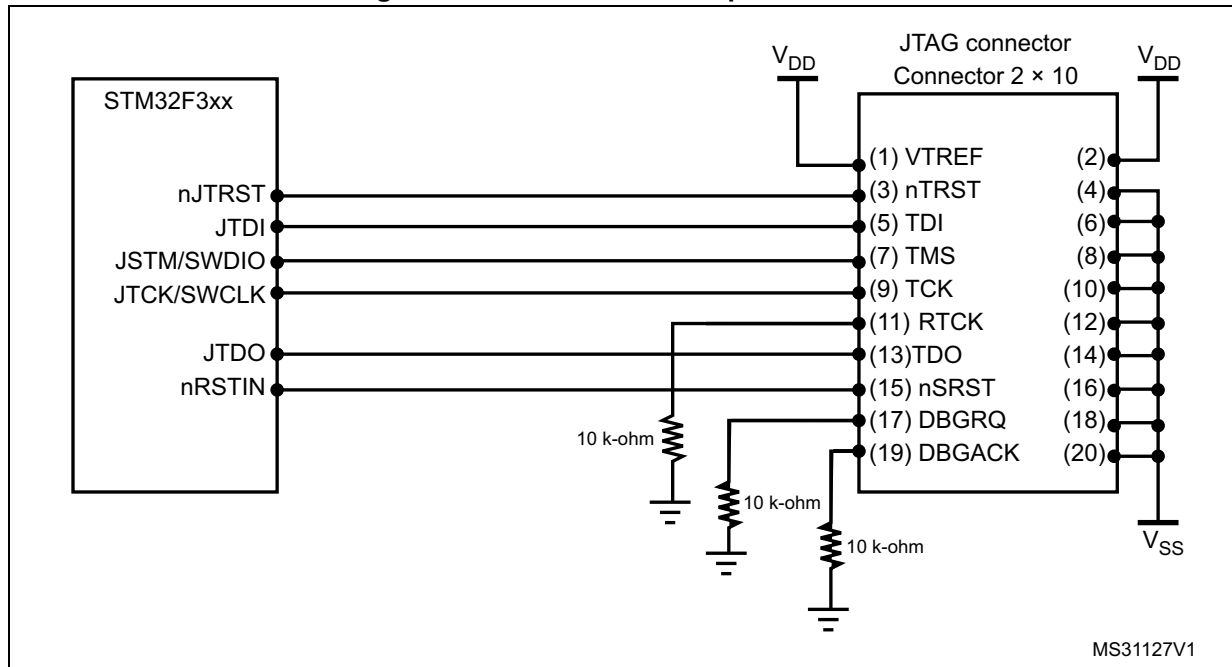
Note: The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but there is no special recommendation for TCK. However, for the STM32F3xx, an integrated pull-down resistor is used for JTCK.

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

4.3.4 SWJ debug port connection with standard JTAG connector

Figure 11 shows the connection between the STM32F3xx and a standard JTAG connector.

Figure 11. JTAG connector implementation



5 Recommendations

5.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economic reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

5.2 Component position

A preliminary layout of the PCB must make separate circuits:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution. This will reduce cross-coupling on the PCB that introduces noise

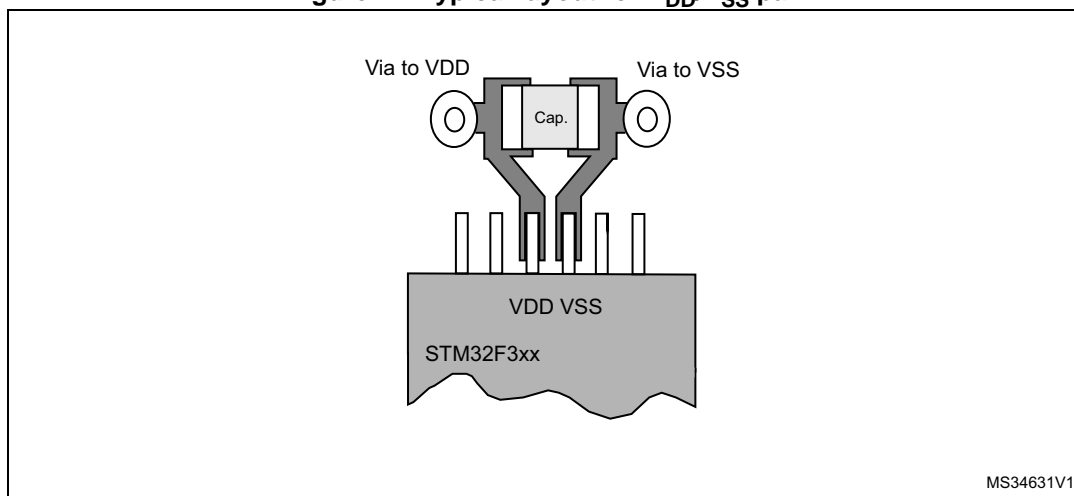
5.3 Ground and power supply (V_{SS} , V_{DD} , V_{SSA} , V_{DDA} , V_{SSSD} , V_{DDSD})

All blocks such as, for example noisy, low-level sensitive and digital should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the area of the supply loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

5.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with 100 nF filtering ceramic capacitors and a chemical capacitor of about 4.7 μ F connected between the supply pins of the STM32F3xx device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. [Figure 12](#) shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 12. Typical layout for V_{DD}/V_{SS} pair

MS34631V1

5.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (such as interrupts and handshaking strobe signals, but not LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
- Digital signals: the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (clock, etc.)
- Sensitive signals (high impedance, etc.)

5.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, unused clocks, counters or I/Os, should not be left free. I/Os should be connected to a fixed logic level of 0 or 1 by an external or internal pull-up or pull-down on the unused I/O pin. The other option is to configure GPIO as output mode using software. Unused features should be frozen or disabled, which is their default value.

6 STM32F3x8 vs STM32F30x/F373

The previous sections are also valid for STM32F3x8 devices (where the internal voltage regulator is bypassed), however the following differences in comparison with STM32F30x and STM32F373 devices need to be taken into account.

- STM32F3x8 devices require a 1.8 V +/- 8% operating voltage supply (VDD) and 1.65 V - 3.6 V analog voltage supply (VDDA). The embedded regulator is OFF and VDD directly supplies the regulator output. The voltage regulator is bypassed and the microcontroller must be powered from a nominal VDD = 1.8 V ± 8% voltage.
- In STM32F3x8 devices, the PB2 I/O (or PB7 I/O, depending on the product and package) is not available and is replaced by the NPOR functionality used for power-on reset. To guarantee a proper power-on reset, the NPOR pin must be held low when VDDA is applied. When VDD is stable, the reset state can be exited by putting the NPOR pin in high impedance. The NPOR pin has an internal pull-up which holds this input to VDDA.
- In STM32F3x8 devices, the POR, PDR and PVD features are not available.
- In STM32F3x8 devices, Standby mode is not available. Stop mode is still available but it is meaningless to distinguish between voltage regulator in Low power mode and voltage regulator in Run mode because the regulator is not used and VDD is applied externally to the regulator output.
- In STM32F3x8 devices USB is not available.
- In STM32F3x8 devices, the bootloader interfaces are different from the ones in devices with internal regulator on. Please refer to the Table 5 for details.

The table below summarizes the differences between the F30x/F37x and F3x8.

Table 4. STM32F30x/F373 versus STM32F3x8

| Feature | STM32F30x/F373 | STM32F3x8 |
|--|---|---|
| Digital supply VDD | 2 - 3.6V | 1.8V +/- 8% |
| Analog supply VDDA | 2 - 3.6V | 1.65 - 3.6V |
| Internal Regulator status | Enabled. Used to supply the internal 1.8V digital power. | Disabled. VDD directly supplies the regulator output. |
| POR/PDR/PVD | Available | Not available |
| Standby mode | Available | Not available |
| VDDA and VDDSD ⁽¹⁾ monitoring | Available | Not available |
| STOP mode | With voltage regulator in Low power mode or Run mode. | It is meaningless to distinguish between voltage regulator in Low power mode and voltage regulator in Run mode because the regulator is not used and VDD is applied externally to the regulator output. |
| USB | Available | Not available |

Table 4. STM32F30x/F373 versus STM32F3x8 (continued)

| Feature | STM32F30x/F373 | STM32F3x8 |
|--|--|--|
| PB2 GPIO (or PB7 GPIO depending on the product and package) | Available | Not available. It is replaced by the NPOR functionality used for power-on reset. |
| Bootloader COM interfaces | <p>F30xB/C and F37x: USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).</p> <p>F30xx6/8/D/E:USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).</p> <p>F303x6/8 and F334x6/8:USART1 (PA9/PA10), USART2 (PA2/PA3) or I2C1 (PB6/PB7).</p> | <p>F358xx and F378xx: USART1 (PA9/PA10), USART2 (PD5/PD6) or I2C1 (PB6/PB7)</p> <p>F328xx:USART1 (PA9/PA10), USART2 (PA2/PA3) or I2C1 (PB6/PB7)</p> <p>F318xx/F398xx:USART1 (PA9/PA10), USART2 (PA2/PA3) or I2C1 (PB6/PB7) or I2C3 (PA8,PB5)</p> |

1. VDDSD on STM32F373 only.

7 Reference design

7.1 Description

The reference design shown in [Figure 13](#), is based on the STM32F3xx, a highly integrated microcontroller running at 72 MHz, that combines the Cortex®-M4 FPU 32-bit RISC CPU core with embedded Flash and SRAM memories.

This reference design can be tailored to any other STM32F3xx device with a different package, using the pins correspondence given in the corresponding datasheet.

7.1.1 Clock

Two clock sources are used by the microcontroller:

- LSE: X1– 32.768 kHz crystal for the embedded RTC
- HSE: X2– 8 MHz crystal for the STM32F3xx microcontroller

Refer to [Section 2: Clocks on page 16](#).

7.1.2 Reset

The reset signal in [Figure 13](#) is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1.

Refer to [Section 1.2: Reset and power supply supervisor on page 13](#).

7.1.3 Boot mode

The boot option is configured by setting switch SW1 (Boot 0) and option bit nBoot1. Refer to [Section 3: Boot configuration on page 19](#).

7.1.4 SWJ interface

The reference design shows the connection between the STM32F3xx and a standard JTAG connector. Refer to [Section 4: Debug management on page 20](#).

Note: It is recommended to connect the reset pins so as to be able to reset the application from the development tools.

7.1.5 Power supply

Refer to [Section 1: Power supplies on page 6](#).

7.1.6 Pinouts and pin descriptions

Please refer the corresponding STM32F3xx datasheet available on ww.st.com for the pinout and pin description.

7.2 Component references

Table 5. Mandatory components

| Component | Value | Reference | Quantity | Comments |
|-----------------|-------------|---|---|--|
| Microcontroller | - | STM32F303VCT/ STM32F358VCT6 STM32F373VCT6/ STM32F378VCT6 | 1 | 100-pin package |
| Capacitor | 100 nF | C3/C5/C7/C9 | 4 for STM32F303 3 for STM32F373 3 for STM32F378 | Ceramic capacitors (decoupling capacitors) |
| Capacitor | 4.7 μ F | C1 | 1 | Ceramic capacitor (decoupling capacitor) |
| Capacitor | 1 μ F | C2/C11 | 2 | Used for VDDA and VREF+ |
| Capacitor | 10 nF | C4/C13 | 2 | Ceramic capacitor (decoupling capacitor) |
| Capacitor | 10 nF | C8/C12/C13 | 3 | Ceramic capacitors for VDDSDx and VREFSD+ (STM32F373 only) |
| Capacitor | 1 μ F | C6/C10/C19 | 3 | Used for VDDSDx and VREFSD+ (STM32F373 only) |

Table 6. Optional components

| Component | Value | Reference | Quantity | Comments |
|-----------|---------------|----------------|----------|--|
| Resistor | 390 Ω | R4 | 1 | Used for HSE: the value depends on the crystal characteristics. This value is given only as a typical example. |
| Resistor | 0 Ω | R6 | 1 | Used for LSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example. |
| Resistor | 10 K Ω | R5/R12/R13/R14 | 4 | Pull up and pull down for JTAG and Boot mode. |
| Capacitor | 100 nF | C16 | 1 | Ceramic capacitors for RESET button. |
| Capacitor | 10 pF | C17/C18 | 2 | Used for LSE: the value depends on the crystal characteristics. |
| Capacitor | 20 pF | C14/C15 | 2 | Used for HSE: the value depends on the crystal characteristics. |
| Quartz | 8 MHz | X1 | 1 | Used for HSE |
| Quartz | 32 kHz | X2 | 1 | Used for LSE |
| Battery | 3V3 | BT1 | 1 | If no external battery is used in the application, it is recommended to connect V _{BAT} externally to V _{DD} |
| Switch | - | SW1 | 1 | Used to select the correct boot mode. |

Table 6. Optional components (continued)

| Component | Value | Reference | Quantity | Comments |
|----------------|-------|-----------|----------|------------------------------------|
| Push-button | - | B1 | 1 | Used as reset button |
| JTAG connector | - | CN1 | 1 | Used for MCU programming/debugging |

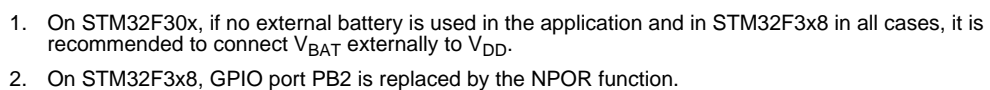
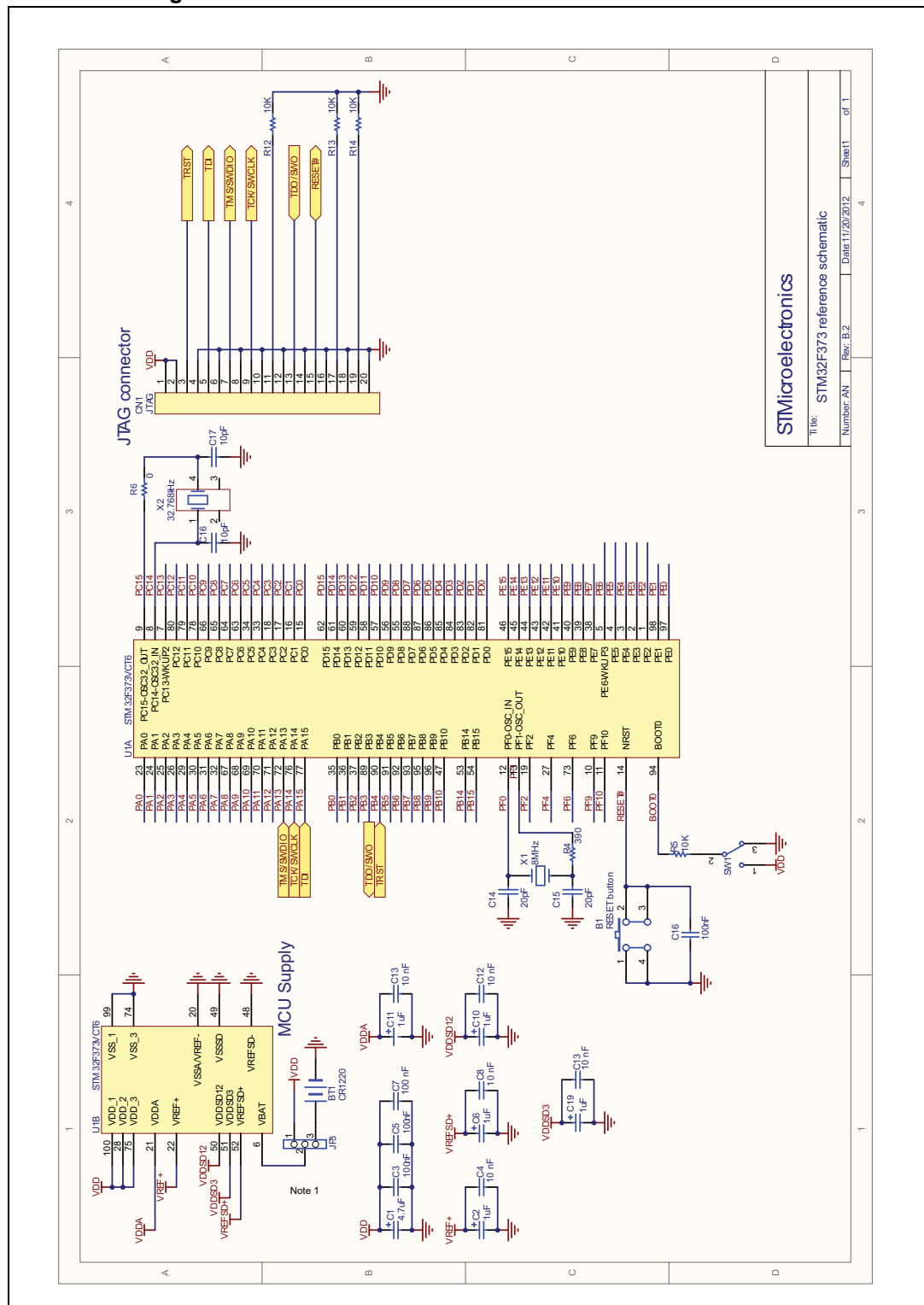


Figure 14. STM32F373 microcontroller reference schematic



1. On STM32F373, if no external battery is used in the application and in STM32F378 in all cases, it is recommended to connect V_{BAT} externally to V_{DD} .
2. On STM32F378, GPIO port PB2 is replaced by the NPOR function.

8 Revision history

Table 7. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 11-Dec-2012 | 1 | Initial release. |
| 27-Mar-2014 | 2 | Modified Introduction . Modified the list of applicable products in Table 1 on the cover page. Added Figure 4 . Modified Chapter 6 and Section 7.1 . |
| 14-Apr-2014 | 3 | Removed any reference to STM32F301x4, STM32F302x4, STM32F303x4 (i.e. part numbers with 16KBytes of flash). Modified Section 6 . Modified Table 4 . |
| 25-Feb-2015 | 4 | Extended the applicability to STM32F303xD/E, STM32F302xD/E and STM32F398VE devices. Removed the Table 1 on the cover page "List of applicable products" as the document applies to the whole STM32F3 series. Updated: <ul style="list-style-type: none"> – Section 1.1: Power supply schemes, – Section 2.3: HSI clock, – Section 2.5: Clock security system (CSS), – Section 3: Boot configuration, – Section 6: STM32F3x8 vs STM32F30x/F373, – Section 7.2: Component references, – Figure 13: STM32F30x microcontroller reference schematic, – Figure 14: STM32F373 microcontroller reference schematic. |

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