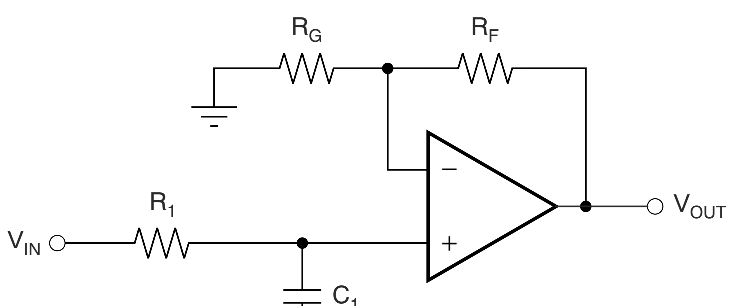
Industry-Standard Dual Operational Amplifiers

1 Features

- Wide supply range of 3 V to 36 V (B version)
- Quiescent current: 300 µA per amplifier (B version, typical)
- Unity-gain bandwidth of 1.2 MHz (B version)
- Common-mode input voltage range includes ground, enabling direct sensing near ground
- Low input offset voltage of 3 mV at 25°C (A and B versions, maximum)
- Internal RF and EMI filter (B version)
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Merchant network and server power supply units
- Multi-function printers
- Power supplies and mobile chargers
- Motor control: AC induction, brushed DC, brushless DC, high-voltage, low-voltage, permanent magnet, and stepper motor
- Desktop PC and motherboard
- Indoor and outdoor air conditioners
- Washers, dryers, and refrigerators
- AC inverters, string inverters, central inverters, and voltage frequency drives
- Uninterruptible power supplies
- Programmable logic controllers
- Electronic point-of-sale systems



$$f_{-3\ dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

3 Description

The LM358B and LM2904B devices are the next-generation versions of the industry-standard operational amplifiers (op amps) LM358 and LM2904, which include two high-voltage (36 V) op amps. These devices provide outstanding value for cost-sensitive applications, with features including low offset (300 µV, typical), common-mode input range to ground, and high differential input voltage capability.

The LM358B and LM2904B op amps simplify circuit design with enhanced features such as unity-gain stability, lower offset voltage of 3 mV (maximum at room temperature), and lower quiescent current of 300 µA per amplifier (typical). High ESD (2 kV, HBM) and integrated EMI and RF filters enable the LM358B and LM2904B devices to be used in the most rugged, environmentally challenging applications.

The LM358B and LM2904B amplifiers are available in micro-sized packaging, such as the SOT23-8, as well as industry standard packages including SOIC, TSSOP, and VSSOP.

Device Information

PART NUMBER[1]	PACKAGE	BODY SIZE (NOM)
LM358B, LM2904B, LM358, LM358A, LM2904, LM2904V, LM258, LM258A	SOIC (8)	4.90 mm × 3.90 mm
LM358B, LM2904B, LM358, LM358A, LM2904, LM2490V	TSSOP (8)	3.00 mm × 4.40 mm
LM358B, LM2904B, LM358, LM358A, LM2904, LM2904V, LM258, LM258A	VSSOP (8)	3.00 mm × 3.00 mm
LM358B, LM2904B	SOT-23 (8)	2.90 mm × 1.60 mm
LM358, LM2904	SO (8)	5.20 mm × 5.30 mm
LM358, LM2904, LM358A, LM258, LM258A	PDIP (8)	9.81 mm × 6.35 mm
LM158, LM158A	CDIP (8)	9.60 mm × 6.67 mm
LM158, LM158A	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Y (February 2021) to Revision Z (July 2021) — **Page**

- Deleted preview tag from LM358B and LM2904B SOT-23 (8) package in *Device Information* table.......... 1
- Updated DDF (SOT-23) package thermal information in the *Thermal Information* table.......... 7
- Deleted *Related Links* from the *Device and Documentation Support* section.......... 32

Changes from Revision X (June 2020) to Revision Y (February 2021) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.......... 1
- Added SOT23-8 (DDF) package information throughout data sheet.......... 1
- Deleted preview tag from LM358B and LM2904B VSSOP (8) package in *Device Information* table.......... 1
- Added SOT23-8 (DDF) package information to *Device Comparison Table*.......... 4
- Added SOT23-8 (DDF) package information to the *Pin Configuration and Functions* section.......... 5
- Added DDF (SOT-23) package to the *Thermal Information* table.......... 7

Changes from Revision W (October 2019) to Revision X (June 2020) — **Page**

- Added application links to *Applications* section.......... 1
- Deleted preview tag from LM358B and LM2904B TSSOP (8) package in *Device Information* table.......... 1

Changes from Revision V (September 2018) to Revision W (October 2019) — **Page**

- Added specification in the *Device Comparison Table*.......... 4
- Changed CDM ESD rating for LM358B and LM2904B in *ESD Ratings*.......... 6
- Changed V_S to V+ in *Recommended Operating Conditions*.......... 7
- Changed *Thermal Information* for the LM158FK and LM158JG devices.......... 7
- Added *Typical Characteristics* section for the LM358B and LM2490B op amps.......... 17

Changes from Revision U (January 2017) to Revision V (September 2018)	Page

Changes from Revision T (April 2015) to Revision U ()	Page

Changes from Revision S (January 2014) to Revision T (April 2015)	Page

Changes from Revision R (July 2010) to Revision S (Jauary 2014)	Page

5 Device Comparison Table

PART NUMBER	SUPPLY VOLTAGE	TEMPERATURE RANGE	V_{OS} (MAXIMUM AT 25°C)	I_Q / CH (TYPICAL AT 25°C)	INTEGRATED EMI FILTER	PACKAGE
LM358B	3 V–36 V	–40°C to 85°C	3 mV	300 µA	Yes	D, DDF, DGK, PW
LM2904B	3 V–36 V	–40°C to 125°C	3 mV	300 µA	Yes	D, DDF, DGK, PW
LM358	3 V–32 V	0°C to 70°C	7 mV	350 µA	No	D, PW, DGK, P, PS
LM2904	3 V–26 V	–40°C to 125°C	7 mV	350 µA	No	D, PW, DGK, P, PS
LM358A	3 V–32 V	0°C to 70°C	3 mV	350 µA	No	D, PW, DGK, P
LM2904V	3 V–32 V	–40°C to 125°C	7 mV	350 µA	No	D, PW
LM158	3 V–32 V	–55°C to 125°C	5 mV	350 µA	No	JG, FK
LM158A	3 V–32 V	–55°C to 125°C	3 mV	350 µA	No	JG, FK
LM258	3 V–32 V	–25°C to 85°C	5 mV	350 µA	No	D, DGK, P
LM258A	3 V–32 V	–25°C to 85°C	3 mV	350 µA	No	D, DGK, P

6 Pin Configuration and Functions

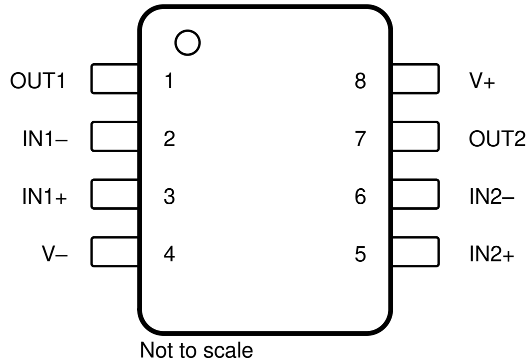
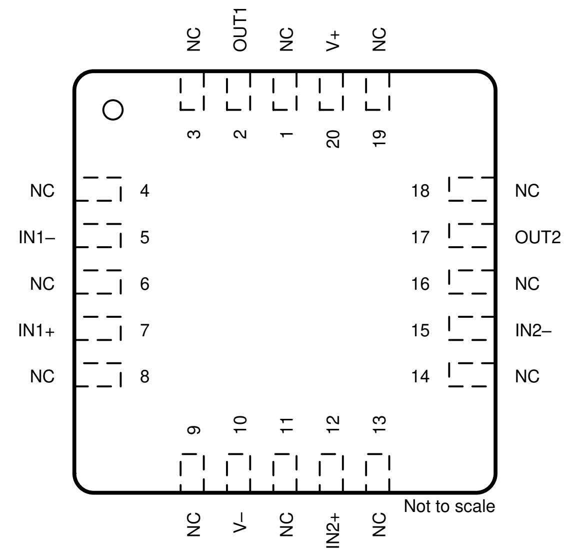


Figure 6-1. D, DDF, DGK, P, PS, PW, and JG Package 8-Pin SOIC, SOT23-8, VSSOP, PDIP, SO, TSSOP, and CDIP Top View



NC - No internal connection

Figure 6-2. FK Package 20-Pin LCCC Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	LCCC(1)	SOIC, SOT23-8, VSSOP, CDIP, PDIP, SO, TSSOP, CFP(1)		
IN1–	5	2	I	Negative input
IN1+	7	3	I	Positive input
IN2–	15	6	I	Negative input
IN2+	12	5	I	Positive input
OUT1	2	1	O	Output
OUT2	17	7	O	Output
V–	10	4	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	—	No internal connection
V+	20	8	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see Section 5.

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage, V_S = ([V+] – [V–])		LM358B, LM358BA, LM2904B, LM2904BA		±20 or 40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V		±16 or 32	
		LM2904		±13 or 26	
Differential input voltage, V_{ID} [2]		LM358B, LM358BA, LM2904B, LM2904BA,LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	–32	32	V
		LM2904	–26	26	
Input voltage, V_I	Either input	LM358B, LM358BA, LM2904B, LM2904BA	–0.3	40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	–0.3	32	
		LM2904	–0.3	26	
Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, V_S ≤ 15 V[3]				Unlimited	s
Operating ambient temperature, T_A		LM158, LM158A	–55	125	°C
		LM258, LM258A	–25	85	
		LM358B, LM358BA	–40	85	
		LM358, LM358A	0	70	
		LM2904B, LM2904BA, LM2904, LM2904V	–40	125	
Operating virtual-junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential voltages are at IN+, with respect to IN−.
(3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction.

7.2 ESD Ratings

			VALUE	UNIT
LM358B, LM358BA, LM2904B, AND LM2904BA				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
LM158, LM258, LM358, LM158, LM258A, LM358A, LM2904, AND LM2904V				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S= ([V+] – [V–])	LM358B, LM358BA, LM2904B, LM2904BA	3	36	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	3	30	
		LM2904	3	26	
V_{CM}	Common-mode voltage		V–	V+ – 2	V
T_A	Operating ambient temperature	LM358B, LM358BA	–40	85	°C
		LM2904B, LM2904BA, LM2904, LM2904V	–40	125	
		LM358, LM358A	0	70	
		LM258, LM258A	–20	85	
		LM158, LM158A	–55	125	

7.4 Thermal Information

THERMAL METRIC(1)		LM258, LM258A, LM358, LM358A, LM358B, LM358BA, LM2904, LM2904B, LM2904BA, LM2904V(2)						LM158, LM158A		UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8PINS	20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.7	181.4	80.9	116.9	171.7	164.3	84.0	112.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.9	69.4	70.4	62.5	68.8	98.1	56.9	63.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.9	102.9	57.4	68.6	99.2	82.1	57.5	100.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.2	11.8	40	21.9	11.5	11.4	51.7	35.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.2	101.2	56.9	67.6	97.9	81.7	57.1	93.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	10.6	22.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) For a listing of which devices are available in what packages, see Section 5.

7.5 Electrical Characteristics: LM358B and LM358BA

V_S = (V+) – (V–) = 5 V – 36 V (±2.5 V – ±18 V), T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10k connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	LM358B				±0.3	±3.0	mV
				T_A = –40°C to +85°C			±4	mV
		LM358BA					±2.0	mV
				T_A = –40°C to +85°C			±2.5	mV
dV_{OS}/d_T	Input offset voltage drift			T_A = -40°C to +85°C[1]		±3.5	11	μV/°C
PSRR	Power supply rejection ratio					±2	15	μV/V
	Channel separation, dc	f = 1 kHz to 20 kHz				±1		μV/V
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 3 V to 36 V			(V–)		(V+) – 1.5	V
		V_S = 5 V to 36 V		T_A = –40°C to +85°C	(V–)		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+) – 1.5 V	V_S = 3 V to 36 V			20	100	μV/V
		(V–) ≤ V_{CM} ≤ (V+) – 2.0 V	V_S = 5 V to 36 V	T_A = –40°C to +85°C		25	316	
INPUT BIAS CURRENT								
I_B	Input bias current					±10	±35	nA
				T_A = –40°C to +85°C[1]			±50	nA
I_{OS}	Input offset current					0.5	4	nA
				T_A = –40°C to +85°C[1]			5	nA
dI_{OS}/d_T	Input offset current drift			T_A = –40°C to +85°C		10		pA/°C
NOISE								
E_n	Input voltage noise	f = 0.1 to 10 Hz				3		$μV_{PP}$
e_n	Input voltage noise density	f = 1 kHz				40		nV/√Hz
INPUT IMPEDANCE								
Z_{ID}	Differential					10 || 0.1		MΩ|| pF
Z_{IC}	Common-mode					4 || 1.5		GΩ|| pF
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V; V_O = 1 V to 11 V; R_L ≥ 10 kΩ, connected to (V–)			70	140		V/mV
				T_A = –40°C to +85°C	35			V/mV
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					1.2		MHz
SR	Slew rate	G = + 1				0.5		V/μs
$Θ_m$	Phase margin	G = + 1, R_L = 10kΩ, C_L = 20 pF				56		°
t_{OR}	Overload recovery time	V_{IN} × gain > V_S				10		μs
t_s	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF				4		μs
THD+N	Total harmonic distortion + noise	G = + 1, f = 1 kHz, V_O = 3.53 V_{RMS}, V_S = 36 V, R_L = 100k, I_{OUT} ≤ ±50 μA, BW = 80 kHz				0.001		%
OUTPUT								
V_O	Voltage output swing from rail	Positive rail (V+)		I_{OUT} = 50 μA		1.35	1.42	V
				I_{OUT} = 1 mA		1.4	1.48	V
				I_{OUT} = 5 mA[1]		1.5	1.61	V
		Negative rail (V–)		I_{OUT} = 50 μA		100	150	mV
				I_{OUT} = 1 mA		0.75	1	V
			V_S = 5 V, RL ≤ 10 kΩ connected to (V–)	T_A = –40°C to +85°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = V–; V_{ID} = 1 V	Source[1]		-20	-30		mA
				T_A = –40°C to +85°C	-10			
		V_S = 15 V; V_O = V+; V_{ID} = –1 V	Sink[1]		10	20		
				T_A = –40°C to +85°C	5			
		V_{ID} = –1 V; V_O = (V–) + 200 mV			60	100		μA
I_{SC}	Short-circuit current	V_S = 20 V, (V+) = 10 V, (V–) = –10 V, V_O = 0 V				±40	±60	mA
C_{LOAD}	Capacitive load drive					100		pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A				300		Ω

7.5 Electrical Characteristics: LM358B and LM358BA (continued)

V_S = (V+) – (V–) = 5 V – 36 V (±2.5 V – ±18 V), T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10k connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5 V; I_O = 0 A	T_A = –40°C to +85°C		300	460	µA
I_Q	Quiescent current per amplifier	V_S = 36 V; I_O = 0 A				800	µA

(1) Specified by characterization only.

7.6 Electrical Characteristics: LM2904B and LM2904BA

V_S = (V+) – (V–) = 5 V – 36 V (±2.5 V – ±18 V), T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10k connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	LM2904B				±0.3	±3.0	mV
		LM2904B		T_A = –40°C to +125°C			±4	mV
		LM2904BA					±2.0	mV
		LM2904BA		T_A = –40°C to +125°C			±2.5	mV
dV_{OS}/d_T	Input offset voltage drift			T_A = –40°C to +125°C(1)		±3.5	12	µV/°C
PSRR	Power supply rejection ratio					±2	15	µV/V
	Channel separation, dc	f = 1 kHz to 20 kHz				±1		µV/V
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 3 V to 36 V			(V–)		(V+) – 1.5	V
		V_S = 5 V to 36 V		T_A = –40°C to +125°C	(V–)		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+) – 1.5 V	V_S = 3 V to 36 V			20	100	µV/V
		(V–) ≤ V_{CM} ≤ (V+) – 2.0 V	V_S = 5 V to 36 V	T_A = –40°C to +125°C		25	316	µV/V
INPUT BIAS CURRENT								
I_B	Input bias current					±10	±35	nA
				T_A = –40°C to +125°C(1)			±50	nA
I_{OS}	Input offset current					0.5	4	nA
				T_A = –40°C to +125°C(1)			5	nA
dI_{OS}/d_T	Input offset current drift			T_A = –40°C to +125°C		10		pA/℃
NOISE								
E_n	Input voltage noise	f = 0.1 to 10 Hz				3		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz				40		nV/√Hz
INPUT IMPEDANCE								
Z_{ID}	Differential					10 || 0.1		MΩ|| pF
Z_{IC}	Common-mode					4 || 1.5		GΩ|| pF
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V; V_O = 1 V to 11 V; R_L ≥ 10 kΩ, connected to (V–)			70	140		V/mV
		V_S = 15 V; V_O = 1 V to 11 V; R_L ≥ 10 kΩ, connected to (V–)		T_A = –40°C to +125°C	35			V/mV
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					1.2		MHz
SR	Slew rate	G = + 1				0.5		V/µs
Θ_m	Phase margin	G = + 1, R_L = 10kΩ, C_L = 20 pF				56		°
t_{OR}	Overload recovery time	V_{IN} × gain > V_S				10		µs
t_s	Settling time	To 0.1%, V_S = 5 V, 2-V Step , G = +1, C_L = 100 pF				4		µs
THD+N	Total harmonic distortion + noise	G = + 1, f = 1 kHz, V_O = 3.53 V_{RMS}, V_S = 36 V, R_L = 100k, I_{OUT} ≤ ±50 µA, BW = 80 kHz				0.001		%
OUTPUT								
V_O	Voltage output swing from rail	Positive rail (V+)		I_{OUT} = 50 µA		1.35	1.42	V
		Positive rail (V+)		I_{OUT} = 1 mA		1.4	1.48	V
		Positive rail (V+)		I_{OUT} = 5 mA(1)		1.5	1.61	V
		Negative rail (V–)		I_{OUT} = 50 µA		100	150	mV
		Negative rail (V–)		I_{OUT} = 1 mA		0.75	1	V
		Negative rail (V–)	V_S = 5 V, RL ≤ 10 kΩ connected to (V–)	T_A = –40°C to +125°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = V–; V_{ID} = 1 V	Source(1)		–20	–30		mA
		V_S = 15 V; V_O = V–; V_{ID} = 1 V	Source(1)	T_A = –40°C to +125°C	–10			mA
		V_S = 15 V; V_O = V+; V_{ID} = –1 V	Sink(1)		10	20		mA
		V_S = 15 V; V_O = V+; V_{ID} = –1 V	Sink(1)	T_A = –40°C to +125°C	5			mA
		V_{ID} = –1 V; V_O = (V–) + 200 mV			60	100		µA
I_{SC}	Short-circuit current	V_S = 20 V, (V+) = 10 V, (V–) = –10 V, V_O = 0 V				±40	±60	mA
C_{LOAD}	Capacitive load drive					100		pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A				300		Ω

7.6 Electrical Characteristics: LM2904B and LM2904BA (continued)

V_S = (V+) – (V–) = 5 V – 36 V (±2.5 V – ±18 V), T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, R_L = 10k connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5 V; I_O = 0 A	T_A = –40°C to +125°C		300	460	µA
I_Q	Quiescent current per amplifier	V_S = 36 V; I_O = 0 A				800	µA

(1) Specified by characterization only.

7.7 Electrical Characteristics: LM358, LM358A

For V_S = (V+) – (V–) = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP[2]	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	V_S = 5 V to 30 V; V_{CM} = 0 V; V_O = 1.4 V	LM358			3	7	mV
			LM358	T_A = 0°C to 70°C			9	
			LM358A			2	3	
			LM358A	T_A = 0°C to 70°C			5	
dV_{OS}/d_T	Input offset voltage drift		LM358	T_A = 0°C to 70°C		7		µV/°C
			LM358A	T_A = 0°C to 70°C		7	20	
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	V_S = 5 V to 30 V			65	100		dB
V_{O1}/V_{O2}	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 5 V to 30 V	LM358		(V–)		(V+) – 1.5	V
		V_S = 30 V	LM358A					
		V_S = 5 V to 30 V	LM358	T_A = 0°C to 70°C	(V–)		(V+) – 2	
		V_S = 30 V	LM358A					
CMRR	Common-mode rejection ratio	V_S = 5 V to 30 V; V_{CM} = 0 V			65	80		dB
INPUT BIAS CURRENT								
I_B	Input bias current	V_O = 1.4 V	LM358			–20	–250	nA
			LM358	T_A = 0°C to 70°C			–500	
			LM358A			–15	–100	
			LM358A	T_A = 0°C to 70°C			–200	
I_{OS}	Input offset current	V_O = 1.4 V	LM358			2	50	nA
			LM358	T_A = 0°C to 70°C			150	
			LM358A			2	30	
			LM358A	T_A = 0°C to 70°C			75	
dI_{OS}/d_T	Input offset current drift					10		pA/°C
			LM358A	T_A = 0°C to 70°C			300	
NOISE								
e_n	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V; V_O = 1 V to 11 V; R_L ≥ 2 kΩ			25	100		V/mV
				T_A = 0°C to 70°C	15			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	G = +1				0.3		V/µs
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	V_S = 30 V; R_L = 2 kΩ	T_A = 0°C to 70°C			4	V
		Positive rail	V_S = 30 V; R_L ≥ 10 kΩ			2	3	
		Positive rail	V_S = 5 V; R_L ≥ 2 kΩ				1.5	
		Negative rail	V_S = 5 V; R_L ≤ 10 kΩ	T_A = 0°C to 70°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = 0 V; V_{ID} = 1 V	Source		–20	–30		mA
			Source	LM358A			–60	
			Source	T_A = 0°C to 70°C	–10			
		V_S = 15 V; V_O = 15 V; V_{ID} = –1 V	Sink		10	20		
			Sink	T_A = 0°C to 70°C	5			
		V_{ID} = –1 V; V_O = 200 mV			12	30		µA
I_{SC}	Short-circuit current	V_S = 10 V; V_O = V_S / 2				±40	±60	mA
POWER SUPPLY								
I_Q	Quiescent current per amplifier	V_O = 2.5 V; I_O = 0 A		T_A = 0°C to 70°C		350	600	µA
		V_S = 30 V; V_O = 15 V; I_O = 0 A		T_A = 0°C to 70°C		500	1000	

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM358 and LM358A.
(2) All typical values are T_A = 25°C.

7.8 Electrical Characteristics: LM2904, LM2904V

For V_S = (V+) – (V–) = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	V_S = 5 V to maximum; V_{CM} = 0 V; V_O = 1.4 V	Non-A suffix devices			3	7	mV
				T_A = –40°C to 125°C			10	
			A-suffix devices			1	2	
				T_A = –40°C to 125°C			4	
dV_{OS}/d_T	Input offset voltage drift			T_A = –40°C to 125°C		7		µV/°C
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	V_S = 5 V to 30 V			65	100		dB
V_{O1}/V_{O2}	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 5 V to maximum			(V–)		(V+) – 1.5	V
				T_A = –40°C to 125°C	(V–)		(V+) – 2	
CMRR	Common-mode rejection ratio	V_S = 5 V to maximum; V_{CM} = 0 V			65	80		dB
INPUT BIAS CURRENT								
I_B	Input bias current	V_O = 1.4 V				–20	–250	nA
				T_A = –40°C to 125°C			–500	
I_{OS}	Input offset current	V_O = 1.4 V	Non-V suffix device			2	50	nA
				T_A = –40°C to 125°C			300	
			V-suffix device			2	50	
				T_A = –40°C to 125°C			150	
dI_{OS}/d_T	Input offset current drift			T_A = –40°C to 125°C		10		pA/°C
NOISE								
e_n	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V; V_O = 1 V to 11 V; $R_L \geq 2$ kΩ			25	100		V/mV
				T_A = –40°C to 125°C	15			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	G = +1				0.3		V/µs
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	$R_L \geq 10$ kΩ		V_S – 1.5			V
			Non-V suffix device; V_S = maximum; R_L = 2 kΩ	T_A = –40°C to 125°C			4	
			Non-V suffix device; V_S = maximum; $R_L \geq 10$ kΩ	T_A = –40°C to 125°C		2	3	
			V-suffix device; V_S = maximum; R_L = 2 kΩ	T_A = –40°C to 125°C			6	
			V-suffix device; V_S = maximum; $R_L \geq 10$ kΩ	T_A = –40°C to 125°C		4	5	
		Negative rail	V_S = 5 V; $R_L \leq 10$ kΩ	T_A = –40°C to 125°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = 0 V; V_{ID} = 1 V	Source		–20	–30		mA
				T_A = –40°C to 125°C	–10			
		V_S = 15 V; V_O = 15 V; V_{ID} = –1 V	Sink		10	20		
				T_A = –40°C to 125°C	5			
		V_{ID} = -1 V; V_O = 200 mV	Non-V suffix device			30		µA
			V-suffix device		12	40		
I_{SC}	Short-circuit current	V_S = 10 V; V_O = V_S / 2				±40	±60	mA
POWER SUPPLY								
I_Q	Quiescent current per amplifier	V_O = 2.5 V; I_O = 0 A		T_A = –40°C to 125°C		350	600	µA
		V_S = maximum; V_O = maximum / 2; I_O = 0 A		T_A = –40°C to 125°C		500	1000	

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 26 V for LM2904 and 32 V for LM2904V.
(2) All typical values are T_A = 25°C.

7.9 Electrical Characteristics: LM158, LM158A

For V_S = (V+) – (V–) = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP[2]	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	V_S = 5 V to 30 V; $V_{C\ M}$ = 0 V; V_O = 1.4 V	LM158			3	5	mV
				T_A = –55°C to 125°C			7	
			LM158A				2	
				T_A = –55°C to 125°C			4	
dV_{OS}/d_T	Input offset voltage drift		LM158	T_A = –55°C to 125°C		7		μV/°C
			LM158A	T_A = –55°C to 125°C		7	15[3]	
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	V_S = 5 V to 30 V			65	100		dB
V_{O1}/V_{O2}	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 5 V to 30 V	LM158		(V–)		(V+) – 1.5	V
		V_S = 30 V	LM158A					
		V_S = 5 V to 30 V	LM158	T_A = –55°C to 125°C	(V–)		(V+) – 2	
		V_S = 30 V	LM158A					
CMRR	Common-mode rejection ratio	V_S = 5 V to 30 V; V_{CM} = 0 V			70	80		dB
INPUT BIAS CURRENT								
I_B	Input bias current	V_O = 1.4 V	LM158			–20	–150	nA
				T_A = –55°C to 125°C			–300	
			LM158A			–15	–50	
				T_A = –55°C to 125°C			–100	
I_{OS}	Input offset current	V_O = 1.4 V	LM158			2	30	nA
				T_A = –55°C to 125°C			100	
			LM158A			2	10	
				T_A = –55°C to 125°C			30	
dI_{OS}/d_T	Input offset current drift					10		pA/°C
			LM158A	T_A = –55°C to 125°C			200	
NOISE								
e_n	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V; V_O = 1 V to 11 V; R_L ≥ 2 kΩ			50	100		V/mV
				T_A = –55°C to 125°C	25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	G = +1				0.3		V/μs
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	V_S = 30 V; R_L = 2 kΩ	T_A = –55°C to 125°C			4	V
			V_S = 30 V; R_L ≥ 10 kΩ			2	3	
			V_S = 5 V; R_L ≥ 2 kΩ				1.5	
		Negative rail	V_S = 5 V; R_L ≤ 10 kΩ	T_A = –55°C to 125°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = 0 V; V_{ID} = 1 V	Source		–20	–30		mA
				LM158A			–60	
				T_A = –55°C to 125°C	–10			
		V_S = 15 V; V_O = 15 V; V_{ID} = –1 V	Sink		10	20		
				T_A = –55°C to 125°C	5			
		V_{ID} = –1 V; V_O = 200 mV			12	30		μA
I_{SC}	Short-circuit current	V_S = 10 V; V_O = V_S / 2				±40	±60	mA

7.9 Electrical Characteristics: LM158, LM158A (continued)

For V_S = (V+) – (V–) = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_O = 2.5 V; I_O = 0 A	T_A = –55°C to 125°C		350	600	μA
		V_S = 30 V; V_O = 15 V; I_O = 0 A			500	1000	

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM158 and LM158A.
(2) All typical values are T_A = 25°C.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.10 Electrical Characteristics: LM258, LM258A

For V_S = (V+) – (V–) = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	V_S = 5 V to 30 V; V_{CM} = 0 V; V_O = 1.4 V	LM258			3	5	mV
				T_A = –25°C to 85°C			7	
			LM258A			2	3	
				T_A = –25°C to 85°C			4	
dV_{OS}/d_T	Input offset voltage drift		LM258	T_A = –25°C to 85°C		7		μV/°C
			LM258A	T_A = –25°C to 85°C		7	15	
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	V_S = 5 V to 30 V			65	100		dB
V_{O1}/V_{O2}	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	V_S = 5 V to 30 V	LM258		(V–)		(V+) – 1.5	V
		V_S = 30 V	LM258A					
		V_S = 5 V to 30 V	LM258	T_A = –25°C to 85°C	(V–)		(V+) – 2	
		V_S = 30 V	LM258A					
CMRR	Common-mode rejection ratio	V_S = 5 V to 30 V; V_{CM} = 0 V			70	80		dB
INPUT BIAS CURRENT								
I_B	Input bias current	V_O = 1.4 V	LM258			–20	–150	nA
				T_A = –25°C to 85°C			–300	
			LM258A			–15	–80	
				T_A = –25°C to 85°C			–100	
I_{OS}	Input offset current	V_O = 1.4 V	LM258			2	30	nA
				T_A = –25°C to 85°C			100	
			LM258A			2	15	
				T_A = –25°C to 85°C			30	
dI_{OS}/d_T	Input offset current drift					10		pA/°C
			LM258A	T_A = –25°C to 85°C			200	
NOISE								
e_n	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	V_S = 15 V; V_O = 1 V to 11 V; R_L ≥ 2 kΩ			50	100		V/mV
				T_A = –25°C to 85°C	25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	G = +1				0.3		V/μs
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	V_S = 30 V; R_L = 2 kΩ	T_A = –25°C to 85°C			4	V
			V_S = 30 V; R_L ≥ 10 kΩ			2	3	
			V_S = 5 V; R_L ≥ 2 kΩ				1.5	
		Negative rail	V_S = 5 V; R_L ≤ 10 kΩ	T_A = –25°C to 85°C		5	20	mV
I_O	Output current	V_S = 15 V; V_O = 0 V; V_{ID} = 1 V	Source		–20	–30		mA
				LM258A			–60	
				T_A = –25°C to 85°C	–10			
		V_S = 15 V; V_O = 15 V; V_{ID} = –1 V	Sink		10	20		
				T_A = –25°C to 85°C	5			
		V_{ID} = –1 V; V_O = 200 mV			12	30		μA
I_{SC}	Short-circuit current	V_S = 10 V; V_O = V_S / 2				±40	±60	mA
POWER SUPPLY								
I_Q	Quiescent current per amplifier	V_O = 2.5 V; I_O = 0 A		T_A = –25°C to 85°C		350	600	μA
		V_S = 30 V; V_O = 15 V; I_O = 0 A				500	1000	

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM258 and LM258A.
(2) All typical values are T_A = 25°C.

7.11 Typical Characteristics: LM358B and LM2904B

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

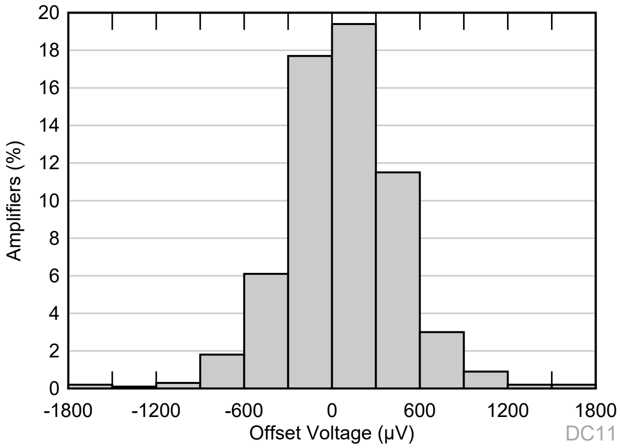


Figure 7-1. Offset Voltage Production Distribution

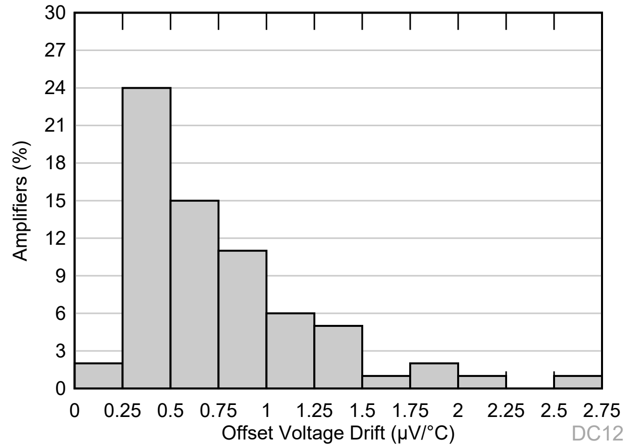


Figure 7-2. Offset Voltage Drift Distribution

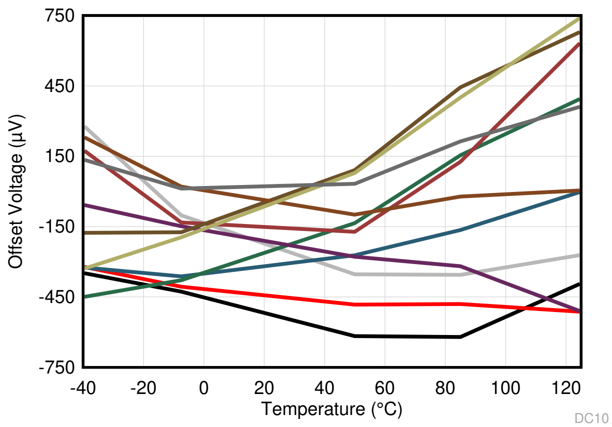


Figure 7-3. Offset Voltage vs Temperature

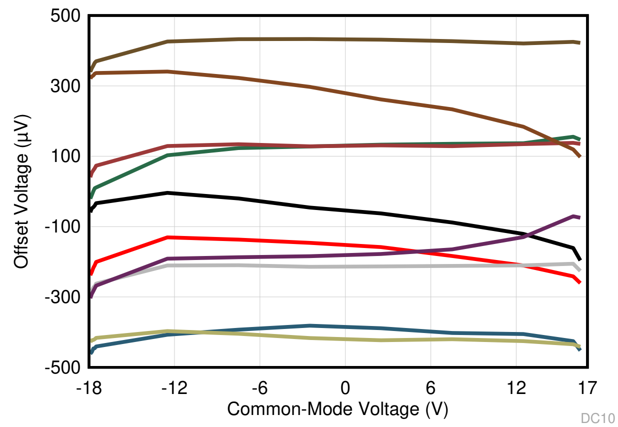


Figure 7-4. Offset Voltage vs Common-Mode Voltage

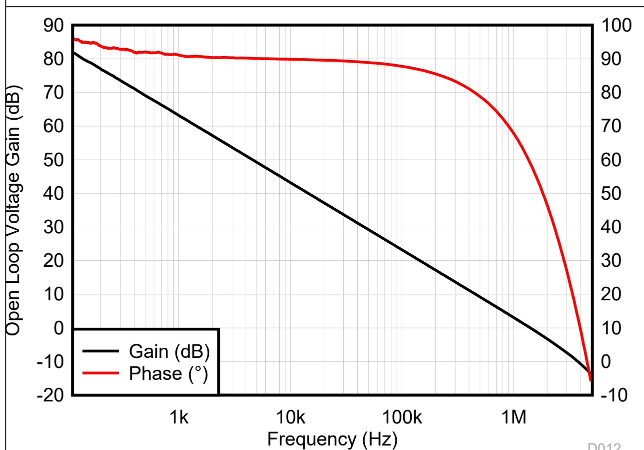


Figure 7-5. Open-Loop Gain and Phase vs Frequency

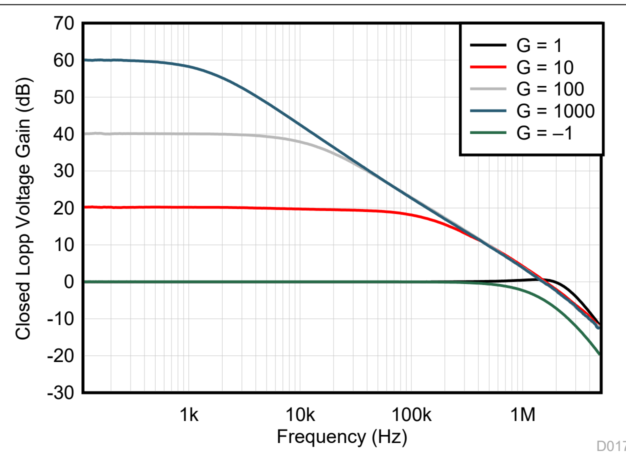


Figure 7-6. Closed-Loop Gain vs Frequency

7.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

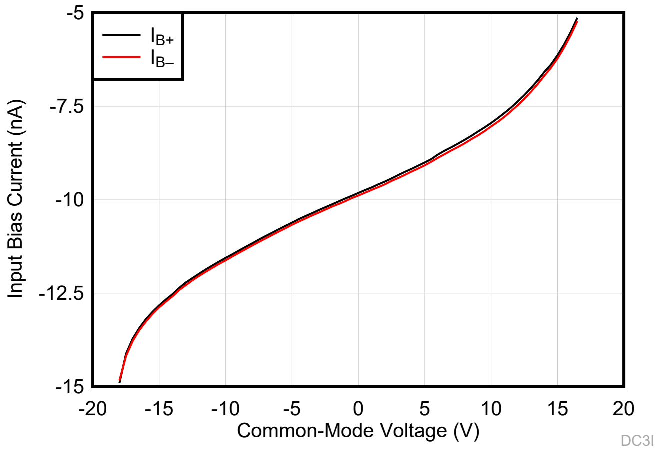


Figure 7-7. Input Bias Current vs Common-Mode Voltage

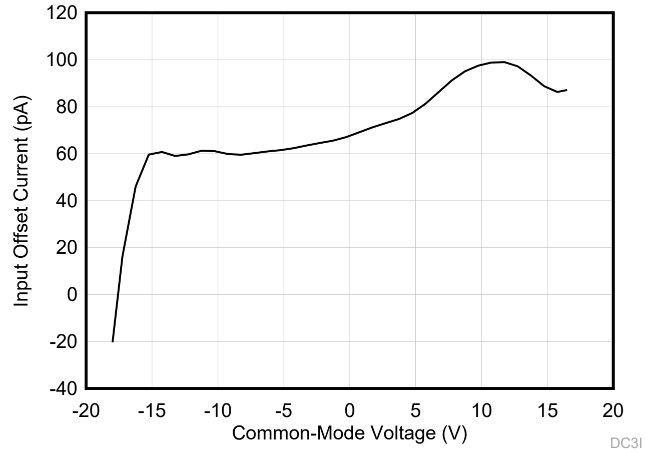


Figure 7-8. Input Offset Current vs Common-Mode Voltage

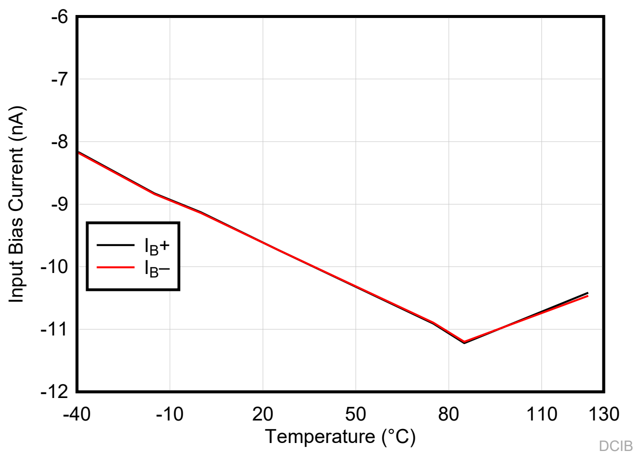


Figure 7-9. Input Bias Current vs Temperature

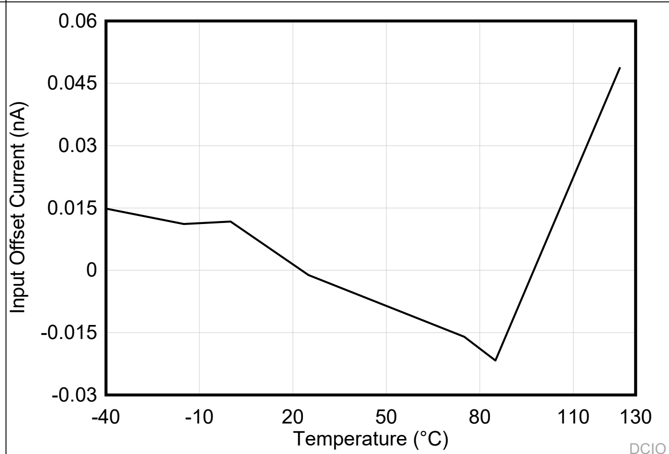


Figure 7-10. Input Offset Current vs Temperature

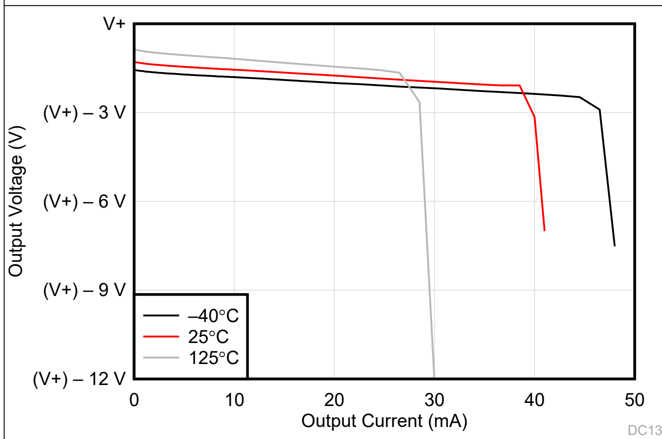


Figure 7-11. Output Voltage Swing vs Output Current (Sourcing)

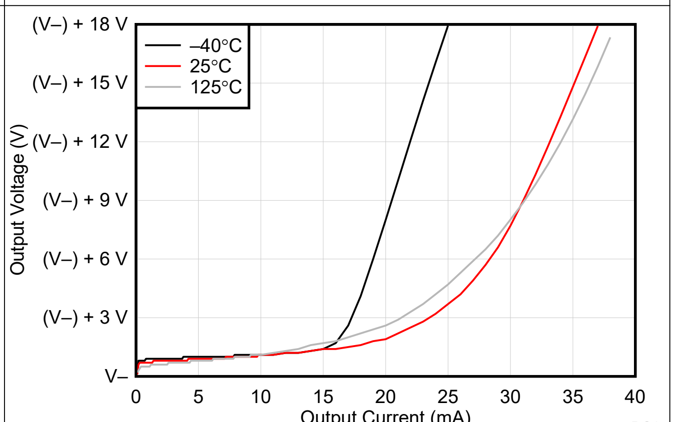


Figure 7-12. Output Voltage Swing vs Output Current (Sinking)

7.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

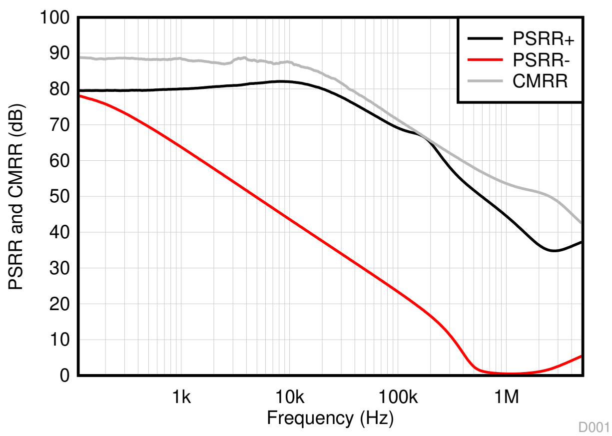


Figure 7-13. CMRR and PSRR vs Frequency

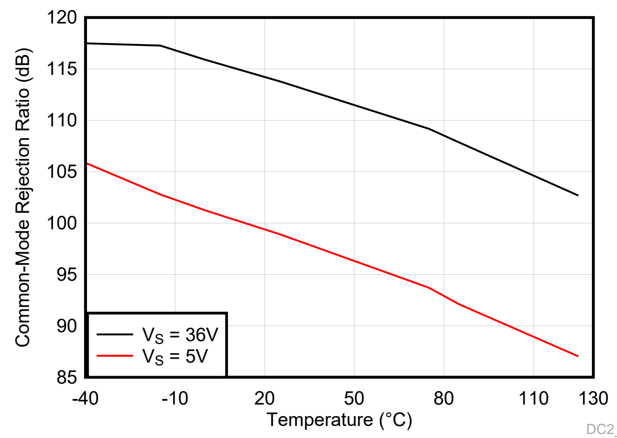
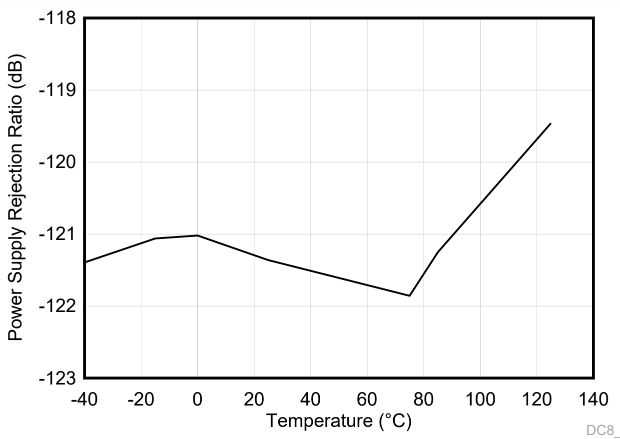


Figure 7-14. Common-Mode Rejection Ratio vs Temperature (dB)



V_S = 5 V to 36 V

Figure 7-15. Power Supply Rejection Ratio vs Temperature (dB)

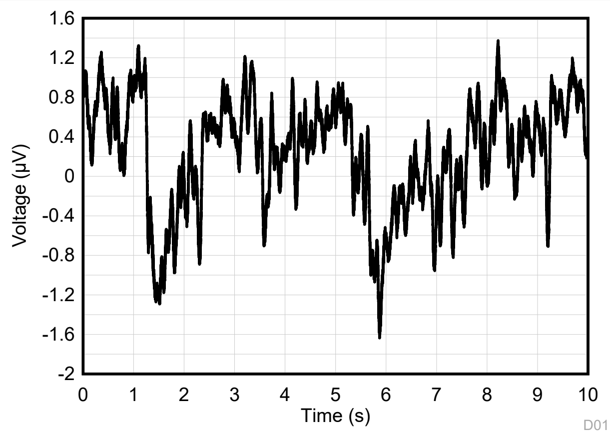


Figure 7-16. 0.1-Hz to 10-Hz Noise

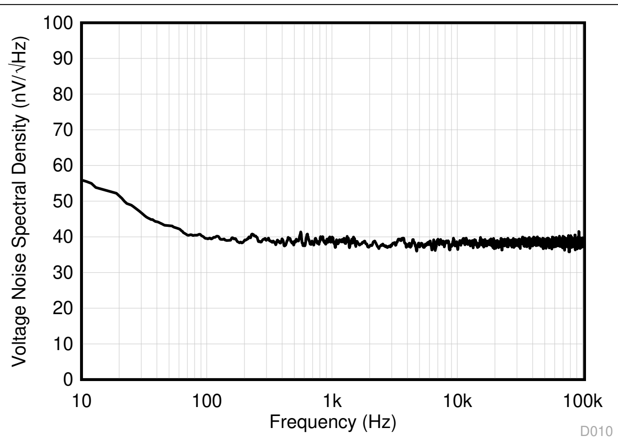
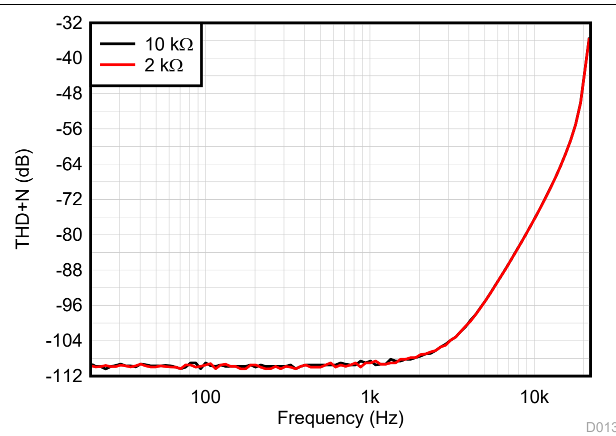


Figure 7-17. Input Voltage Noise Spectral Density vs Frequency



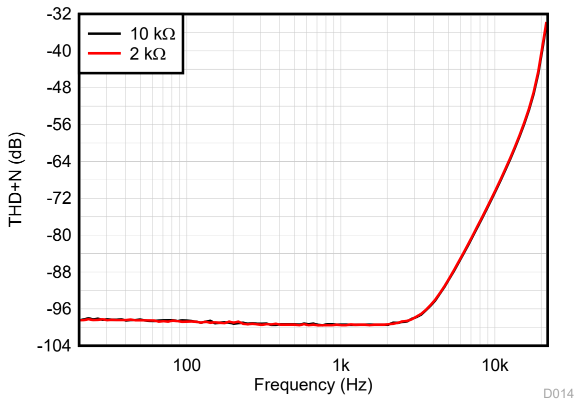
G = 1, f = 1 kHz, BW = 80 kHz,

V_{OUT} = 10 V_{PP}, R_L connected to V–

Figure 7-18. THD+N Ratio vs Frequency, G = 1

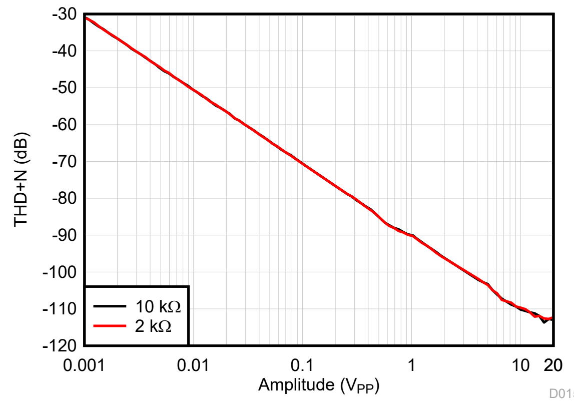
7.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).



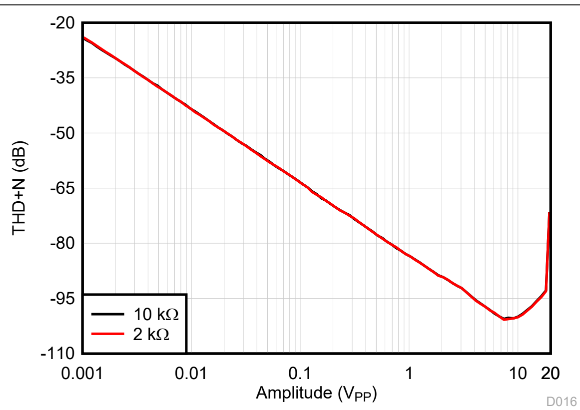
G = –1, f = 1 kHz, BW = 80 kHz,
V_{OUT} = 10 V_{PP}, R_L connected to V–
See Figure 8-3

Figure 7-19. THD+N Ratio vs Frequency, G = –1



G = 1, f = 1 kHz, BW = 80 kHz,
R_L connected to V–

Figure 7-20. THD+N vs Output Amplitude, G = 1



G = –1, f = 1 kHz, BW = 80 kHz,
R_L connected to V–
See Figure 8-3

Figure 7-21. THD+N vs Output Amplitude, G = –1

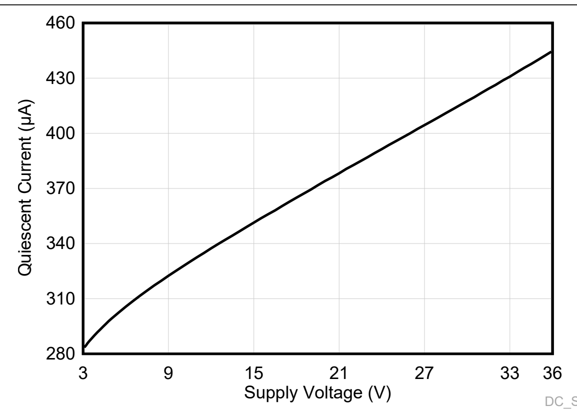


Figure 7-22. Quiescent Current vs Supply Voltage

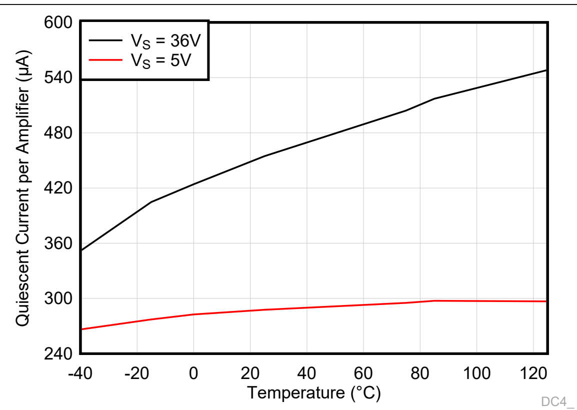


Figure 7-23. Quiescent Current vs Temperature

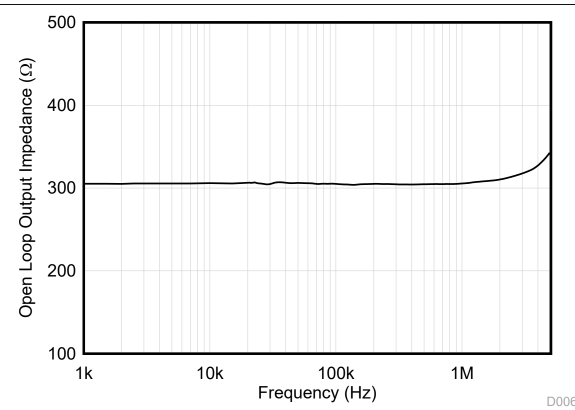
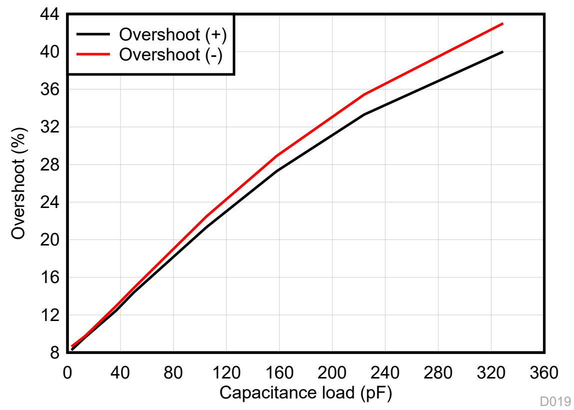


Figure 7-24. Open-Loop Output Impedance vs Frequency

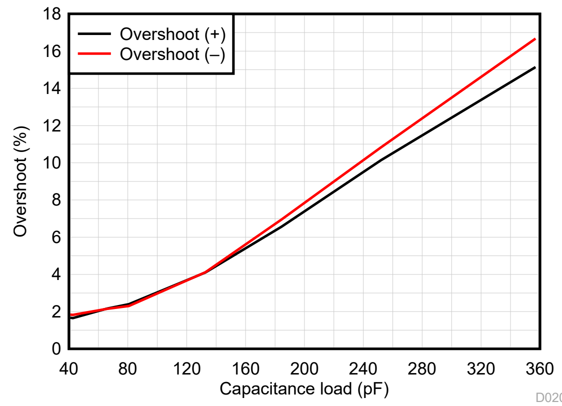
7.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).



G = 1, 100-mV output step, R_L = open

Figure 7-25. Small-Signal Overshoot vs Capacitive Load



G = –1, 100-mV output step, R_L = open

Figure 7-26. Small-Signal Overshoot vs Capacitive Load

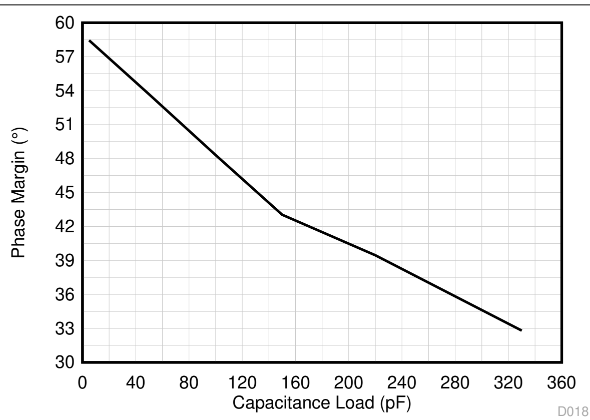
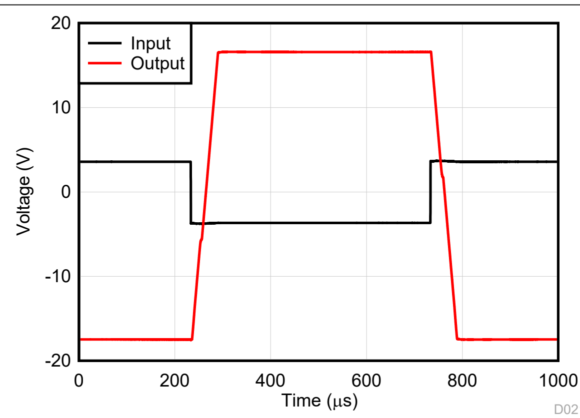
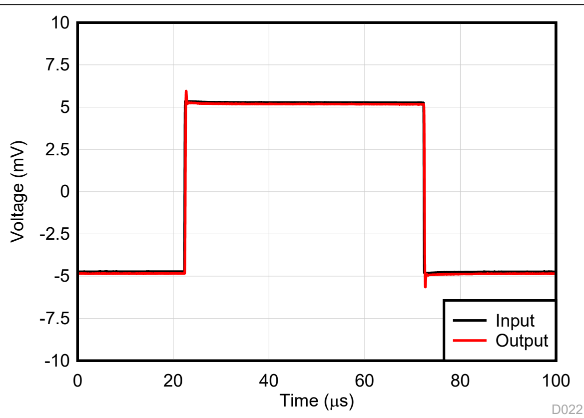


Figure 7-27. Phase Margin vs Capacitive Load



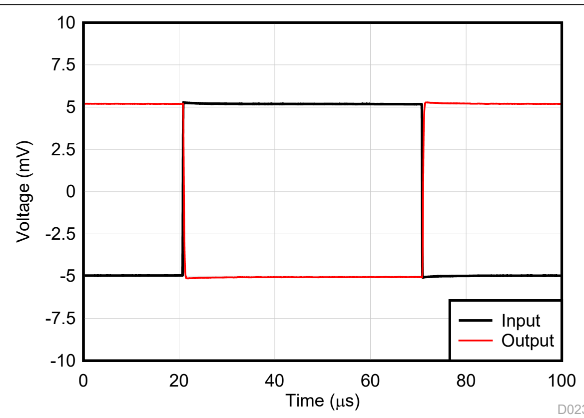
G = –10

Figure 7-28. Overload Recovery



G = 1, R_L = open

Figure 7-29. Small-Signal Step Response, G = 1



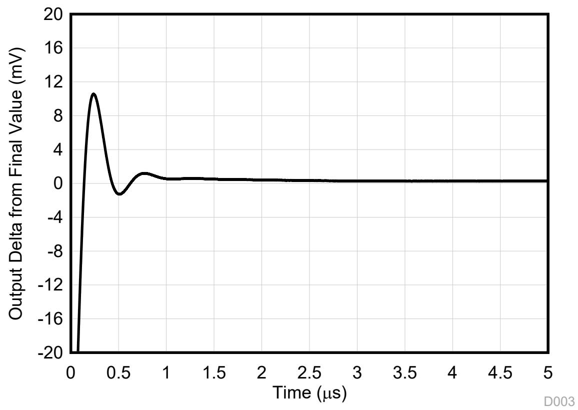
G = –1, R_L = open, R_{FB} = 10K

See Figure 8-3

Figure 7-30. Small-Signal Step Response, G = –1

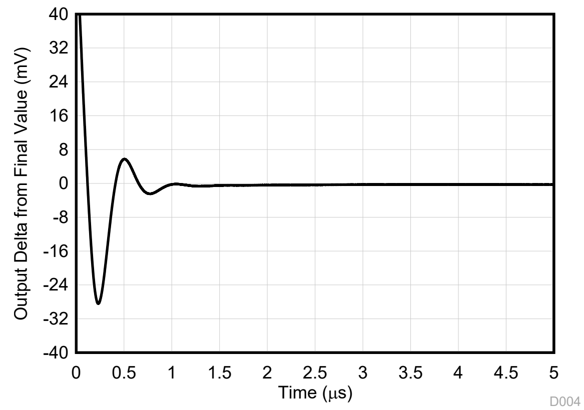
7.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).



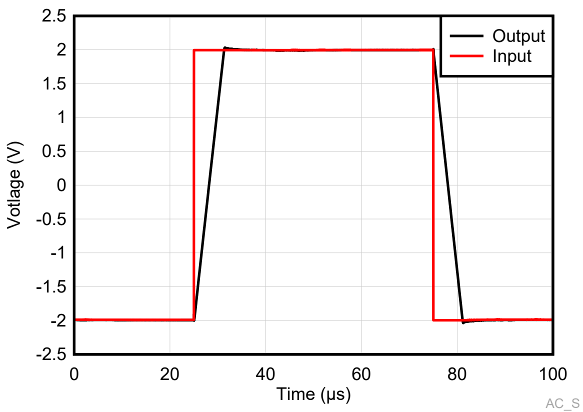
G = 1, R_L = open

Figure 7-31. Large-Signal Step Response (Rising)



G = 1, R_L = open

Figure 7-32. Large-Signal Step Response (Falling)



G = 1, R_L = open

Figure 7-33. Large-Signal Step Response

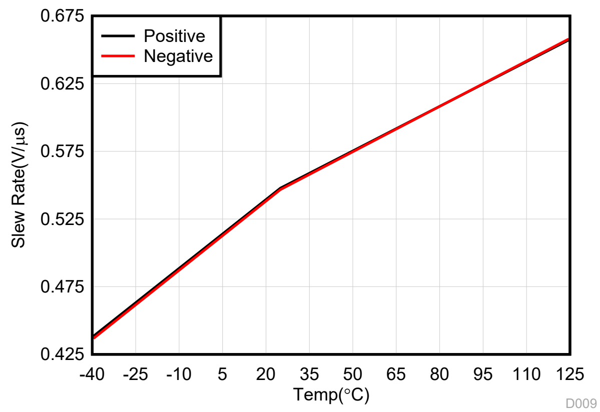


Figure 7-34. Slew Rate vs Temperature

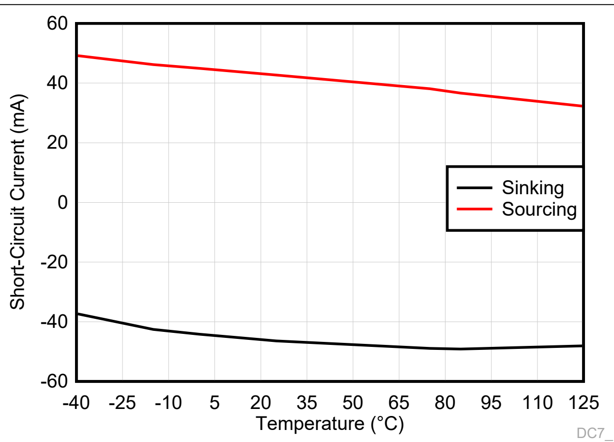
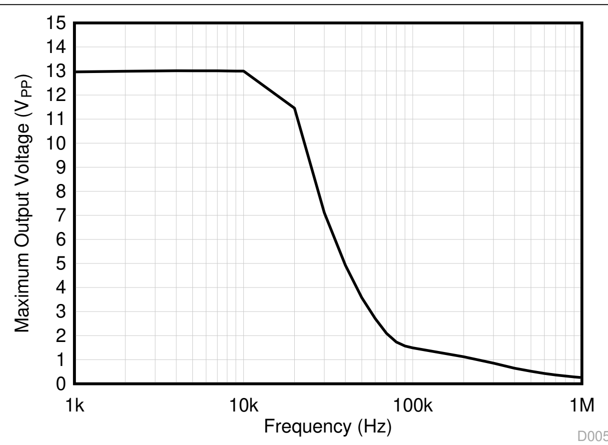


Figure 7-35. Short-Circuit Current vs Temperature



V_S = 15 V

Figure 7-36. Maximum Output Voltage vs Frequency

7.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with T_A = 25°C, V_S = 36 V (±18 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted).

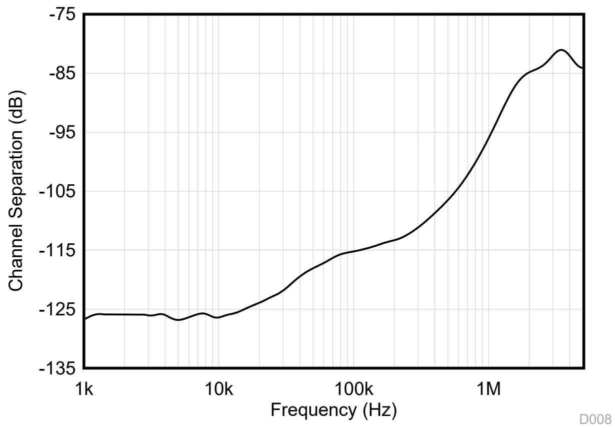


Figure 7-37. Channel Separation vs Frequency

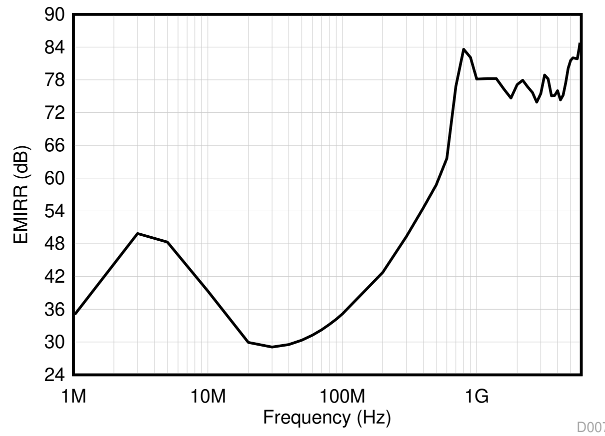


Figure 7-38. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

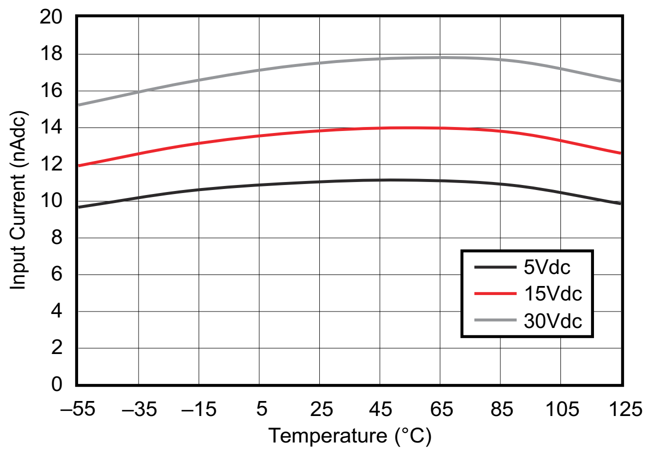


Figure 7-39. Input Current vs Temperature

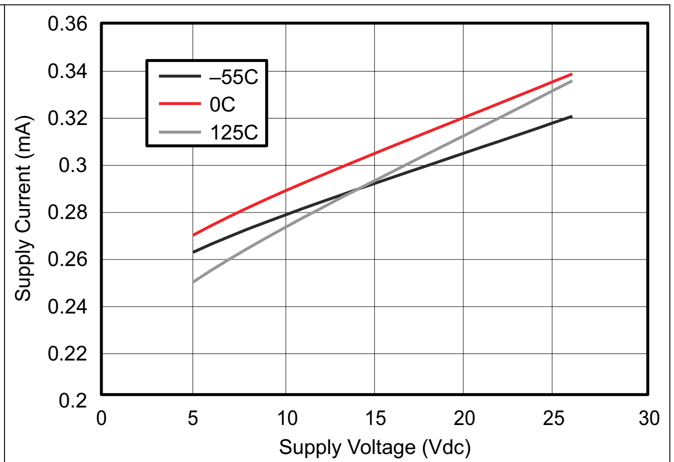


Figure 7-40. Supply Current vs Supply Voltage

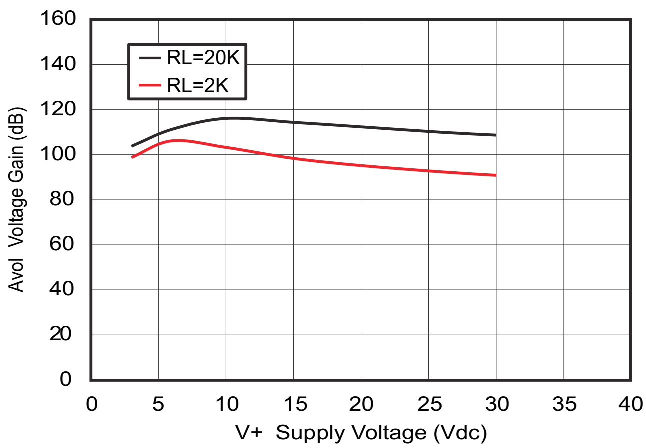


Figure 7-41. Voltage Gain vs Supply Voltage

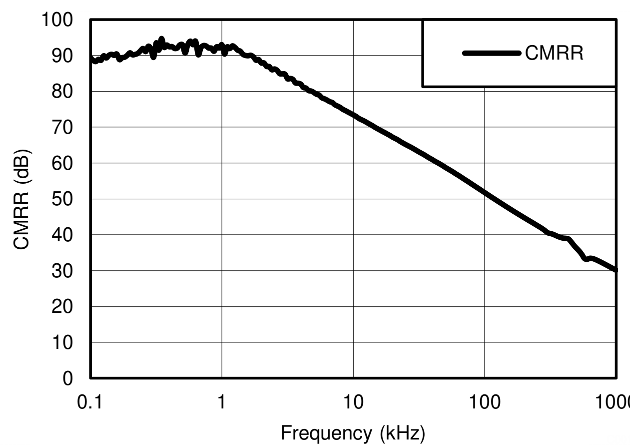


Figure 7-42. Common-Mode Rejection Ratio vs Frequency

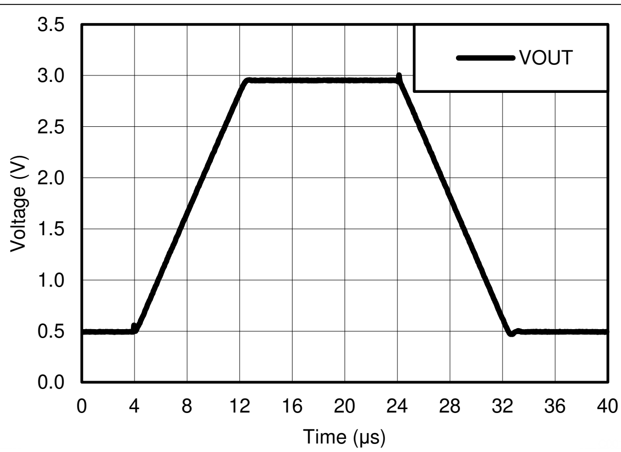


Figure 7-43. Voltage Follower Large Signal Response (50 pF)

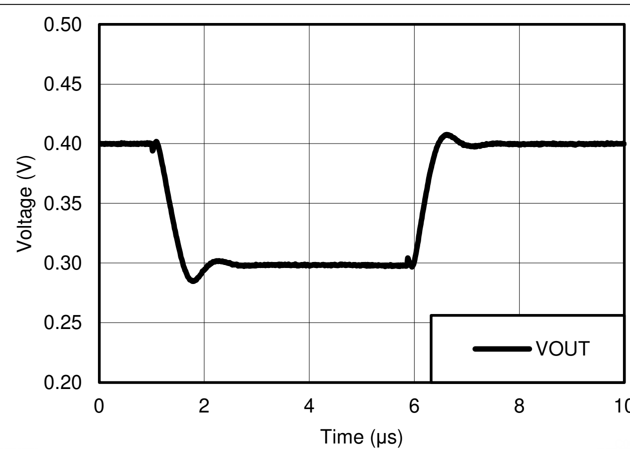


Figure 7-44. Voltage Follower Small Signal Response (50 pF)

7.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V (continued)

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

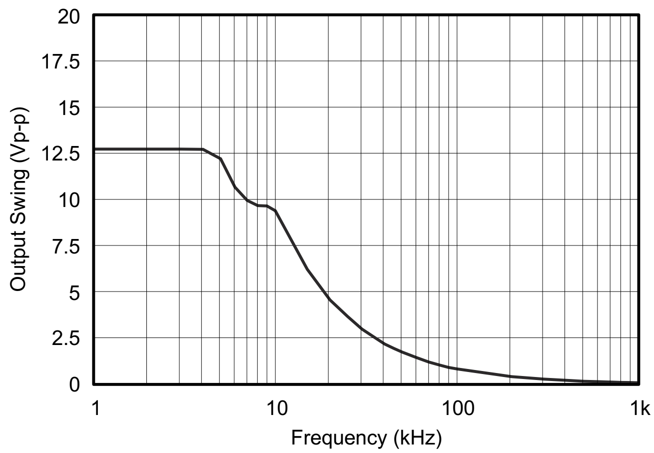


Figure 7-45. Maximum Output Swing vs Frequency (V_{CC} = 15 V)

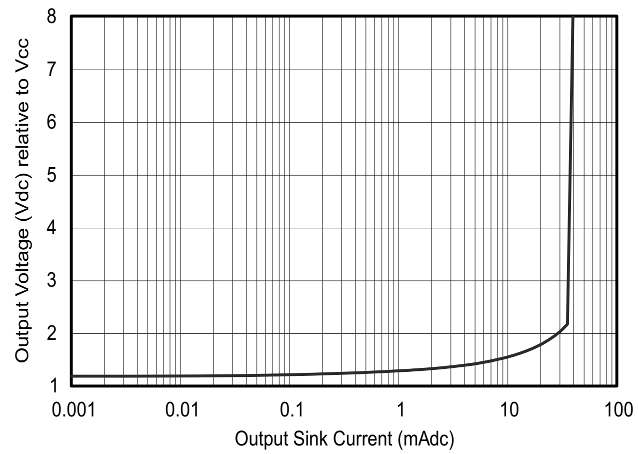


Figure 7-46. Output Sourcing Characteristics

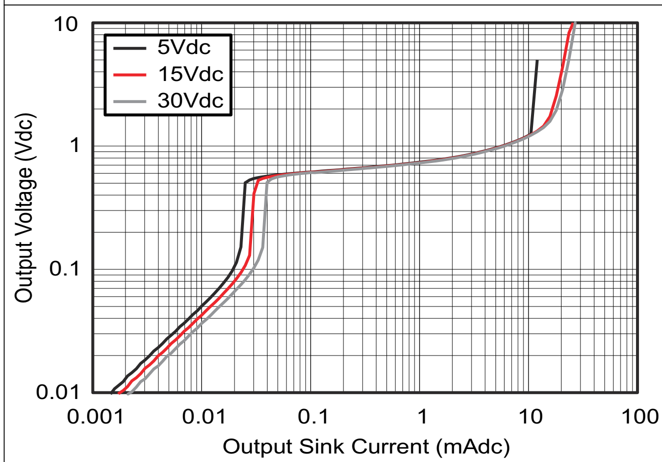


Figure 7-47. Output Sinking Characteristics

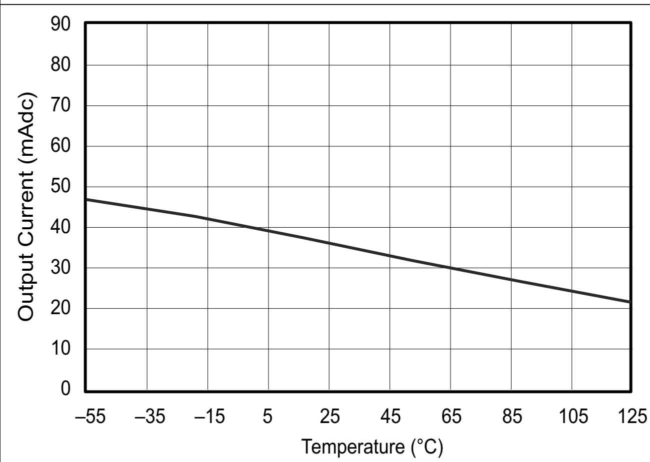


Figure 7-48. Source Current Limiting

8 Parameter Measurement Information

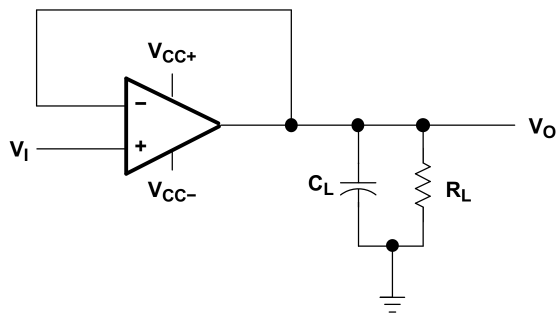


Figure 8-1. Unity-Gain Amplifier

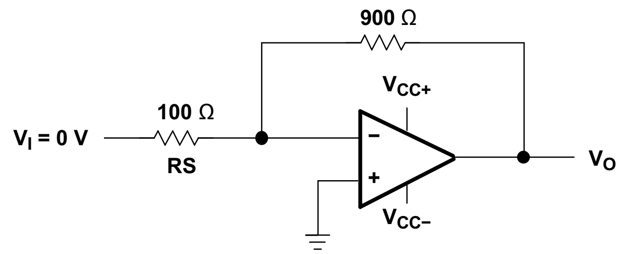


Figure 8-2. Noise-Test Circuit

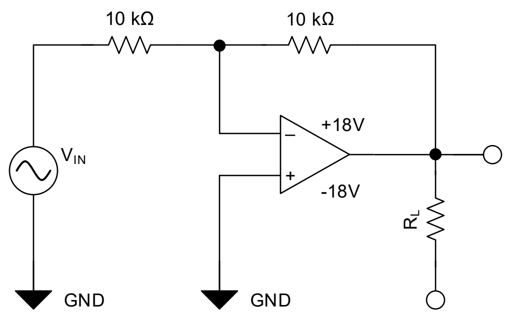


Figure 8-3. Test Circuit, G = –1, for THD+N and Small-Signal Step Response

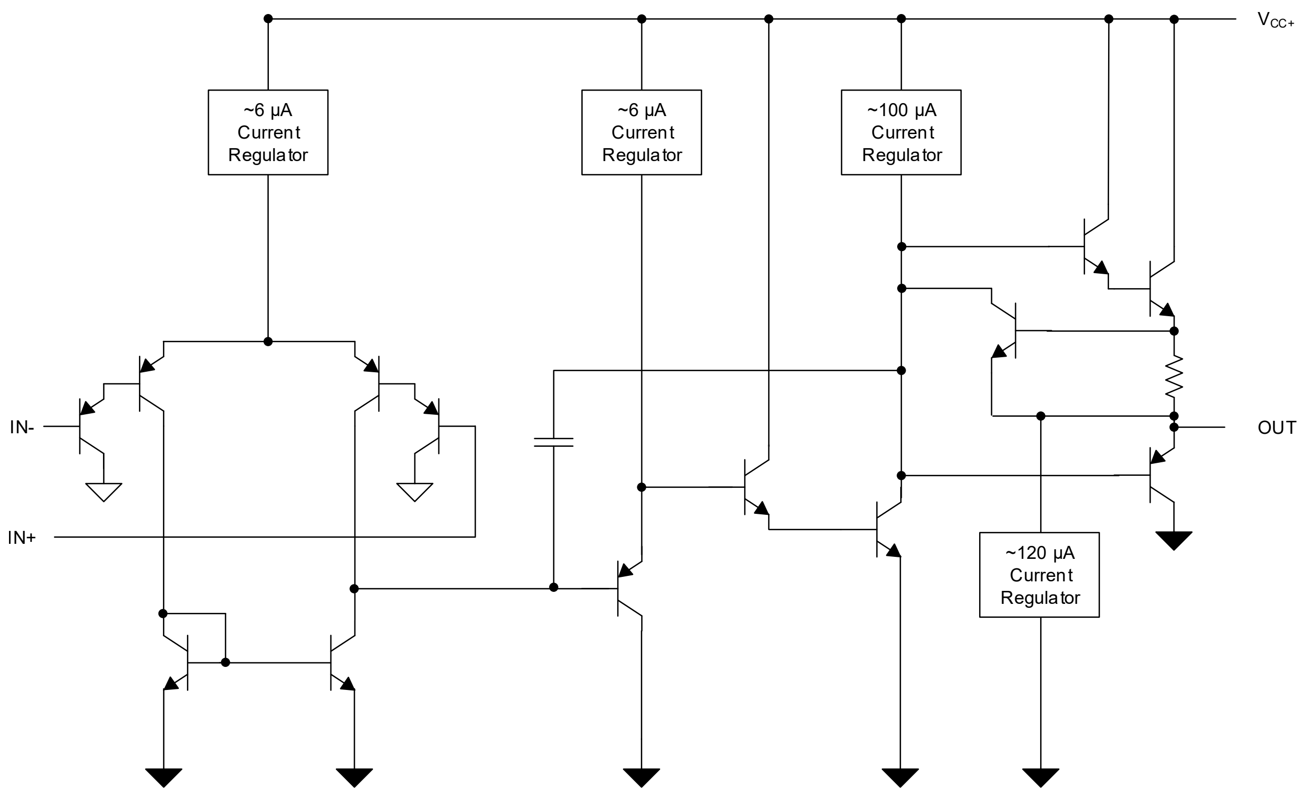
9 Detailed Description

9.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in Section 7.3 and V_S is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional ±5-V supplies.

9.2 Functional Block Diagram: LM358B, LM358BA, LM2904B, LM2904BA



9.3 Feature Description

9.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (B Version).

9.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/µs slew rate (B Version).

9.3.3 Input Common Mode Range

The valid common mode range is from device ground to V_S – 1.5 V (V_S – 2 V across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below V– then input current should be limited to 1 mA and the output phase is undefined.

9.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LMx58 and LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before $V_S$for flexibility in multiple supply circuits.

10.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

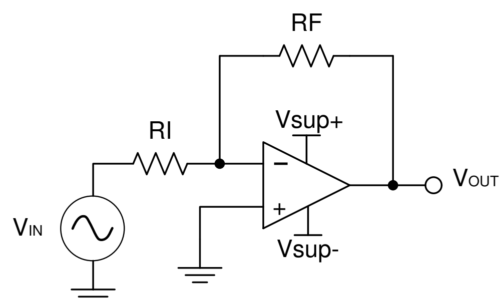


Figure 10-1. Application Schematic

10.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

10.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for R_I or R_F. [Subscripts should be fixed in the accompanying figures and equations also.] Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliampere range. This ensures the part does not draw too much current. This example uses 10 kΩ for R_I which means 36 kΩ is used for R_F. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

10.2.3 Application Curve

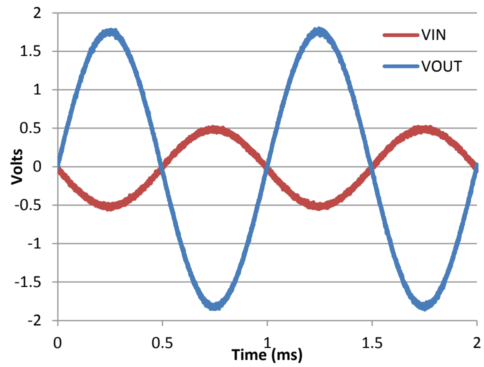


Figure 10-2. Input and Output Voltages of the Inverting Amplifier

11 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see Section 7.1).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 12.

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in Section 12.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

12.2 Layout Examples

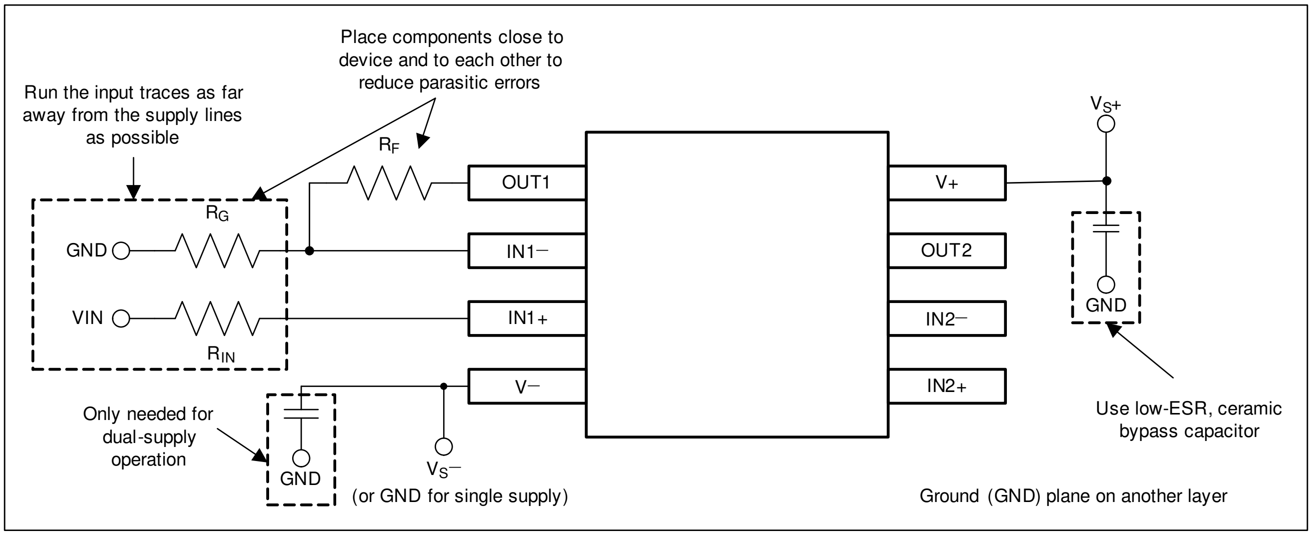


Figure 12-1. Operational Amplifier Board Layout for Noninverting Configuration

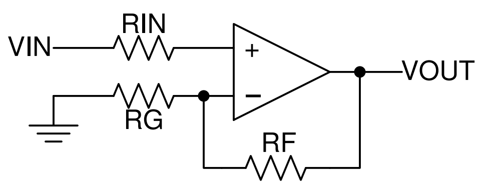


Figure 12-2. Operational Amplifier Schematic for Noninverting Configuration

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87710012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87710012A LM158FKB	Samples
5962-8771001PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	Samples
5962-87710022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87710022A LM158AFKB	Samples
5962-8771002PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	Samples
LM158 MW8	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM158AFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87710022A LM158AFKB	Samples
LM158AJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158AJG	Samples
LM158AJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	Samples
LM158FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87710012A LM158FKB	Samples
LM158JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158JG	Samples
LM158JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	Samples
LM258AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	
LM258ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M3L, M3P, M3S, M3 U)	Samples
LM258ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples
LM258ADRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples
LM258ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-25 to 85	LM258AP	Samples
LM258APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	Samples
LM258D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	
LM258DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	
LM258DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2 U)	Samples
LM258DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-25 to 85	LM258P	Samples
LM258PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258P	Samples
LM2904AVQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2904BA	Samples
LM2904BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28BB	Samples
LM2904BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L2904B	Samples
LM2904BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904B	Samples
LM2904D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	
LM2904DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	
LM2904DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	
LM2904DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-40 to 125	LM2904P	Samples
LM2904PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	Samples
LM2904PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904VQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM358AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	
LM358ADE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358ADG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	
LM358ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6 U)	Samples
LM358ADGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6 U)	
LM358ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358ADRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	0 to 70	LM358AP	Samples
LM358APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	Samples
LM358APW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358APWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358APWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	L358BA	Samples
LM358BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	358B	Samples
LM358BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LM358B	Samples
LM358BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358B	Samples
LM358D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358D-JF	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5 U)	Samples
LM358DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5 U)	
LM358DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM358	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	SN	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PE3	ACTIVE	PDIP	P	8	50	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM258A, LM2904, LM2904B :

- Automotive : LM2904-Q1, LM2904B-Q1

- Enhanced Product : LM258A-EP, LM2904-EP

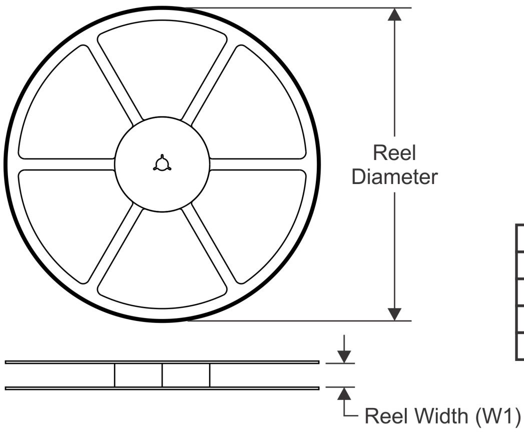
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

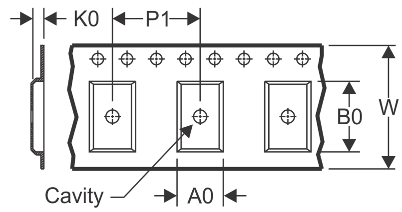
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

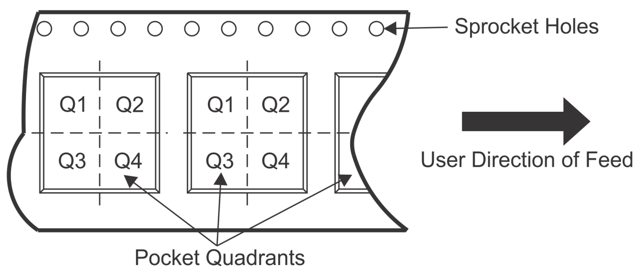


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



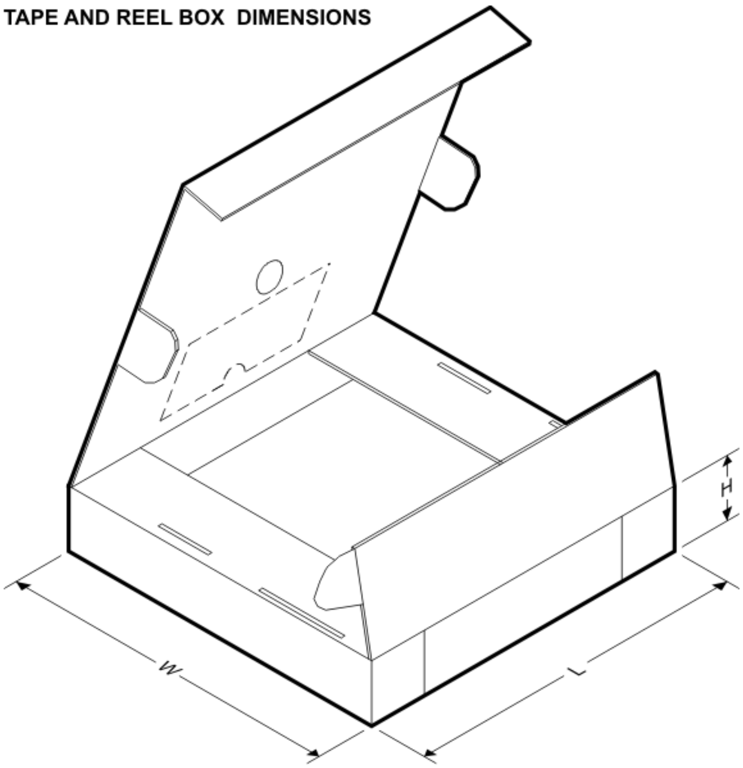
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADR	SOIC	D	8	2500	853.0	449.0	35.0
LM258ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM258DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	853.0	449.0	35.0
LM258DR	SOIC	D	8	2500	340.5	336.1	25.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258DR	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM258DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM2904AVQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BIPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2904DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM2904DR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DR	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DR	SOIC	D	8	2500	853.0	449.0	35.0
LM2904DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM2904DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM2904PSR	SO	PS	8	2000	853.0	449.0	35.0
LM2904PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904PWRG4-JF	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904QDR	SOIC	D	8	2500	350.0	350.0	43.0
LM2904VQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADR	SOIC	D	8	2500	853.0	449.0	35.0
LM358ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM358ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM358APWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358APWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM358BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358BIDR	SOIC	D	8	2500	340.5	336.1	25.0

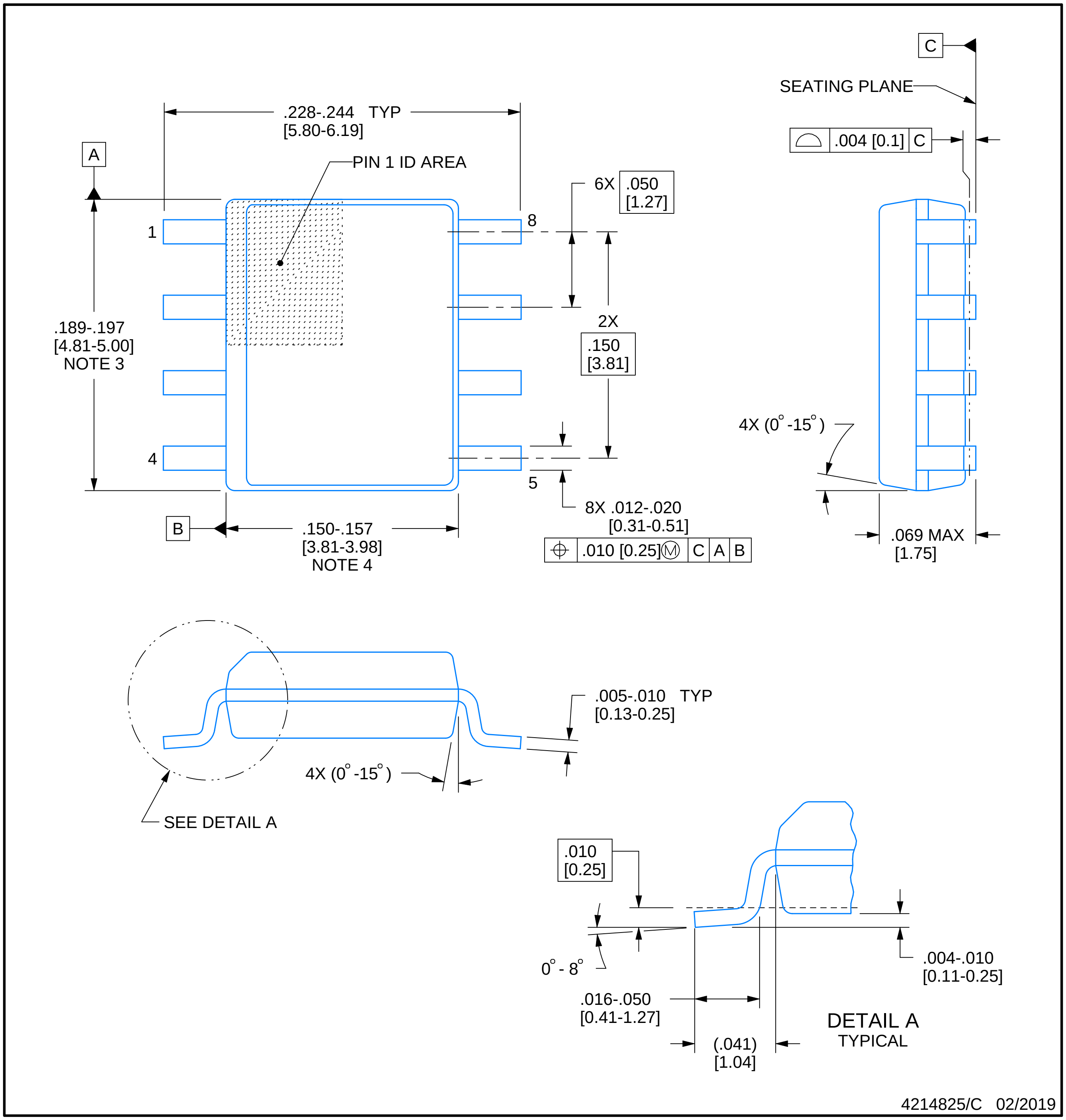
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM358BIPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	853.0	449.0	35.0
LM358DR	SOIC	D	8	2500	340.5	336.1	25.0
LM358DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM358DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM358DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM358DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358PSR	SO	PS	8	2000	853.0	449.0	35.0
LM358PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358PWRG4-JF	TSSOP	PW	8	2000	853.0	449.0	35.0

PACKAGE OUTLINE

D0008A

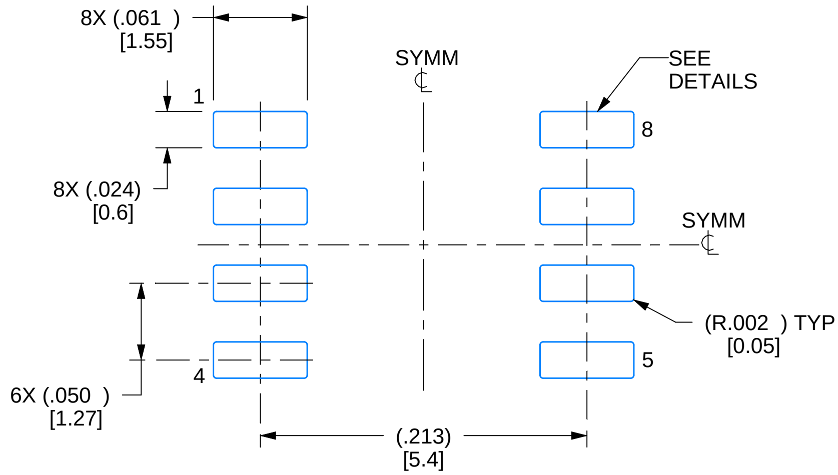
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

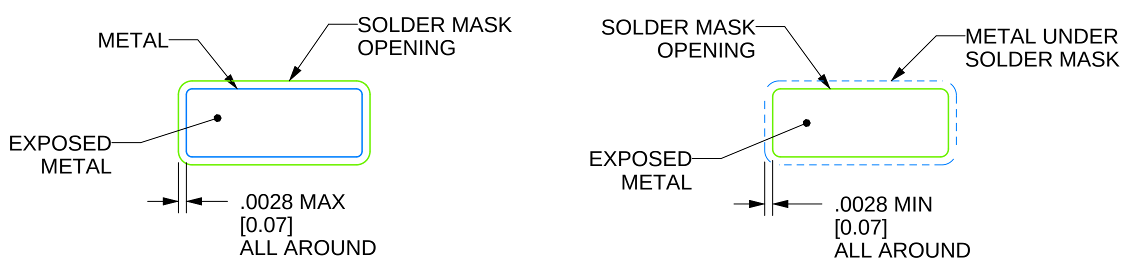


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

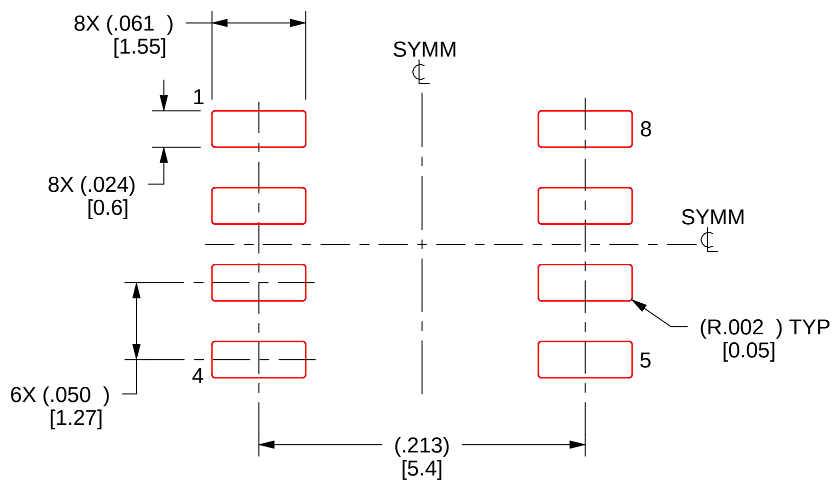
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



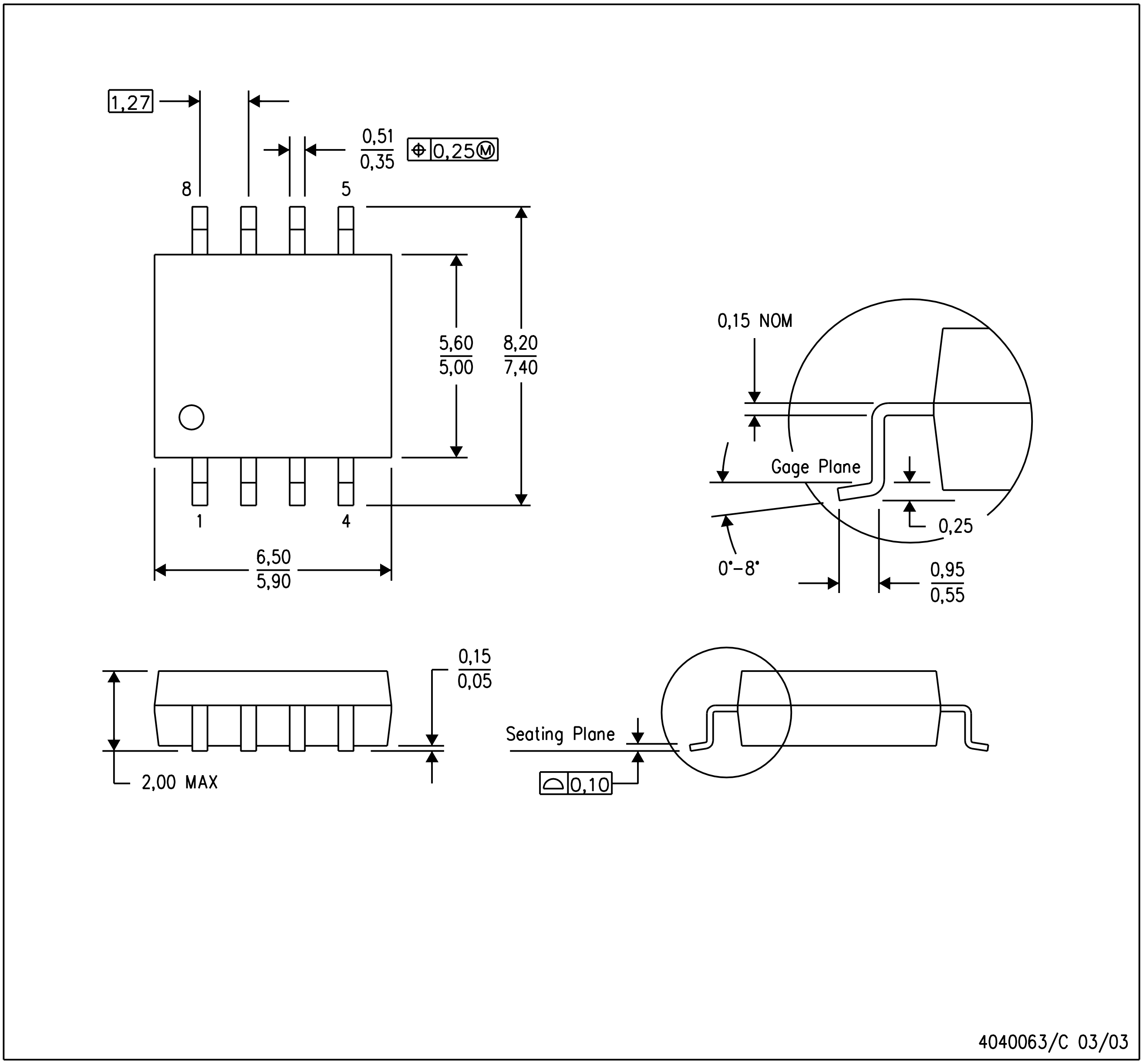
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

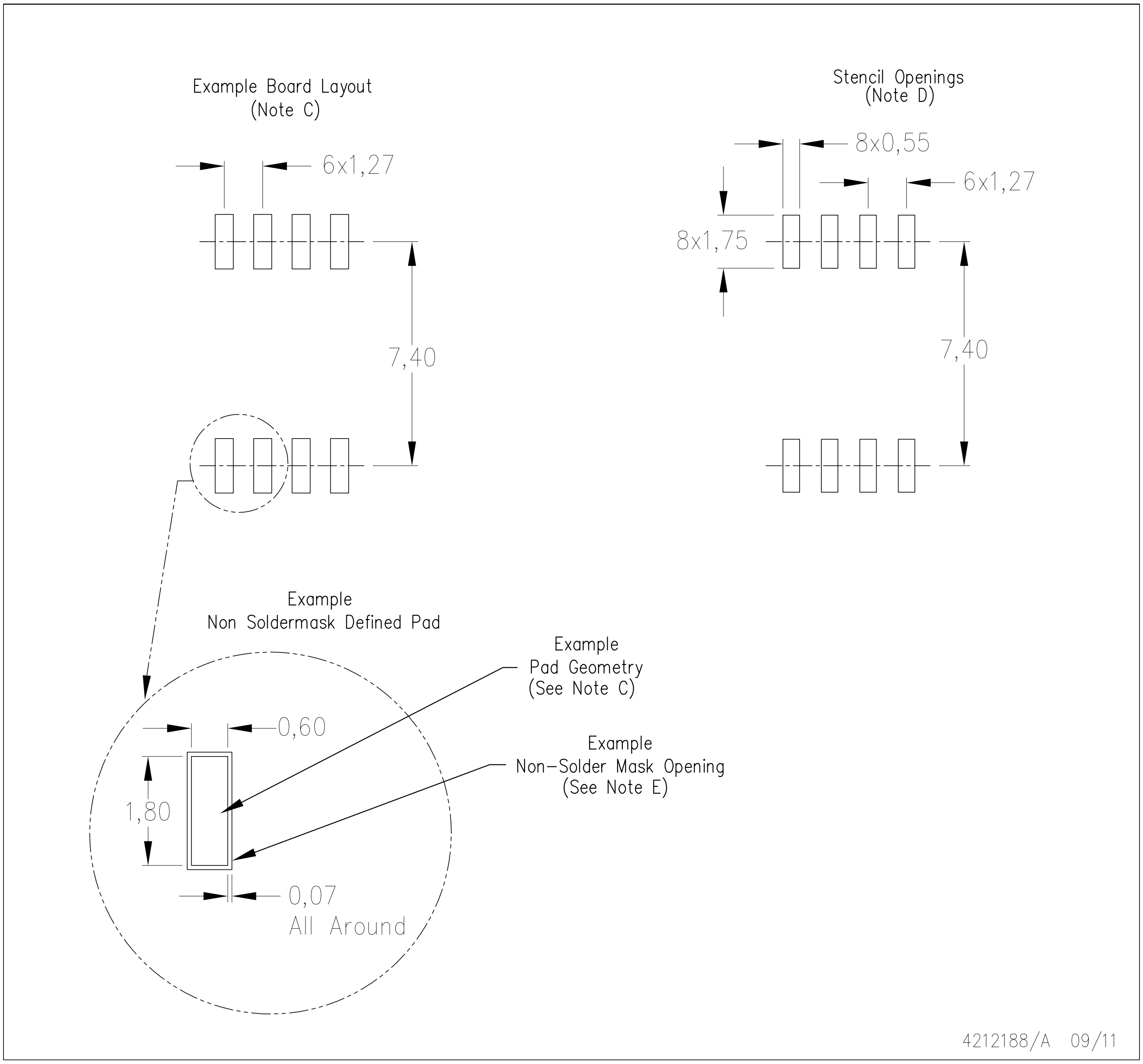
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



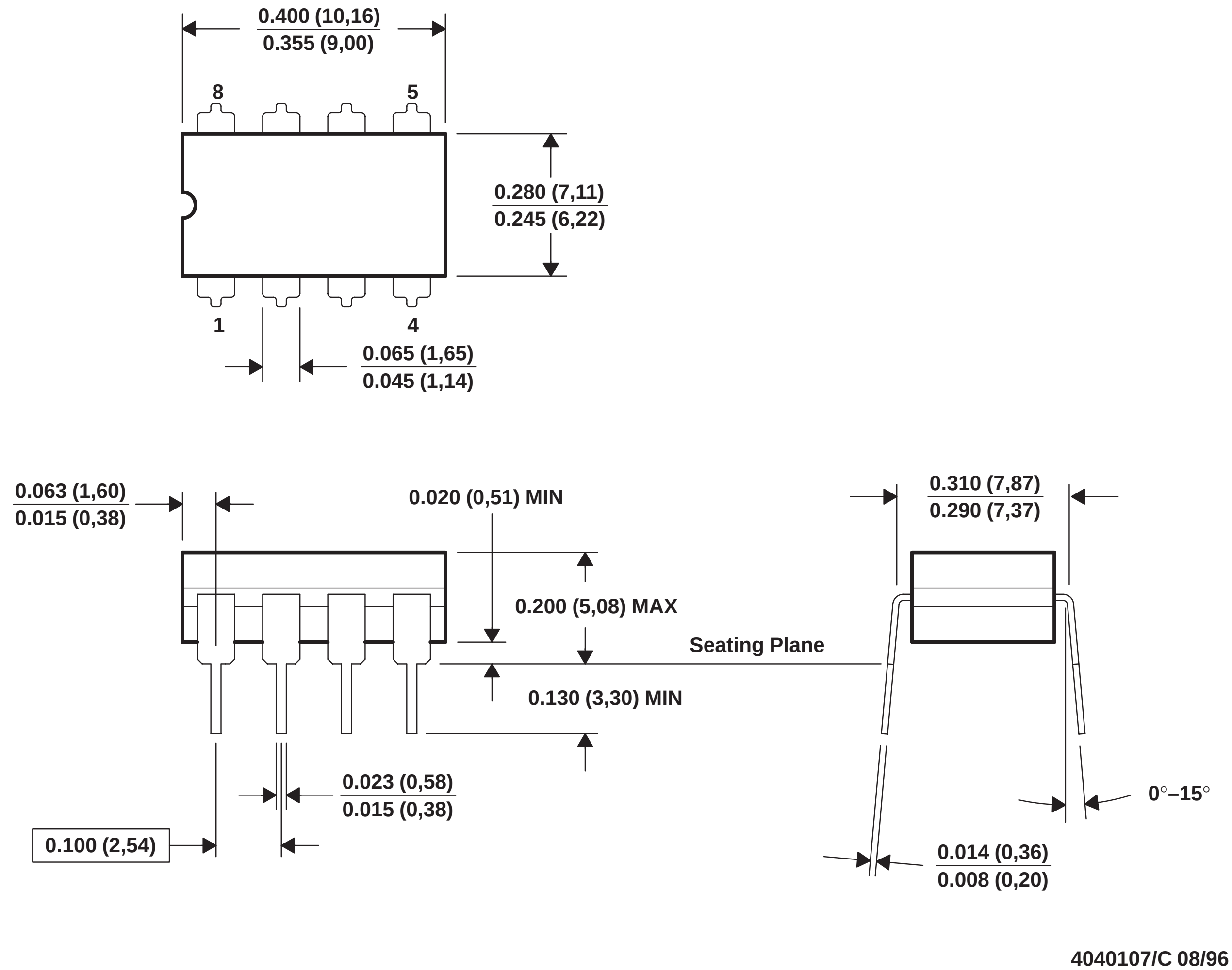
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



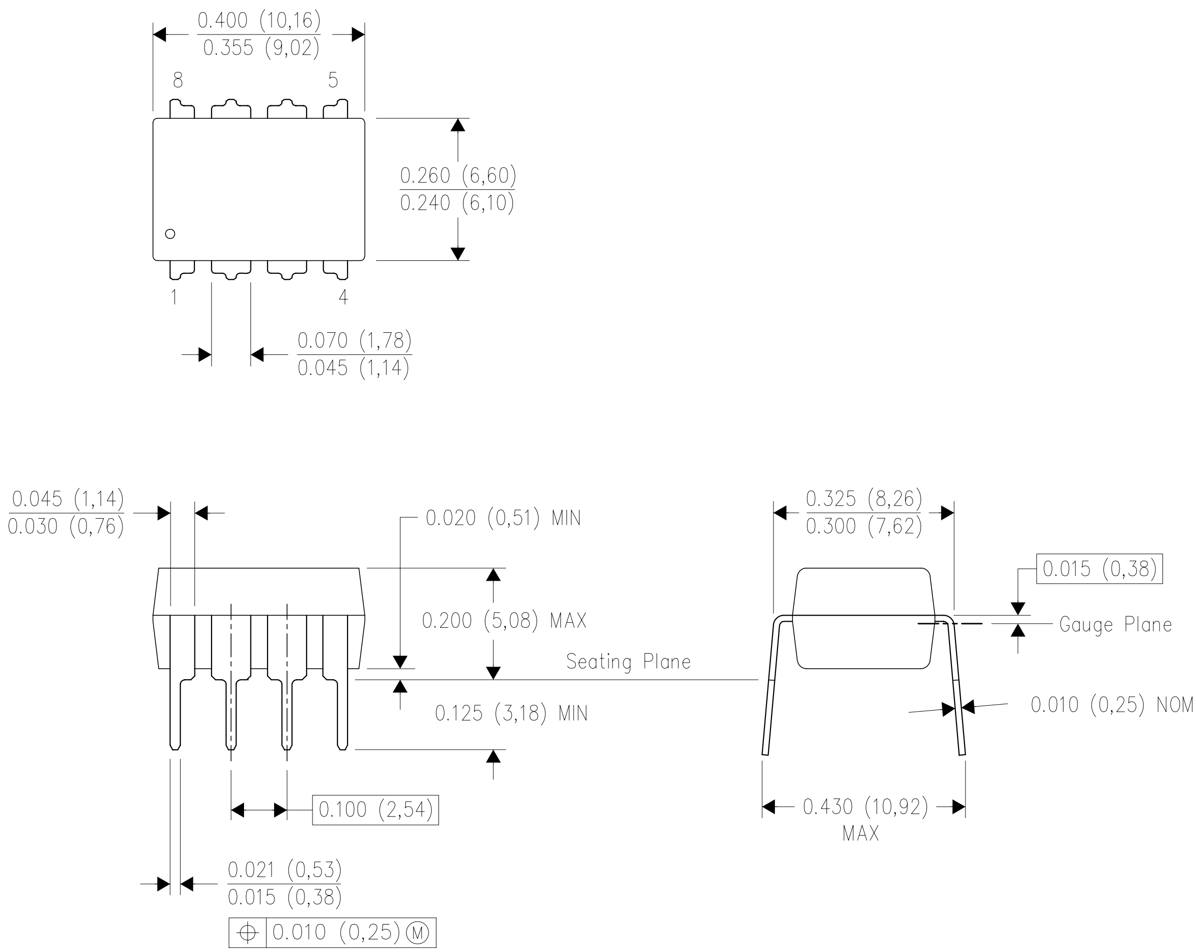
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

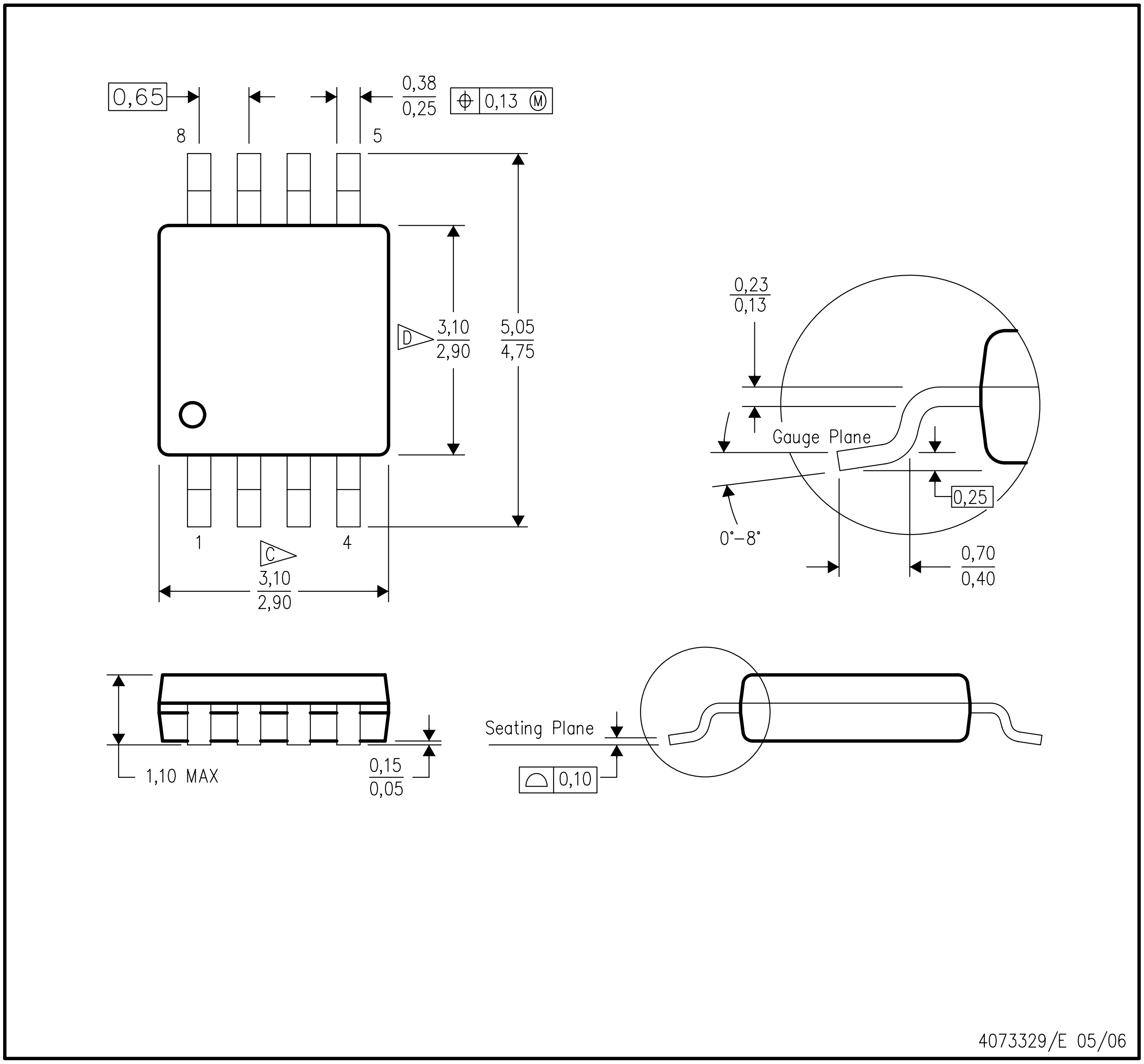
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

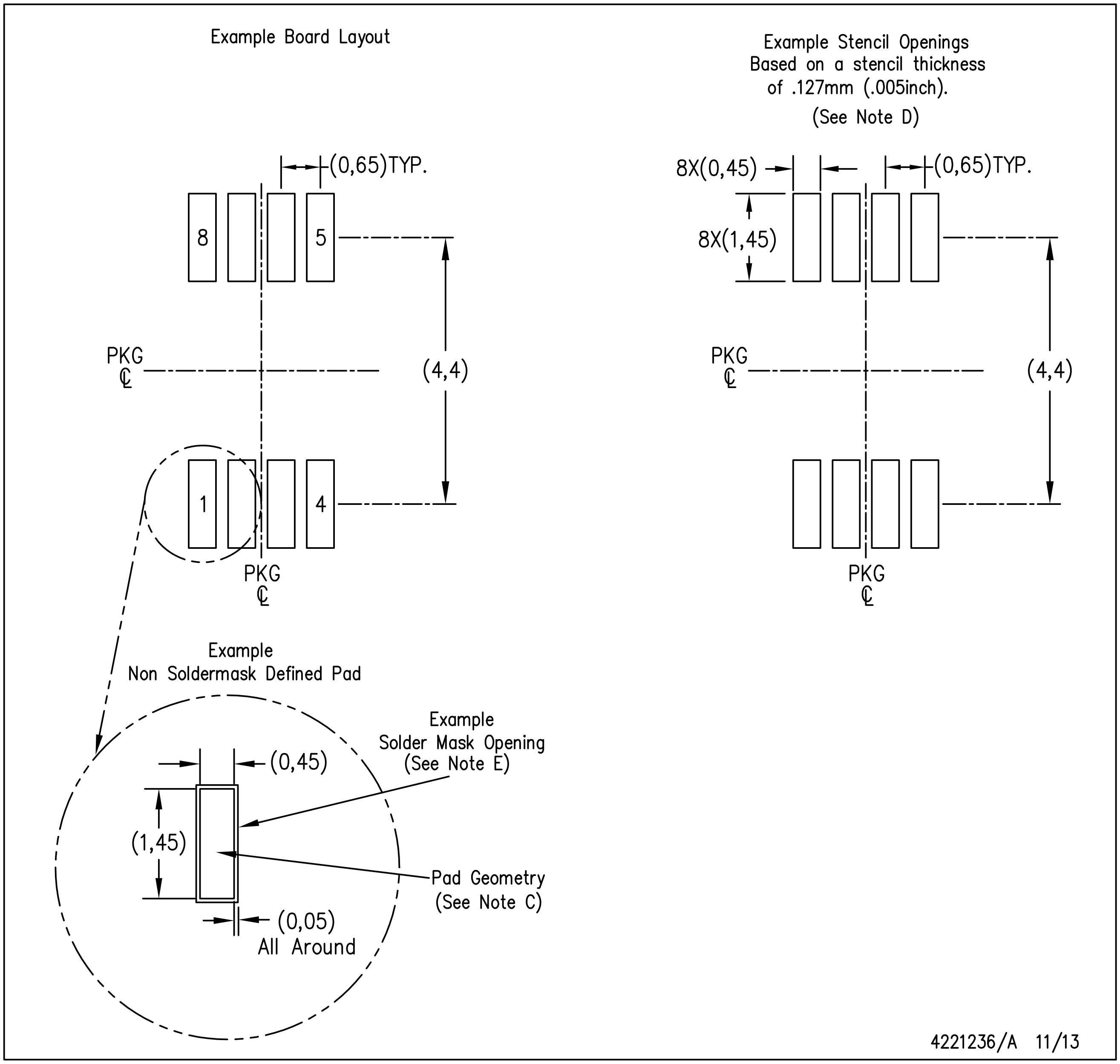
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

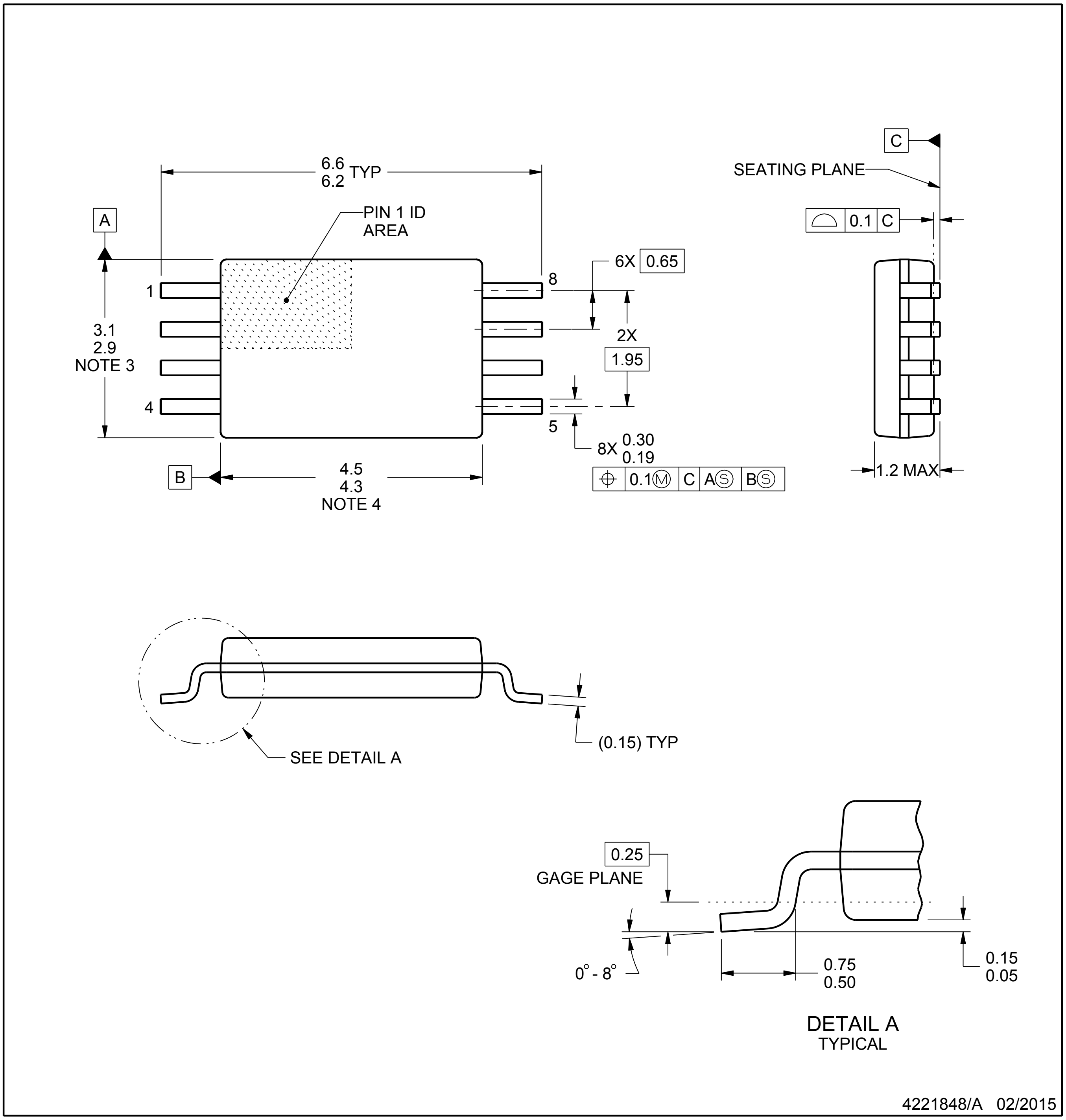


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE

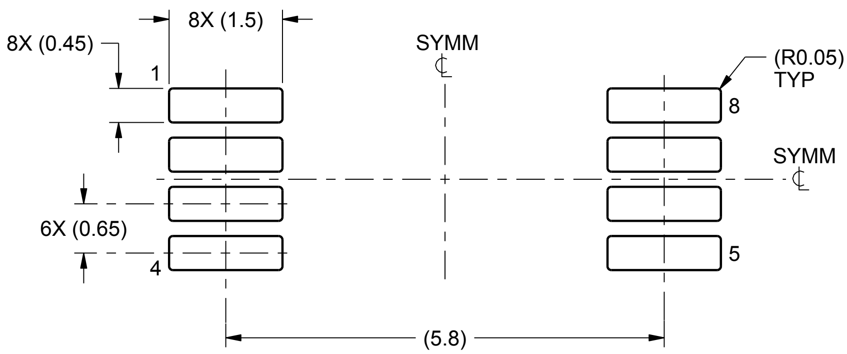


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

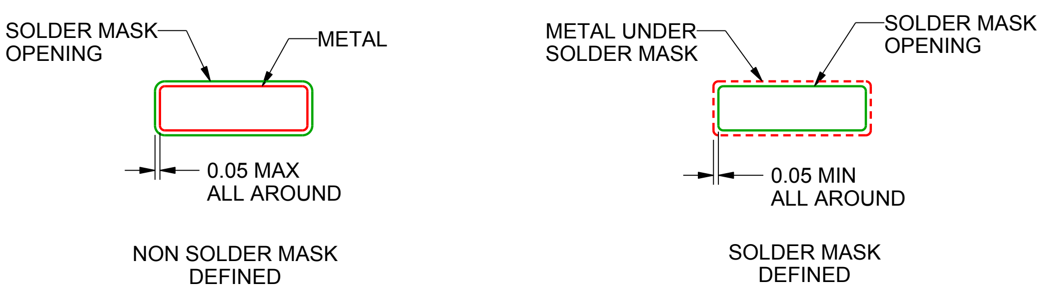


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

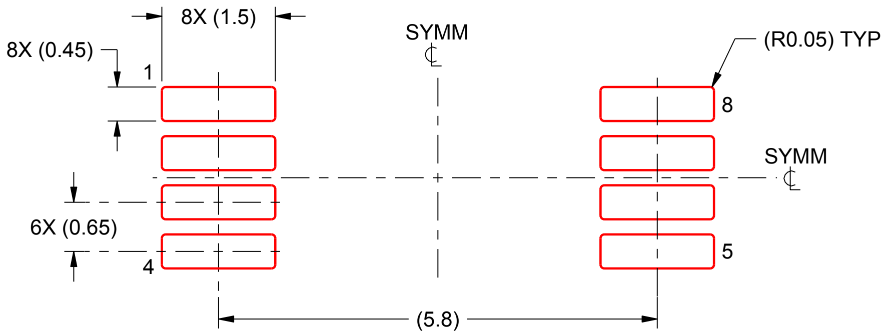


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

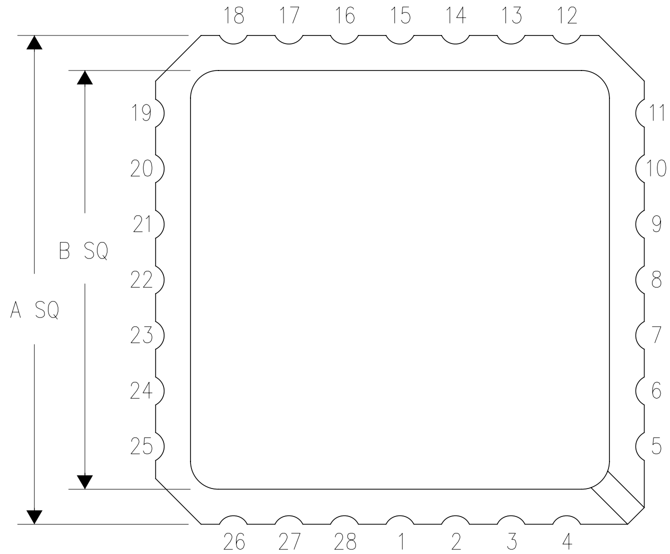
4221848/A 02/2015

NOTES: (continued)

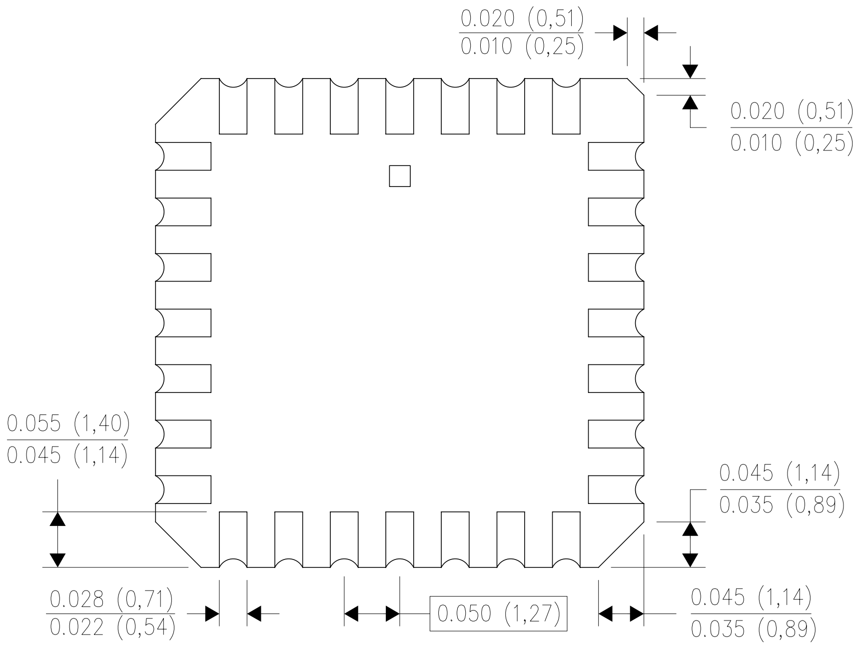
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

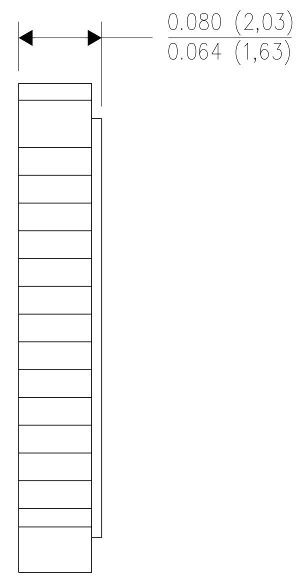
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)





4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004