APPLICATION NOTE for SMIA95-5M Auto Focus camera module Module model name : TCM8341MD Sensor model name : ET8EK8-AS

Ver. 2.30b

CONTENTS

a. Overview

This document specifies a very compact size of 1/2.5" 5M pixel auto-focus camera module compatible with SMIA95 size.

(1) SMIA95 size auto focus camera module suitable for the main stream cameras
(2) Superb picture quality by employing Toshiba's best-in-class 5 Mega-pixel CMOS sensor with 2.2 um pixel.
(3) Good object distance coverage by auto-focus actuator.
(4) Mitigated motion artifact for downsized picture by enabling 30 fps operation .

Table 1 General Overview

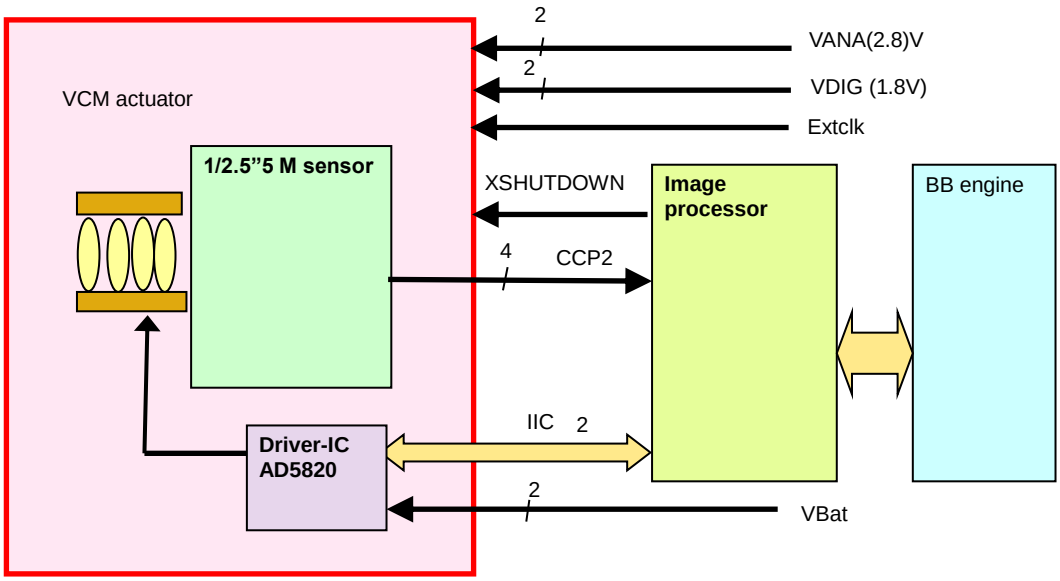
Area	Item	Type
Sensor (model name ET8EK8-AS)	Maximum Resolution	2592 (H) x 1968 (V)
	Color filtering type	Bayer
	Optical format	1/2.5 "
	Pixel size	2.2 um
Optical System	F number	F2.8
	Focusing type: fixed / auto focus	Auto Focus
Module System	Actuator Driver	Embedded inside camera Module
Data interface	Image data bus	CCP2 sub LVDS
	Supported output formats	10 bit RAW Bayer
	Control bus	IIC bus
Mechanical specification	Module size	9.5 (D) x 9.5(W) x 8.0(H) mm
	PAD count	16

VCM

(1) Operating Condition
- Actuator type: Voice Coil Motor
- Rated Current: 80mA
- Absolute Maximum Current : 100mA

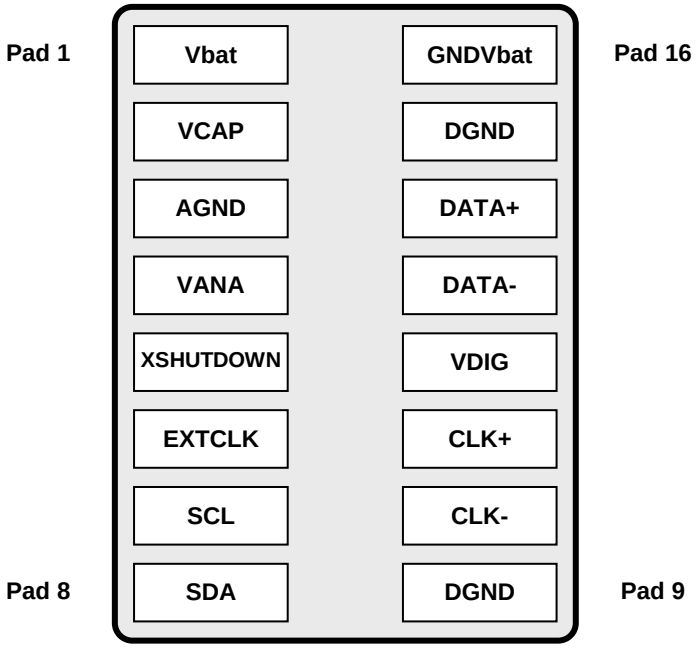
(2) Performance and Characteristics
- Stroke : min 0.31mm (at all directions, when applied 80mA)
- Starting Current : min 10mA (at horizontal direction)

b. System diagram



c. INTERFACE TERMINAL DESCRIPTION

Bottom view



Pad No.	*Signal name*	*Signal description*
1	Vbat	Battery voltage supply Can not be connected to VANA directly
2	VCAP	Open or can be connected to GND via a capacitor
3	AGND	Ground for VANA
4	VANA	Voltage source to camera module
5	XSHUTDOWN	Power down control
6	ExtClk	External clock signal from BB engine.
7	SCL	I2C clock
8	SDA	I2C data line
9	DGND	Digital GND
10	CLK-	CCP2 bus: Differential clock output, negative polarity signal
11	CLK+	CCP2 bus: Differential clock output, positive polarity signal
12	VDIG	Digital GND
13	DATA-	CCP2 bus: Differential data output, negative polarity signal
14	DATA+	CCP2 bus: Differential data output, positive polarity signal
15	DGND	Digital GND
16	GNDVbat	Ground for Battery voltage supply

1. Power supply control

1-1 Power up/down sequence

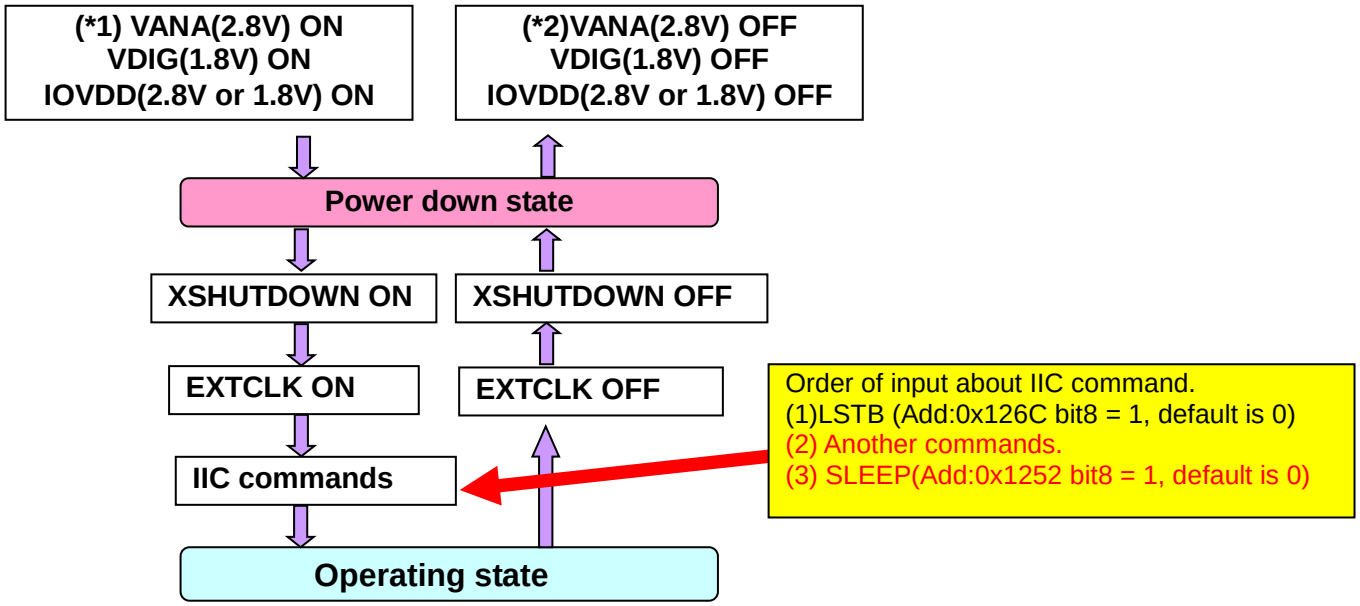


Fig1-1: Power up/down sequence

1-2 Timing chart of POWER ON

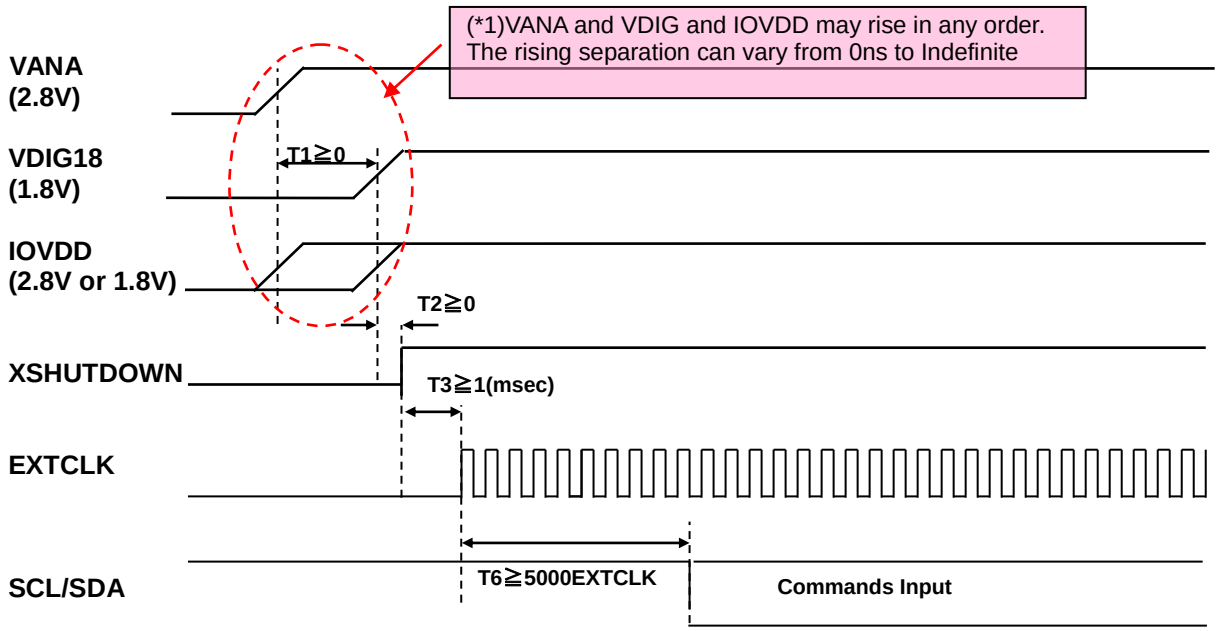


Fig1-2: Timing chart of POWER ON

1-3 Initial command settings

When power on, please set these commands only one time.
This initial setting is below status. Please also refer to command settings section.
(1) Serial out
(2)RAW10
(3)5M output, w/o embedded data, 640Mbps

Below file is initial command settings and changing history of setting based on mode2 (5M full output)
And also we recommended input order of register settings about both sensors.
This version is ver1.7


Command Setting_v1.7.xls

1-4 Timing chart of POWER OFF

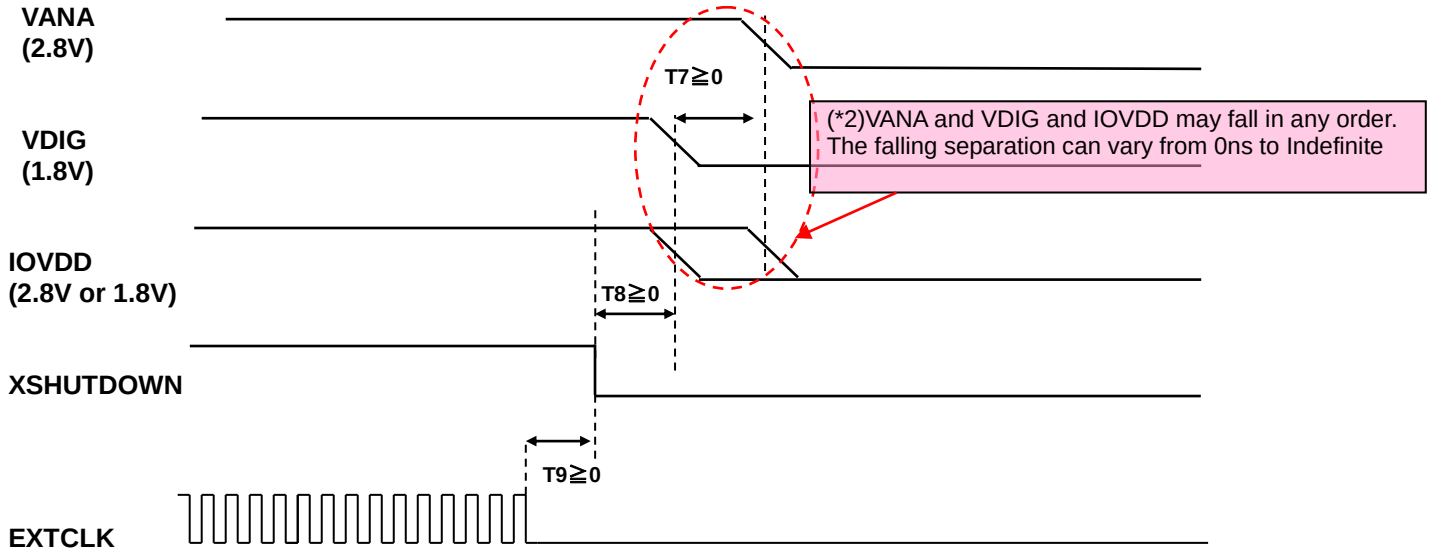


Fig1-3: Timing chart of POWER ON

1-5 Software Stand-by

If changing to software standby status, SLEEP set from H to L (Address: 0x1252, D7).

Address	Data	Bit Symbol	Description
0x1252	D7	SLEEP	0d: Software Standby status 1d: Streaming (Active)

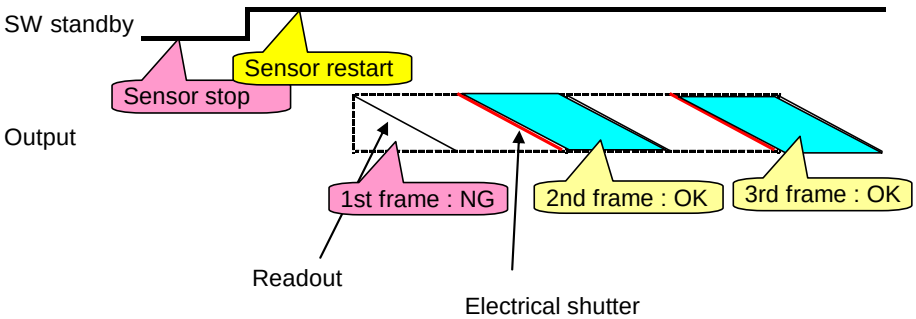
Software standby status

	CCI I/F	Sensor	CCP2	ISP	VCO
Software standby(*1)	Active	Stop	Hi-Z	Stop	Stop
Operation	Active	Active	Active	Active	Active

(*1)-Software standby is from High level of Xshutdown to first I2C command input
-During after input 30h (Add: 0x1252) and before input B0h (Add: 0x1252).

1-6 Image data of sensor restart

When sensor restarts, Normal image can get 2 frames after.



Firstly readout operation is started. And then Electrical shutter is started.

2. IIC control I/F

Sub address is 2 bytes, and first data is MSB, last data is LSB.

Write mode

S	Slave Address	0	A	Sub Address1	A	Sub Address2	A	DATA1	A	- - - - -	DATAn	A	P
	MSB 7bit			MSB 8bit		MSB 8bit		MSB 8bit					

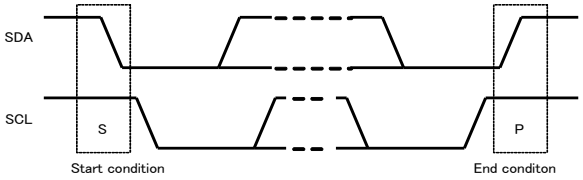
Read mode

S	Slave Address	0	A	Sub Address1	A	Sub Address2	A	S	Slave Address	1	A	DATA1	A	- - - - -	DATAn	N	P
	MSB 7bit			MSB 8bit		MSB 8bit			MSB 8bit			MSB 8bit					

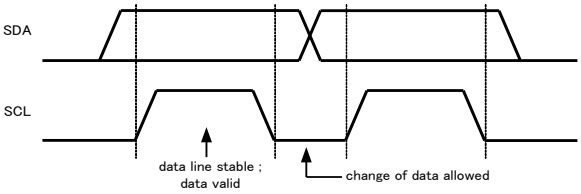
Host Command **Camera**

S : Start condition , P : End condition , A : Acknowledge, Ā : not Acknowledge

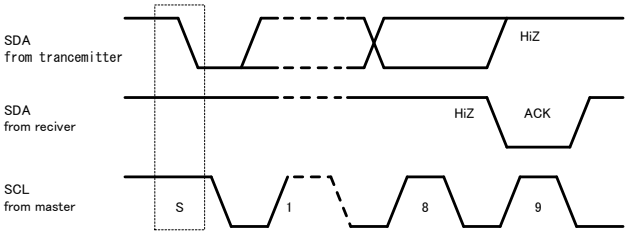
Start condition , End condition



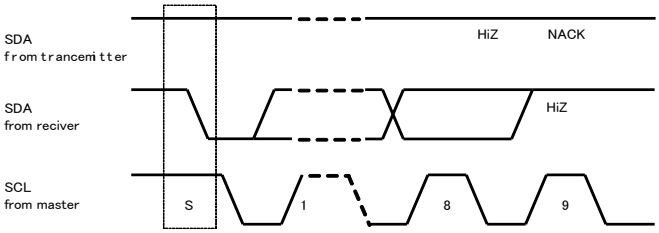
Bit Transfer



Acknowledge



Not Acknowledge



Slave Address (2 table can be selected)

Sensor

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	1	1	1	1	0	1/0

7bit Slave address is used.
The system conforms to the I2C Standard Specification defined by Philips.

Actuator driver

A6	A5	A4	A3	A2	A1	A0	R/W
0	0	0	1	1	0	0	1/0

3. Register map

Gray mesh area is not defined. Default value is recommended in white area.

Add	INIT	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x1100	00	R								
0x1101	00	R								
0x1102	00	R								
0x1103	00	R								
0x1104	00	R								
0x1105	00	R								
0x1106	00	R								
0x1107	00	R								
0x1108	00	R								
0x1109	00	R								
0x110A	00	R								
0x110B	00	R								
0x110C	00	R								
0x110D	00	R								
0x110E	00	R								
0x110F	00	R								
0x1110	00	R/W								
0x1111	00	R/W								
0x1112	02	R/W								
0x1113	00	R/W								
0x1114	02	R/W								
0x1115	00	R/W								
0x1116	00	R/W								
0x1117	00	R/W								
0x1118	00	R/W								
0x1119	00	R								
0x111A	00	R								
0x111B	00	R/W		TP_MODE[2-0]						
0x111C	0C	R/W								
0x111D	04	R/W								
0x111E	04	R/W								
0x111F	09	R/W								
0x1120	FC	R/W								
0x1121	80	R/W	CBH_MODE							
0x1122	06	R/W								
0x1123	C0	R/W								
0x1124	80	R/W	CBV_MODE							
0x1125	27	R/W								
0x1126	77	R/W								
0x1127	C0	R/W								
0x1128	00	R/W								
0x1129	30	R/W								
0x112A	00	R/W								
0x112B	40	R/W								
0x112C	01	R/W	DIN_SW[1-0]							
0x112D	30	R/W								
0x112E	30	R/W								
0x112F	30	R/W								
0x1130	0C	R/W	DL_RDIN[7-0]							
0x1131	0C	R/W								
0x1132	34	R/W								
0x1133	34	R/W								
0x1134	C0	R/W								
0x1135	80	R/W								
0x1136	00	R/W								
0x1137	00	R/W								
0x1138	80	R/W								
0x1139	80	R/W								
0x113A	80	R/W								
0x113B	80	R/W								
0x113C	00	R								
0x113D	00	R								
0x113E	08	R/W								
0x113F	32	R/W								
0x1140	01	R/W								
0x1141	00	R								
0x1142	00	R								
0x1143	41	R/W								
0x1144	10	R/W								
0x1145	3D	R/W								
0x1146	1C	R/W								
0x1147	14	R/W								
0x1148	1C	R/W								
0x1149	22	R/W								
0x114A	11	R/W								
0x114B	40	R/W								
0x114C	57	R/W								
0x114D	40	R/W								
0x114E	23	R/W								
0x114F	40	R/W								
0x1150	54	R/W								
0x1151	00	R/W								
0x1152	13	R/W								
0x1153	23	R/W								
0x1154	23	R/W								
0x1155	01	R/W								
0x1156	2B	R/W								
0x1157	D9	R/W								
0x1158	62	R/W								
0x1159	15	R/W								
0x115A	17	R/W								
0x115B	0B	R/W								
0x115C	11	R/W								
0x115D	1B	R/W								
0x115E	05	R/W								
0x115F	0E	R/W								
0x1160	27	R/W								
0x1161	14	R/W								
0x1162	00	R/W								
0x1163	38	R/W								
0x1164	52	R/W								
0x1165	80	R/W								
0x1166	35	R/W								
0x1167	70	R/W								
0x1168	02	R/W								
0x1169	56	R/W								
0x116A	80	R/W								
0x116B	30	R/W								
0x116C	30	R/W								
0x116D	08	R/W								
0x116E	33	R/W								
0x116F	1F	R/W								
0x1170	44	R/W								
0x1171	E4	R/W								
0x1172	C2	R/W								
0x1173	08	R/W								
0x1174	08	R/W								
0x1175	00	R/W								
0x1176	08	R/W								
0x1177	40	R/W								
0x1178	00	R/W								
0x1179	00	R								
0x117A	00	R								
0x117B	00	R								
0x117C	00	R								
0x117D	00	R								
0x117E	00	R								
0x117F	00	R								

Add	INIT	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x1200	00	R	VER_NUM[7-0]							
0x1201	00	R	VER_NUM[15-8]							
0x1202	00	R								
0x1203	00	R								
0x1204	00	R								
0x1205	00	R								
0x1206	00	R								
0x1207	00	R								
0x1208	00	R								
0x1209	00	R								
0x120A	00	R								
0x120B	00	R								
0x120C	00	R								
0x120D	00	R								
0x120E	00	R								
0x120F	00	R								
0x1210	00	R/W								
0x1211	78	R/W								
0x1212	02	R/W								
0x1213	FC	R/W								
0x1214	05	R/W								
0x1215	00	R/W								
0x1216	00	R/W								
0x1217	00	R/W								
0x1218	00	R/W								
0x1219	00	R/W								
0x121A	00	R								
0x121B	64	R/W		PIC_SIZE[2-0]				MONI_MODE[2-0]		
0x121C	10	R/W								
0x121D	64	R/W		H_SIZE[2-0]				H_INTERMIT[2-0]		
0x121E	00	R/W								
0x121F	80	R/W								
0x1220	7E	R/W	H_COUNT[7-0]							
0x1221	00	R/W						H_COUNT[10-8]		
0x1222	54	R/W	V_COUNT[7-0]							
0x1223	00	R/W				V_COUNT[12-8]				
0x1224	00	R/W			F_COUNT[5:0]					
0x1225	04	R/W	TBINV	RLINV						
0x1226	01	R/W								
0x1227	81	R/W								
0x1228	00	R								
0x1229	00	R								
0x122A	00	R/W								
0x122B	00	R/W								
0x122C	00	R/W								
0x122D	00	R/W								
0x122E	00	R/W								
0x122F	00	R/W								
0x1230	64	R/W								
0x1231	00	R/W								
0x1232	00	R/W								
0x1233	00	R								
0x1234	00	R								
0x1235	3F	R/W								
0x1236	00	R/W								
0x1237	80	R/W								
0x1238	02	R/W	CKVAR_DIV[0]				CKREF_DIV[3-0]			
0x1239	64	R/W	CKVAR_DIV[8-1]							
0x123A	06	R/W	VCO_DIV[3-0]				SPCK_DIV[3-0]			
0x123B	70	R/W	MRCK_DIV[3-0]				LVDSCK_DIV[3-0]			
0x123C	80	R/W	VCOSTP_X							
0x123D	01	R/W								
0x123E	00	R								
0x123F	00	R								
0x1240	00	R/W								
0x1241	54	R/W								
0x1242	03	R/W								
0x1243	2C	R/W	MES[7-0]							
0x1244	01	R/W	MES[15-8]							
0x1245	00	R/W								
0x1246	00	R/W								
0x1247	20	R/W								
0x1248	1F	R/W								
0x1249	20	R/W	MAG[7-0]							
0x124A	00	R/W					MAG[11-8]			
0x124B	80	R/W								
0x124C	00	R/W	MDG[7-0]							
0x124D	00	R/W	DGM_MODE[1-0]						MDG[9-8]	
0x124E	00	R/W			WB_BG[1-0]		WB_GG[1-0]		WB_RG[1-0]	
0x124F	40	R/W	WB_RG[9-2]							
0x1250	40	R/W	WB_GG[9-2]							
0x1251	40	R/W	WB_BG[9-2]							
0x1252	30	R/W	SLEEP							
0x1253	00	R								
0x1254	00	R								
0x1255	54	R/W								
0x1256	8A	R/W								
0x1257	00	R/W								
0x1258	08	R/W								
0x1259	01	R/W								
0x125A	01	R/W								
0x125B	00	R								
0x125C	00	R								
0x125D	08	R/W	CCP_LVDS_MODE				USE_PRED2	CCP_COMP_MODE[2-0]		
0x125E	E0	R/W			EMBEDDED_DATA					
0x125F	11	R/W								
0x1260	22	R/W								
0x1261	33	R/W								
0x1262	44	R/W								
0x1263	99	R/W								
0x1264	00	R/W								
0x1265	00	R/W								
0x1266	00	R/W								
0x1267	00	R/W								
0x1268	46	R/W								
0x1269	88	R/W								
0x126A	00	R								
0x126B	00	R								
0x126C	4C	R/W	LSTB							
0x126D	00	R								
0x126E	00	R								
0x126F	00	R								
0x1270	00	R								
0x1271	00	R								
0x1272	00	R								
0x1273	00	R								
0x1274	00	R								
0x1275	00	R								
0x1276	00	R								
0x1277	00	R								
0x1278	00	R								
0x1279	00	R								
0x127A	00	R								
0x127B	00	R								
0x127C	00	R								
0x127D	00	R								
0x127E	00	R								
0x127F	00	R								

Add	INIT	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x1400	00	R								
0x1401	00	R								
0x1402	00	R								
0x1403	00	R								
0x1404	00	R								
0x1405	00	R								
0x1406	00	R								
0x1407	00	R								
0x1408	00	R								
0x1409	00	R								
0x140A	00	R								
0x140B	00	R								
0x140C	00	R								
0x140D	00	R								
0x140E	00	R								
0x140F	00	R								
0x1410	13	R/W								
0x1411	04	R/W								
0x1412	7D	R/W								
0x1413	04	R/W								
0x1414	00	R/W								
0x1415	00	R								
0x1416	30	R/W								
0x1417	30	R/W								
0x1418	80	R/W								
0x1419	82	R/W								
0x141A	80	R/W								
0x141B	3F	R/W								
0x141C	80	R/W								
0x141D	00	R/W								
0x141E	00	R								
0x141F	00	R								
0x1420	F0	R/W								
0x1421	40	R/W								
0x1422	40	R/W								
0x1423	30	R/W								
0x1424	30	R/W								
0x1425	04	R/W								
0x1426	10	R/W								
0x1427	80	R/W								
0x1428	AB	R/W								
0x1429	80	R/W								
0x142A	80	R/W								
0x142B	80	R/W								
0x142C	80	R/W								
0x142D	80	R/W								
0x142E	80	R/W								
0x142F	80	R/W								
0x1430	80	R/W								
0x1431	00	R/W								
0x1432	00	R								
0x1433	00	R								
0x1434	55	R/W								
0x1435	10	R/W	PWB_RG[7-0]							
0x1436	00	R/W	PWB_GRG[7-0]							
0x1437	00	R/W	PWB_GBG[7-0]							
0x1438	80	R/W	PWB_BG[7-0]							

4. Sensor version information

This sensor can be recognized if reading below address data.

Address	Data	Bit Symbol	Description
0x1200	D7-D0	VER_NUM[7:0]	VER_NUM[15:0] =01h in case of #1Sensor.
0x1201	D7-D0	VER_NUM[15:8]	

5. Output-mode

This sensor has 14 modes of output. (7 type serial and 7 type parallel)

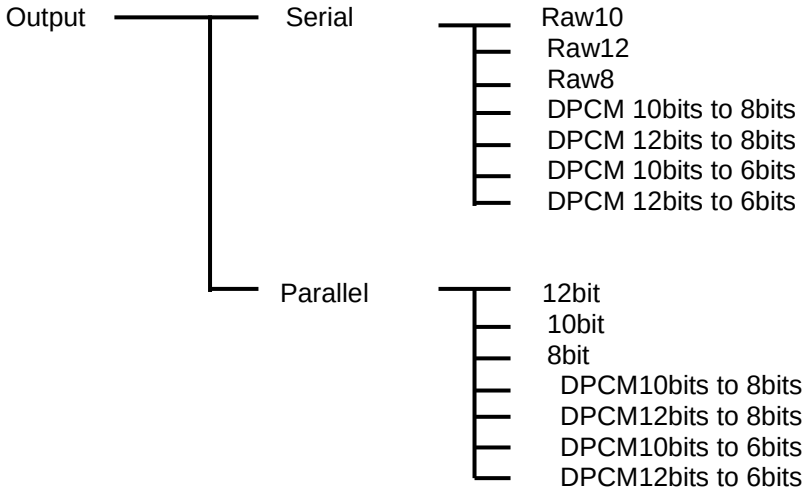


Table5-1: Explanation of Output-mode parameter

Address	Data	Bit Symbol	Description
0x125D	D7	CCP_LVDS_MODE	0h : Parallel output (default) 1h : Serial output
	D3	USE_PRED2	The predictor for DPCM compression. 0h : use predictor1 for DPCM 10bits to 8bits 1h : use predictor2 for other DPCMs (default)
	D2-D0	CCP_COMP_MODE[2:0]	**(1) Serial output case** 0h RAW10 1h RAW12 2h RAW8 3h DPCM 10bits to 8bits 4h DPCM 12bits to 8bits (default) 5h DPCM 10bits to 6bits 6h DPCM 12bits to 6bits **(2) Parallel output case** 0h 12bit 1h 10bit (from LSB to 2nd LSB output “L” level) 2h 8bit (from LSB to 4th LSB output “L” level) 3h DPCM 10bits to 8bits (from LSB to 4th LSB output “L” level) (default) 4h DPCM 12bits to 8bits (from LSB to 4th LSB output “L” level) 5h DPCM 10bits to 6bits (from LSB to 6th LSB output “L” level) 6h DPCM 12bits to 6bits (from LSB to 6th LSB output “L” level)

How to set DPCM

[1] DPCM 10bits to 8bits

(1) CCP_COMP_MODE = 3d
(2) USE_PRED2 = 0d
(3) MRCK = SPCK = 1/8 and MRCK=1/8,SPCK=1/7 and MRCK=1/8,SPCK=1/6

[2] DPCM 12bits to 8bits

(1) CCP_COMP_MODE = 4d
(2) USE_PRED2 = 1d
(3) MRCK = SPCK = 1/8

[3] DPCM 10bits to 6bits

(1) CCP_COMP_MODE = 5d
(2) USE_PRED2 = 1d
(3) MRCK = SPCK = 1/6

How to set MRCK and SPCK,
Please refer to the Section 9. PLL and Frame rate Setting when CCP2 output.

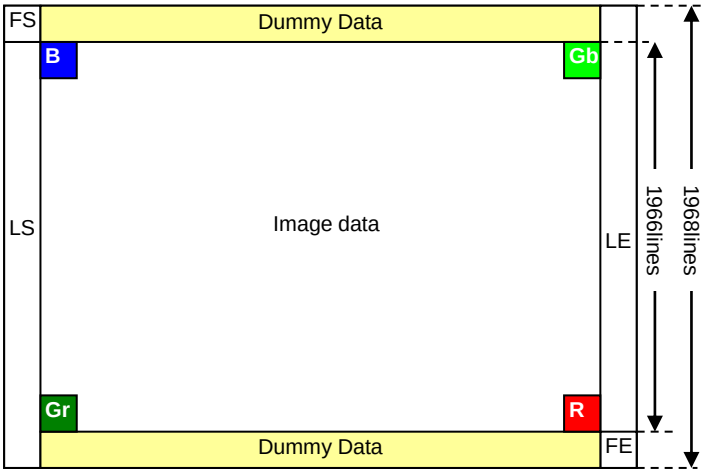
6. Start pixel information

Start pixel information is as follows.

(1) B pixel (In case of No top/bottom flip and No right/left flip)
(2) Gb pixel (In case of No top/bottom flip and right/left flip)
(3) Gr pixel (In case of top/bottom flip and No right/left flip)
(4) R pixel (In case of top/bottom flip and right/left flip)

7. Data output specification

This sensor has dummy data at 1st line and end line.
All of output mode(e.g.binning mode/crop mode) have dummy data.
5M full output case (No top/bottom flip and No right/left flip)



Dummy data specification

RAW10 case
0A 07 07 07 55 07 07 07 07 55 07 ・・・・・・ 07 07 07 07 55

RAW8 and other format
0A 07 07 07 ・・・・・・ 07

Dummy bit of multiple of 32 in serial output mode
Dummy data is without 0x00

With or without Dummy data can be selected by a resister. (Add:0x125E, D5. Resister name is EMBEDDED_DATA. 0h:OFF(without dummy data) 1h:ON(with dummy data) ,default setting is 1h)

Fig7-1: In case of WITH dummy data

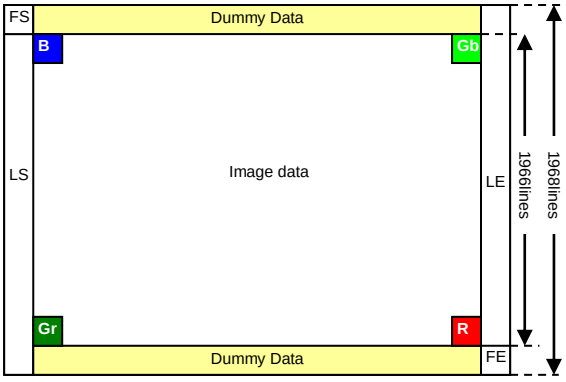
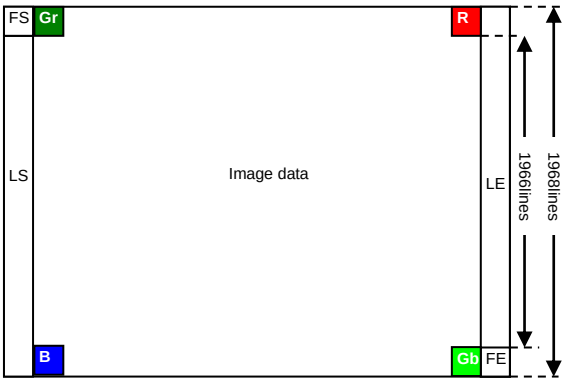


Fig7-2: In case of WITHOUT dummy data



8. Command effect timing

If changing parameter setting, input at period of imaging data. Setting parameter will be effected next frame.
About electrical shutter, will be effected 2 flames after.

In detail, Command latch timing from FE are following formula.
LTfFE(=Latch Timing from FE) = V blanking -7 (line)
These values depend on mode setting. Also refer to “column M” in a excel sheet at Page14

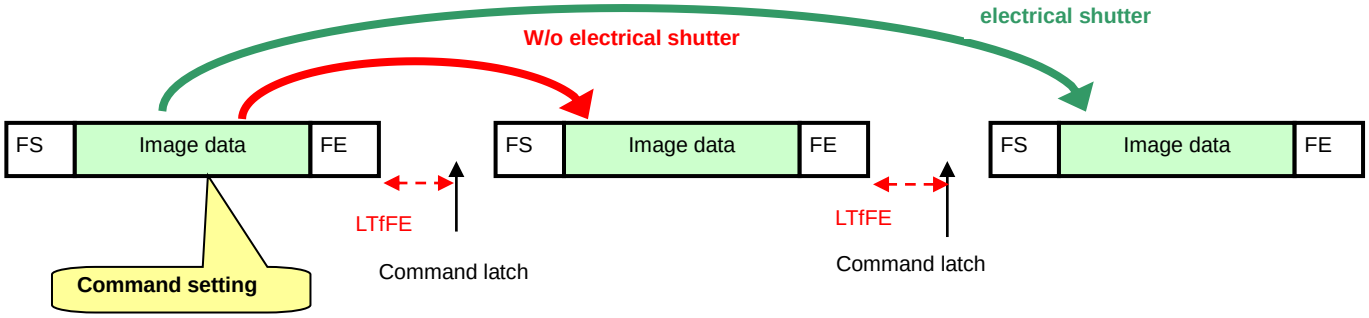


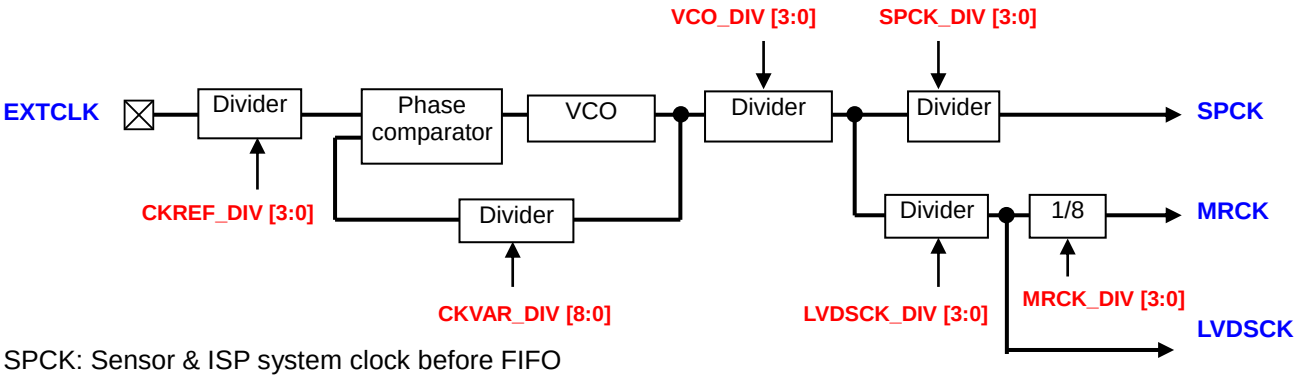
Fig8-1: Command effect timing

9. PLL and Frame rate setting when CCP2 output

(1) About CCP2 output case, please keep to the following relation of frequency

LVDSCK : MRCK = 8 : 1 (w/o DPCM 10bits to 6bits)

(2) Fastest frame rate will be needed, relation(1) and VCO_DIV=0d(x1 setting)



SPCK: Sensor & ISP system clock before FIFO
MRCK: 1/8 of CCP2 data rate

Fig9-1: PLL circuit

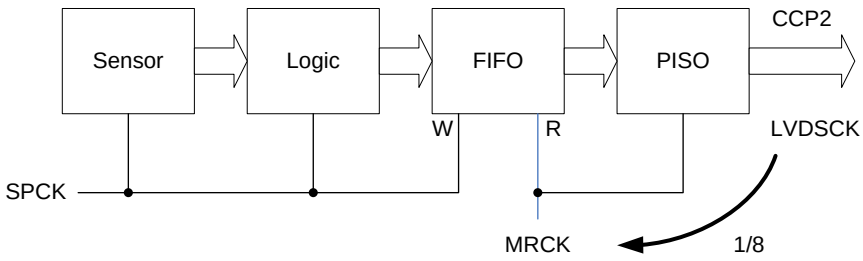


Fig9-2: Relation between SPCK, MRCK and LVDSCK

Table9-1: Explanation of PLL parameter

Address	Data	Bit Symbol	Description
0x1238	D3-D0	CKREF_DIV[3:0]	Selection of reference clock for PLL 0d: 1/1, 1d: 1/2 , 2d: 1/3 , 3d: 1/4 ,,,, 15d: 1/16
0x1239	D7-D0	CKVAR_DIV [8:0]	Selection of divider clock for PLL 0d to 15d : N/A , 16d: 1/16 , 17d: 1/17 ,,,, 510d: 1/510 , 511d: 1/511
0x1238	D7		
0x123A	D7-D4	VCO_DIV[3:0]	Selection of divider of VCO clock 0d: 1/1, 1d: 1/2 , 2d: 1/3 , 3d: 1/4 ,,,, 15d: 1/16
	D3-D0	SPCK_DIV[3:0]	Selection of divider for Clock for LOGIC 0d: 1/1, 1d: 1/2 , 2d: 1/3 , 3d: 1/4 ,,,, 15d: 1/16
0x123B	D7-D4	MRCK_DIV[3:0]	Selection of divider for Clock for LOGIC 0d: 1/1, 1d: 1/2 , 2d: 1/3 , 3d: 1/4 ,,,, 15d: 1/16
	D3-D0	LVDSCK_DIV[3:0]	Selection of divider for LVDS clock 0d: 1/1, 1d: 1/2 , 2d: 1/3 , 3d: 1/4 ,,,, 15d: 1/16

Detail of PLL and Frame rate setting, please refer to below a excel sheet (table2).
This version is ver1.7.

Stingray_Sensor_Mo
de_Setting_Calculatc

Formula is as follows

VCO [MHz] = EXTCLK * CKVAR_DIV / 3

CCP2 [Mbps] = VCO / { (LVDSCK_DIV + 1) * (VCO_DIV + 1) }

spck [MHz] = VCO / { (SPCK_DIV +1) * (VCO_DIV + 1) }

Frame rate [fps] = { spck / (IA_H * IA_V) } * 1,000,000
(IA_H and IA_V : H and V values of Image area readout with blanking.)

10. Picture size and View finder setting

10-1 Picture size setting

Table10-1: Explanation of output format parameter

Address	Data	Bit Symbol	Description
0x1221	D2-D0	H_COUNT[10:0]	Selection of total horizontal clock count including blanking Please refer to excel sheet of table of Setting rage(*1)
0x1220	D7-D0		
0x1223	D4-D0	V_COUNT[12:0]	Selection of total Vertical line count including blanking Setting rage is from 84d to 2730d.
0x1222	D7-D0		
0x1225	D7	TBINV	ON/OFF of vertical inversion 0d: OFF(normal), 1d:ON (vertical flip)
	D6	RLINV	ON/OFF of horizontal inversion 0d: OFF(normal), 1d:ON (horizontal flip)
0x121D	D6-D4	H_SIZE[2:0]	Horizontal CROP mode 0d:1/6, 1d: 1/4, 2d: 1/3, 3d: 1/2, 4d: 2/3, 5d: 3/4, 6d-7d: no crop (=full)
	D2-D0	H_INTERMIT[2:0]	Horizontal digital scaling mode 0d:1/6, 1d:1/4, 2d: 1/3, 3d:1/2 4d-7d: 1/1(=full)
0x121B	D6-D4	PIC_SIZE[2:0]	Vertical CROP mode 0d:1/6, 1d: 1/4, 2d: 1/3, 3d: 1/2, 4d: 2/3, 5d: 3/4, 6d-7d: no crop (=full)
	D2-D0	MONI_MODE[2:0]	Horizontal pixel binning mode 0d:1/6, 1d:1/4, 2d: 1/3, 3d:1/2 4d-7d: 1/1(=full)
0x1224	D5-D0	F_COUNT[5:0]	Selection of intermittent frame output mode 0d: 1/1, 1d: 1/2 , 2d: 1/3 , 3d: 1/4 ,,,, 63d: 1/64

Below excel sheet is table of H_count setting range.

Reccomend H_COUNT ra

If Night mode setting like a long exposure is needed, please increase value of V_COUNT (not slowing down of vco/pixclk).

10-1-1 Output format setting

Please refer to a excel sheet at Page 11(table2)

10-2 VGA view finder with zoom setting

Please refer to a excel sheet at Page 11 (table3)

10-3 How to digital zoom in case of VGA

Please refer to a excel sheet at Page 11 (digital zoom page)

11. Analog gain and Digital gain setting

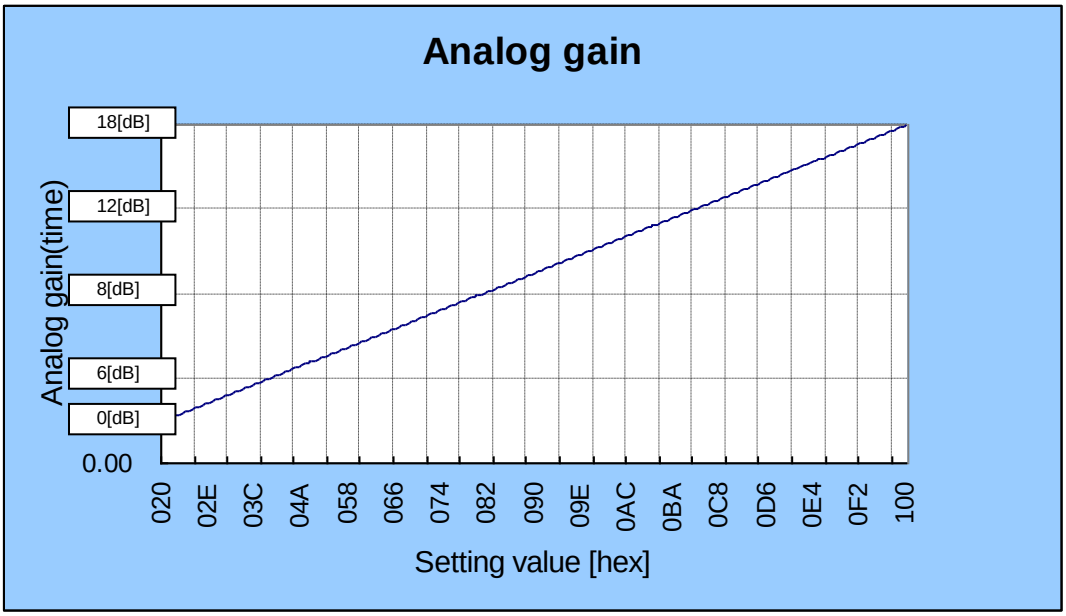
Table11-1: Explanation of Gain setting parameter

Address	Data	Bit Symbol	Description
0x124A	D3-D0	MAG[11:0]	Analog gain setting 20h: 0dB, 40h: 6dB, 80h: 12dB, 100h: 18dB(max recommended)
0x1249	D7-D0		
0x124D	D1-D0	MDG[9:0]	Gain setting of digital gain 0h: x1, 3FF: x 2 (Normal mode) (**Depend on setting of DGM_MODE)
0x124C	D7-D0		
0x124D	D7-D6	DGM_MODE[1:0]	0d : from x1 to x2 1d : from x0 to x2 2d : from x1 to x3 3d : from x0 to x4

11-1 Analog gain

Analog gain can be changed by MAG [11-0]. (Add:0x1249 Data:D7-D0 and Add:0x124A Data:D3-D0)

Analog gain [dB] = 20*log10 (setting value(decimal) /32)
Setting range is from 0x020 to 0x100.



11-2 Digital gain

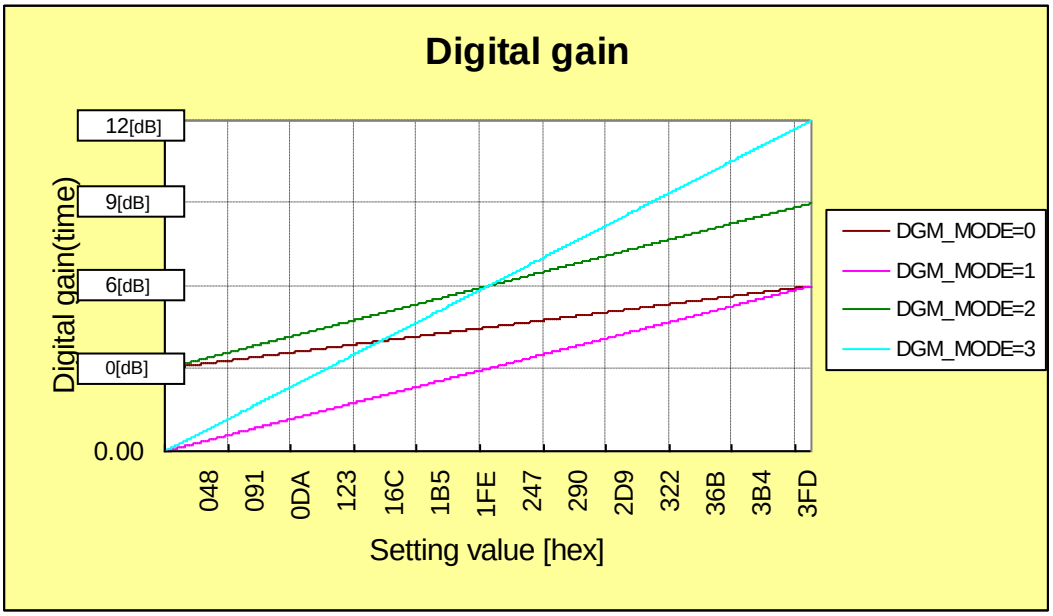
Digital gain can be changed by MDG [9-0]. (Add:0x124C Data:D7-D0 and Add:0x124D Data:D1-D0)
Changing DGM_MODE(Add:124D D7-D6), characteristics of digital gain can be changed.

DGM_MODE=0d
Digital gain[dB] = 20*log10(1/1023*Setting value(hex)+1)

DGM_MODE=1d
Digital gain[dB] = 20*log10(2/1023* Setting value(hex))

DGM_MODE=2d
Digital gain[dB] = 20*log10(2/1023* Setting value(hex)+1)

DGM_MODE=3d
Digital gain[dB] = 20*log10(4/1023* Setting value(hex))



13. Preset gain and White balance gain

Table13-1: Explanation of White balance parameter

Address	Data	Bit Symbol	Description
0x1435	D7-D0	PWB_RG[7:0]	Pre-set gain for Red pixel (00h:x1, FFh:x3)
0x1436	D7-D0	PWB_GRG[7:0]	Pre-set gain for G pixel in Red line. (00h:x1, FFh:x3)
0x1437	D7-D0	PWB_GBG[7:0]	Pre-set gain for G pixel in Blue line. (00h:x1, FFh:x3)
0x1438	D7-D0	PWB_BG[7:0]	Pre-set gain for Blue pixel（00h:x1, FFh: x3)
0x124E	D1-D0	WB_RG[9:0]	Gain setting of B digital gain for white balance 0h: x0, 100h: x1, 200h: x2, 3FFh: x 4
0x124F	D7-D0		
0x124E	D3-D2	WB_GG[9:0]	Gain setting of G digital gain for white balance 0h: x0, 100h: x1, 200h: x2, 3FFh: x 4
0x1250	D7-D0		
0x124E	D5-D4	WB_BG[9:0]	Gain setting of B digital gain for white balance 0h: x0, 100h: x1, 200h: x2, 3FFh: x 4
0x1251	D5-D4		
0x1439	D7	DIG_PWB_SW	Switch of Preset-White-balance (0d:disable / 1d:enable)

14. Electrical shutter

Table14-1: Explanation of Electrical shutter parameter

Address	Data	Bit Symbol	Description
0x1244	D7-D0	MES[15:0]	Setting of electrical exposure time 1h: 1H ~ FFFFh: 65535H (max)
0x1243	D7-D0		

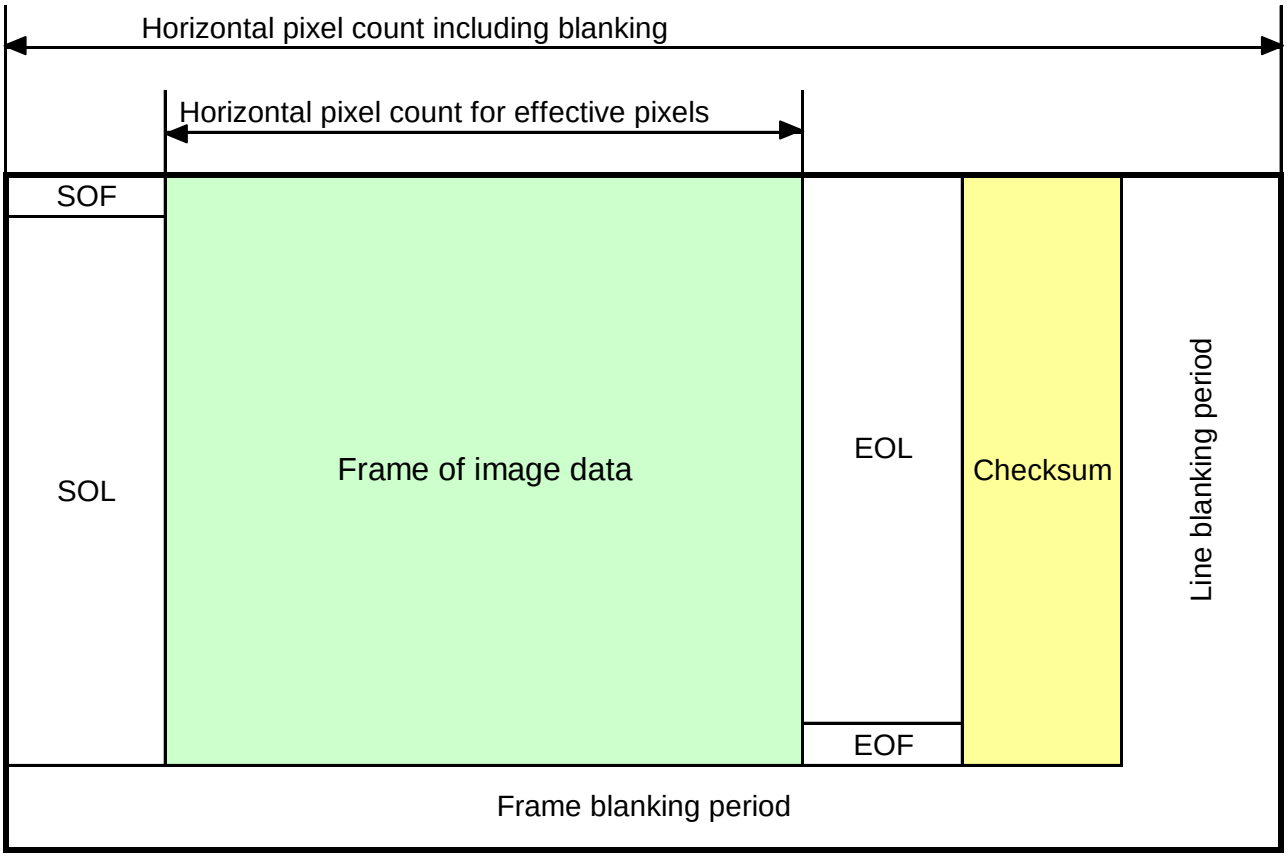
max exp time(MES) = VCOUNT value (=Total line numbers) - 4line

15. Data format of CCP2 Output

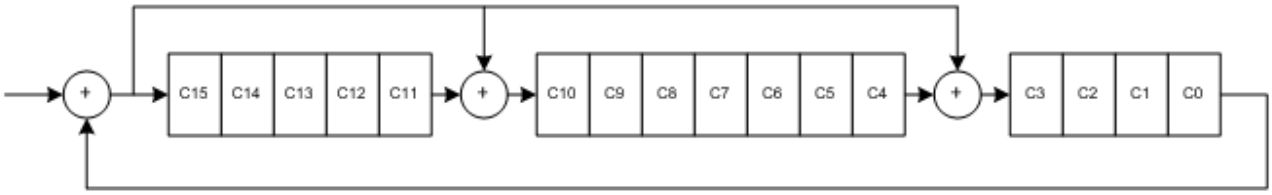
8 byte of synchronization codes are attached at the start and the end of each frame and each line.

	Code	Value
SOL	Line start code	FF_H 00_H 00_H 00_H
EOL	Line end code	FF_H 00_H 00_H 01_H
SOF	Frame start code	FF_H 00_H 00_H 02_H
EOF	Frame end code	FF_H 00_H 00_H 03_H

<Data structure in one vertical scan for CCP2 output>

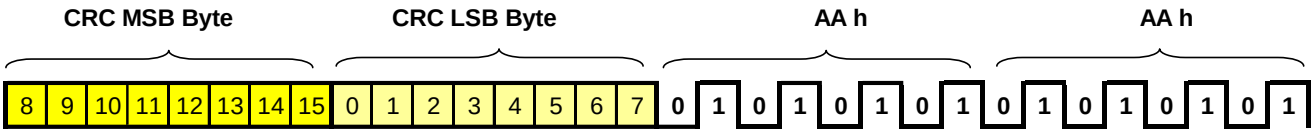


To detect possible errors in transmission, a checksum is calculated over each data line. The checksum is realized as 16-bit CRC. The generator polynomial is x^16+x^12+x^5+1. The checksum sequence is then padded with 16-bit padding sequence (101010 ---10) to fulfill the 32-bit word alignment requirement in the CCP link. The transmission of checksum is illustrated in the figure below.



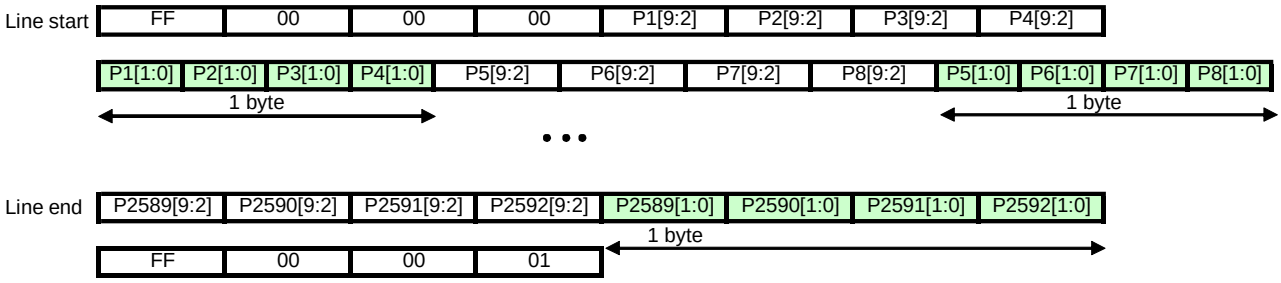
Polynomial: $x^{16} + x^{12} + x^5 + 1$

Note: C15 represents x^0, C0 represents x^{15}

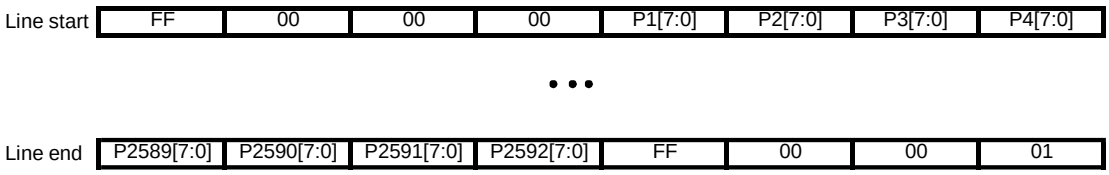


Data description in each byte in one line (LSB first expression)

(1) RAW10 case



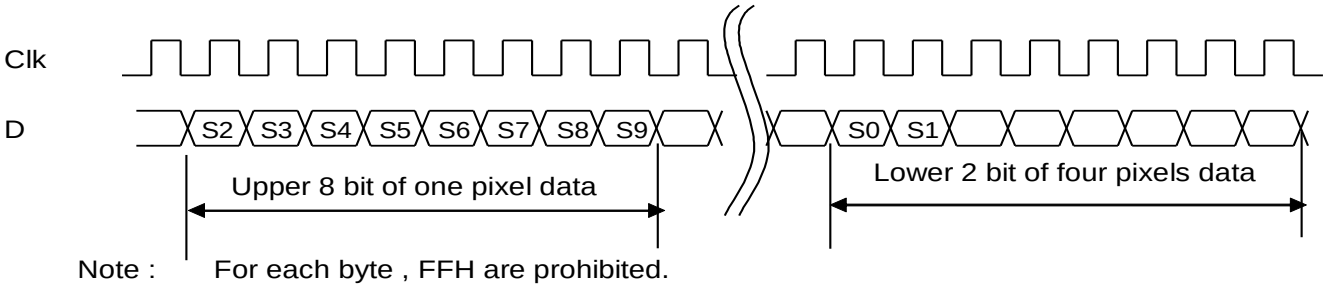
(2) RAW8,DPCM mode case



<Bit by bit structure>

Output mode of sensor raw data

Sensor raw data (R or G or B pixel by pixel)



Note : For each byte , FFH are prohibited.

10 bit sensor raw data are divided into upper 8 bit and lower 2 bit to send 10 bit depth data in 8 bit data scheme of CCP serial output. The following procedure and data arrangement is implemented to avoid 00h and FFh appearance in each 8 bit data.

(1) Sensor raw data range is compressed from 0 -1023 to 4 -1023 .
Namely 0-3 data are set to 4 .
This compaction does not affect the picture quality, because ,
for example, the black level is set to 64 level .

(2) 10 bit data (4 - 1023) is separated into upper 8bit and lower 2 bit.
The upper 8 bit has never all "0" value.
The four pixel data with 10 bit are arranged into the following five bytes.

1	upper 8 bit of pixel A
2	upper 8 bit of pixel B
3	upper 8 bit of pixel C
4	upper 8 bit of pixel D
5	4 of lower 2 bit for 4 pixels

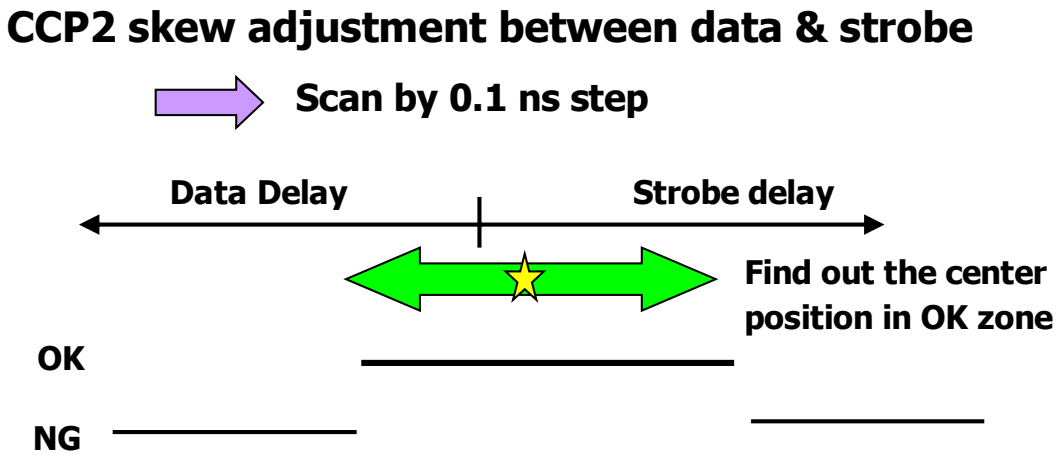
When all bits of No.5 byte are 0, 00h is replaced by 10h. In the LSB first form, “00001000” is used in conformity with CCP2 specification.

(3) The host rearranges the five bytes to 4 pixel data with 10 bit.

16. CCP2 Skew Adjustment

I²C command at 0x1269 address is used to adjust the delay of data and strobe signal in CCP2 to compensate skew between data and strobe. CRC data is checked for a certain pattern data by changing the data at address 0x1269 as 40h->30h->20h->10h->00h->01h->02h->03h->04h to find out OK zone. After that 0x1269 is set corresponding to the center of the OK zone.

Address	Data	Bit Symbol	Description
0x1269	D7-D4	CCP2SDLY[3:0]	CCP2 strobe signal delay adjustment 0h: No delay, 1h: 0.1nsec delay, 2h: 0.2nsec delay, ~ Fh: 1.5nsec delay
	D3-D0	CCP2DDLY[3:0]	CCP2 data signal delay adjustment 0h: No delay, 1h: 0.1nsec delay, 2h: 0.2nsec delay, ~ Fh: 1.5nsec delay
0x1268	D7	CCP2STP_X	CCP2 output ON/OFF 0h: ON(=operate), 1h: OFF(=stop)
0x1263	D4	CCP2CRCSW	CRC data output ON/OFF 0h: OFF, 1h: ON(CRC data are added)



17. Revision History

Revision	Date	Comments
Ver2.30a	21th Dec, 2008	Draft
Ver2.30b	11th May, 2009	Following yellow hatched items are added. Sensor/Module model name (P1,P3) Data format of CCP2 Output(P21) CCP2 Skew Adjustment(P24)