EE5733：數位通訊電路設計

(Digital Communication IC Design)

Instructor: 施信毓教授

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Objectives: You will learn digital-communication circuits by introducing basic concepts and modeling with Verilog.

Prerequisites: Logic Design

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Course Outline:

Lecture 1: Introduction

Lecture 1-1: Introduction to Digital IC Design Flow

Lecture 1-2: Hardware Description Language (HDL) - Verilog

Lecture 1-3: Hardware Modeling with the Verilog HDL

Lecture 2: Simulation & Testbench

Lecture 2-1: Event-Driven Simulation and Test-benches

Lecture 2-2: Logic System, Data Types, and Operators for Modeling in Verilog HDL

Lecture 3: Syntax of Verilog Model

Lecture 3-1: User-Defined Primitives

Lecture 3-2: Verilog Models of Propagation Delay

Lecture 3-3: Syntax, System Tasks, System Functions, and Compiler Directives

Lecture 4: Behavioral Descriptions in Verilog HDL

Lecture 5: Synthesis of Combinational Logic

Lecture 6: Synthesis of Sequential Logic

Lecture 7: Synthesis of Language Constructs

Lecture 8: Design Examples

Grading Policy:

- **No writing homework.**
- **Final exam** (**10%**) **@ Week 17**
- **Term project I: Teaching Edge** (**20%**)
- **Term project II: Combinational World** (**20%**)
- **Term project III: Enjoyable Party** (**30%**)
- **Term project IV: Checking Farmer** (**20%**)

< Details >

(1) **Term project I: Teaching Edge (TE)**

- Main purpose: **Learn to be a teacher, how to design the topics to test others and solve the problem in more details?**
- Each group has **2** students.
- Basic requirements:
  - For the chosen specified lecture, you should design **2** different topics with your innovative ideas to show what you learn in the lecture actually.
  - Under **4-page** oral presentation slides (at most) for each topic, the shown content should provide the following items,
    - Problem statement
    - Solving procedure
    - Final solution
- Totally at most **8 pages** for one group oral presentation with **15 minutes**. (No hard copy)
- Naming rule of presentation slides: **TE_GXX.ppt** (where XX is your group number)

(2) **Term project II: Combinational World (CW)**

- Each group has **2** students. (Group members should be very different with term project I).
- Main purpose: **Make familiar with pure combinational circuits in Verilog coding.**
- Basic requirements:
  - Develop an interesting game **(only combinational circuits)** with your innovative ideas.
  - Finish the RTL circuits.
  - Under **8-page** oral presentation slides, the shown content should provide the following items,
    - Game description in details

- ✧ C/Matlab test patterns verified
- ✧ Detailed hardware circuit with showing Verilog codes (*no more than 80 code lines*)
- ✧ Verification with testbench
- ✧ References: website, textbook, or other any possible study resources

- Totally at most **8 pages** for one group oral presentation with **15 minutes**. (No hard copy)
- Naming rule of presentation slides: **CW_GXX.ppt** (where XX is your group number)

(3) **Term project III: Enjoyable Party (EP)**

- Each group has **2** students. (Group members should be very different with term project I~II).
- Main purpose: **Solve the given IC problem/topic and develop the innovative thought with your team member co-operation.**
- Basic requirements:
  - ✓ Pass all of the test patterns in RTL-level for the given IC design topic.
  - ✓ Finish synthesis steps (showing area, speed, and power results) & pass all of the test patterns in gate-level.
- Totally at most **8 pages** for one group oral presentation with **15 minutes**. (No hard copy)
- Naming rule of presentation slides: **EP_GXX.ppt** (where XX is your group number)
- Also, you have to send out all your RTL Verilog codes in **only one file** (*.v) to **TA** by deadline of **11pm, the day before your oral presentation**. If you violate the hard rule, your term project score will be finally punished by discounted one half.
- Naming rule of your RTL Verilog file: **ep_gxx.v** (where xx is your group number)

(4) **Term project IV: Checking Farmer (CF)**

- Each group has **2** students. (Group members should be very different with term project I~III).
- Main purpose: **Have a precious opportunity to check other's Verilog codes.**
- Basic requirements:
  - ➢ You have to be assigned to check other's Verilog codes (from

different team at Term Project III: Enjoyable Party).
    - Find out the good and bad coding styles to show at the presentation stage.
- Totally at most **8 pages** for one group oral presentation with **15 minutes**. (No hard copy)
- Naming rule of presentation slides: **CF_GXX.ppt** (where XX is your group number)

< Attention for all of the term projects >

- **Grading criterion**:
    - **Completeness** (50%)
    - **Innovation** (50%)
- Presentation day:
    - Teaching Edge (TE): **2 weeks** after your chosen specified lecture is finished by the instructor.
    - Combinational World (CW): **@ Week 8**
    - Enjoyable Party (EP): **@ Week 15**
    - Checking Farmer (CF): **@ Week 18**
- You have to send out your presentation slides (*.ppt / *.pptx files) to **TA** by deadline of **11pm, the day before your oral presentation**. If you violate the hard rule, your term project score will be finally punished by discounted one half.