Fistful instruction set

Word length and bus width

The native word length and memory bus width of the fistful CPU is 12-bit. There is no distinction between registers and other memory, all 4096 12-bit address are directly accessible.

Register 4095 is the program counter (PC) and will be automatically incremented after each instruction has been processed.

Instruction set

Every instruction is a fixed 32-bit wide. The output is always stored in the first operand. The second operand can be either a register address, an immediate value or be ignored (in case of the identity and invert instructions).

The output of the compare operation will always be either 0x000 or 0xFFF.

All instructions can be made conditional through the first 3 bits of the instruction.

Jumps and conditional jumps can be executed by adding or subtracting from the program counter (register 4095) directly. However the program counter will be incremented by one after the instruction, this needs to be accounted for in the jump instruction.