Name:..... Reg. No.....

Department of Computer Science & Engineering
Motilal Nehru National Institute of Technology, Allahabad
End Semester (Theory) Examination (ODD-Semester) 2017-18
Class: MCA First Semester 2017-18
Subject: Digital Computer Organization(Code:CA-3103)

M.M. : 60 **Time: 3 Hrs**

Note: 1. Attempt any FIVE(05) questions including Q. No. (1) which is COMPULSORY to ALL.
2. All parts of a question should be answered in one attempt SEQUENTIALLY.
3. Write to the point, exactly what is asked.
4.Make & State necessary Assumptions clearly.

Q.No. 1 (COMPULSORY to ALL)

(A) Define the following terms in brief:
(i) **OS** (ii) **Cross Assembler** (iii) **Loader** (iv) **Linker** (v) **Macro processor** (vi) **Microprocessor** (vii) **Address** (viii) **ASCII Code** (ix) **I/O Controller** (x) **BIOS Program** (xi) **Mother Board** (xii) **Universal Gates** (xiii) **Lan Card** (xiv) **Power Card**

(B) Write down the program for **division** of **two 1-Byte numbers A& B (A div B : A>B) as discussed in the Class.**

(C) What is **Cache Memory?** What do you mean by **levels of cache?** Is the **cache memory** also Expandable as **RAM? Justify.**

(D) A CPU needs 512 X 8 RAM & 512X8 ROM with the help of available 128X8 RAM & 512X8 ROM. Trace a neat diagram for the following:
(i)Block diagram of the RAM chip (ii) Block diagram of the ROM chip
(iii) Relevant **Memory Address Map for the CPU (iv) Memory connection to the CPU**
(07+03+02+(1+1+2+4)=20)

Q.No. 2(A) Simplify the function $F(A,B,C,D)=\sum(0,1,2,5,8,9,10)$ using K-Map in SOP & POS forms.

(B) What is a **Multiplexer?**Trace Logic Diagram **&** Function Table for 4-to-1-Line Multiplexer.

(C) Define a **"BUS".** Construct a BUS System using 4X1 MUX for 4 Registers, each with Size of 4 bits.
(D) Convert $(9AFC)_{16}$ to binary & find it's $2^{'s}$ Complement. **(03+03+03+01=10)**

Q.No. 3 (A) Construct the following:
(i) **4-bit Adder – Subtractor** using Full Adder.
(ii) 4-bit Binary Incrementer using Half Adder.

(B) A digital Computer has a Common BUS System for 16 Registers of 32 bits each. The BUS is constructed with **Multiplexer**. Answer the followings:
(i) How many selection inputs are there in each **Multiplexer?**
(ii)What size of **Multiplexer** are needed?
(iii)How many multiplexers are there in the BUS.

(C) What is **"Negative Logic"?** **((03+03)+03+1=10)**

(....Continued on Page No. 02)

Q.No. 4 **(A)** Classify 8085 Instructions according to following **(with one example in each)**:
(i) Functions performed by the Instructions.
(ii) Size of Instructions
(B) Write down an Assembly Language program with proper comments for the followings:
(i) Sum of a Series of 8-Bit Numbers; SUM is also 8-Bit.
(ii) Product of two 8-Bit Numbers; Product is 8-Bit. **(04+(03+03)=10)**

Q.No. 5(A) What do you understand by **"Addressing Modes"** ? Discuss various Addressing Mode of **INTEL 8085** Microprocessor with Example.
(B) Trace a Logic for setting the bits of **Status Register** of a CPU.
(C) What is an **Instruction Cycle?** Explain properly.
(D) What is **Interrupt & PSW** ? Explain. **(03 + 02 +03 +02=10)**

Q.No. 6(A) Define the Followings in reference to **Control Memory**:
(i) Control Word (ii) Microinstruction (iii) microprogram (iv) Control Memory (v) Control Address Register (vi) Sequencer (vii) Pipe line Register (viii) Hard wired Control
(B) Explain properly **the Selection of Addresses for Control Memory**.
(C) Is it possible to design a Microprocessor without a microprogram? Are all microprogrammed Computers also Microprocessors. **(04+04+02 = 10)**

Q.No. 7(A) What is **Associative Memory**? Explain its organization using Block diagram. What is rol **of Argument, Key & Match Registers?** Explain with a simple example.
(B) Explain in brief **Match Logic** for **one word** of **Associative Memory** with relevant associated derivations.
(C) How **write operation** is performed in **Associative Memory?** **(04+04+02=10)**

Q.No. 8(A) What exactly we mean by **"Mapping Process"** in Cache Memory? Explain **any TWO** of the following "Mapping Process" in brief:
(i) Associative Mapping (ii) Direct Mapping (iii) Set-Associative Mapping
(B) Explain in brief : "Writing into Cache". **((03+03)+04=10)**

Q.No.9 Write Short Notes on any **FIVE** of the followings:
(A) Computer Generations **(B)** Flip-Flops **(C)** Stack Organized CPU
(D) Decoders **(E)** Counters **(F)** Booting steps of an IBM PC
(G) Hard Disk **(H)** Optical Disks **(I)** Pen Drive **(2 X 5 =10)**

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