

# Parity Generator & Parity Checker Using Sub-threshold Adiabatic Logic

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**Abstract**—Power dissipation becomes an essential criterion in VLSI system in the current ultra-low power applications scenario. Sub-threshold adiabatic logic designing has shown its potential as more efficient logic for ultra low energy-consuming circuits. Parity generator and parity checker are important combination circuit for error-free transmission of data. Both of these circuits are widely used for communication to encode the data. These circuits are realized using sub-threshold adiabatic logic (SAL) by deploying CADENCE 45nm technology. Extensive simulation study has been carried out to validate the mathematical expressions. Our study validates the enhanced circuit performance using sub-threshold adiabatic logic. The present work will facilitate researchers for circuit realization for energy applications.

**Index Terms**—Adiabatic Logic, Subthreshold regime, Parity generator, Parity Checker, Ultra low power

## I. INTRODUCTION

Power dissipation has become an important parameter in low power VLSI circuit designs because of the increasing application of portable electronic devices and the assessment of microelectronic technology. Various methods to considerably decrease the power dissipation of the circuits by decreasing supply voltage, load capacitance and switching activities. Adiabatic logic is one such technique to reduce the power dissipation in comparison to CMOS logic counterparts. In order to achieve the low power consumption the supply are gradually decreasing. Parity generators and parity checkers are combinational circuits that are widely deployed in digital systems for the detection of the single-bit errors in the transmitted data word. Adiabatic process is defined as a thermodynamic process in which there is no exchange of energy with the environment [1]- [6]. The power dissipation can be reduced by using adiabatic approach/mechanism. In adiabatic logic, the load capacitor re-utilizes the stored energy. Area required and delays are also comparatively lower in adiabatic logic as compared to conventional CMOS logic. The transistors count will also be nearly half. A static CMOS inverter circuit is shown in Fig. 1. After modelling these transistors have been modeled as optimal switches in conjugation with load capacitance and resistor as shown in Fig. 2(a),(b). The channel resistance of each transistor is equal to the resistor. Fig. 2 (c) shows the dc supply voltage in conventional CMOS. As the switch is turned on, there will be an abrupt flow of current through the resistance, and a charge  $Q$  is delivered to load capacitance  $C_L$  which is equal to  $C_L V_{DD}$ . The amount of

energy provided is  $E_{supply} = QV_{DD} = C_L V_{DD}^2$ . Partly the energy is stored in load capacitance, and the other half is consumed. During the charging operation, total energy consumption is

$$E_{Charge} = \frac{C_L V_{DD}^2}{2} \quad (1)$$

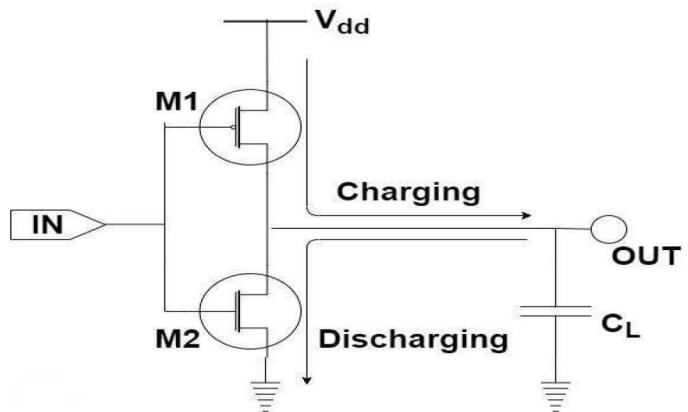


Fig. 1. Static CMOS inverter.

During the discharge operation, NMOS transistor is used to emancipate the load capacitance. Due to the charging and discharging operation in a conventional CMOS inverter the total energy consumption can be represented by the given equations:

$$E_{Total} = E_{Charge} + E_{Discharge} \quad (2)$$

$$E_{Total} = \frac{C_L V_{DD}^2}{2} + \frac{C_L V_{DD}^2}{2} \quad (3)$$

$$E_{Total} = C_L V_{DD}^2 \quad (4)$$

Whereas, the supply voltage applied to the adiabatic logic changes deliberately (e.g. ramped waveform) as shown in Fig. 2(c). The voltage drop across the resistor becomes small due to the ramp waveform voltage. Therefore, the current across the resistance will be small. As a result, the energy dissipation across the resistance during the charge-discharge operation decreases. Power can be represented as  $P = E_{Total}/T = C_L V_{DD}^2 f$ , if the supplied voltage is a

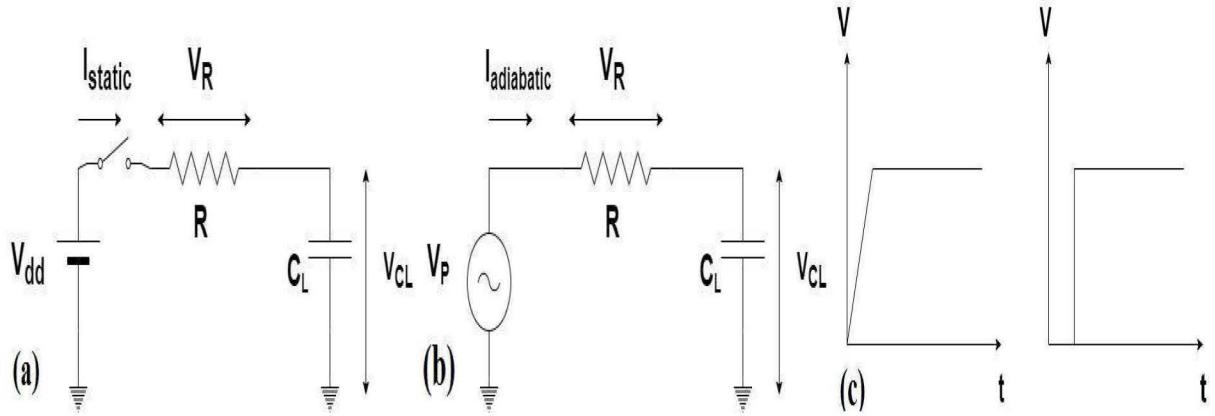


Fig. 2. (a) Circuit diagram with constant dc voltage source (used in CMOS logic); (b) circuit diagram with ramp voltage source (used in adiabatic logic); and (c) supply voltage plot of adiabatic logic and conventional CMOS logic respectively.

TABLE I  
CIRCUIT PARAMETERS OF PARITY GENERATOR AND CHECKER WITH CMOS LOGIC AND SAL LOGIC AT 45 NM TECHNOLOGY NODE.

Supply voltage $V_{DD}$ (V)	CMOS parity checker power dissipation (nW)	CMOS parity generator power dissipation (nW)	SAL parity checker power dissipation (pW)	SAL parity generator power dissipation (pW)
0.4	3.528	508.273	11.15	7.82
0.6	5.718	710.344	17.44	11.01
0.8	6.119	778.237	18.98	11.99
1.0	6.566	882.311	20.75	13.17
1.2	36.73	1119.833	119.9	113.2

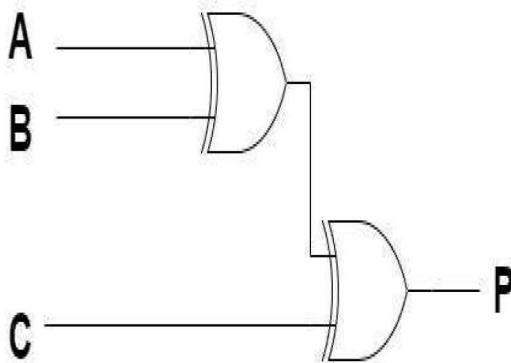


Fig. 3. Schematic of even parity generator.

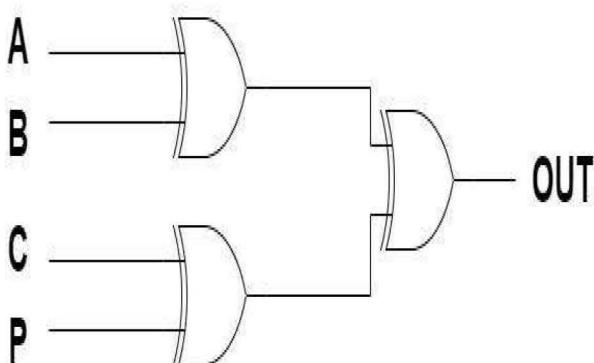


Fig. 4. Schematic of even parity checker.

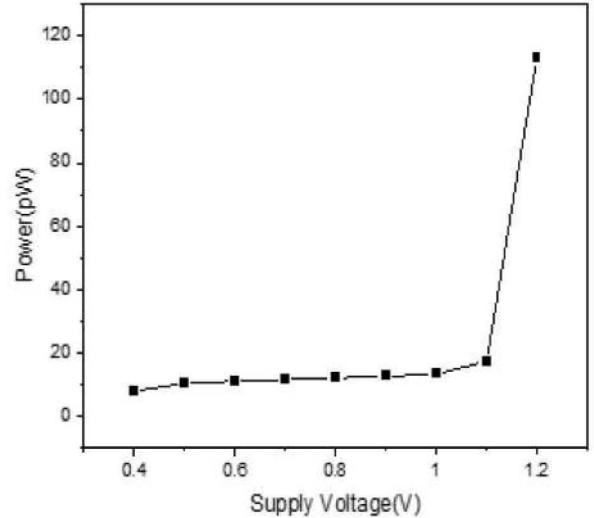


Fig. 5. Power dissipation as a function of the supply voltage curve for SAL parity generator.

ramped waveform with the period T (i.e. frequency  $f = 1/T$ ). Overall energy consumption for each operation in the above case is given by,

$$E_{Adiabatic} = k(PT) = kI^2RT = k[C_LV_{DD}^2/T]^2RT \quad (5)$$

Where,  $k$ =shape factor, shape of the clock edges decides the value of  $k$ . It can be concluded that when the signal period is adequately large, the energy consumption in adiabatic logic can be reduced

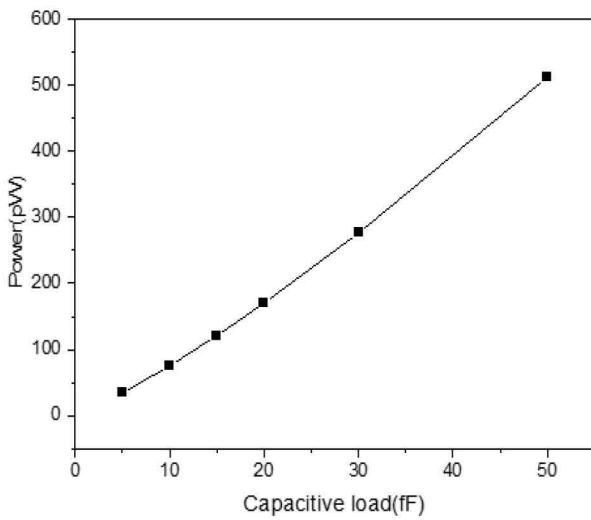


Fig. 6. Power dissipation as a function of capacitive loads, for SAL parity generator.

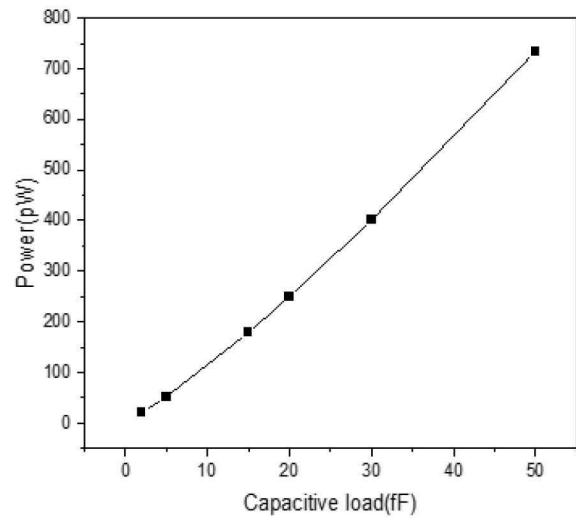


Fig. 8. Power dissipation versus capacitive loads for SAL parity checker.

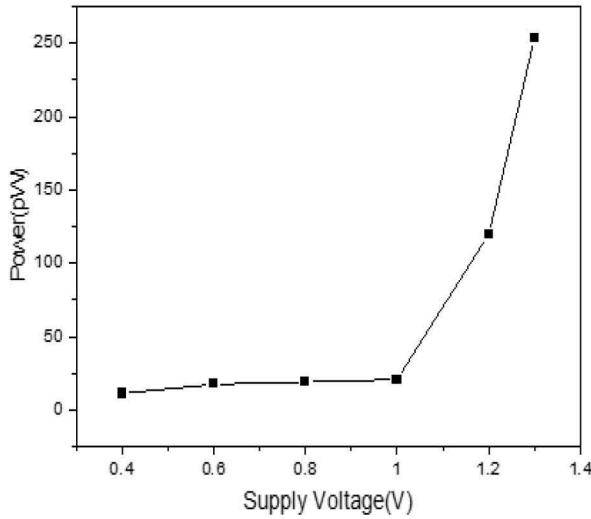


Fig. 7. Power dissipation as a function of the supply voltage, for SAL parity checker.

considerably as compared to CMOS logic. This logic has been widely used for many combinational circuits realization. Here two combinational circuits parity generator and parity checker circuits are realized using novel sub-threshold adiabatic logic (SAL) by deploying CADENCE 45 nm technology. Here the primary focus is on the power dissipation saving of the adiabatic logic based circuit realization.

The article is classified into three section including: basics of adiabatic logic is discussion in section II. In section III the operation of parity generator and checker circuit is discussed along with our simulation results findings. Finally, the conclusions are drawn in section IV.

## II. SUBTHRESHOLD ADIABATIC LOGIC

When  $V_{GS} < V_T$ , transistor operates in sub-threshold region. Due to minute leakage current sub-threshold region is operated which results in ultra-low power consumption. Sub-threshold adiabatic circuits is mainly adiabatic circuits which work in sub-threshold region. The analysis of  $I_D - V_{GS}$  characteristics of a NMOS transistor (W/L ratio:45 nm/45 nm) suggests that at  $V_{GS}=V_T$  (where  $V_T$  is the threshold voltage of MOSFET) drain current is not equal to zero because MOS already conducts at  $V_{GS} < V_T$ . This process is called “sub-threshold” or “weak-inversion” conduction [7]- [13].

For the long channel devices sub-threshold conduction is very negligible in OFF state. However it becomes very predominant for the scaled devices. There are many constituent leakage current components in a scaled transistor. In which this sub-threshold conduction dominates in the digital circuit designing. The gate leakage current is very minimal as compared to the this sub-threshold leakage current. The requirement of threshold current is inadmissible in most digital applications as it distracts from the behaviour of ideal switch. The delay of the circuit increases sharply since the driving current reduces exponentially. Therefore, SAL logic can only be applied to limited areas where performance is not of primary importance. The number of transistors used in conventional CMOS logic is almost double of that used in SAL. In low frequency regime SAL circuits are preferred over conventional CMOS logic [14]- [16].

## III. SIMULATION RESULTS AND DISCUSSION

### A. Parity Bit

Error Detection for the data transmission is most widely done using parity generating technique. Parity Bit is used to detect error. When transmission of binary data takes place in digital systems, data may be corrupted due to noise. Due to the noise, the data bits may change from 0s to 1s or 1s to 0s.

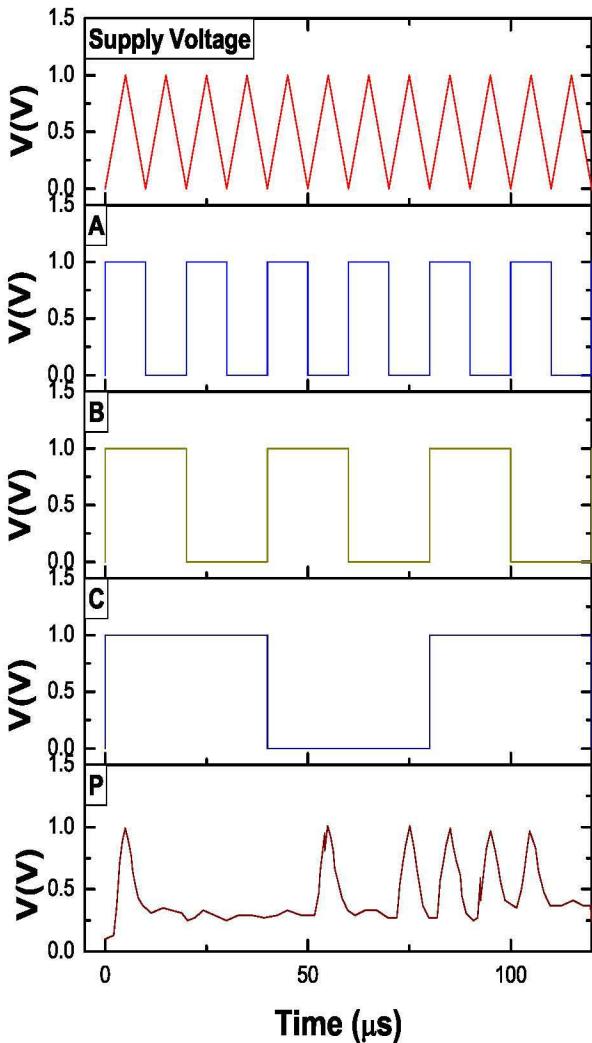


Fig. 9. Output waveform of SAL even parity generator for  $V_{DD}=1V$ ,  $C_L=2fF$ .

Parity Bit is added to the word containing data so as to make total number of 1's even and odd in even parity generator and odd parity generator, respectively. The message bits along with the parity bit is sent from transmitter side to receiver side. There will be no error in the data if the number of 1's in the receiver side matches with that of the transmitted bits. Ex-OR gates are used for implementing message signal's error detection and correction. Two input XOR gates produces 0 and 1 when the input bits are same and different respectively. The limitation of parity detection is that it can only detect an odd number of bit errors, i.e. if there are even number of errors in message signal the parity detection will give no error output.

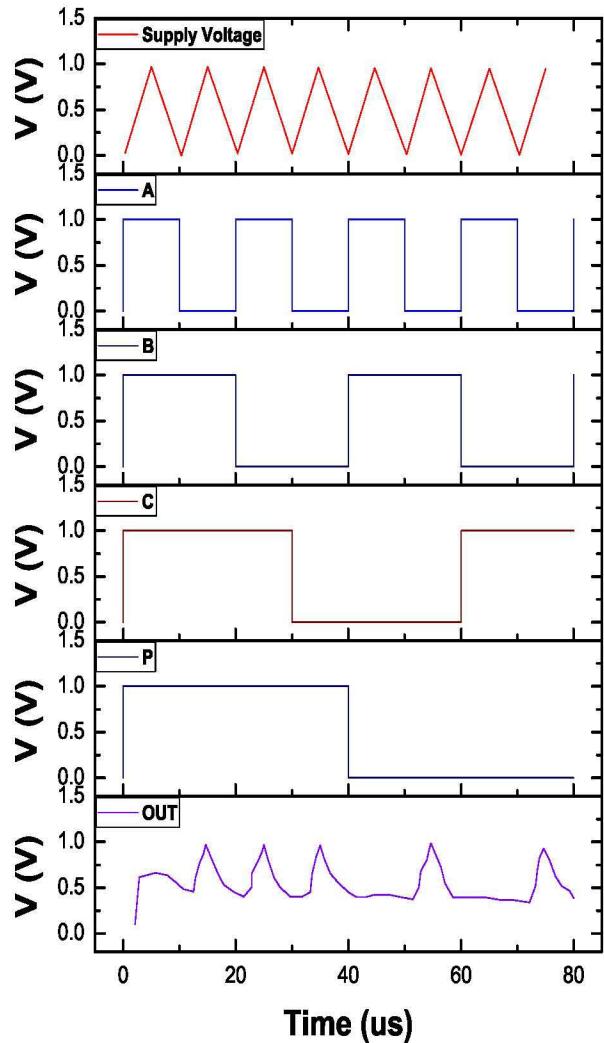


Fig. 10. Output waveform of SAL even parity checker for  $V_{DD}=1V$ ,  $C_L=2fF$ .

### B. Parity Generator

Generation of parity bits in the transmission end is done with the help of parity generator. Parity bit will make total number of 1's (data bit + parity bit) an odd amount in odd parity generator and an even amount in even parity generator. For e.g. even parity bit generator generates parity bit 1 if number of 1 in data bit is odd and parity bit 0 if number of 1 in data bit is even. Consider a three bit message A, B and C are applied to the transmitter end with an even parity bit P. A, B and C are applied as input to the even parity generator and P is the output. P will be 1 if total number of message bits is odd and 0 if total number of 1 is even. Schematic diagram of an even parity generator is shown in Fig. 3.

$$P = A \oplus B \oplus C \quad (6)$$

### C. Parity Checker

A combinational logic circuit that checks whether there is any error in the transmission of data bits. Let us consider that three bit data along with an even parity bit (i.e. generated using even parity generator) is at the transmitting end. We have simulated even parity checker circuit which checks the possibility of any error in the data on receiving end. The output of the circuit is 1 if there is an error in the data bits and it will be 0 if there is no error in the data bits. If there are even number of 1's in the data bits along with even parity bit, then no error occurs and output will be 0 and if there are odd number of 1's in the data bits along with even parity bit, then error occurs and output will be 1.

$$P_{out} = (A \oplus B) \oplus (C \oplus P) \quad (7)$$

Parity checker circuit can be implemented using three xor gate. The logic expression of the output is as given in eqn. 7. The circuit diagram for even parity checker circuit is shown in Fig. 4.

This simulation analysis has been carried out at 45 nm technology node with NMOS and PMOS transistor using SAL logic in CADENCE tool. Fig. 5 demonstrates the power dissipation with respect to supply voltage curve. Similarly Fig. 6 shows the power dissipation versus capacitive loads for SAL based parity generator. The power dissipation versus supply voltage for the SAL parity checker circuit is shown Fig. 7. In the same series power dissipation as a function of capacitive loads are shown in Fig. 8. From a brief perusal of Fig. 5 and Fig. 7, it can be concluded that with increase in supply voltage power dissipation increases linearly till 1 V and then it shows a sudden increase. Moreover, when the supply voltage is more than 1.2 V, we can get a wrong output. The capacitive load was considered to be constant at 2 fF. Similarly by observing the Fig. 6 and Fig. 8, it can be concluded that with increase in capacitive load power dissipation increases linearly keeping supply voltage constant i.e. 1 V. Fig.9 demonstrates the detailed variations for SAL even parity generator circuit. In Fig. 9, the first plot is of supply voltage; second, third and fourth plot are respective inputs. The fourth plot is of parity bit. The last plot is the output plot which is high when total number of 1's is not even, i.e., whenever there is an error in 1-bit while transmission. Fig. 10 illustrates the detailed variations for SAL even parity checker circuit. In Fig. 10, the first plot is of supply voltage; second, third and fourth plot are respective inputs. The last plot is of output i.e. parity bit. For parity generator, the adiabatic circuit has a considerably low power dissipation of 13.17 pW as compared to conventional CMOS logic, 882.3 nW. These findings are in accordance with the state-of-art of adiabatic logic [17]- [20]. For parity checker, the adiabatic circuit has a considerably low power dissipation of 20 pW as compared to conventional CMOS logic, 6.56 nW. The detailed performance comparison of SAL and CMOS based parity generator parity checker circuits is shown Table. 1. For CMOS circuit  $V_{DD}$  is the peak dc voltage connected and for SAL circuit  $V_{DD}$  is the peak ramp voltage applied.

### IV. CONCLUSION

In this study, we have designed the parity generator and parity checker using sub-threshold adiabatic logic (SAL) and compared with conventional CMOS logic. Our simulation concludes that the SAL reduces appreciable amount of energy as compared with conventional CMOS logic. The reduced power dissipation in sub-threshold adiabatic circuits is primarily due to the recycling of energy stored across these capacitive loads. CMOS circuits are preferred for application which requires exhaustive range of frequencies whereas SAL is preferred for application which requires low frequency of operation. Due to the low power dissipation it can be widely employed for the energy efficient devices.

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