



## L1: Introduction and Basic Device Models

VLSI3 - 227-0147-10L

© 2021 Prof. Dr. Christoph Studer and Oscar Castañeda

1

1

Who are we?

## About us

2

2

1

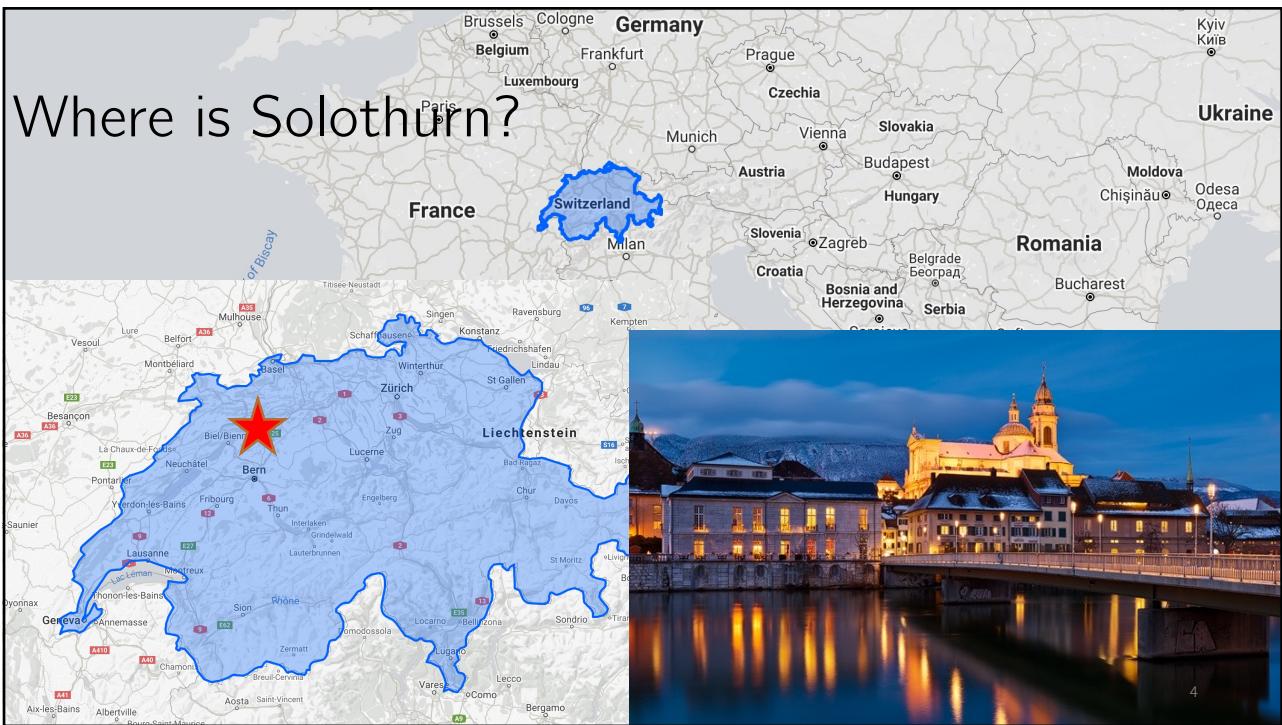
# Prof. Dr. Christoph Studer



- Born in Solothurn
- Matura Type B... from 1992 to 2000
- Dipl. Ing. in Elektrotechnik at ETH from 2000 to 2005
- Dr. Sc. in Elektrotechnik at ETH from 2006 to 2009
- Postdoc at ETH from 2009 to 2011
- Postdoc at Rice University from 2011 to 2013
- Assistant Professor at Cornell University from 2014 to 2019
- Associate Professor at Cornell and Cornell Tech from 2019 to 2020
- Since June 2020, Associate Professor in Integrated Information Processing at the Institute for Integrated Systems (IIS) at D-ITET

3

3

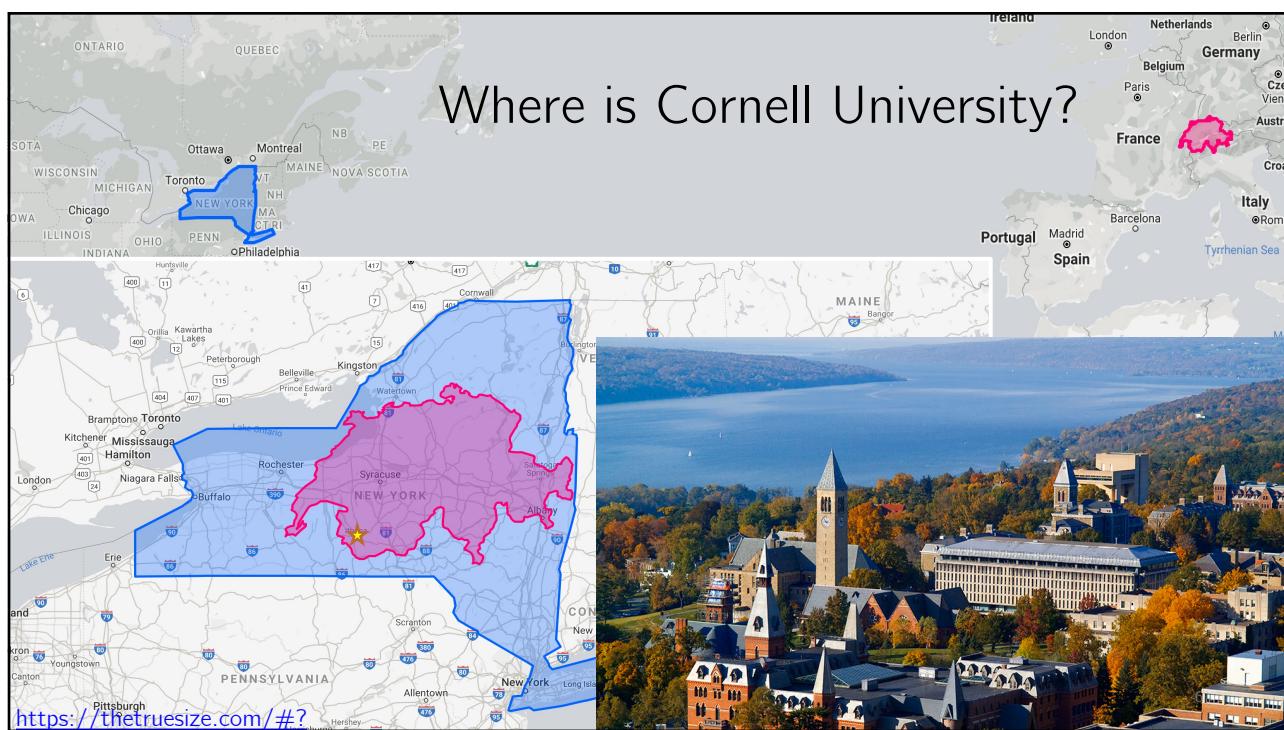


4

2



5



6



7

## Oscar Castañeda

- Born in Guatemala City
- B.Sc. in Electronics Engineering at Del Valle de Guatemala University from 2011 to 2015
- M.Sc./Ph.D. student in Electrical and Computer Engineering (ECE) at Cornell University from 2016 to 2020
- Since September 2020, Ph.D. student at ETH
- Research interests: Digital signal processing for multi-antenna wireless systems, emerging computer architectures and digital VLSI circuit and system design



8

8



9

## Research overview: Integrated Information Processing (IIP)

### Applications



### Theory & Algorithms

**Algorithm 1.** Suppose that  $\mathbf{H}$  satisfies (A) and (B0, Lem. 5.56) holds. Then, the complex Bayesian AMP (cB-AMP) algorithm performs the following steps for each iteration  $t = 1, 2, \dots$

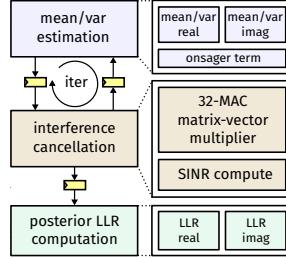
$$\begin{aligned} s^{t+1} &= \mathbf{F}(s^t + \mathbf{H}^\dagger r^t, N_0^{\text{post}}(1 + \tau^t)) \\ r^{t+1} &= \mathbf{y} - \mathbf{H}s^{t+1} \\ &\quad + \frac{\beta t}{2} \langle (\partial_1 \mathbf{F}^R + \partial_2 \mathbf{F}^I)(s^t + \mathbf{H}^\dagger r^t, N_0^{\text{post}}(1 + \tau^t)) \rangle \\ &\quad - \frac{\beta t}{2} \langle (\partial_2 \mathbf{F}^R - \partial_1 \mathbf{F}^I)(s^t + \mathbf{H}^\dagger r^t, N_0^{\text{post}}(1 + \tau^t)) \rangle \end{aligned} \quad (8)$$

$$\tau^{t+1} = \frac{\beta}{N_0^{\text{post}}} \langle \mathbf{G}(s^t + \mathbf{H}^\dagger r^t, N_0^{\text{post}}(1 + \tau^t)) \rangle,$$

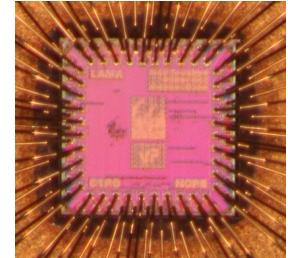
where the functions  $\partial_{(1,2)} \mathbf{F}^{(R,I)}(x + iy, \tau)$  are defined as

$$\begin{aligned} \partial_1 \mathbf{F}^R &\triangleq \frac{\partial \text{Re}\{\mathbf{F}(x + iy, \tau)\}}{\partial x}, \quad \partial_2 \mathbf{F}^R \triangleq \frac{\partial \text{Re}\{\mathbf{F}(x + iy, \tau)\}}{\partial y}, \\ \partial_1 \mathbf{F}^I &\triangleq \frac{\partial \text{Im}\{\mathbf{F}(x + iy, \tau)\}}{\partial x}, \quad \partial_2 \mathbf{F}^I \triangleq \frac{\partial \text{Im}\{\mathbf{F}(x + iy, \tau)\}}{\partial y} \end{aligned}$$

### Architectures



### Integrated Circuits



- We pursue a holistic research approach

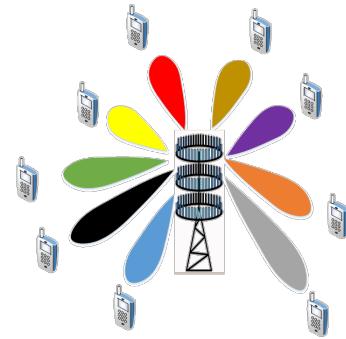
10

10

# Current research interests

## Theory and Algorithms for

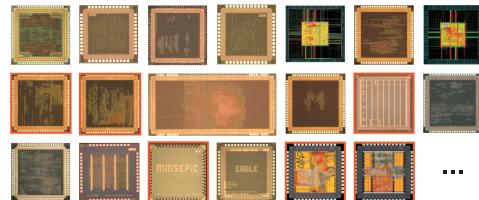
- Future multi-antenna communication systems (MIMO)
- Millimeter-wave and terahertz communication (beyond 5G)
- Real-time signal and image processing
- Machine learning



**Goal: More efficient integrated circuits through high-performance algorithms**

## Digital circuit design with

- application-specific integrated circuits (ASICs)
- field-programmable gate arrays (FPGAs)



**Goal: Demonstration of feasibility**

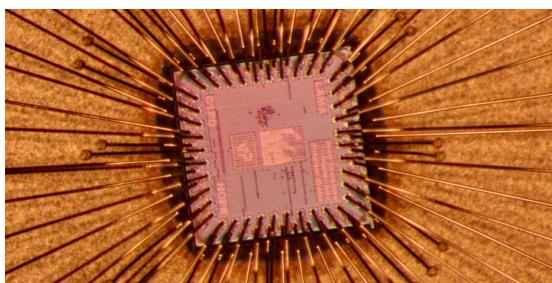
11

11

# Digital ASIC design

**Our research group develops new algorithms and corresponding digital integrated circuits for fifth-generation (5G) and beyond-5G wireless communication systems**

Three baseband-processing algorithms for 5G



28nm CMOS, 1.4x1.4mm<sup>2</sup>, ~1'300'000 transistors

Multi-antenna detector for beyond-5G (B5G)

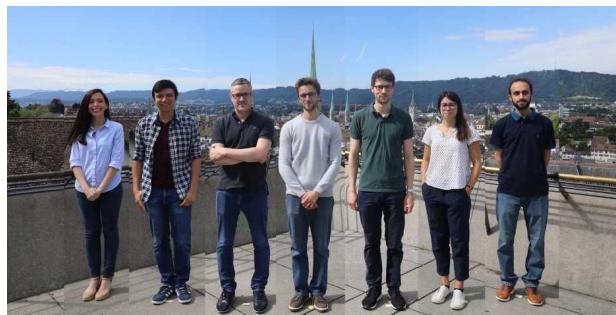


65nm CMOS, 2x4mm<sup>2</sup>, ~4'000'000 transistors

12

12

## Two research groups



- Seven Ph.D. Students at ETH (Group picture not up-to-date)
  - Two Ph.D. Students still at Cornell University in Ithaca... ☺

13

13

## General information

## About the course

14

---

14

## Please follow the ETH COVID rules!

- It is mandatory to wear a mask
- A valid COVID Certificate is required
- Observe distancing rules (1.5m if possible)
- Up-to-date rules at <https://ethz.ch/services/en/news-and-events/coronavirus.html>

15

15

## Lectures

- Lecturers:
  - Prof. Dr. Christoph Studer ([studer@ethz.ch](mailto:studer@ethz.ch))
  - Oscar Castañeda ([caoscar@ethz.ch](mailto:caoscar@ethz.ch))
- Mondays, 10:15-11:00 and 11:15-12:00 ETZ E8 (break from 11:00 to 11:15)
- Available for questions during the break and after the lecture

Number	Title	Hours	Lecturers
227-0147-10 V	VLSI 3: Full-Custom Digital Circuit Design   Permission from lecturers required for all students.	2 hrs	Mon 10-12 ETZ E 8 « <b>C. Studer, O. Castañeda Fernández</b>
227-0147-10 U	VLSI 3: Full-Custom Digital Circuit Design   Permission from lecturers required for all students.	3 hrs	Thu 13-16 ETZ G 91 « <b>C. Studer, O. Castañeda Fernández</b>

16

16

## zoom Information

- Lecture is broadcast and recorded on Zoom
  - No guarantee for good audio quality
  - Zoom questions will only be answered during the break  
→ Please write your questions in the chat
- Link <https://ethz.zoom.us/j/64681515513>
  - Meeting ID 646 8151 5513 and Password vlsi3eth21
- Direct Link:  
<https://ethz.zoom.us/j/64681515513?pwd=S2NBUmFZaHpFeEUwcmxrbXIqK20rdz09>

The screenshot shows the 'Meetings' section of the Zoom web interface. It displays a 'Personal Room' for 'Christoph Studer's Personal Meeting Room'. The room has a meeting ID of 232 870 4600 and a password of 101010. A 'Join URL' is also provided.

17

17

## Moodle for lecture notes

- Link: <https://moodle-app2.let.ethz.ch/course/view.php?id=15931>
- Link to Zoom
- Slides from lectures
- Discussion forum
- Video recordings of Zoom lecture
- Exercise documents and solutions
- Additional material

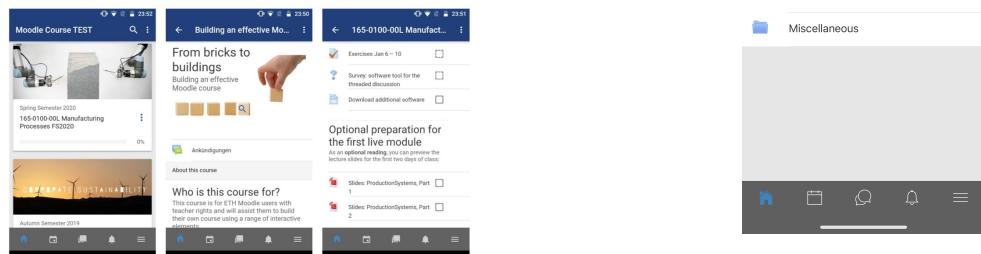
The screenshot shows the Moodle course page for 'VLSI 3: Full-Custom Digital Circuit Design 2021'. It includes a navigation bar with 'Dashboard' and 'Meine Kurse', and a 'Bearbeiten einschalten' button. Below the navigation is a 'General' section containing links to 'Course Website', 'Discussion Forum', 'Slides', 'Exercises', and 'Miscellaneous'.

18

18

# Moodle App

- Link: <https://blogs.ethz.ch/letblog/2020/09/11/eth-moodle-app/>
- Smartphone Apps
  - <https://apps.apple.com/app/id1521806822>
  - <https://play.google.com/store/apps/details?id=ch.ethz.ethmoodle>



19

19

# Moodle discussion forum

- Link: <https://moodle-app2.let.ethz.ch/mod/forum/view.php?id=637016>
- For questions about the lecture and exercises
- We will answer the questions
- **Students are also allowed to answer!**
- **Please do not post any solutions**

Discussion Forum

Questions and answers for lecture and exercises.

Add a new discussion topic

(There are no discussion topics yet in this forum)

[Course Website](#) [Jump to...](#) [Slides](#)

20

20

# Course website

<http://vlsi3.ethz.ch>

- Accessible within ETH network
- Here you can find:
  - All the previous links
  - Up-to-date class schedule

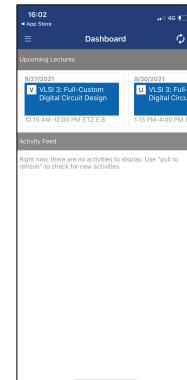
The screenshot shows the course website for "VLSI 3: Full-Custom Digital Circuit Design". At the top, it says "VLSI 3: Full-Custom Digital Circuit Design" and "Prof. Dr. Christoph Studer and Oscar Castañeda". Below that is a "Course Information" section for "Autumn Semester 2021". It lists the course code "227-0147-10 (Course catalogue)", lecture times "Monday, 10:00 - 12:00, ETZ E8", and exercise times "Thursday, 13:00 - 16:00, ETZ D61.1". There's also a "Book" section mentioning "CMOS VLSI Design: A Circuits and Systems Perspective (4th ed.)" by Neil H. E. Weste, David M. Haas, and Alan E. Steven, Addison Wesley, 2011. The "Online resources" section includes a note about Zoom and Moodle.

21

21

# Real-time clicker questions in lecture

- ETH EduApp: <https://eduapp-app1.ethz.ch/>
- Smartphone Apps
  - <https://itunes.apple.com/app/eth-eduapp/id1277289797?l=en&mt=8>
  - <https://play.google.com/store/apps/details?id=ch.ethz.eduapp&hl=en>
- Warm-up questions
- Interactive questions about the lecture
- Trivia and fun facts
- **Lecture feedback ← important!**
- **Clicker questions are not graded!**



22

22

## Clicker: Test Question

ETH

Edu



- Randomly choose an option from 1 to 4
- Agree on one option
- Same number of clicks per option

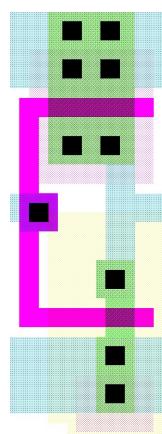
23

23

## Clicker: What is this?

ETH

Edu



1. Layout of a circuit ✓
2. An inverter ✓
3. CMOS logic ✓
4. A logic gate ✓

24

24

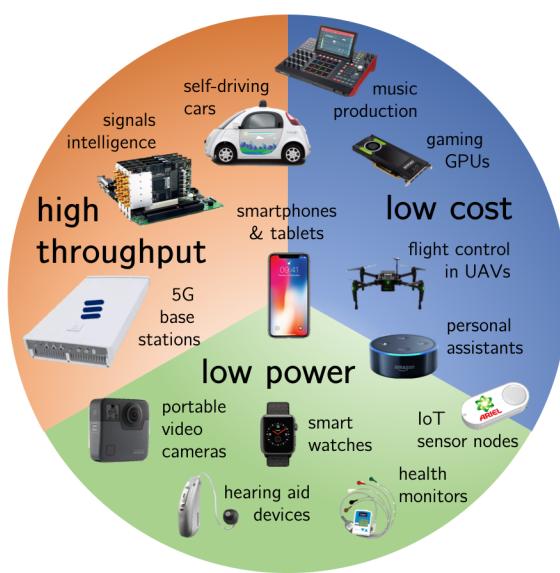
Asking the real question

## So... what is this course about?

25

25

VLSI is (almost) everywhere!

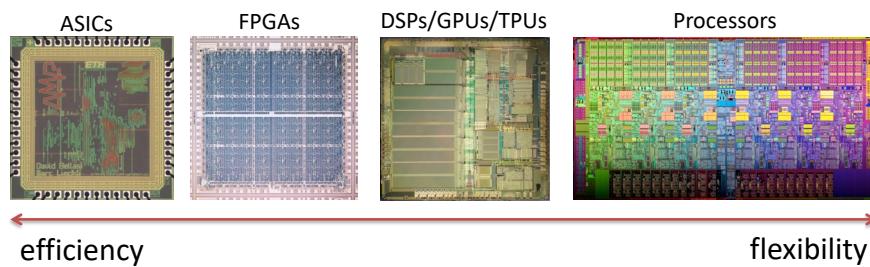


26

26

## VLSI comes in different flavors

- Application specific integrated circuits
- Programmable logic (e.g., FPGAs)
- Dedicated processors (e.g., DSPs, GPUs, AI accelerators)
- General-purpose processors



27

27

## VLSI courses at ETH

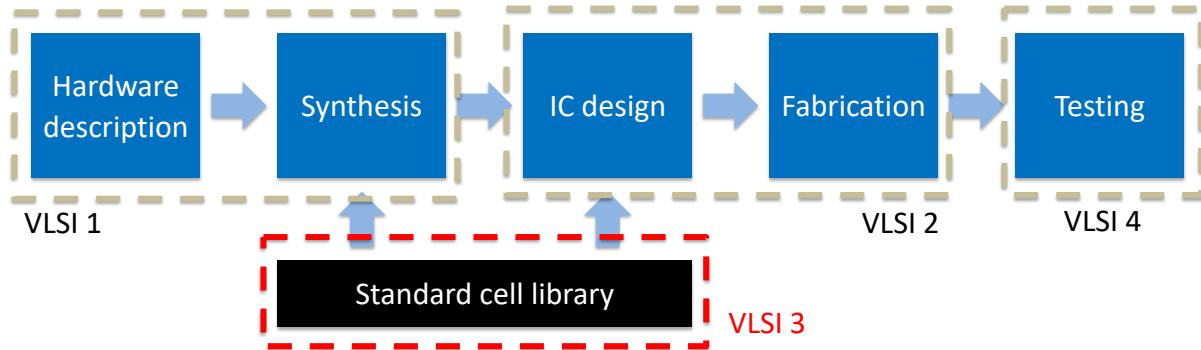
	<b>VLSI lecture series</b>		<b>Other lectures</b>	<b>Bachelor / Semester / Master Theses</b>
<b>Fall</b>	<b>VLSI1</b> Tue 08-10 Wed 13-16 HDL design - FPGAs	<b>VLSI3</b> Mon 10-12 Thu 13-16 Transistor level digital	<b>AIC</b> Fri 10-12 Fri 14-16 Transistor level analog	
<b>Spring</b>	<b>VLSI2</b> IC design	<b>VLSI4</b> Testing	<b>SoCDAML</b> System design	

28

28

## Where does VLSI3 fit?

- Digital IC design



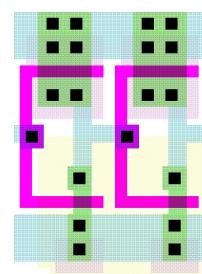
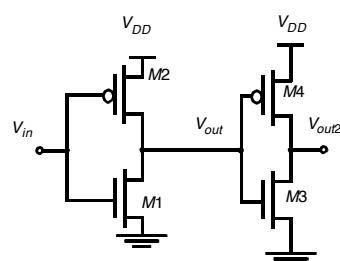
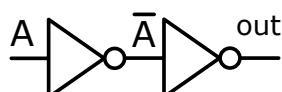
- In this course, you will acquire the fundamental knowledge and skills for creating your own standard cells

29

29

## Why full-custom design?

- Design of standard-cell libraries
- High-performance ICs
  - Flagship microprocessors (e.g., Intel)
  - Used in data converters (DACs/ADCs)
  - RF/mixed-signal designs
  - Ultra low-power



30

30

## Advantages and disadvantages

- Full-custom design gives total control over all possible design parameters:
  - (potentially) **lower power**
  - (potentially) **lower area**
  - (potentially) **higher throughput**
  - (potentially) **higher yield**
  - (potentially) **more fun**
- Drawback:
  - **A lot of (tedious) work**
  - Difficult to quickly develop large designs
  - CAD tools are getting better and better

31

31

## Why should I be interested?

- Understand the **fundamentals** behind digital IC design
- Better understanding (and appreciation) of CAD tools
- **Improve power, performance, and area of ICs**
- Top journals/conferences in solid-state circuits and VLSI favor digital designs with transistor-level schematics

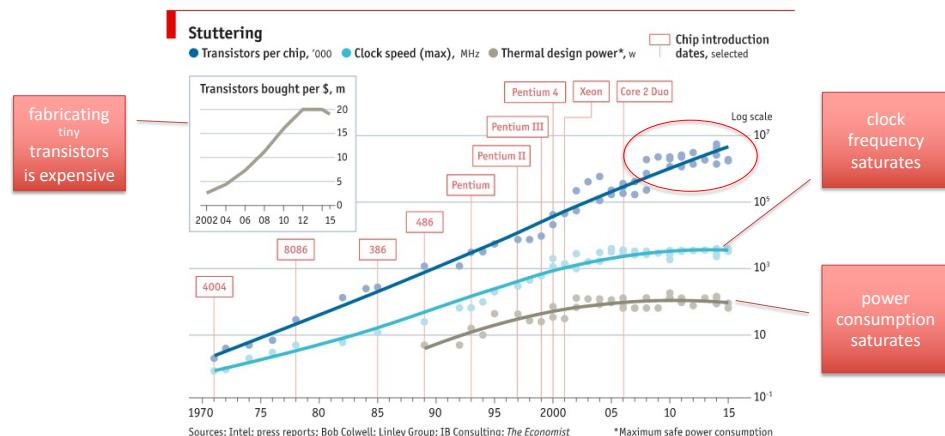


32

32

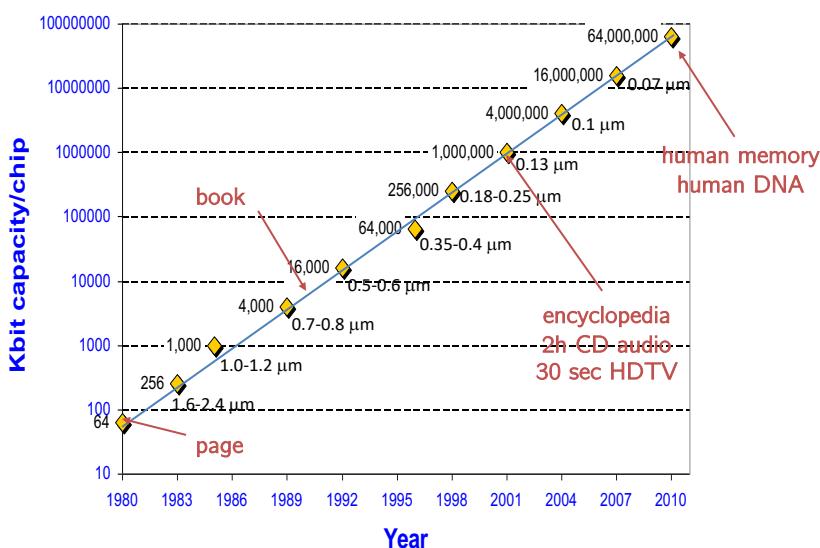
## Moore's Law (1965)

- # of transistors doubled every 18 months



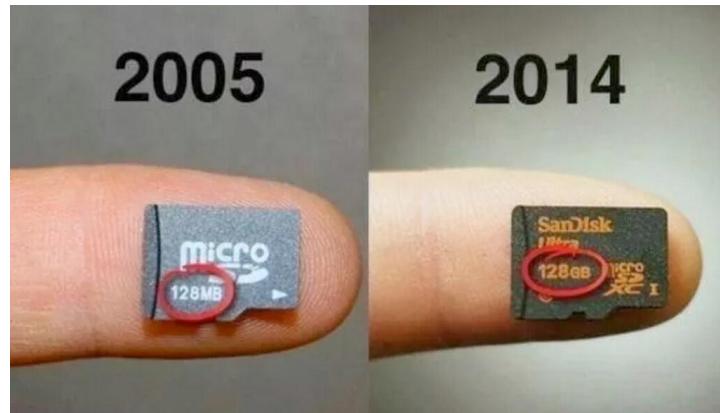
33

## Evolution of DRAM capacity



34

## Impressive “example:” Flash memory



What is interesting about this?

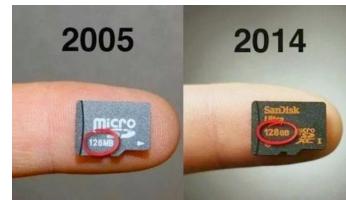
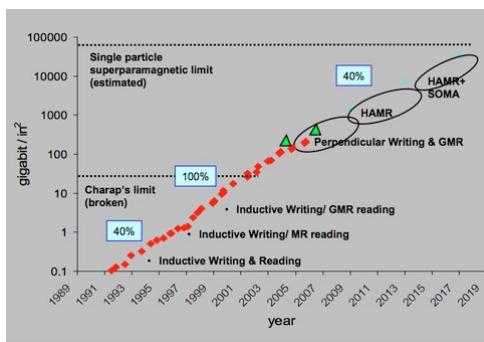
In 2017, we had 400GB; in 2018, we had 512GB; in mid 2021, we have 1TB!

35

35

## Kryder's Law

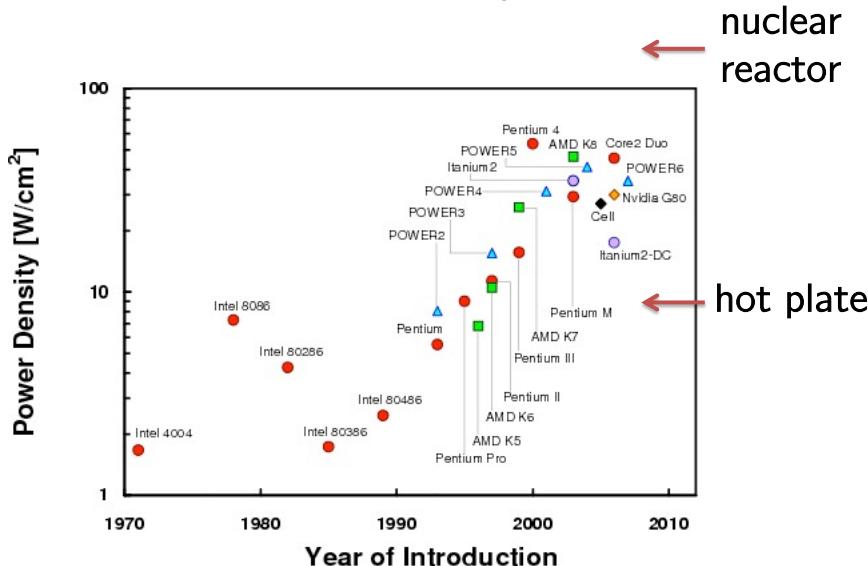
- 10 years have about  $6.66 \times 18$  months
- Moore's law only predicts  $2^{(6.66)} \approx 101$
- But storage density increased 1000x in 1 decade



36

36

## Power dissipation



37

37

## Can we master these challenges?

- Moore's Law is slowing down, demands for higher data rates and processing capabilities are continuously increasing
- Need to design increasingly complex ICs, but we also have to ensure they work 100%
- Circuits must be energy-efficient and have low power density
- Require denser and faster on-chip memories
- Full-custom digital design gives you an edge to find solutions that address these challenges!

38

38

## Lecture and exercise overview\*

L-Nr.	Date	Lecture	E-Nr.	Date	Exercise
L1	27.9	Introduction and Basic Device Models	E1	30.9	Basic Circuit Recap
L2	4.10	Nanometer MOSFETs	E2	7.10	Calculations with MOSFETs
L3	11.10	The CMOS Inverter: Static and Dynamic Behavior	E3	14.10	CMOS Inverter 1: Schematic and Simulation
L4	18.10	CMOS Gates and Sizing	E4	21.10	CMOS Inverter 2: Layout
L5	25.10	Full-Custom Standard-Cell Design	E5	28.10	CMOS Inverter 3: Extraction and Power
L6	1.11	Wire Models and Parasitics	E6	4.11	2-to-4 Decoder: Schematic
L7	8.11	Static and Dynamic Power	E7	11.11	2-to-4 Decoder: Layout
L8	15.11	Sequential Circuits: Latch and Flip-Flop	E8	18.11	2-to-4 Decoder: Simulation
L9	22.11	Alternative Logic Styles	E9	25.11	Flip-Flop: Schematic and Simulation
L10	29.11	Adders and Other Logic Circuits	E10	2.12	Mirror Adder 1: Schematic
L11	6.12	Numerical Representation: Fixed- and Floating-Point	E11	9.12	Mirror Adder 2: Layout and Simulation
L12	13.12	Memories	E12	16.12	8-bit Adder
L13	20.12	Full-Custom Design for Machine Learning	E13	23.12	Asynchronous Design and Interview Questions

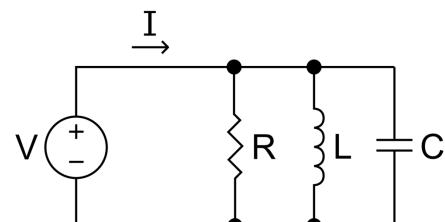
\*Up-to-date schedule on website and Moodle

39

39

## Prerequisites

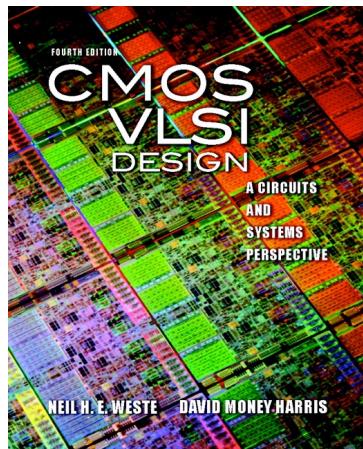
- VLSI lectures 1, 2, 3, and 4 are largely independent
- You can take VLSI 3 in parallel with VLSI 1
- For VLSI 3, you need a solid understanding of:
  - Digital logic
  - RLC circuits
- Basic RLC review in Exercise 1



40

40

## Primary textbook



Neil E. Weste  
David M. Harris

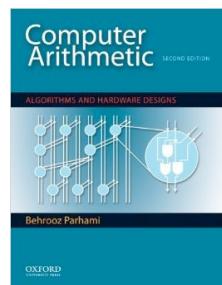
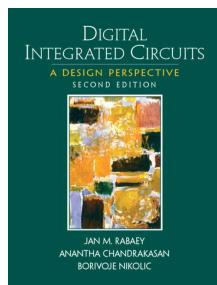
### CMOS VLSI Design: A Circuits and Systems Perspective

4th Ed., Pearson

41

41

## (Optional textbooks)



- For those who want to learn more (details)
- For those who plan to do a PhD in VLSI
- Note that VLSI 3 lecture slides are **self-contained**

42

42

## Exercises

- First two exercises will be written problems
  - Good practice for exam
- Most exercises are hands-on layout experience
  - Cadence Virtuoso
  - Calibre DRC, LVS, and PEX
- Last exercise:
  - Asynchronous digital design
  - Real digital VLSI interview questions

43

43

## Exercise organization

- Individual work and we have **over 60 students...**
- Thursday: 13:00 to 16:00
  - ETZ D61.1: 38 workstations
  - ETZ G91: 32 (remote) working places
  - Home “remote lab”
- Teaching assistants in both ETZ rooms and on Zoom
- **We will allocate workspaces to students in the following weeks**
- All computer-based exercises build on the previous exercises
  - **Try not to miss any exercise → if you do, try to catch up**

44

44

## Exam information

- Written exam (Sessionsprüfung)
  - Duration: 120 minutes
  - Multiple choice as well as circuit design and analysis problems
  - Everything covered in the exercises can be part of the exam...
- Exam rules:
  - Hand-written summary: max. 6 one-sided A4 pages
  - No photocopies or printouts of any form
  - No electronic help, including calculators or communication devices



45

45

- This is a completely new course at ETH
- Builds upon Prof. Studer's Cornell VLSI course, which was held six times and had 2x the lecture time
- The course will be quite intense
- Unfortunately, we are limited in teaching assistants and available lab space (we expected 20 students)
- Please be flexible where to do the labs



46

46

Now or never

**Questions?**

47

47

**BREAK**

48

48

## Let's get started

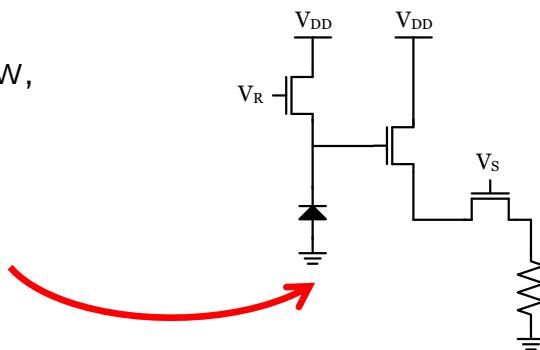
L-Nr.	Lecture
L1	Introduction and Basic Device Models
L2	Nanometer MOSFETs
L3	The CMOS Inverter: Static and Dynamic Behavior

49

49

## Goals for next two lectures

- Device basics:
  - Diode
  - MOS(FET) transistors
- Origin of  $V_T$ , square law, regions of operation
- Able to quickly analyze the functionality of such circuits:



50

50

Device basics

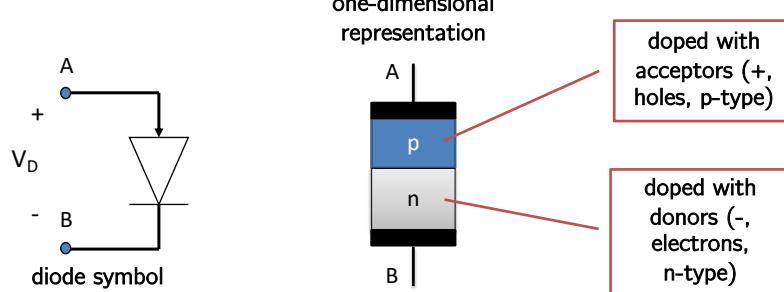
## The diode

51

51

## Basics: PN-junction diode

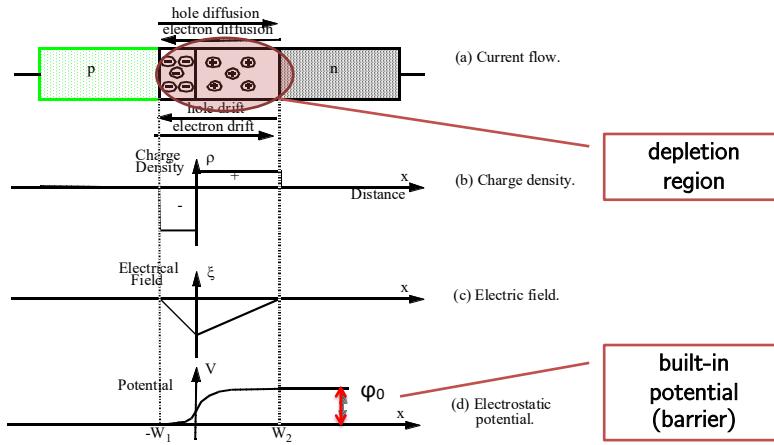
- Simplest semiconductor device
- Mostly occurs as **parasitic element**
- Used to protect chips against electrostatic discharge (ESD)



52

52

## (Depletion region)

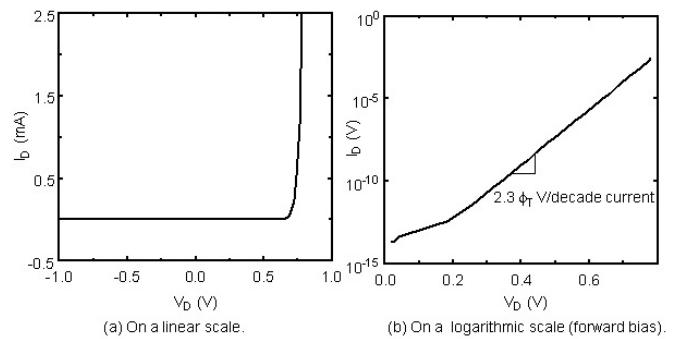


- Forward-bias lowers barrier; carriers can flow across junction
- Reverse-bias raises barrier; diode becomes non-conducting

53

## What is it doing?

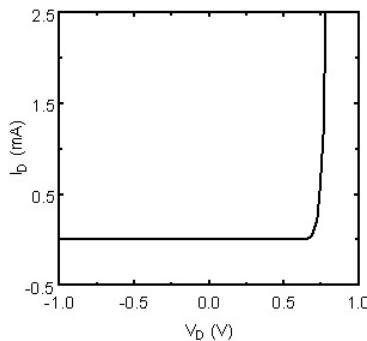
- Diode allows current in **forward** direction
- Blocks current in **reverse** direction



54

54

## Shockley (ideal) diode equation



saturation current  
~ 1e-14A

ideality factor  
(emission coefficient)  
 $n=1\dots2$

$$I_D = I_S \left( e^{\frac{V_D}{n\phi_T}} - 1 \right)$$

$$\phi_T = \frac{kT}{q} = 26 \text{ mV}$$

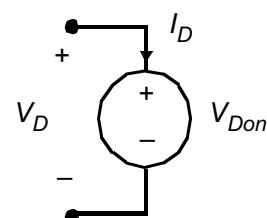
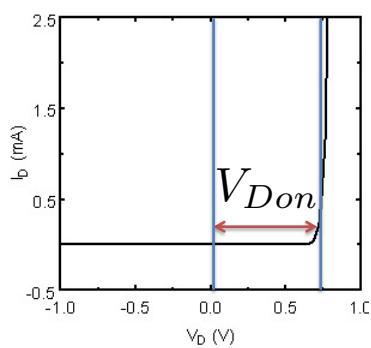
thermal voltage  
(usually at 300K)

- Saturation current is proportional to the **area** of the diode:  
Roughly  $17e-17 \text{ A}/\mu\text{m}^2$

55

55

## Model for manual analysis



$$V_{Don} \approx 0.7 \text{ V}$$

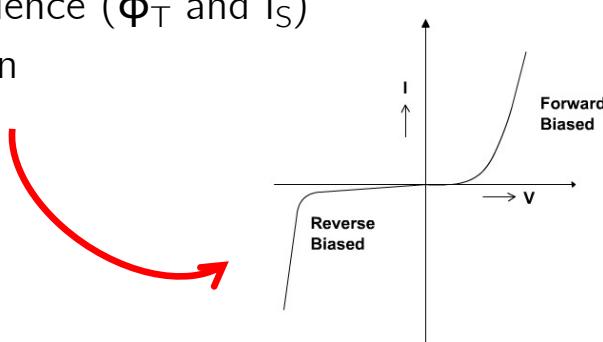
- Model for **fully conducting** (forward-biased) diode
- Non-conducting diode is simply an **open circuit**
- In digital ICs, diodes are usually reverse biased!

56

56

## Secondary effects

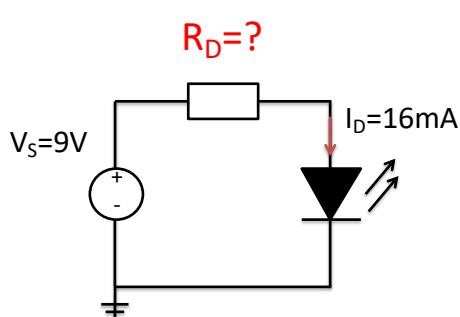
- Serial resistivity ( $1\Omega$ - $100\Omega$ )
- Junction capacitance: one way to build (small) capacitors for analog circuits
- Temperature dependence ( $\phi_T$  and  $I_S$ )
- Avalanche breakdown



57

57

## Example: Don't destroy the LED!



LED parameters:

- $I_S = 10^{-18} \text{ A}$
- $n = 1.8$
- $\phi_T = 26 \text{ mV} @ 300 \text{ K}$

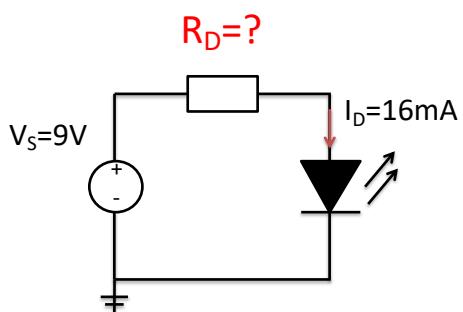
- Size the resistor  $R_D$ !
  - Use simple model with  $V_{D_{on}} = 0.7 \text{ V}$
  - Use Shockley model



58

58

## Solution for simple model



- Once the diode conducts,  $V_{D_{on}}=0.7\text{V}$
- Voltage drop across the resistor is 8.3V
- We want the current to not exceed 16mA

$$R = \frac{8.3\text{V}}{16\text{mA}} \approx 520\Omega$$

59

59

## Solution for Shockley model

- Solve for  $V_D$  first:

log = natural logarithm (almost everywhere in engineering)

$$n\phi_T \log \left( \frac{I_D}{I_S} + 1 \right) = V_D$$

- Gives  $V_D=1.7462\ldots\text{V}$
- Solve for R

The simple diode model gives pretty accurate results!

$$R = \frac{9\text{V} - 1.7462\text{V}}{16\text{mA}} \approx 453\Omega$$

60

60

Basic but important devices

## MOS(FET) transistors

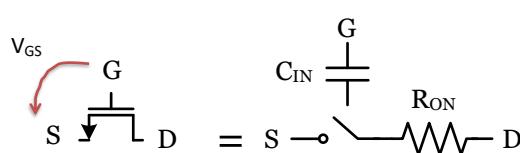
61

61

## MOSFET transistor

- Metal-oxide-semiconductor (MOS)
- Field-effect transistor (FET)

$V_{GS} < V_T$ : open  
 $V_{GS} > V_T$ : closed



G = gate, S = source, D = drain, B = bulk

IT'S  
A  
SWITCH!



62

62

## MOSFET transistor = RAS syndrome

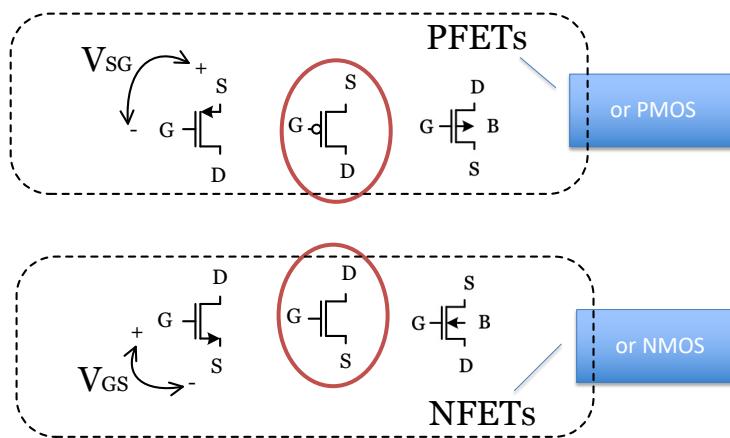
- RAS = redundant acronym syndrome...
- Other examples:
  - LCD display
  - PIN number
  - PDF format
  - ISBN number
  - AC current



63

63

## MOSFETs are 4-terminal devices



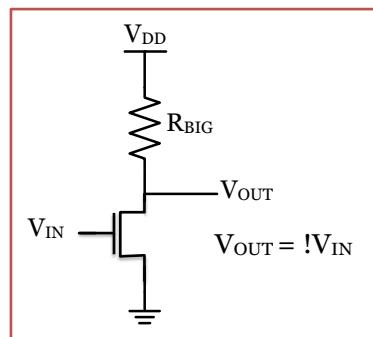
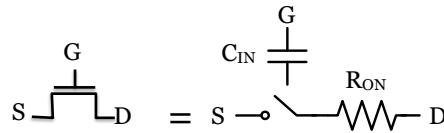
- In most cases  $V_{BS}=0$ ; can be used to alter  $V_T$
- Bulk connection is often not shown

64

64

## MOSFET as switches

$V_{GS} < V_T$ : open  
 $V_{GS} > V_T$ : closed

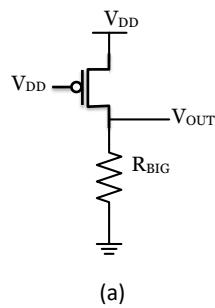


- What happens if  $V_{IN}=0$ ?
- What happens if  $V_{IN}=V_{DD}$ ?

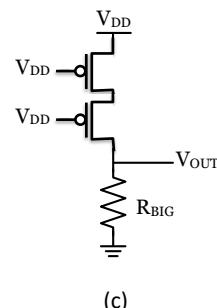
65

65

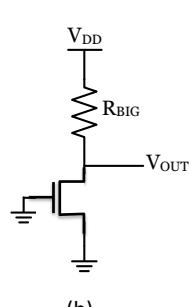
## MOSFET as switches (cont'd)



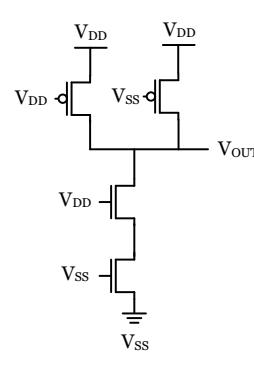
(a)



(c)



(b)



66

66

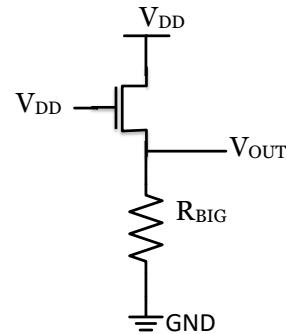
## Clicker: MOSFET Q1

ETH

Edu

- What is  $V_{OUT}$ ?

1.  $V_{OUT} = GND + V_T$
2.  $V_{OUT} = V_{DD}$
3.  $V_{OUT} = V_{DD} - V_T$  ✓
4.  $V_{OUT} = GND + V_T$
5. I don't know

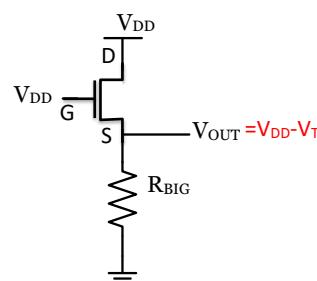


67

67

## What is going on here?

- Assume that NMOS is **on**
- Assume that  $V_{OUT}=V_{DD}$
- Then, node S would be  $V_{DD}$
- Hence,  $V_{GS}=0 \rightarrow$  **NMOS off!**
- If, however,  $V_{OUT}=V_{DD}-V_T$ , then transistor is on
- $V_{DD}-V_T$  is highest voltage for which that transistor can be on



68

68

## Clicker: MOSFET Q2

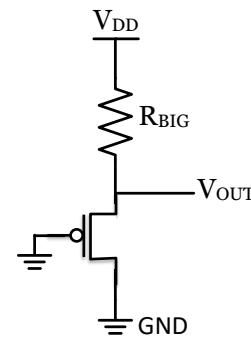
ETH

Edu

- What is  $V_{OUT}$ ?

1.  $V_{OUT} = GND$
2.  $V_{OUT} = V_{DD}$
3.  $V_{OUT} = V_{DD} - |V_T|$
4.  $V_{OUT} = GND + |V_T|$  ✓
5.  $V_{OUT} = GND - V_T$

$V_T$  of a PMOS is  
usually  
negative

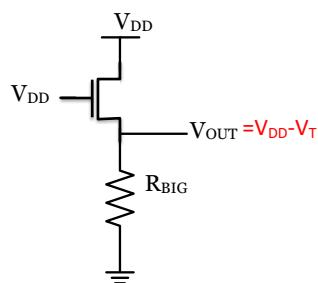


69

69

## Important to remember

- NFET is a bad pull up ( $\max V_{DD} - V_T$ )
- PFET is a bad pull down ( $\min GND + |V_T|$ )

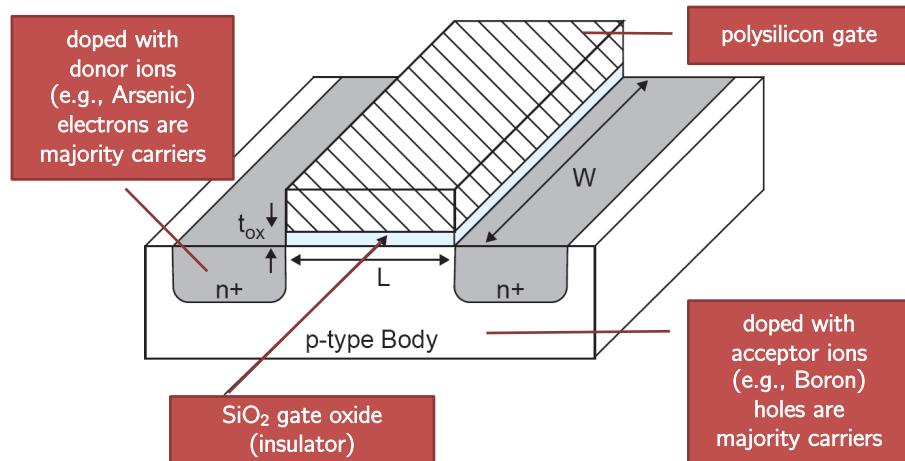


If  $V_{out}$  would be  $V_{DD}$ , then  $V_{GS} < V_T$  and hence, NFET would be off!

70

70

## 3-D view: NMOS

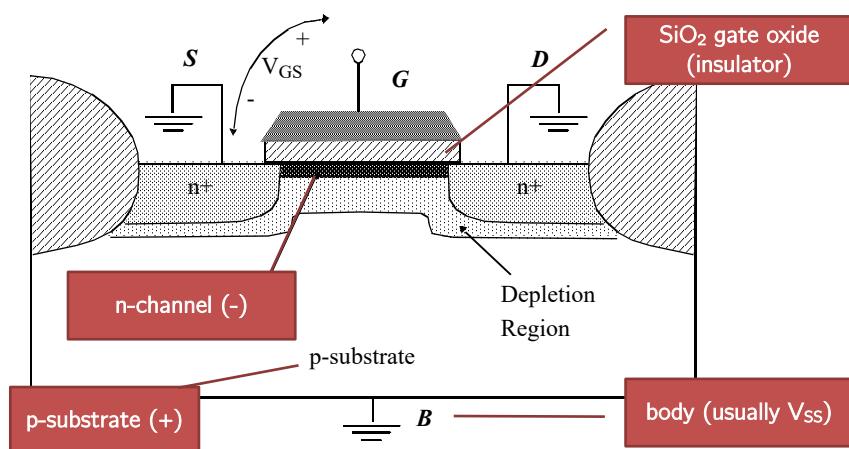


- Key design parameters:  $W$  = width;  $L$  = length

71

71

## Depletion region: NMOS



- Situation:  $V_S=V_D=V_B=0$  and  $V_{GS}>0$

72

72

## Threshold voltage $V_T$

- Increasing gate voltage  $V_{GS}$ 
  - n-channel forms below gate dielectric
  - onset of strong inversion
  - additional electrons from n+ source region
- Happens if  $V_{GS} > V_T$

$$V_T = V_{T_0} + \gamma \left( \sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

empirical parameter  
for  $V_{SB}=0$

Fermi potential  
(influenced by doping)

$$\phi_F = \phi_T \log \left( \frac{N_A}{n_i} \right)$$

73

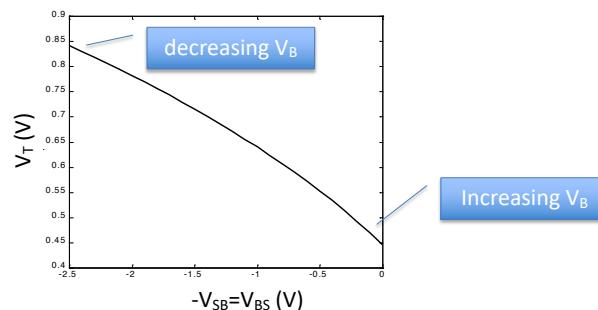
73

## Bulk voltage affects $V_T$ : Body effect

- Increasing  $V_B$ ?
- Decreasing  $V_B$ ?

called body-effect  
coefficient:  $\gamma \approx 0.4V$

$$V_T = V_{T_0} + \gamma \left( \sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$



74

74

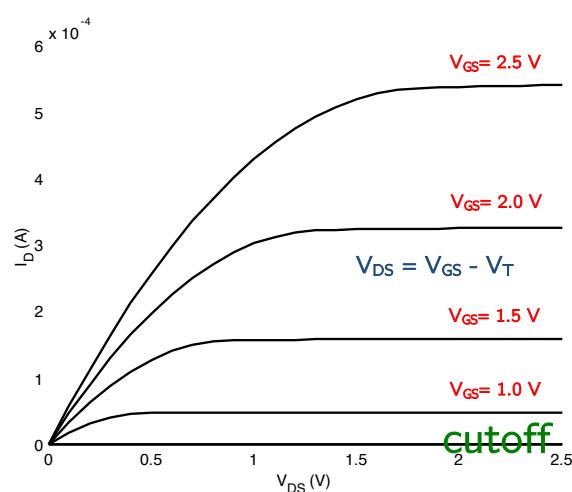
MOSFET model

## Operation regions

75

75

## Current-voltage characteristics

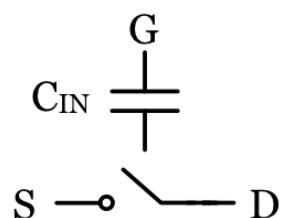


76

76

Cutoff region:  $V_{GS} < V_T$

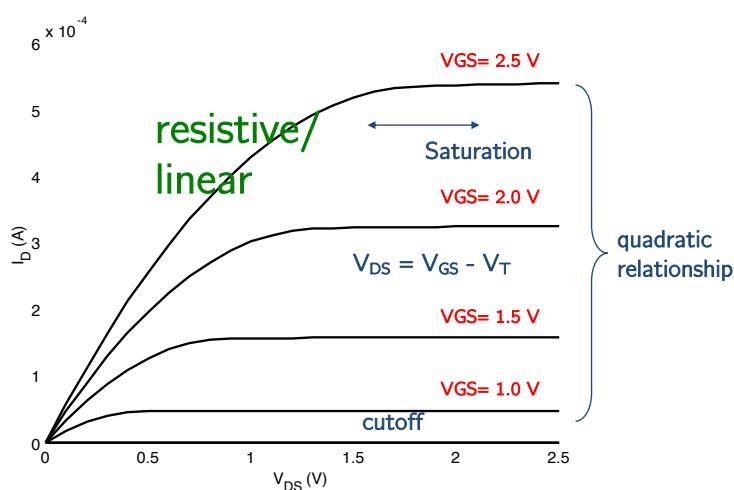
- If  $V_{GS} < V_T$ , then FET is (almost) off
  - Ideally, open circuit between drain and source and no current flows
  - $I_{DS} \approx 0A$  independent of  $V_{DS}$



77

77

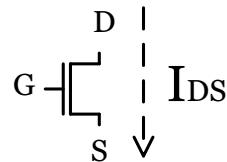
## Current-voltage characteristics



78

78

## Resistive (or linear) operation region



Assume:

- $V_{GS} - V_T > V_{DS}$
- L large ( $> 0.25\mu\text{m}$ )

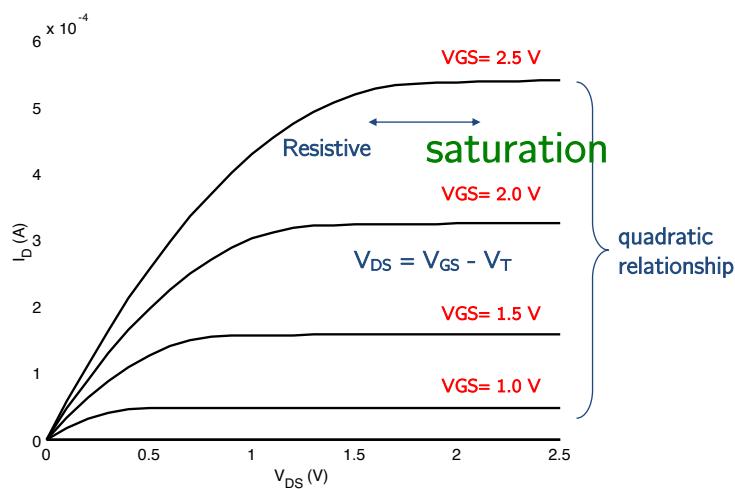
$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

- For small  $V_{DS} \rightarrow I_{DS}$  is linear in  $V_{DS}$

79

79

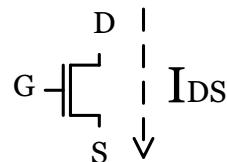
## Current-voltage characteristics



80

80

## Saturation region



Assume:

- $V_{GS} - V_T < V_{DS}$
- L large ( $> 0.25\mu\text{m}$ )

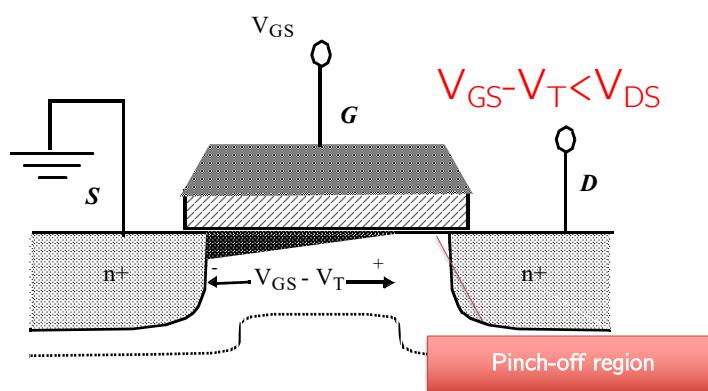
$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \boxed{\frac{W}{L}} (V_{GS} - V_T)^2$$

- Ideally, current no longer a function of  $V_{DS}$

81

81

## What happens in the channel?

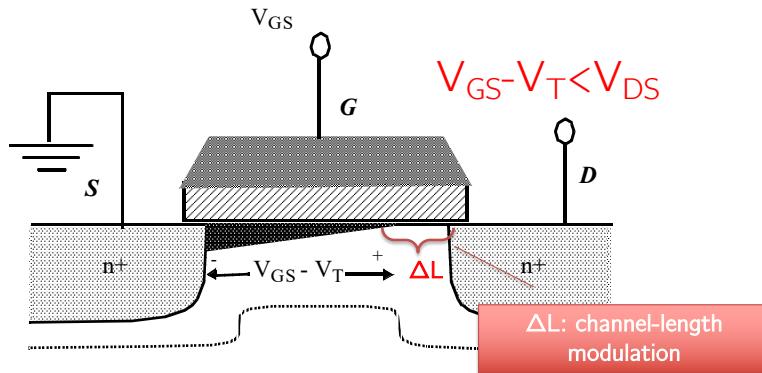


$$V_{DS}(\text{sat}) = V_{GS} - V_T$$

82

82

## Channel-length modulation

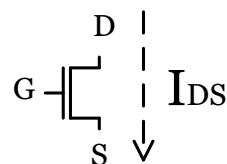


- Effective channel length is modulated by  $V_{DS}$
- Increasing  $V_{DS}$  reduces effective length

83

83

## Saturation region revisited



Assume:

- $V_{GS} - V_T < V_{DS}$
- $L$  large ( $> 0.25\mu\text{m}$ )

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

- $\lambda$  is an empirical parameter:
  - Effect is called channel-length modulation
  - inversely proportional to channel length  $L$

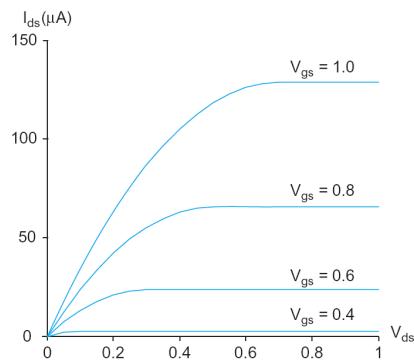


84

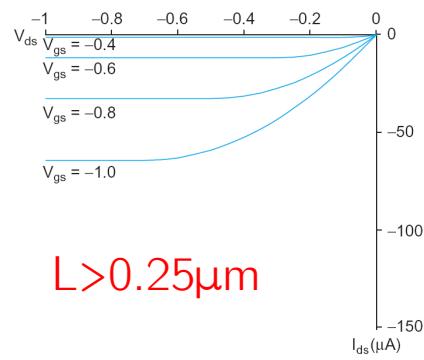
84

## Current-voltage characteristics of long-channel devices

NMOS



PMOS

 $L > 0.25\mu\text{m}$ 

85

85

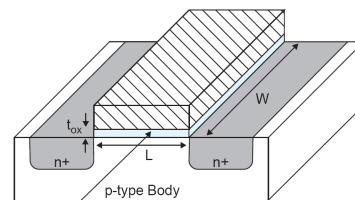
## Clicker: MOSFET Q3

ETH

Edu

- If the width  $W$  of an NFET increases, then the current will

1. Increase ✓
2. Decrease
3. Not change
4. I don't know

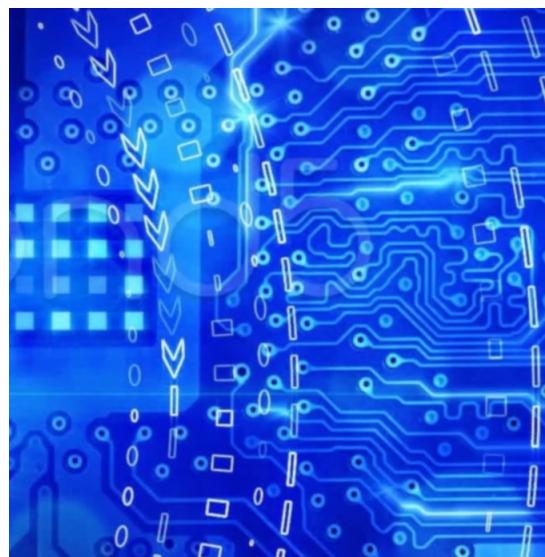


86

86

## To-do List

- Read Chapters 2.1 and 2.2
- Exercise 1 this Thursday
  - Brush up your RLC circuit knowledge
  - Review MOSFET switch model



87