Printable Version

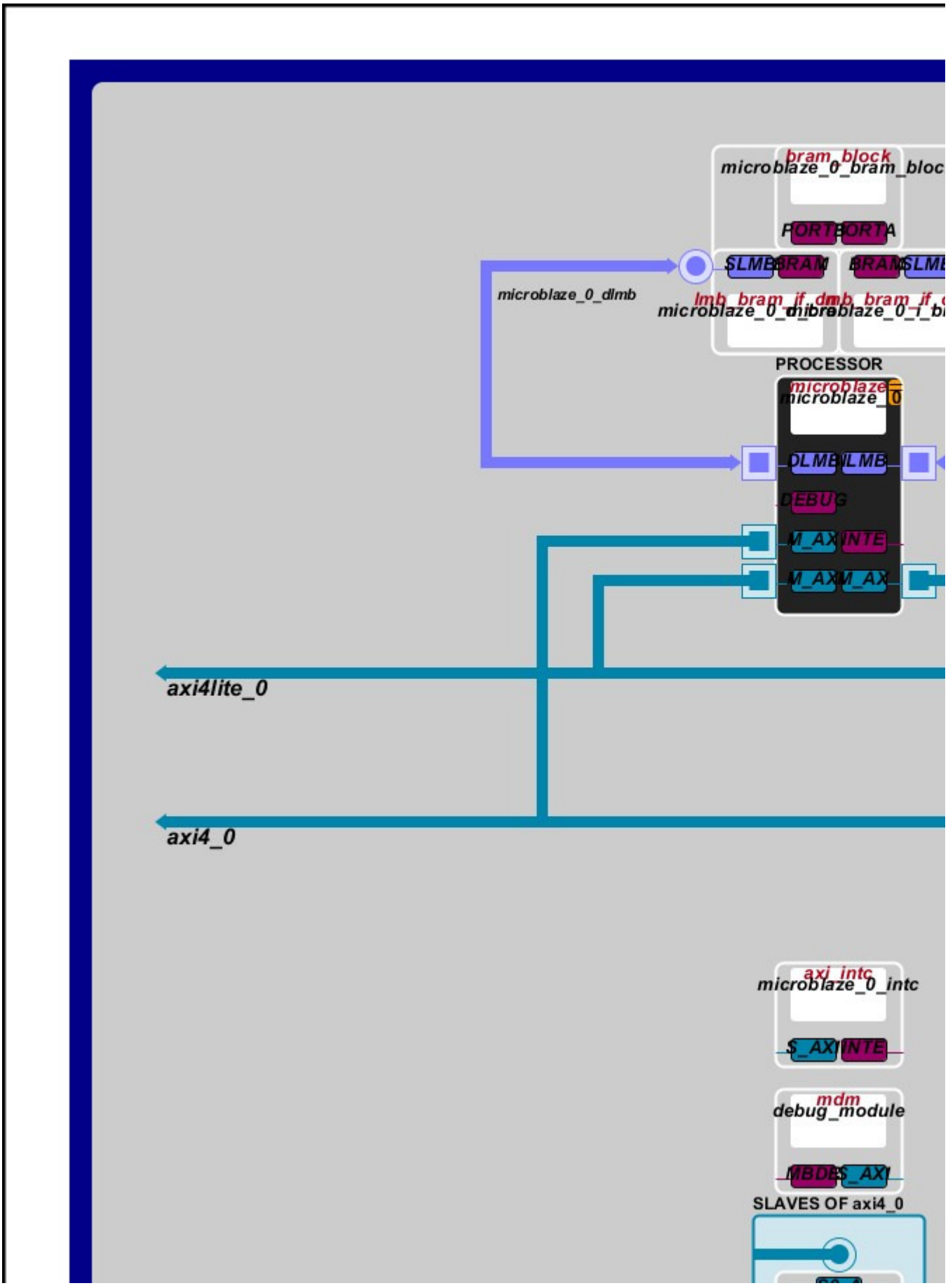
Overview

Resources Used

1	*MicroBlaze*
2	*Local Memory Bus (LMB) 1.0*
2	*AXI Interconnect*
1	*Block RAM (BRAM) Block*
2	*LMB BRAM Controller*
1	*AXI S6 Memory Controller(DDR/DDR2/DDR3)*
1	*Processor System Reset Module*
1	*AXI Interrupt Controller*
1	*MicroBlaze Debug Module (MDM)*
1	*Clock Generator*
1	*AXI Timer/Counter*
1	*AXI UART (Lite)*
1	*AXI 10/100 Ethernet MAC Lite*
1	*PATTERN_MATCHER*

Generated	**Fr**
EDK Version	
Device Family	
Device	

Block Diagram


bram_block
microblaze_0_bram_bloc
PORTB PORTA
SLMB BRAM
BRAM SLMB
microblaze_0_dlmb
lmb_bram_if_dmb_bram_if_
microblaze_0_dlmb microblaze_0_i_bl
PROCESSOR
microblaze
microblaze_0
DLMB ILMB
DEBUG
M_AX INTE
M_AX M_AX
axi4lite_0
axi4_0
axi_intc
microblaze_0_intc
S_AXI INTE
mdm
debug_module
MBDB S_AXI
SLAVES OF axi4_0

External Ports

These are the external ports defined in the MHS file.

Attributes Key
The attributes are obtained from the SIGIS and IOB_STATE parameters set on the PORT in the MHS file
CLK indicates Clock ports, (SIGIS = CLK)
INTR indicates Interrupt ports,(SIGIS = INTR)
RESET indicates Reset ports, (SIGIS = RST)
BUF or REG Indicates ports that instantiate or infer IOB primitives, (IOB_STATE = BUF or REG)

#	NAME	DIR	[LSB:MSB]	SIG	ATTRIBU
SHARED	RESET	I	1	RESET	RESET
Ethernet_Lite	Ethernet_Lite_COL	I	1	Ethernet_Lite_COL	
Ethernet_Lite	Ethernet_Lite_CRS	I	1	Ethernet_Lite_CRS	
Ethernet_Lite	Ethernet_Lite_RXD	I	0:3	Ethernet_Lite_RXD	
Ethernet_Lite	Ethernet_Lite_RX_CLK	I	1	Ethernet_Lite_RX_CLK	
Ethernet_Lite	Ethernet_Lite_RX_DV	I	1	Ethernet_Lite_RX_DV	
Ethernet_Lite	Ethernet_Lite_RX_ER	I	1	Ethernet_Lite_RX_ER	
Ethernet_Lite	Ethernet_Lite_TX_CLK	I	1	Ethernet_Lite_TX_CLK	
Ethernet_Lite	Ethernet_Lite_MDIO	IO	1	Ethernet_Lite_MDIO	
Ethernet_Lite	Ethernet_Lite_MDC	O	1	Ethernet_Lite_MDC	
Ethernet_Lite	Ethernet_Lite_PHY_RST_N	O	1	Ethernet_Lite_PHY_RST_N	
Ethernet_Lite	Ethernet_Lite_TXD	O	0:3	Ethernet_Lite_TXD	
Ethernet_Lite	Ethernet_Lite_TX_EN	O	1	Ethernet_Lite_TX_EN	
MCB_DDR2	mcbx_dram_dq	IO	0:15	mcbx_dram_dq	
MCB_DDR2	mcbx_dram_dqs	IO	1	mcbx_dram_dqs	
MCB_DDR2	mcbx_dram_dqs_n	IO	1	mcbx_dram_dqs_n	
MCB_DDR2	mcbx_dram_udqs	IO	1	mcbx_dram_udqs	
MCB_DDR2	mcbx_dram_udqs_n	IO	1	mcbx_dram_udqs_n	
MCB_DDR2	rzq	IO	1	rzq	
MCB_DDR2	zio	IO	1	zio	
MCB_DDR2	mcbx_dram_addr	O	0:12	mcbx_dram_addr	
MCB_DDR2	mcbx_dram_ba	O	0:2	mcbx_dram_ba	
MCB_DDR2	mcbx_dram_cas_n	O	1	mcbx_dram_cas_n	
MCB_DDR2	mcbx_dram_cke	O	1	mcbx_dram_cke	
MCB_DDR2	mcbx_dram_clk	O	1	mcbx_dram_clk	CLK
MCB_DDR2	mcbx_dram_clk_n	O	1	mcbx_dram_clk_n	CLK
MCB_DDR2	mcbx_dram_ldm	O	1	mcbx_dram_ldm	
MCB_DDR2	mcbx_dram_odt	O	1	mcbx_dram_odt	
MCB_DDR2	mcbx_dram_ras_n	O	1	mcbx_dram_ras_n	
MCB_DDR2	mcbx_dram_udm	O	1	mcbx_dram_udm	
MCB_DDR2	mcbx_dram_we_n	O	1	mcbx_dram_we_n	
RS232_Uart_1	RS232_Uart_1_sin	I	1	RS232_Uart_1_sin	

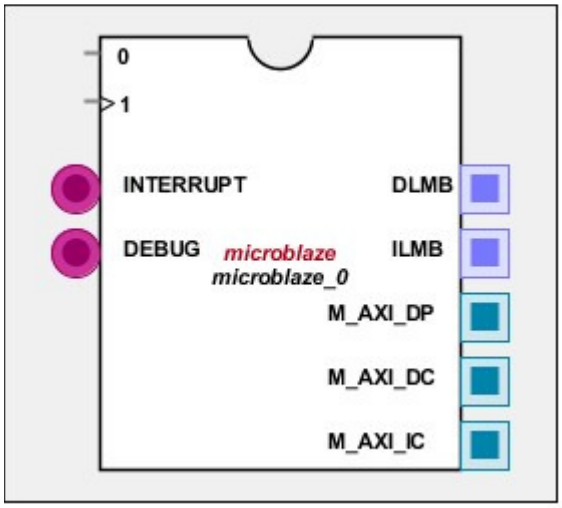
RS232_Uart_1	RS232_Uart_1_sout	O	1	RS232_Uart_1_sout	
clock_generator_0	GCLK	I	1	GCLK	CLK
pattern_matcher_0	pattern_matcher_0_LED_pin	O	0:7	pattern_matcher_0_LED	

Processors

microblaze_0 *MicroBlaze*

The MicroBlaze 32 bit soft processor

IP Specs		
Core	**Version**	**Documentation**
microblaze	**8.40.a**	***IP***



These are the ports listed in the MHS file. Ple

#	NAME
0	MB_RESET
1	CLK

NAME	TYPE	BUSSTD
DLMB	**MASTER**	**LMB**
ILMB	**MASTER**	**LMB**
M_AXI_DP	**MASTER**	**AXI**
M_AXI_DC	**MASTER**	**AXI**
M_AXI_IC	**MASTER**	**AXI**
INTERRUPT	**TARGET**	**XIL_MBINTERR**
DEBUG	**TARGET**	**XIL_MBDEBU**

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_SCO	0	C_S14_AXIS_PROTOCOL
C_FREQ	100000000	C_M15_AXIS_PROTOCOL
C_DATA_SIZE	32	C_S15_AXIS_PROTOCOL
C_DYNAMIC_BUS_SIZING	1	C_M0_AXIS_DATA_WIDTH
C_FAMILY	spartan6	C_S0_AXIS_DATA_WIDTH
C_INSTANCE	microblaze_0	C_M1_AXIS_DATA_WIDTH
C_AVOID_PRIMITIVES	0	C_S1_AXIS_DATA_WIDTH
C_FAULT_TOLERANT	0	C_M2_AXIS_DATA_WIDTH
C_ECC_USE_CE_EXCEPTION	0	C_S2_AXIS_DATA_WIDTH
C_LOCKSTEP_SLAVE	0	C_M3_AXIS_DATA_WIDTH
C_ENDIANNESS	1	C_S3_AXIS_DATA_WIDTH
C_AREA_OPTIMIZED	0	C_M4_AXIS_DATA_WIDTH

C_OPTIMIZATION	0	C_S4_AXIS_DATA_WIDTH	
C_INTERCONNECT	2	C_M5_AXIS_DATA_WIDTH	
C_STREAM_INTERCONNECT	0	C_S5_AXIS_DATA_WIDTH	
C_DPLB_DWIDTH	32	C_M6_AXIS_DATA_WIDTH	
C_DPLB_NATIVE_DWIDTH	32	C_S6_AXIS_DATA_WIDTH	
C_DPLB_BURST_EN	0	C_M7_AXIS_DATA_WIDTH	
C_DPLB_P2P	0	C_S7_AXIS_DATA_WIDTH	
C_IPLB_DWIDTH	32	C_M8_AXIS_DATA_WIDTH	
C_IPLB_NATIVE_DWIDTH	32	C_S8_AXIS_DATA_WIDTH	
C_IPLB_BURST_EN	0	C_M9_AXIS_DATA_WIDTH	
C_IPLB_P2P	0	C_S9_AXIS_DATA_WIDTH	
C_M_AXI_DP_SUPPORTS_THREADS	0	C_M10_AXIS_DATA_WIDTH	
C_M_AXI_DP_THREAD_ID_WIDTH	1	C_S10_AXIS_DATA_WIDTH	
C_M_AXI_DP_SUPPORTS_READ	1	C_M11_AXIS_DATA_WIDTH	
C_M_AXI_DP_SUPPORTS_WRITE	1	C_S11_AXIS_DATA_WIDTH	
C_M_AXI_DP_SUPPORTS_NARROW_BURST	0	C_M12_AXIS_DATA_WIDTH	
C_M_AXI_DP_DATA_WIDTH	32	C_S12_AXIS_DATA_WIDTH	
C_M_AXI_DP_ADDR_WIDTH	32	C_M13_AXIS_DATA_WIDTH	
C_M_AXI_DP_PROTOCOL	AXI4LITE	C_S13_AXIS_DATA_WIDTH	
C_M_AXI_DP_EXCLUSIVE_ACCESS	0	C_M14_AXIS_DATA_WIDTH	
C_INTERCONNECT_M_AXI_DP_READ_ISSUING	1	C_S14_AXIS_DATA_WIDTH	
C_INTERCONNECT_M_AXI_DP_WRITE_ISSUING	1	C_M15_AXIS_DATA_WIDTH	
C_M_AXI_IP_SUPPORTS_THREADS	0	C_S15_AXIS_DATA_WIDTH	
C_M_AXI_IP_THREAD_ID_WIDTH	1	C_ICACHE_BASEADDR	
C_M_AXI_IP_SUPPORTS_READ	1	C_ICACHE_HIGHADDR	
C_M_AXI_IP_SUPPORTS_WRITE	0	C_USE_ICACHE	
C_M_AXI_IP_SUPPORTS_NARROW_BURST	0	C_ALLOW_ICACHE_WR	
C_M_AXI_IP_DATA_WIDTH	32	C_ADDR_TAG_BITS	
C_M_AXI_IP_ADDR_WIDTH	32	C_CACHE_BYTE_SIZE	
C_M_AXI_IP_PROTOCOL	AXI4LITE	C_ICACHE_USE_FSL	
C_INTERCONNECT_M_AXI_IP_READ_ISSUING	1	C_ICACHE_LINE_LEN	
C_D_AXI	1	C_ICACHE_ALWAYS_USED	
C_D_PLB	0	C_ICACHE_INTERFACE	
C_D_LMB	1	C_ICACHE_VICTIMS	
C_I_AXI	0	C_ICACHE_STREAMS	
C_I_PLB	0	C_ICACHE_FORCE_TAG_LUTRAM	
C_I_LMB	1	C_ICACHE_DATA_WIDTH	
C_USE_MSR_INSTR	1	C_M_AXI_IC_SUPPORTS_THREADS	
C_USE_PCMP_INSTR	1	C_M_AXI_IC_THREAD_ID_WIDTH	
C_USE_BARREL	1	C_M_AXI_IC_SUPPORTS_READ	
C_USE_DIV	0	C_M_AXI_IC_SUPPORTS_WRITE	
C_USE_HW_MUL	1	C_M_AXI_IC_SUPPORTS_NARROW_B	
C_USE_FPU	0	C_M_AXI_IC_DATA_WIDTH	
C_USE_REORDER_INSTR	1	C_M_AXI_IC_ADDR_WIDTH	
C_UNALIGNED_EXCEPTIONS	0	C_M_AXI_IC_PROTOCOL	
C_ILL_OPCODE_EXCEPTION	0	C_M_AXI_IC_USER_VALUE	
C_M_AXI_I_BUS_EXCEPTION	0	C_M_AXI_IC_SUPPORTS_USER_SIGN	
C_M_AXI_D_BUS_EXCEPTION	0	C_M_AXI_IC_AWUSER_WIDTH	
C_IPLB_BUS_EXCEPTION	0	C_M_AXI_IC_ARUSER_WIDTH	
C_DPLB_BUS_EXCEPTION	0	C_M_AXI_IC_WUSER_WIDTH	
C_DIV_ZERO_EXCEPTION	0	C_M_AXI_IC_RUSER_WIDTH	

	0	C_M_AXI_IC_BUSER_WIDTH
C_FSL_EXCEPTION	0	C_INTERCONNECT_M_AXI_IC_READ_
C_USE_STACK_PROTECTION	0	C_DCACHE_BASEADDR
C_PVR	0	C_DCACHE_HIGHADDR
C_PVR_USER1	0x00	C_USE_DCACHE
C_PVR_USER2	0x00000000	C_ALLOW_DCACHE_WR
C_DEBUG_ENABLED	1	C_DCACHE_ADDR_TAG
C_NUMBER_OF_PC_BRK	1	C_DCACHE_BYTE_SIZE
C_NUMBER_OF_RD_ADDR_BRK	0	C_DCACHE_USE_FSL
C_NUMBER_OF_WR_ADDR_BRK	0	C_DCACHE_LINE_LEN
C_INTERRUPT_IS_EDGE	0	C_DCACHE_ALWAYS_USED
C_EDGE_IS_POSITIVE	1	C_DCACHE_INTERFACE
C_RESET_MSR	0x00000000	C_DCACHE_USE_WRITEBACK
C_OPCODE_0x0_ILLEGAL	0	C_DCACHE_VICTIMS
C_FSL_LINKS	0	C_DCACHE_FORCE_TAG_LUTRAM
C_FSL_DATA_SIZE	32	C_DCACHE_DATA_WIDTH
C_USE_EXTENDED_FSL_INSTR	0	C_M_AXI_DC_SUPPORTS_THREADS
C_M0_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_THREAD_ID_WIDTH
C_S0_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_SUPPORTS_READ
C_M1_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_SUPPORTS_WRITE
C_S1_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_SUPPORTS_NARROW_E
C_M2_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_DATA_WIDTH
C_S2_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_ADDR_WIDTH
C_M3_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_PROTOCOL
C_S3_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_EXCLUSIVE_ACCESS
C_M4_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_USER_VALUE
C_S4_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_SUPPORTS_USER_SIGN
C_M5_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_AWUSER_WIDTH
C_S5_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_ARUSER_WIDTH
C_M6_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_WUSER_WIDTH
C_S6_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_RUSER_WIDTH
C_M7_AXIS_PROTOCOL	GENERIC	C_M_AXI_DC_BUSER_WIDTH
C_S7_AXIS_PROTOCOL	GENERIC	C_INTERCONNECT_M_AXI_DC_READ_
C_M8_AXIS_PROTOCOL	GENERIC	C_INTERCONNECT_M_AXI_DC_WRITE
C_S8_AXIS_PROTOCOL	GENERIC	C_USE_MMU
C_M9_AXIS_PROTOCOL	GENERIC	C_MMU_DTLB_SIZE
C_S9_AXIS_PROTOCOL	GENERIC	C_MMU_ITLB_SIZE
C_M10_AXIS_PROTOCOL	GENERIC	C_MMU_TLB_ACCESS
C_S10_AXIS_PROTOCOL	GENERIC	C_MMU_ZONES
C_M11_AXIS_PROTOCOL	GENERIC	C_MMU_PRIVILEGED_INSTR
C_S11_AXIS_PROTOCOL	GENERIC	C_USE_INTERRUPT
C_M12_AXIS_PROTOCOL	GENERIC	C_USE_EXT_BRK
C_S12_AXIS_PROTOCOL	GENERIC	C_USE_EXT_NM_BRK
C_M13_AXIS_PROTOCOL	GENERIC	C_USE_BRANCH_TARGET_CACHE
C_S13_AXIS_PROTOCOL	GENERIC	C_BRANCH_TARGET_CACHE_SIZE
C_M14_AXIS_PROTOCOL	GENERIC	C_PC_WIDTH

Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

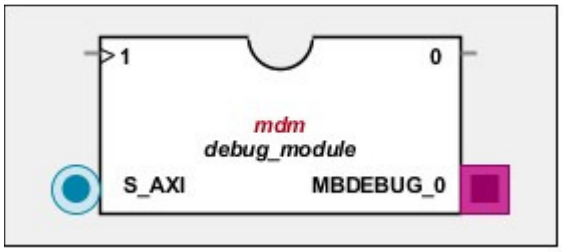
Debuggers

debug_module *MicroBlaze Debug Module (MDM)*

Debug module for MicroBlaze Soft Processor.

IP Specs

Core	Version
mdm	**2.10.a**



These

#	NAME
0	Debug_SYS_Rst
1	S_AXI_ACLK

NAME	TYPE	BUSSTD
MBDEBUG_0	**INITIATOR**	**XIL_MBDEB**
S_AXI	**SLAVE**	**AXI**

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_FAMILY	spartan6	C_SPLB_NUM_MASTERS
C_JTAG_CHAIN	2	C_SPLB_NATIVE_DWIDTH
C_INTERCONNECT	2	C_SPLB_SUPPORT_BURSTS
C_BASEADDR	0x41400000	C_MB_DBG_PORTS
C_HIGHADDR	0x4140FFFF	C_USE_UART
C_SPLB_AWIDTH	32	C_USE_BSCAN
C_SPLB_DWIDTH	32	C_S_AXI_ADDR_WIDTH
C_SPLB_P2P	0	C_S_AXI_DATA_WIDTH
C_SPLB_MID_WIDTH	3	C_S_AXI_PROTOCOL

Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

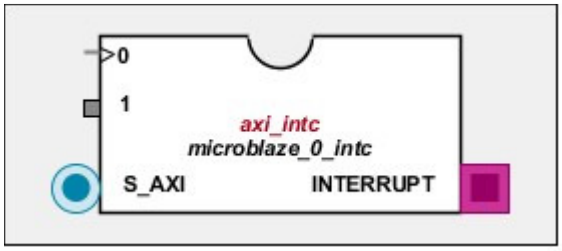
Interrupt Controllers

microblaze_0_intc *AXI Interrupt Controller*

intc core attached to the AXI

IP Specs

Core	Version	Documentation
axi_intc	**1.02.a**	***IP***



These are the ports listed in the MHS file. Please

#	NAME
0	S_AXI_ACLK
1	INTR

NAME	TYPE	BUSSTD
INTERRUPT	**INITIATOR**	**XIL_MBINTE**
S_AXI	**SLAVE**	**AXI**

Priority	SIG
0	Ethernet_Lite_IP2INT
1	axi_timer_0_Interr

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_FAMILY	spartan6	C_HAS_IPR
C_INSTANCE	microblaze_0_intc	C_HAS_SIE
C_BASEADDR	0x41200000	C_HAS_CIE
C_HIGHADDR	0x4120FFFF	C_HAS_IVR
C_S_AXI_ADDR_WIDTH	9	C_IRQ_IS_LEVEL
C_S_AXI_DATA_WIDTH	32	C_IRQ_ACTIVE
C_NUM_INTR_INPUTS	2	C_DISABLE_SYNCHRONIZERS
C_KIND_OF_INTR	0B11111111111111111111111111111110	C_MB_CLK_NOT_CONNECTED
C_KIND_OF_EDGE	0B11111111111111111111111111111111	C_HAS_FAST
C_KIND_OF_LVL	0B11111111111111111111111111111111	C_S_AXI_PROTOCOL

Post Synthesis Device Utilization

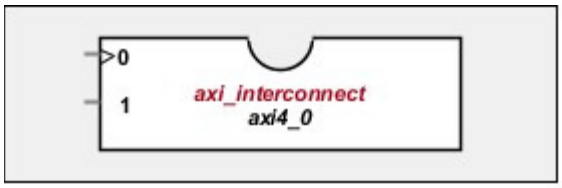
Device utilization information is not available for this IP. Run platgen to generate synthesis informati

Busses

axi4_0 *AXI Interconnect*
AXI4 Memory-Mapped Interconnect

	IP Specs	
Core	**Version**	**Documentation**
axi_interconnect	**1.06.a**	***IP***

POR



These are the ports listed in the MHS file. Ple
information ab

#	NAME	DIR	[LSB:MS
0	interconnect_aclk	**I**	**1**
1	INTERCONNECT_ARESETN	**I**	**1**

Bus Co

INSTANCE
microblaze_0
microblaze_0
MCB_DDR2

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name
C_FAMILY
C_BASEFAMILY
C_NUM_SLAVE_SLOTS
C_NUM_MASTER_SLOTS
C_AXI_ID_WIDTH
C_AXI_ADDR_WIDTH
C_AXI_DATA_MAX_WIDTH
C_S_AXI_DATA_WIDTH
C_M_AXI_DATA_WIDTH
C_INTERCONNECT_DATA_WIDTH
C_S_AXI_PROTOCOL
C_M_AXI_PROTOCOL
C_M_AXI_BASE_ADDR
C_M_AXI_HIGH_ADDR
C_S_AXI_BASE_ID
C_S_AXI_THREAD_ID_WIDTH
C_S_AXI_IS_INTERCONNECT
C_S_AXI_ACLK_RATIO
C_S_AXI_IS_ACLK_ASYNC
C_M_AXI_ACLK_RATIO
C_M_AXI_IS_ACLK_ASYNC
C_INTERCONNECT_ACLK_RATIO
C_S_AXI_SUPPORTS_WRITE
C_S_AXI_SUPPORTS_READ
C_M_AXI_SUPPORTS_WRITE
C_M_AXI_SUPPORTS_READ
C_AXI_SUPPORTS_USER_SIGNALS
C_AXI_AWUSER_WIDTH
C_AXI_ARUSER_WIDTH
C_AXI_WUSER_WIDTH
C_AXI_RUSER_WIDTH
C_AXI_BUSER_WIDTH
C_AXI_CONNECTIVITY

C_S_AXI_SINGLE_THREAD
C_M_AXI_SUPPORTS_REORDERING
C_S_AXI_SUPPORTS_NARROW_BURST
C_M_AXI_SUPPORTS_NARROW_BURST
C_S_AXI_WRITE_ACCEPTANCE
C_S_AXI_READ_ACCEPTANCE
C_M_AXI_WRITE_ISSUING

Post Synthesis Device Utilization

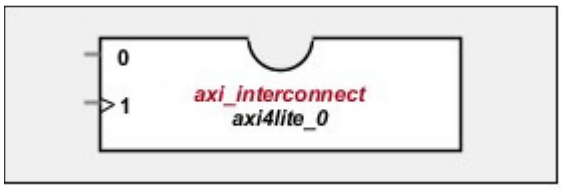
Device utilization information is not available for this IP. Run platgen to generate synthesis informati

axi4lite_0 *AXI Interconnect*

AXI4 Memory-Mapped Interconnect

IP Specs

Core	Version	Documentation
axi_interconnect	**1.06.a**	***IP***



POR

These are the ports listed in the MHS file. Ple information ab

#	NAME	DIR	[LSB:MS
0	INTERCONNECT_ARESETN	**I**	**1**
1	INTERCONNECT_ACLK	**I**	**1**

Bus Co

INSTANCE
microblaze_0
microblaze_0_intc
debug_module
axi_timer_0
RS232_Uart_1
Ethernet_Lite
pattern_matcher_0

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name
C_FAMILY
C_BASEFAMILY
C_NUM_SLAVE_SLOTS
C_NUM_MASTER_SLOTS
C_AXI_ID_WIDTH
C_AXI_ADDR_WIDTH
C_AXI_DATA_MAX_WIDTH
C_S_AXI_DATA_WIDTH
C_M_AXI_DATA_WIDTH

C_INTERCONNECT_DATA_WIDTH
C_S_AXI_PROTOCOL
C_M_AXI_PROTOCOL
C_M_AXI_BASE_ADDR
C_M_AXI_HIGH_ADDR
C_S_AXI_BASE_ID
C_S_AXI_THREAD_ID_WIDTH
C_S_AXI_IS_INTERCONNECT
C_S_AXI_ACLK_RATIO
C_S_AXI_IS_ACLK_ASYNC
C_M_AXI_ACLK_RATIO
C_M_AXI_IS_ACLK_ASYNC
C_INTERCONNECT_ACLK_RATIO
C_S_AXI_SUPPORTS_WRITE
C_S_AXI_SUPPORTS_READ
C_M_AXI_SUPPORTS_WRITE
C_M_AXI_SUPPORTS_READ
C_AXI_SUPPORTS_USER_SIGNALS
C_AXI_AWUSER_WIDTH
C_AXI_ARUSER_WIDTH
C_AXI_WUSER_WIDTH
C_AXI_RUSER_WIDTH
C_AXI_BUSER_WIDTH
C_AXI_CONNECTIVITY
C_S_AXI_SINGLE_THREAD
C_M_AXI_SUPPORTS_REORDERING
C_S_AXI_SUPPORTS_NARROW_BURST
C_M_AXI_SUPPORTS_NARROW_BURST
C_S_AXI_WRITE_ACCEPTANCE
C_S_AXI_READ_ACCEPTANCE
C_M_AXI_WRITE_ISSUING

Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

microblaze_0_dlmb *Local Memory Bus (LMB) 1.0*

'The LMB is a fast, local bus for connecting MicroBlaze I and D ports to peripherals and BRAM'

IP Specs

Core	Version
lmb_v10	**2.00.b**

PORT LIST

These are the ports listed ir

#	NAME	DIR	[LSB:MSB]	
0	SYS_RST	**I**	**1**	proc_sys_r
1	LMB_CLK	**I**	**1**	clk_100_0(

Bus Connecti

INSTANCE	INTERFAC
microblaze_0	**MAST**

microblaze_0_d_bram_ctrl **SLA**

Parameters	
These are the current parameter settings for this module. Parameters marked with yellow indicate parameters set by the user. Parameters marked with blue indicate parameters set by the system.	
Name	**Value**
C_LMB_NUM_SLAVES	1
C_LMB_AWIDTH	32
C_LMB_DWIDTH	32
C_EXT_RESET_HIGH	1

Post Synthesis Device Utilization

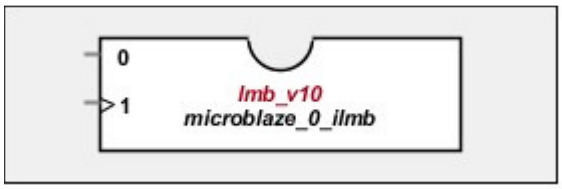
Device utilization information is not available for this IP. Run platgen to generate synthesis information.

microblaze_0_ilmb *Local Memory Bus (LMB) 1.0*

'The LMB is a fast, local bus for connecting MicroBlaze I and D ports to peripherals and BRAM'

IP Specs

Core	Version
lmb_v10	**2.00.b**



PORT LIST

These are the ports listed ir

#	NAME	DIR	[LSB:MSB]	
0	SYS_RST	**I**	**1**	proc_sys_r
1	LMB_CLK	**I**	**1**	clk_100_0(

Bus Connecti

INSTANCE	INTERFAC
microblaze_0	**MAST**
microblaze_0_i_bram_ctrl	**SLA**

Parameters	
These are the current parameter settings for this module. Parameters marked with yellow indicate parameters set by the user. Parameters marked with blue indicate parameters set by the system.	
Name	**Value**
C_LMB_NUM_SLAVES	1
C_LMB_AWIDTH	32
C_LMB_DWIDTH	32
C_EXT_RESET_HIGH	1

Post Synthesis Device Utilization

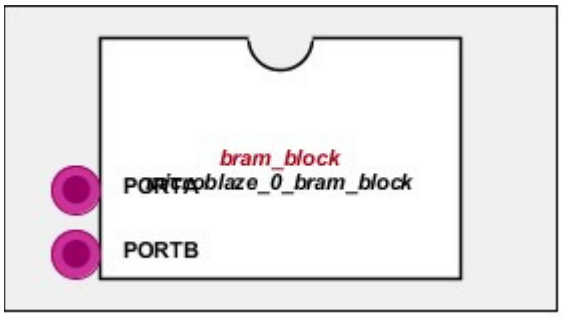
Device utilization information is not available for this IP. Run platgen to generate synthesis information.

Memorys

microblaze_0_bram_block *Block RAM (BRAM) Block*

The BRAM Block is a configurable memory module that attaches to a variety of BRAM Interface Controllers.

	IP Specs	
Core	**Version**	**Documentation**
bram_block	**1.00.a**	***IP***



NAME	TYPE	BUSSTD	
PORTA	**TARGET**	**XIL_BRAM**	*microblaze*
PORTB	**TARGET**	**XIL_BRAM**	*microblaze_*

Parameters	
These are the current parameter settings for this module. **Parameters marked with yellow indicate parameters set by the user.** **Parameters marked with blue indicate parameters set by the system.**	
Name	**Value**
C_MEMSIZE	0x4000
C_PORT_DWIDTH	32
C_PORT_AWIDTH	32
C_NUM_WE	4
C_FAMILY	spartan6

Post Synthesis Device Utilization

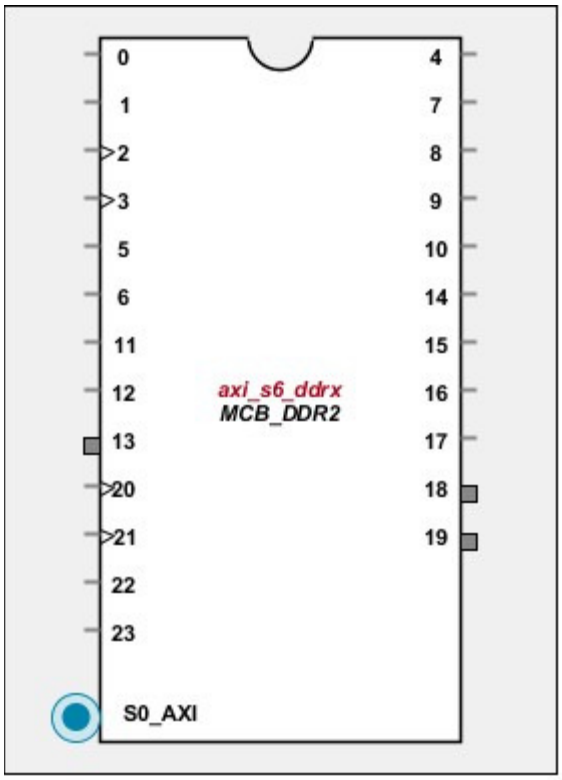
Device utilization information is not available for this IP. Run platgen to generate synthesis information.

Memory Controllers

MCB_DDR2 *AXI S6 Memory Controller(DDR/DDR2/DDR3)*

Spartan-6 memory controller

	IP Specs	
Core	**Version**	**Documentation**
axi_s6_ddrx	**1.06.a**	***IP***



POR

These are the ports listed in the MHS file. Pl
information ab

#	NAME	DIR	[LSB:M
0	zio	IO	1
1	rzq	IO	1
2	s0_axi_aclk	I	1
3	ui_clk	I	1
4	mcbx_dram_we_n	O	1
5	mcbx_dram_udqs_n	IO	1
6	mcbx_dram_udqs	IO	1
7	mcbx_dram_udm	O	1
8	mcbx_dram_ras_n	O	1
9	mcbx_dram_odt	O	1
10	mcbx_dram_ldm	O	1
11	mcbx_dram_dqs_n	IO	1
12	mcbx_dram_dqs	IO	1
13	mcbx_dram_dq	IO	0:15
14	mcbx_dram_clk_n	O	1
15	mcbx_dram_clk	O	1
16	mcbx_dram_cke	O	1
17	mcbx_dram_cas_n	O	1
18	mcbx_dram_ba	O	0:2
19	mcbx_dram_addr	O	0:12
20	sysclk_2x	I	1
21	sysclk_2x_180	I	1
22	SYS_RST	I	1
23	PLL_LOCK	I	1

Bus In

NAME	TYPE	BUSSTD	BUS
S0_AXI	SLAVE	AXI	axi4_0

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value
C_MCB_LOC	MEMC3
C_MCB_RZQ_LOC	L6
C_MCB_ZIO_LOC	C2
C_MCB_PERFORMANCE	STANDARD
C_BYPASS_CORE_UCF	0
C_S0_AXI_BASEADDR	0xA8000000
C_S0_AXI_HIGHADDR	0xAFFFFFFF
C_S1_AXI_BASEADDR	0xFFFFFFFF
C_S1_AXI_HIGHADDR	0x00000000

Name
C_INTERCONNECT_S0_AXI_READ_
C_INTERCONNECT_S0_AXI_WRITE_
C_S1_AXI_ENABLE
C_S1_AXI_PROTOCOL
C_S1_AXI_ID_WIDTH
C_S1_AXI_ADDR_WIDTH
C_S1_AXI_DATA_WIDTH
C_S1_AXI_SUPPORTS_READ
C_S1_AXI_SUPPORTS_WRITE
C_S1_AXI_SUPPORTS_NARROW_BU

C_S2_AXI_BASEADDR	0xFFFFFFFF	C_S1_AXI_REG_EN0
C_S2_AXI_HIGHADDR	0x00000000	C_S1_AXI_REG_EN1
C_S3_AXI_BASEADDR	0xFFFFFFFF	C_S1_AXI_STRICT_COHERENCY
C_S3_AXI_HIGHADDR	0x00000000	C_S1_AXI_ENABLE_AP
C_S4_AXI_BASEADDR	0xFFFFFFFF	C_INTERCONNECT_S1_AXI_READ_
C_S4_AXI_HIGHADDR	0x00000000	C_INTERCONNECT_S1_AXI_WRITE_
C_S5_AXI_BASEADDR	0xFFFFFFFF	C_S2_AXI_ENABLE
C_S5_AXI_HIGHADDR	0x00000000	C_S2_AXI_PROTOCOL
C_MEM_TYPE	DDR2	C_S2_AXI_ID_WIDTH
C_MEM_PARTNO	EDE1116AXXX-8E	C_S2_AXI_ADDR_WIDTH
C_MEM_BASEPARTNO	NOT_SET	C_S2_AXI_DATA_WIDTH
C_NUM_DQ_PINS	16	C_S2_AXI_SUPPORTS_READ
C_MEM_ADDR_WIDTH	13	C_S2_AXI_SUPPORTS_WRITE
C_MEM_BANKADDR_WIDTH	3	C_S2_AXI_SUPPORTS_NARROW_BU
C_MEM_NUM_COL_BITS	10	C_S2_AXI_REG_EN0
C_MEM_TRAS	42500	C_S2_AXI_REG_EN1
C_MEM_TRCD	15000	C_S2_AXI_STRICT_COHERENCY
C_MEM_TREFI	7800000	C_S2_AXI_ENABLE_AP
C_MEM_TRFC	127500	C_INTERCONNECT_S2_AXI_READ_
C_MEM_TRP	15000	C_INTERCONNECT_S2_AXI_WRITE_
C_MEM_TWR	15000	C_S3_AXI_ENABLE
C_MEM_TRTP	7500	C_S3_AXI_PROTOCOL
C_MEM_TWTR	7500	C_S3_AXI_ID_WIDTH
C_PORT_CONFIG	B32_B32_B32_B32	C_S3_AXI_ADDR_WIDTH
C_SKIP_IN_TERM_CAL	0	C_S3_AXI_DATA_WIDTH
C_SKIP_IN_TERM_CAL_VALUE	NONE	C_S3_AXI_SUPPORTS_READ
C_MEMCLK_PERIOD	3333	C_S3_AXI_SUPPORTS_WRITE
C_MEM_ADDR_ORDER	ROW_BANK_COLUMN	C_S3_AXI_SUPPORTS_NARROW_BU
C_MEM_TZQINIT_MAXCNT	512	C_S3_AXI_REG_EN0
C_MEM_CAS_LATENCY	5	C_S3_AXI_REG_EN1
C_SIMULATION	TRUE	C_S3_AXI_STRICT_COHERENCY
C_MEM_DDR1_2_ODS	FULL	C_S3_AXI_ENABLE_AP
C_MEM_DDR1_2_ADDR_CONTROL_SSTL_ODS	CLASS_II	C_INTERCONNECT_S3_AXI_READ_
C_MEM_DDR1_2_DATA_CONTROL_SSTL_ODS	CLASS_II	C_INTERCONNECT_S3_AXI_WRITE_
C_MEM_DDR2_RTT	50OHMS	C_S4_AXI_ENABLE
C_MEM_DDR2_DIFF_DQS_EN	YES	C_S4_AXI_PROTOCOL
C_MEM_DDR2_3_PA_SR	FULL	C_S4_AXI_ID_WIDTH
C_MEM_DDR2_3_HIGH_TEMP_SR	NORMAL	C_S4_AXI_ADDR_WIDTH
C_MEM_DDR3_CAS_WR_LATENCY	5	C_S4_AXI_DATA_WIDTH
C_MEM_DDR3_CAS_LATENCY	6	C_S4_AXI_SUPPORTS_READ
C_MEM_DDR3_ODS	DIV6	C_S4_AXI_SUPPORTS_WRITE
C_MEM_DDR3_RTT	DIV4	C_S4_AXI_SUPPORTS_NARROW_BU
C_MEM_DDR3_AUTO_SR	ENABLED	C_S4_AXI_REG_EN0
C_MEM_MOBILE_PA_SR	FULL	C_S4_AXI_REG_EN1
C_MEM_MDDR_ODS	FULL	C_S4_AXI_STRICT_COHERENCY
C_ARB_ALGORITHM	0	C_S4_AXI_ENABLE_AP
C_ARB_NUM_TIME_SLOTS	12	C_INTERCONNECT_S4_AXI_READ_
C_ARB_TIME_SLOT_0	0b000000000001010011	C_INTERCONNECT_S4_AXI_WRITE_
C_ARB_TIME_SLOT_1	0b000000001010011000	C_S5_AXI_ENABLE
C_ARB_TIME_SLOT_2	0b000000010011000001	C_S5_AXI_PROTOCOL
C_ARB_TIME_SLOT_3	0b000000011000001010	C_S5_AXI_ID_WIDTH

	0b0000000000001010011	C_S5_AXI_ADDR_WIDTH
C_ARB_TIME_SLOT_5	0b0000000001010011000	C_S5_AXI_DATA_WIDTH
C_ARB_TIME_SLOT_6	0b0000000010011000001	C_S5_AXI_SUPPORTS_READ
C_ARB_TIME_SLOT_7	0b0000000011000001010	C_S5_AXI_SUPPORTS_WRITE
C_ARB_TIME_SLOT_8	0b0000000000001010011	C_S5_AXI_SUPPORTS_NARROW_BU
C_ARB_TIME_SLOT_9	0b0000000001010011000	C_S5_AXI_REG_EN0
C_ARB_TIME_SLOT_10	0b0000000010011000001	C_S5_AXI_REG_EN1
C_ARB_TIME_SLOT_11	0b0000000011000001010	C_S5_AXI_STRICT_COHERENCY
C_S0_AXI_ENABLE	1	C_S5_AXI_ENABLE_AP
C_S0_AXI_PROTOCOL	AXI4	C_INTERCONNECT_S5_AXI_READ_
C_S0_AXI_ID_WIDTH	1	C_INTERCONNECT_S5_AXI_WRITE_
C_S0_AXI_ADDR_WIDTH	32	C_MCB_USE_EXTERNAL_BUFPLL
C_S0_AXI_DATA_WIDTH	32	C_SYS_RST_PRESENT
C_S0_AXI_SUPPORTS_READ	1	
C_S0_AXI_SUPPORTS_WRITE	1	C_INTERCONNECT_S0_AXI_MASTE
C_S0_AXI_SUPPORTS_NARROW_BURST	0	
C_S0_AXI_REG_EN0	0x00000	C_INTERCONNECT_S0_AXI_AW_RE
C_S0_AXI_REG_EN1	0x01000	C_INTERCONNECT_S0_AXI_AR_RE
C_S0_AXI_STRICT_COHERENCY	0	C_INTERCONNECT_S0_AXI_W_REG
C_S0_AXI_ENABLE_AP	0	C_INTERCONNECT_S0_AXI_R_REG
		C_INTERCONNECT_S0_AXI_B_REG

Post Synthesis Device Utilization

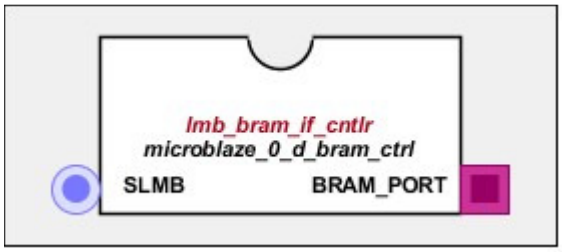
Device utilization information is not available for this IP. Run platgen to generate synthesis informati

microblaze_0_d_bram_ctrl *LMB BRAM Controller*

Local Memory Bus (LMB) Block RAM (BRAM) Interface Controller connects to an lmb bus

IP Specs

Core	Version
lmb_bram_if_cntlr	**3.10.a**



NAME	TYPE	BUSSTD
BRAM_PORT	**INITIATOR**	**XIL_BRAM**
SLMB	**SLAVE**	**LMB**

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_BASEADDR	0x00000000	C_WRITE_ACCESS
C_HIGHADDR	0x00003FFF	C_NUM_LMB
C_FAMILY	spartan6	C_SPLB_CTRL_BASEADDR
C_MASK	0x48000000	C_SPLB_CTRL_HIGHADDR
C_MASK1	0x00800000	C_SPLB_CTRL_AWIDTH

C_MASK2	0x00800000	C_SPLB_CTRL_DWIDTH
C_MASK3	0x00800000	C_SPLB_CTRL_P2P
C_LMB_AWIDTH	32	C_SPLB_CTRL_MID_WIDTH
C_LMB_DWIDTH	32	C_SPLB_CTRL_NUM_MASTERS
C_ECC	0	C_SPLB_CTRL_SUPPORT_BURSTS
C_INTERCONNECT	0	C_SPLB_CTRL_NATIVE_DWIDTH
C_FAULT_INJECT	0	C_SPLB_CTRL_CLK_FREQ_HZ
C_CE_FAILING_REGISTERS	0	C_S_AXI_CTRL_ACLK_FREQ_HZ
C_UE_FAILING_REGISTERS	0	C_S_AXI_CTRL_BASEADDR
C_ECC_STATUS_REGISTERS	0	C_S_AXI_CTRL_HIGHADDR
C_ECC_ONOFF_REGISTER	0	C_S_AXI_CTRL_ADDR_WIDTH
C_ECC_ONOFF_RESET_VALUE	1	C_S_AXI_CTRL_DATA_WIDTH
C_CE_COUNTER_WIDTH	0	C_S_AXI_CTRL_PROTOCOL

Post Synthesis Device Utilization

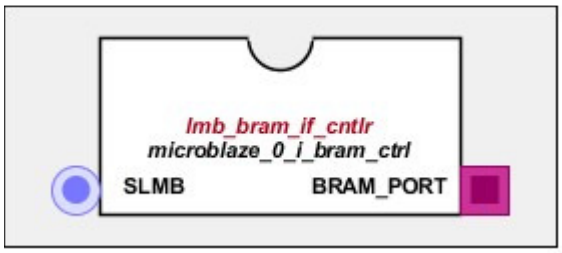
Device utilization information is not available for this IP. Run platgen to generate synthesis informati

microblaze_0_i_bram_ctrl *LMB BRAM Controller*

Local Memory Bus (LMB) Block RAM (BRAM) Interface Controller connects to an lmb bus

IP Specs

Core	Version
lmb_bram_if_cntlr	**3.10.a**



NAME	TYPE	BUSSTD
BRAM_PORT	**INITIATOR**	**XIL_BRAM** *n*
SLMB	**SLAVE**	**LMB**

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_BASEADDR	0x00000000	C_WRITE_ACCESS
C_HIGHADDR	0x00003FFF	C_NUM_LMB
C_FAMILY	spartan6	C_SPLB_CTRL_BASEADDR
C_MASK	0x48000000	C_SPLB_CTRL_HIGHADDR
C_MASK1	0x00800000	C_SPLB_CTRL_AWIDTH
C_MASK2	0x00800000	C_SPLB_CTRL_DWIDTH
C_MASK3	0x00800000	C_SPLB_CTRL_P2P
C_LMB_AWIDTH	32	C_SPLB_CTRL_MID_WIDTH
C_LMB_DWIDTH	32	C_SPLB_CTRL_NUM_MASTERS
C_ECC	0	C_SPLB_CTRL_SUPPORT_BURSTS
C_INTERCONNECT	0	C_SPLB_CTRL_NATIVE_DWIDTH
C_FAULT_INJECT	0	C_SPLB_CTRL_CLK_FREQ_HZ
C_CE_FAILING_REGISTERS	0	C_S_AXI_CTRL_ACLK_FREQ_HZ

C_UE_FAILING_REGISTERS	0	C_S_AXI_CTRL_BASEADDR
C_ECC_STATUS_REGISTERS	0	C_S_AXI_CTRL_HIGHADDR
C_ECC_ONOFF_REGISTER	0	C_S_AXI_CTRL_ADDR_WIDTH
C_ECC_ONOFF_RESET_VALUE	1	C_S_AXI_CTRL_DATA_WIDTH
C_CE_COUNTER_WIDTH	0	C_S_AXI_CTRL_PROTOCOL

Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

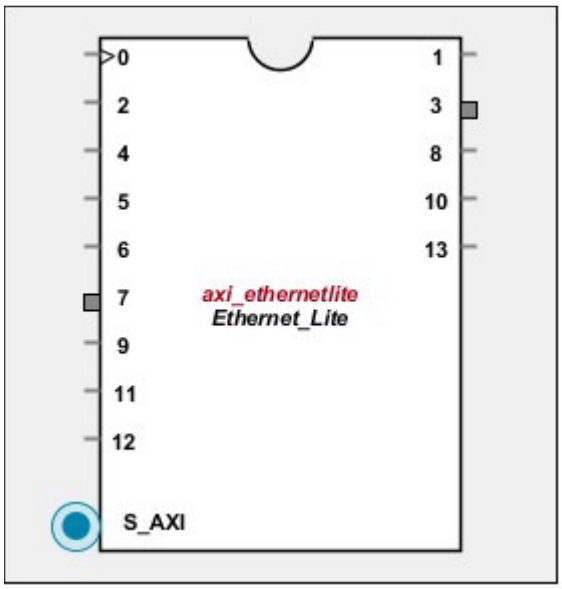
Peripherals

Ethernet_Lite *AXI 10/100 Ethernet MAC Lite*

'IEEE Std. 802.3 MII interface MAC with AXI interface, lightweight implementation'

IP Specs

Core	Version	Documentation
axi_ethernetlite	**1.01.b**	***IP***



PORT LIST

These are the ports listed in the MHS file. Please complete information about

#	NAME	DIR	[LSB:MSB]
0	S_AXI_ACLK	**I**	**1**
1	PHY_tx_en	**O**	**1**
2	PHY_tx_clk	**I**	**1**
3	PHY_tx_data	**O**	**0:3**
4	PHY_rx_er	**I**	**1**
5	PHY_dv	**I**	**1**
6	PHY_rx_clk	**I**	**1**
7	PHY_rx_data	**I**	**0:3**
8	PHY_rst_n	**O**	**1**
9	PHY_MDIO	**IO**	**1**
10	PHY_MDC	**O**	**1**
11	PHY_crs	**I**	**1**
12	PHY_col	**I**	**1**
13	IP2INTC_Irpt	**O**	**1**

Bus Interfac

NAME	TYPE	BUSSTD	BUS
S_AXI	**SLAVE**	**AXI**	*axi4lite_0*

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name

C_S_AXI_PROTOCOL	AXI4LITE	C_INCLUDE_GLOBAL_BUFFERS
C_FAMILY	spartan6	C_INCLUDE_INTERNAL_LOOPBACK
C_INSTANCE	Ethernet_Lite	C_DUPLEX
C_BASEADDR	0x40E00000	C_TX_PING_PONG
C_HIGHADDR	0x40E0FFFF	C_RX_PING_PONG
C_S_AXI_ACLK_PERIOD_PS	10000	C_INCLUDE_PHY_CONSTRAINTS
C_S_AXI_ADDR_WIDTH	13	C_INTERCONNECT_S_AXI_WRITE_AC
C_S_AXI_DATA_WIDTH	32	C_INTERCONNECT_S_AXI_READ_ACC
C_S_AXI_ID_WIDTH	1	C_S_AXI_SUPPORTS_NARROW_BURS
C_INCLUDE_MDIO	1	

Post Synthesis Device Utilization

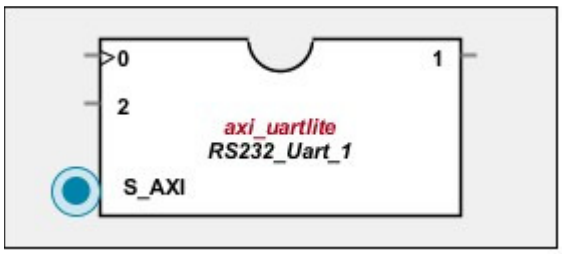
Device utilization information is not available for this IP. Run platgen to generate synthesis informati

RS232_Uart_1 *AXI UART (Lite)*

Generic UART (Universal Asynchronous Receiver/Transmitter) for AXI.

IP Specs

Core	Version	Documentation
axi_uartlite	**1.02.a**	***IP***



PORT LIST

These are the ports listed in the MHS file. Please complete information about

#	NAME	DIR	[LSB:M
0	S_AXI_ACLK	**I**	**1**
1	TX	**O**	**1**
2	RX	**I**	**1**

Bus Interfac

NAME	TYPE	BUSSTD	BUS
S_AXI	**SLAVE**	**AXI**	*axi4lite_*

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_FAMILY	spartan6	C_S_AXI_DATA_WIDTH
C_INSTANCE	RS232_Uart_1	C_BAUDRATE
C_S_AXI_ACLK_FREQ_HZ	100000000	C_DATA_BITS
C_BASEADDR	0x40600000	C_USE_PARITY
C_HIGHADDR	0x4060FFFF	C_ODD_PARITY
C_S_AXI_ADDR_WIDTH	4	C_S_AXI_PROTOCOL

Post Synthesis Device Utilization

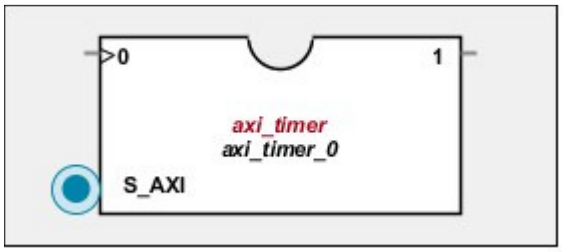
Device utilization information is not available for this IP. Run platgen to generate synthesis informati

axi_timer_0 *AXI Timer/Counter*

Timer counter with AXI interface

IP Specs

Core	Version	Documentation
axi_timer	**1.03.a**	***IP***



PORT LIST

These are the ports listed in the MHS file. Please complete information about

#	NAME	DIR	[LSB:M
0	S_AXI_ACLK	**I**	**1**
1	Interrupt	**O**	**1**

Bus Interfac

NAME	TYPE	BUSSTD	BUS
S_AXI	**SLAVE**	**AXI**	*axi4lite_*

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_S_AXI_PROTOCOL	AXI4LITE	C_GEN0_ASSERT
C_FAMILY	spartan6	C_GEN1_ASSERT
C_INSTANCE	axi_timer_0	C_BASEADDR
C_COUNT_WIDTH	32	C_HIGHADDR
C_ONE_TIMER_ONLY	0	C_S_AXI_ADDR_WIDTH
C_TRIG0_ASSERT	1	C_S_AXI_DATA_WIDTH
C_TRIG1_ASSERT	1	

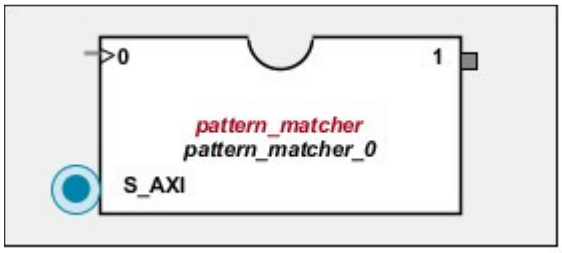
Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

pattern_matcher_0 *PATTERN_MATCHER*

IP Specs

Core	Version
pattern_matcher	**1.00.a**



PORT LIST

These are the ports listed ir

#	NAME	DIR	[LSB:MS
0	S_AXI_ACLK	**I**	**1**
1	LED	**O**	**0:7**

Bus Interfac

NAME	TYPE	BUSSTD	BUS
S_AXI	**SLAVE**	**AXI**	*axi4lite_(*

Parameters		
These are the current parameter settings for this module. Parameters marked with yellow indicate parameters set by the user. Parameters marked with blue indicate parameters set by the system.		
Name	**Value**	**Name**
C_S_AXI_DATA_WIDTH	32	C_FAMILY
C_S_AXI_ADDR_WIDTH	32	C_NUM_REG
C_S_AXI_MIN_SIZE	0x000001FF	C_NUM_MEM
C_USE_WSTRB	0	C_SLV_AWIDTH
C_DPHASE_TIMEOUT	8	C_SLV_DWIDTH
C_BASEADDR	0x75E00000	C_S_AXI_PROTOCOL
C_HIGHADDR	0x75E0FFFF	

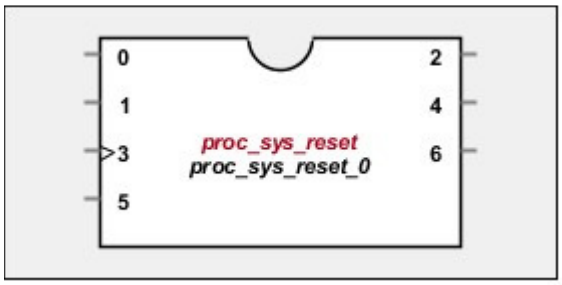
Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

proc_sys_reset_0 *Processor System Reset Module*

Reset management module

IP Specs		
Core	**Version**	**Documentation**
proc_sys_reset	**3.00.a**	***IP***



PORT L

These are the ports listed in the MHS file. Pleas
information about

#	NAME	DIR	[LSB:MSB]	
0	MB_Debug_Sys_Rst	**I**	**1**	pr
1	Dcm_locked	**I**	**1**	pr
2	MB_Reset	**O**	**1**	pr
3	Slowest_sync_clk	**I**	**1**	clk
4	Interconnect_aresetn	**O**	**1**	pr
5	Ext_Reset_In	**I**	**1**	RE
6	BUS_STRUCT_RESET	**O**	**1**	pr

Parameters	
These are the current parameter settings for this module. Parameters marked with yellow indicate parameters set by the user. Parameters marked with blue indicate parameters set by the system.	
Name	**Value**
C_EXT_RST_WIDTH	4
C_AUX_RST_WIDTH	4
C_EXT_RESET_HIGH	0
C_AUX_RESET_HIGH	1
C_NUM_BUS_RST	1

C_NUM_PERP_RST	1
C_NUM_INTERCONNECT_ARESETN	1
C_NUM_PERP_ARESETN	1
C_FAMILY	spartan6

Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis information.

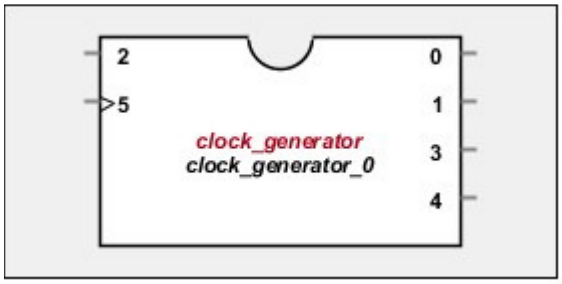
IP

clock_generator_0 *Clock Generator*

Clock generator for processor system.

IP Specs

Core	Version	Documentation
clock_generator	**4.03.a**	***IP***



PORT LIST

These are the ports listed in the MHS file. Please complete information about

#	NAME	DIR	[LSB:MSB]	
0	LOCKED	**O**	**1**	proc
1	CLKOUT2	**O**	**1**	clk_
2	RST	**I**	**1**	RESI
3	CLKOUT0	**O**	**1**	clk_
4	CLKOUT1	**O**	**1**	clk_
5	CLKIN	**I**	**1**	GCLI

Parameters

These are the current parameter settings for this module.

Parameters marked with yellow indicate parameters set by the user.
Parameters marked with blue indicate parameters set by the system.

Name	Value	Name
C_FAMILY	spartan6	C_CLKOUT10_PHASE
C_DEVICE	6slx45	C_CLKOUT10_GROUP
C_PACKAGE	csg324	C_CLKOUT10_BUF
C_SPEEDGRADE	-3	C_CLKOUT10_VARIABLE_PHASE
C_CLKIN_FREQ	100000000	C_CLKOUT11_FREQ
C_CLKOUT0_FREQ	600000000	C_CLKOUT11_PHASE
C_CLKOUT0_PHASE	0	C_CLKOUT11_GROUP
C_CLKOUT0_GROUP	PLL0	C_CLKOUT11_BUF
C_CLKOUT0_BUF	FALSE	C_CLKOUT11_VARIABLE_PHASE
C_CLKOUT0_VARIABLE_PHASE	FALSE	C_CLKOUT12_FREQ
C_CLKOUT1_FREQ	600000000	C_CLKOUT12_PHASE
C_CLKOUT1_PHASE	180	C_CLKOUT12_GROUP

C_CLKOUT1_GROUP	PLL0	C_CLKOUT12_BUF	
C_CLKOUT1_BUF	FALSE	C_CLKOUT12_VARIABLE_PHASE	
C_CLKOUT1_VARIABLE_PHASE	FALSE	C_CLKOUT13_FREQ	
C_CLKOUT2_FREQ	100000000	C_CLKOUT13_PHASE	
C_CLKOUT2_PHASE	0	C_CLKOUT13_GROUP	
C_CLKOUT2_GROUP	PLL0	C_CLKOUT13_BUF	
C_CLKOUT2_BUF	TRUE	C_CLKOUT13_VARIABLE_PHASE	
C_CLKOUT2_VARIABLE_PHASE	FALSE	C_CLKOUT14_FREQ	
C_CLKOUT3_FREQ	0	C_CLKOUT14_PHASE	
C_CLKOUT3_PHASE	0	C_CLKOUT14_GROUP	
C_CLKOUT3_GROUP	NONE	C_CLKOUT14_BUF	
C_CLKOUT3_BUF	TRUE	C_CLKOUT14_VARIABLE_PHASE	
C_CLKOUT3_VARIABLE_PHASE	FALSE	C_CLKOUT15_FREQ	
C_CLKOUT4_FREQ	0	C_CLKOUT15_PHASE	
C_CLKOUT4_PHASE	0	C_CLKOUT15_GROUP	
C_CLKOUT4_GROUP	NONE	C_CLKOUT15_BUF	
C_CLKOUT4_BUF	TRUE	C_CLKOUT15_VARIABLE_PHASE	
C_CLKOUT4_VARIABLE_PHASE	FALSE	C_CLKFBIN_FREQ	
C_CLKOUT5_FREQ	0	C_CLKFBIN_DESKEW	
C_CLKOUT5_PHASE	0	C_CLKFBOUT_FREQ	
C_CLKOUT5_GROUP	NONE	C_CLKFBOUT_PHASE	
C_CLKOUT5_BUF	TRUE	C_CLKFBOUT_GROUP	
C_CLKOUT5_VARIABLE_PHASE	FALSE	C_CLKFBOUT_BUF	
C_CLKOUT6_FREQ	0	C_PSDONE_GROUP	
C_CLKOUT6_PHASE	0	C_EXT_RESET_HIGH	
C_CLKOUT6_GROUP	NONE	C_CLK_PRIMITIVE_FEEDBACK_BUF	
C_CLKOUT6_BUF	TRUE	C_CLKOUT0_DUTY_CYCLE	
C_CLKOUT6_VARIABLE_PHASE	FALSE	C_CLKOUT1_DUTY_CYCLE	
C_CLKOUT7_FREQ	0	C_CLKOUT2_DUTY_CYCLE	
C_CLKOUT7_PHASE	0	C_CLKOUT3_DUTY_CYCLE	
C_CLKOUT7_GROUP	NONE	C_CLKOUT4_DUTY_CYCLE	
C_CLKOUT7_BUF	TRUE	C_CLKOUT5_DUTY_CYCLE	
C_CLKOUT7_VARIABLE_PHASE	FALSE	C_CLKOUT6_DUTY_CYCLE	
C_CLKOUT8_FREQ	0	C_CLKOUT7_DUTY_CYCLE	
C_CLKOUT8_PHASE	0	C_CLKOUT8_DUTY_CYCLE	
C_CLKOUT8_GROUP	NONE	C_CLKOUT9_DUTY_CYCLE	
C_CLKOUT8_BUF	TRUE	C_CLKOUT10_DUTY_CYCLE	
C_CLKOUT8_VARIABLE_PHASE	FALSE	C_CLKOUT11_DUTY_CYCLE	
C_CLKOUT9_FREQ	0	C_CLKOUT12_DUTY_CYCLE	
C_CLKOUT9_PHASE	0	C_CLKOUT13_DUTY_CYCLE	
C_CLKOUT9_GROUP	NONE	C_CLKOUT14_DUTY_CYCLE	
C_CLKOUT9_BUF	TRUE	C_CLKOUT15_DUTY_CYCLE	
C_CLKOUT9_VARIABLE_PHASE	FALSE	C_CLK_GEN	
C_CLKOUT10_FREQ	0		

Post Synthesis Device Utilization

Device utilization information is not available for this IP. Run platgen to generate synthesis informati

Timing Information

Post Synthesis Clock Limits
No clocks could be identified in the design. Run platgen to generate synthesis information.