EE 577b Spring 2018

Conformal Logic Equivalence Checking (LEC) Tutorial

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This tutorial provides a quick getting-strated guide to Cadence Conformal logic equivalence checking. The basic flow is to input both an RTL netlist and a synthesized netlist and then have Conformal check whether both netlists are equal. Think of it as an LVS for Verilog. This is a powerful tool to get a formal proof that the output from Synthesis matches the original RTL code without having to run simulation.

The following files are the example used in this tutorial:

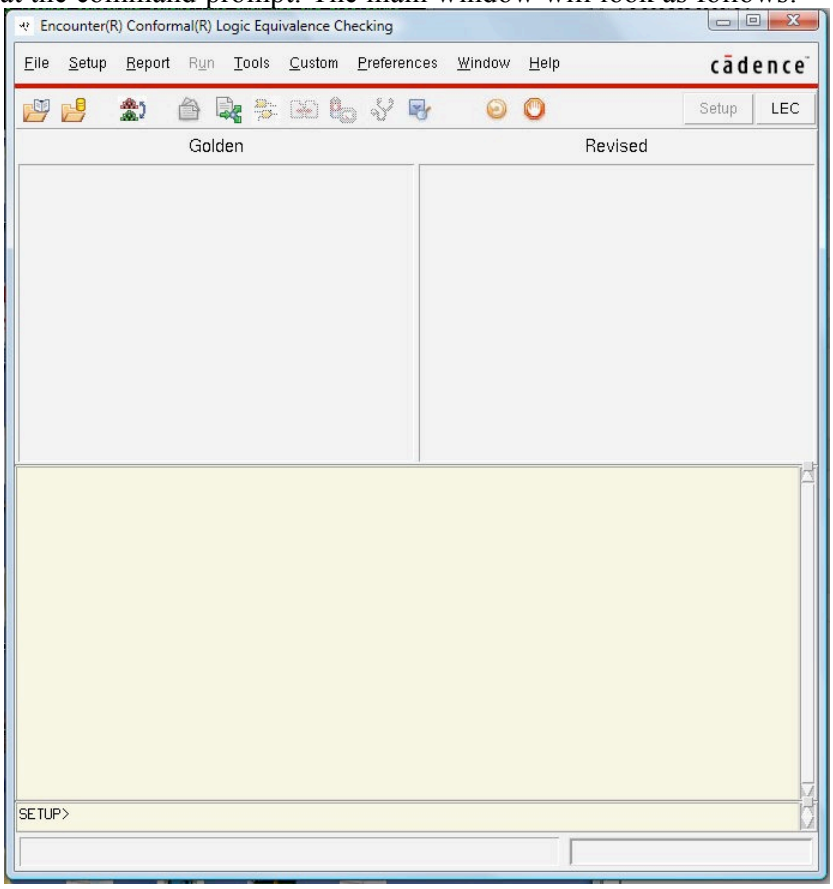
- adder1bit.v: The RTL netlist
- adder1bit.syn.v: The gate level netlist

You may find the cell library at
"/~/ ee577BToolDemo/libs/gscl45nm.v"

1. To start the tool, type

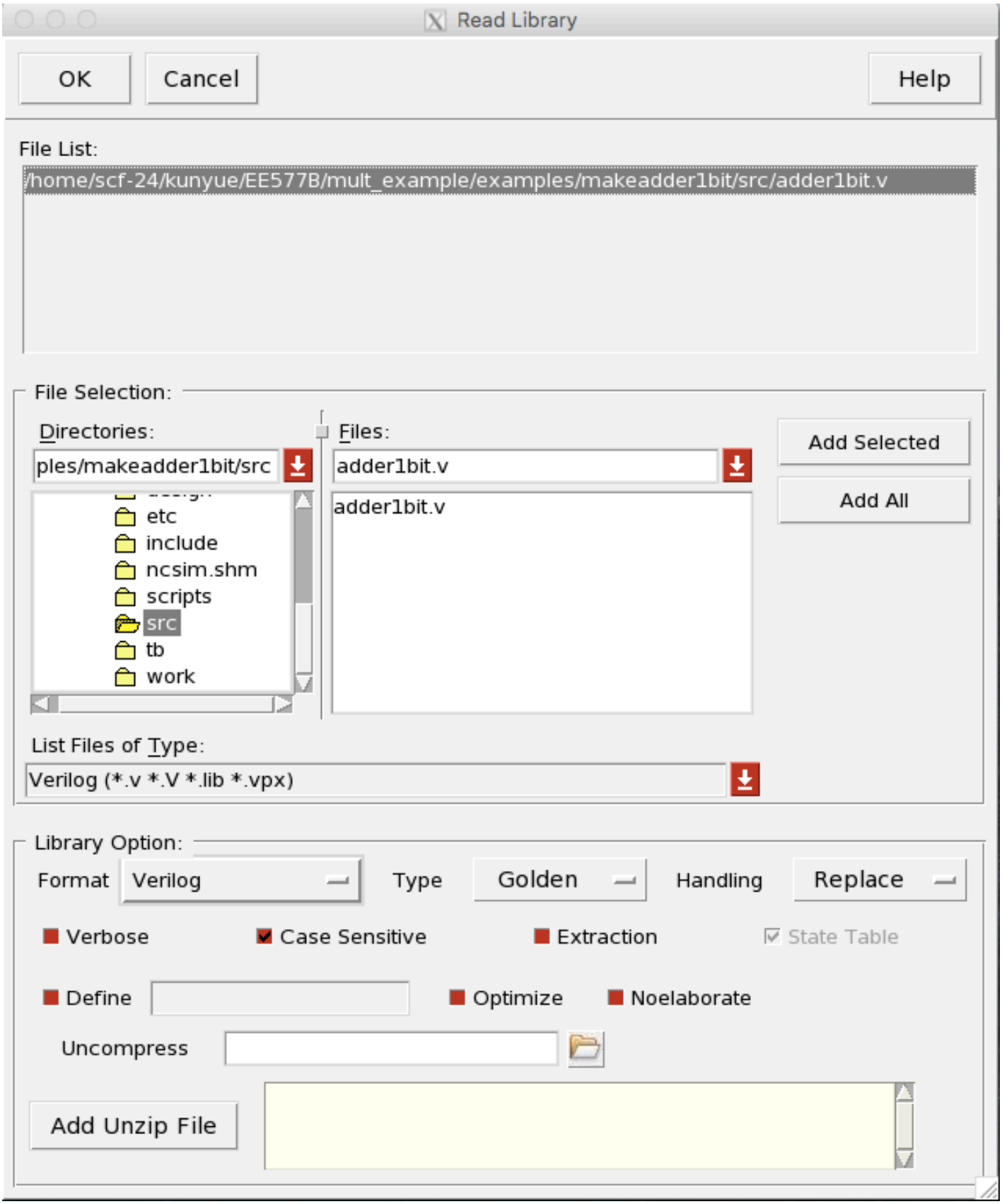
```
% lec &
```

at the command prompt. The main window will look as follows:



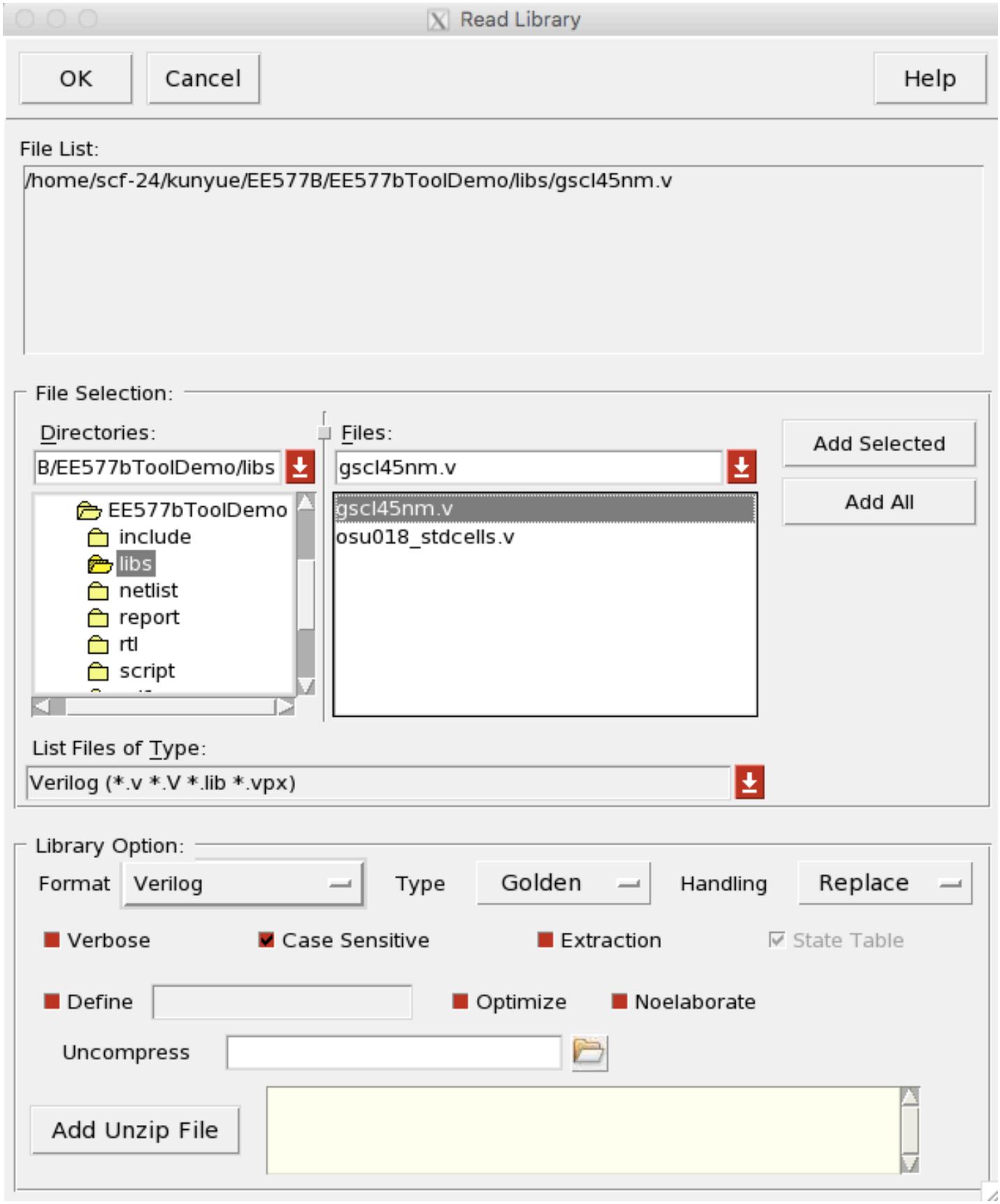
2. Read the RTL Netlist

First we read in the original RTL netlist. This will be considered as the "golden" design. It will serve as the reference for the comparison. Click on "File -> Read Design". Find " adder1bit.v" and double-click on it. Also note that "Type" is set to "Golden", which is correct. The dialog should look like the following. Then, load the file by clicking "OK".



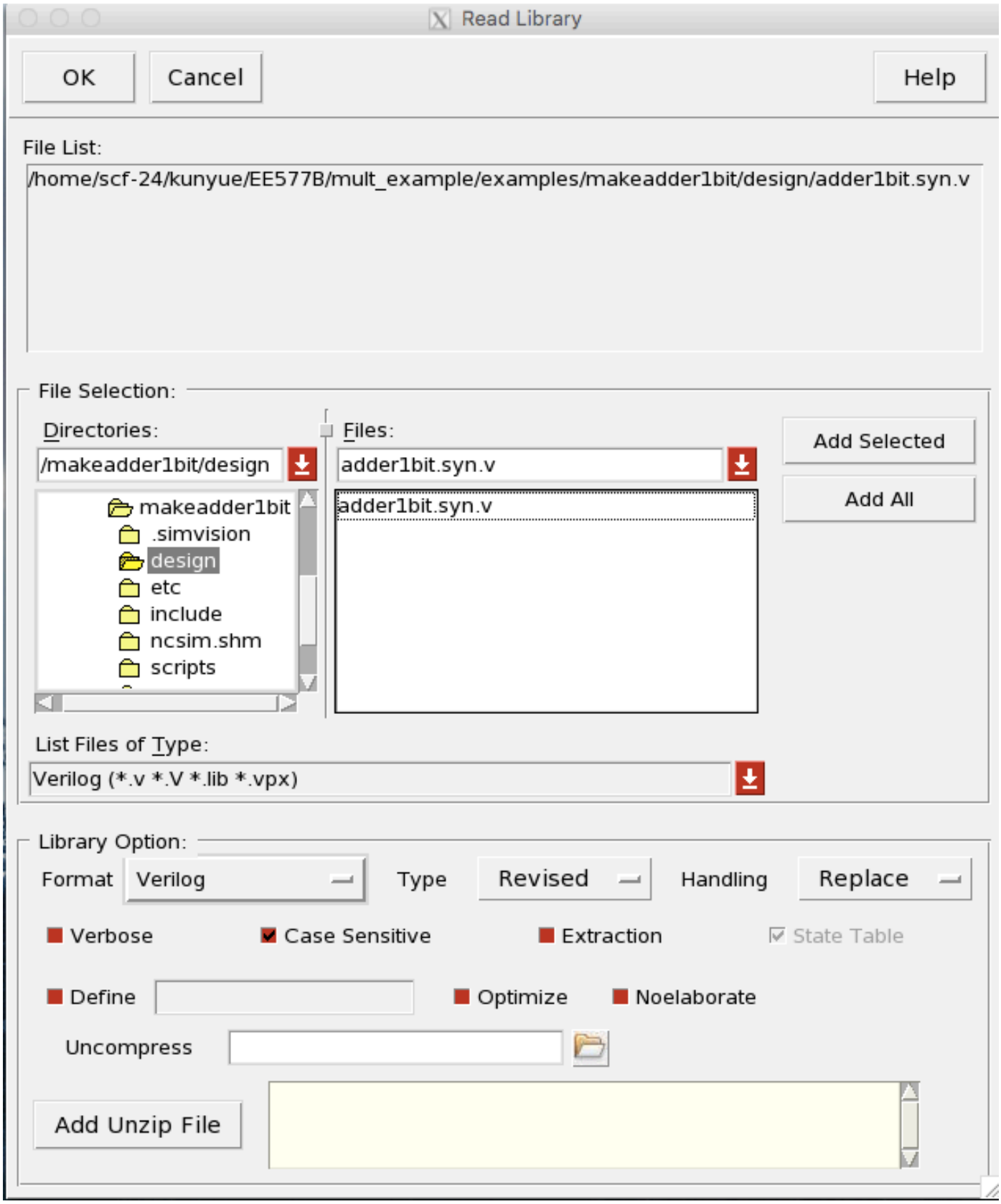
3. Read the Library

Since the gate level netlist contains standard cells we also need to read in a file with the cell definitions. Click on "File -> Read Library" and find the cell library at "/~/ ee577BToolDemo/libs/gscl45nm.v". Double-click on it. Then change the type from "Both" to "Revised" since the cells are only used in the revised design. This should look as follows. Again, load the cell library by clicking "OK".



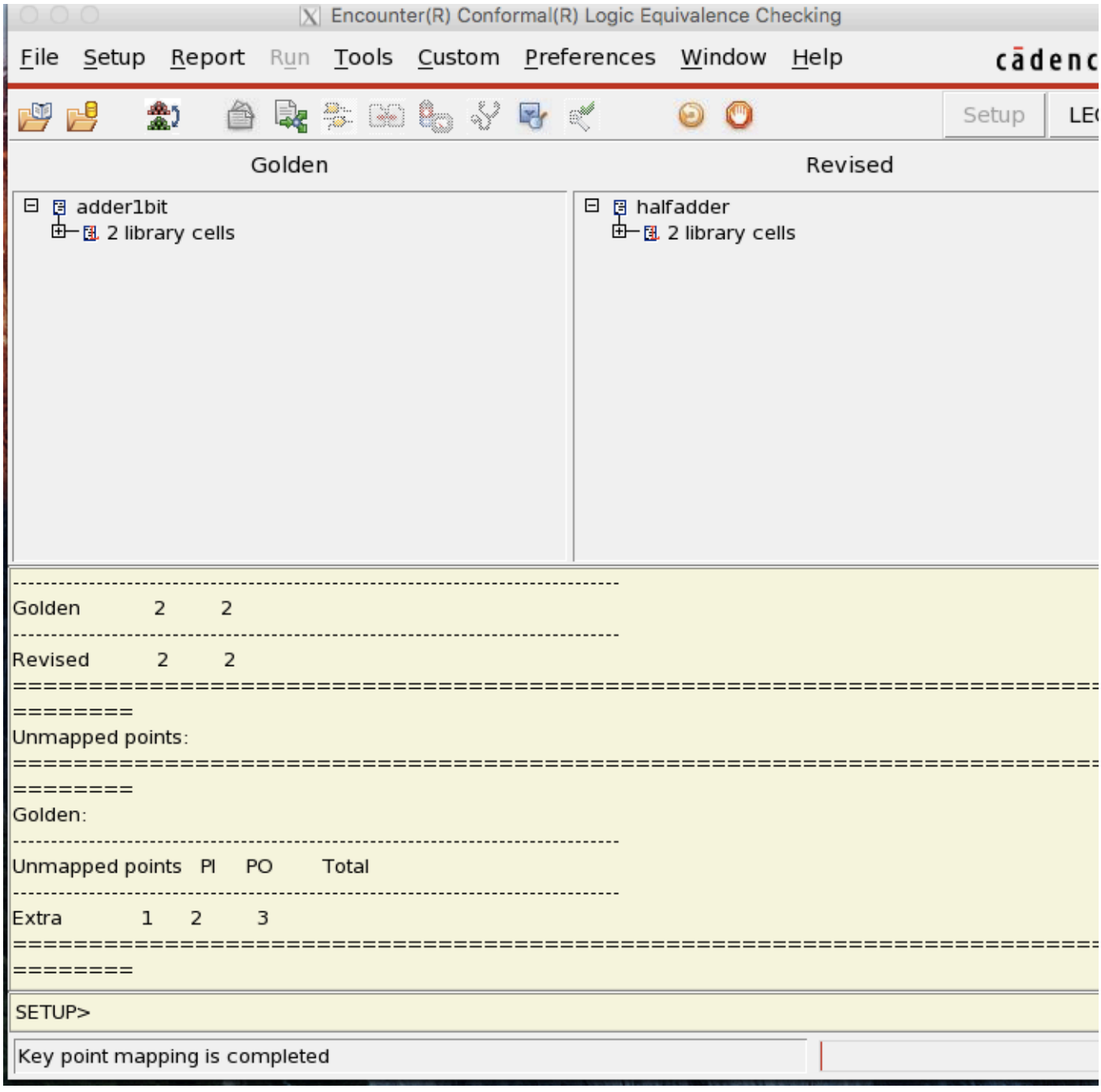
4. Read the Gate Level Netlist

Now, the cells are loaded. We can bring in the netlist. Do "File -> Read Design" and double-click on "adder1bit.syn.v". Note that Conformal changed the "Type" for us to "Revised". The window should look like this. Load the cell library by clicking "OK".



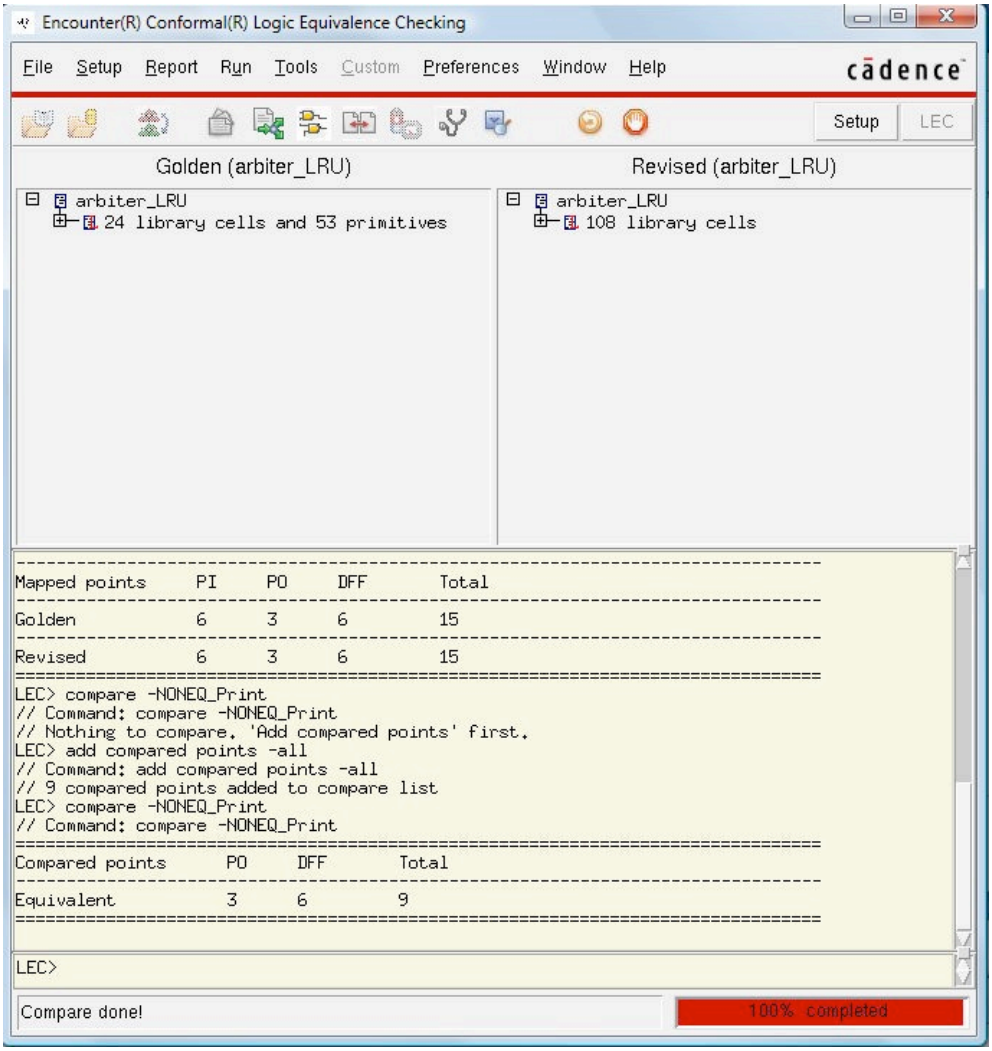
5. Running Comparison

Conformal has 2 operating modes: "Setup" and "LEC". So far we worked in "Setup" mode, where we input designs and setup pin mappings if we needed to. Now we switch to "LEC" mode. Click on the "LEC" icon the upper right hand corner. The window should look like this:



Note the table that was printed. It lists the primary inputs (PI) and primary outputs (PO) in both the revised and golden design. They are equal, which is a good sign. There could be a difference, e.g. if the revised design had differential outputs. Conformal has commands to specify those conditions.

The final step is to do "Run -> Compare" and to select “Display Non-equivalent Points” and “Add All Compare Points”. Then click “Compare”. Now Conformal will reduce both designs to a canonical representation and check if they are equal. In Conformal, if you see "Equivalent" after running "compare" command, it means golden design and revised design are equivalent. If they don't match with each other, you will see "Non-equivalent".



You may save the result by doing the following.

1) Go to File-> “Save transcript”
2) Choose a file name and save it by clicking OK.
3) You may find the file under the directory where you saved the file.

[Ref] http://www.chiptalk.org/modules/wfsection/article.php?articleid=3