Question 1:

1. Yes, the synthesis results meet the timing contraints.

The critical path is from stage_reg[2] to RA output port and the slack is 4.51ns.

2. The binary design has smaller area which is 380.13.

3. The simulation will not successfully run because you need to include the library Verilog file and annotate path delay to your design using .sdf file. After doing that, simulation can run successfully and the results of RTL model match with netlist which means the function of netlist is correct. Besides, there are glitches in combinational output because we consider the path delay of each cell.