Lecture 2
Platform 0 revisited

Computing platforms, semester 2

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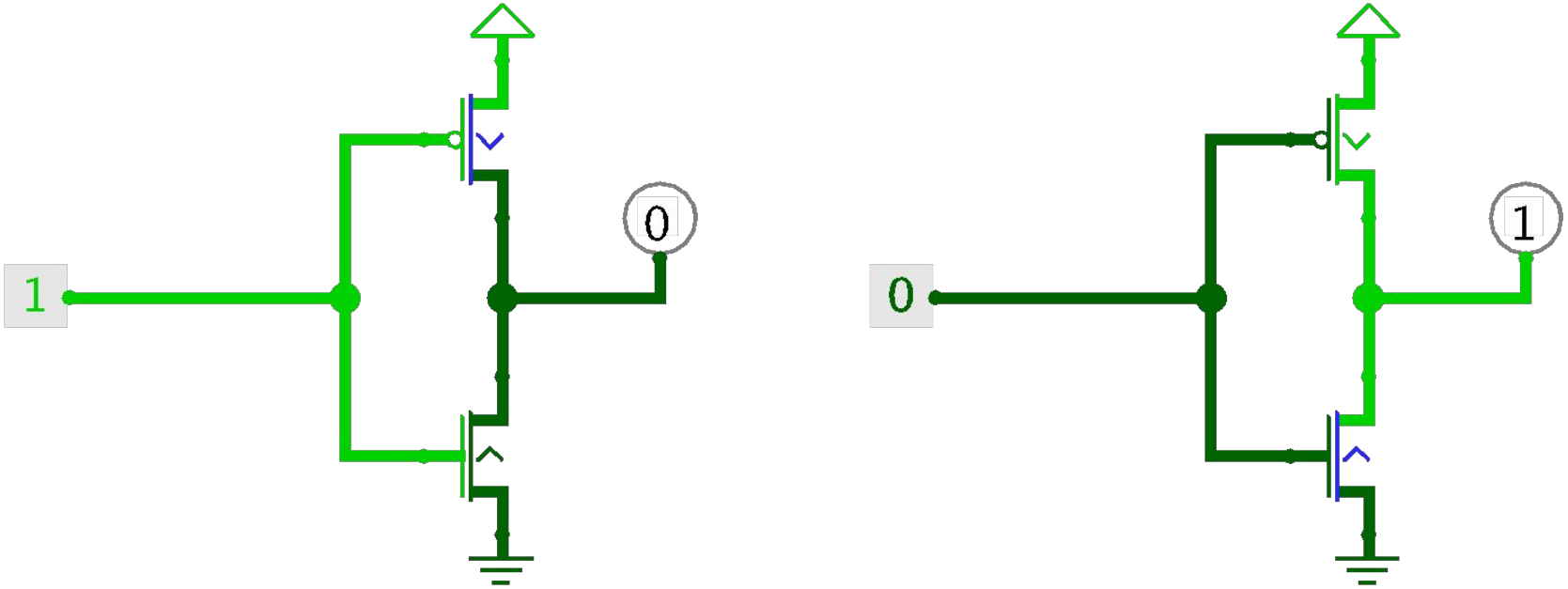
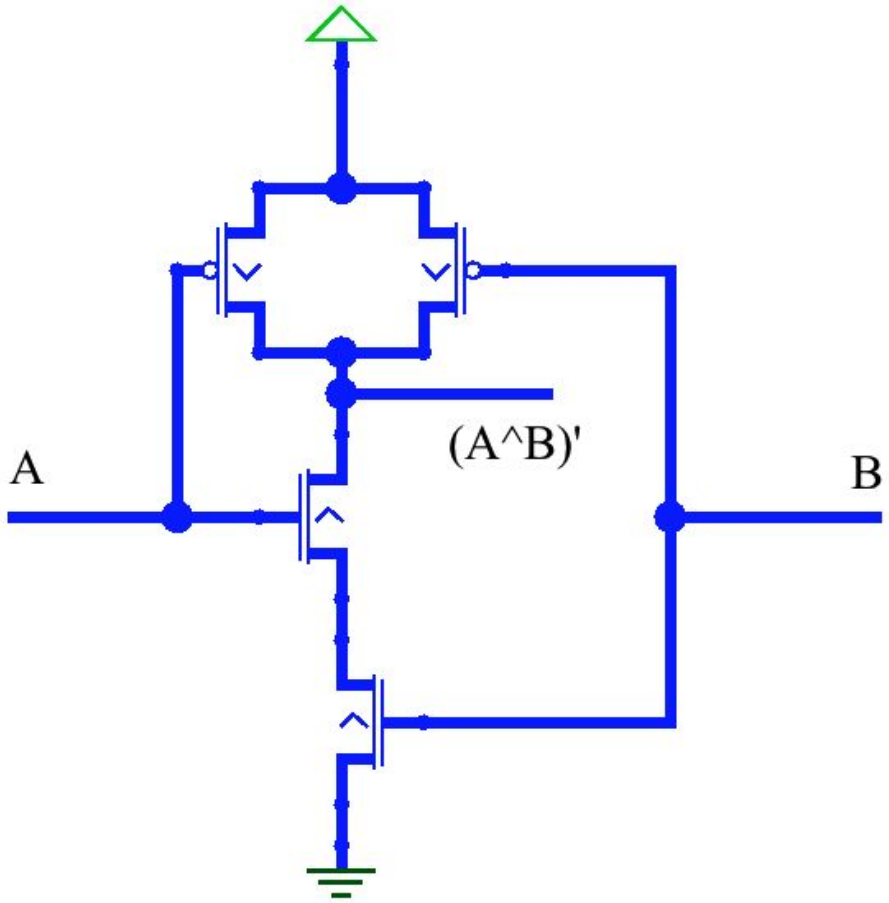
2019

NOT gate (logical invertor)



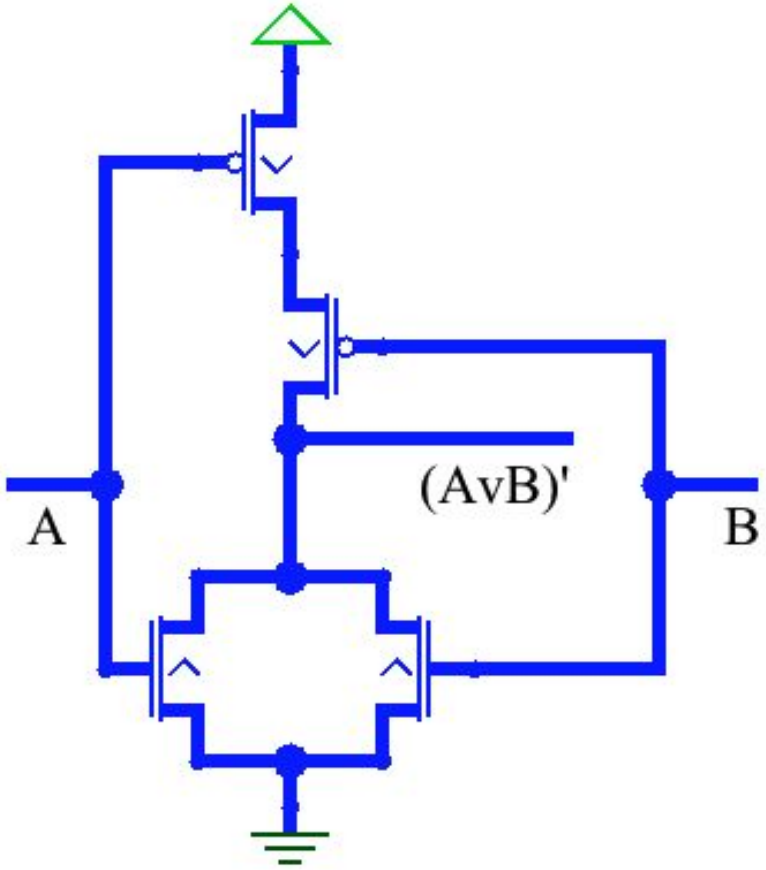
NAND gate

Output=Not(A and B)
(A^B)’ in Boolean notation
You can turn in into ”normal” AND
By adding invertor (Not gate)



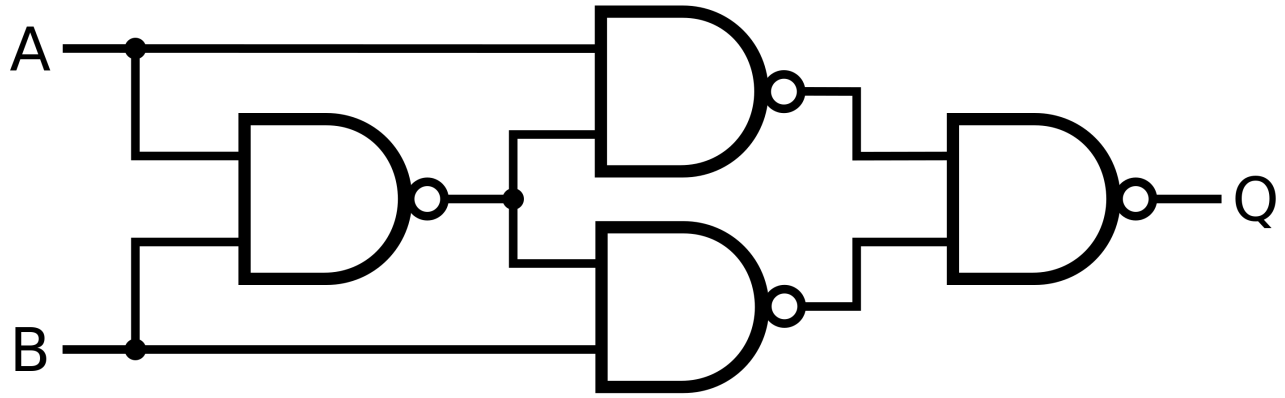
NOR gate

NAND gate turned upside down
From Boolean algebra, you should remember, that (AvB)'=(A')^(B')
Having AND, OR and NOT operations, we can implement any logical expression

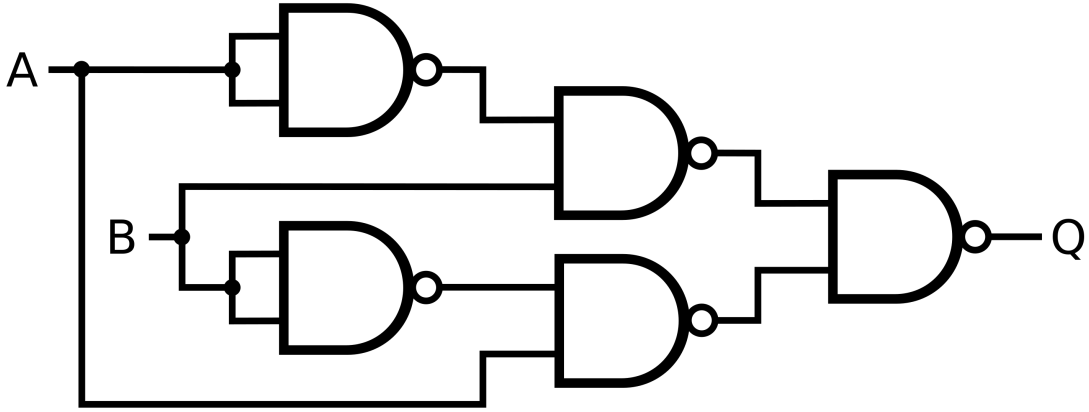


XOR gate

A	B	*A* xor *B*
0	0	0
0	1	1
1	0	1
1	1	0

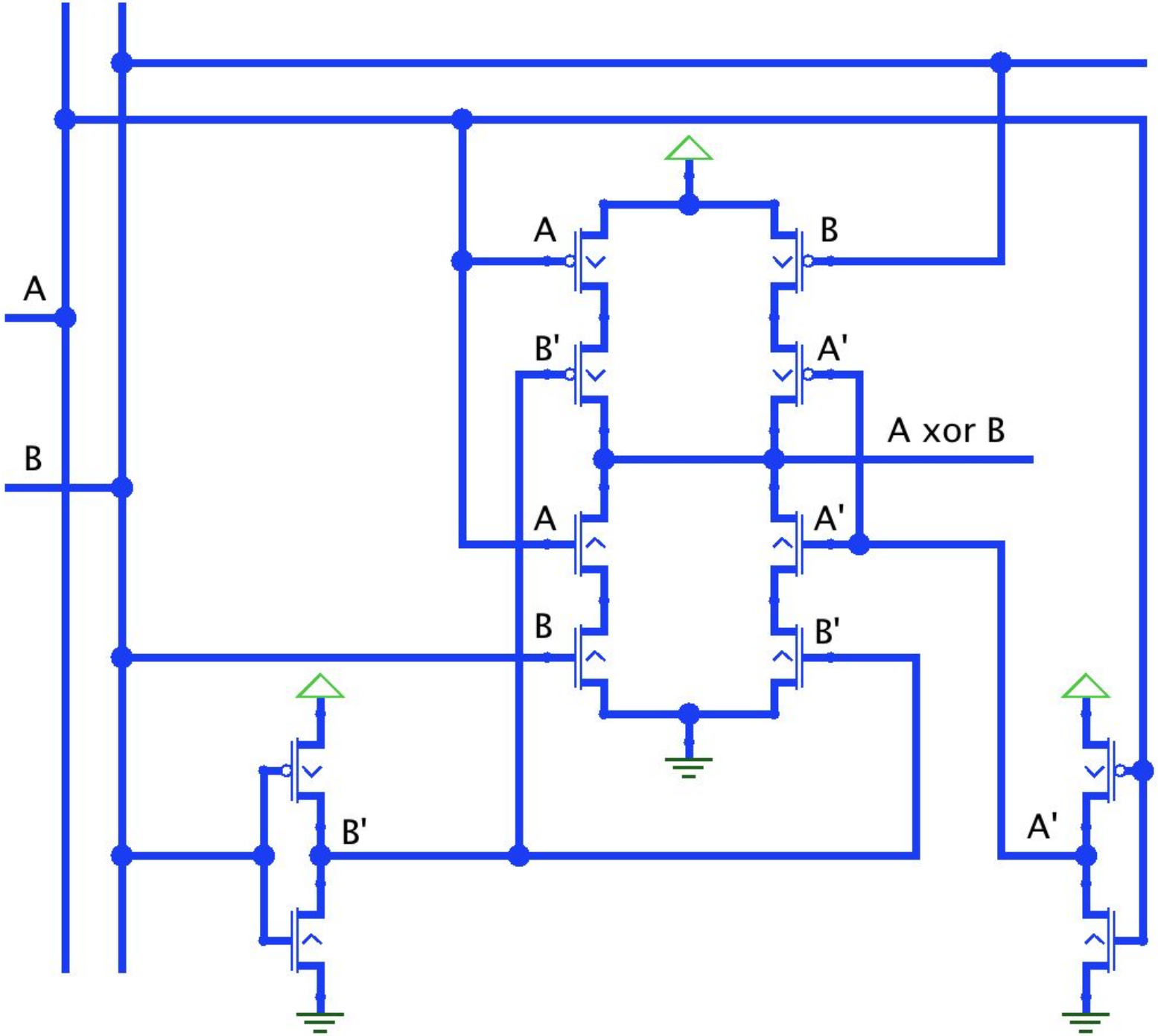


4 NAND gates * 4 transistors each = 16 transistors



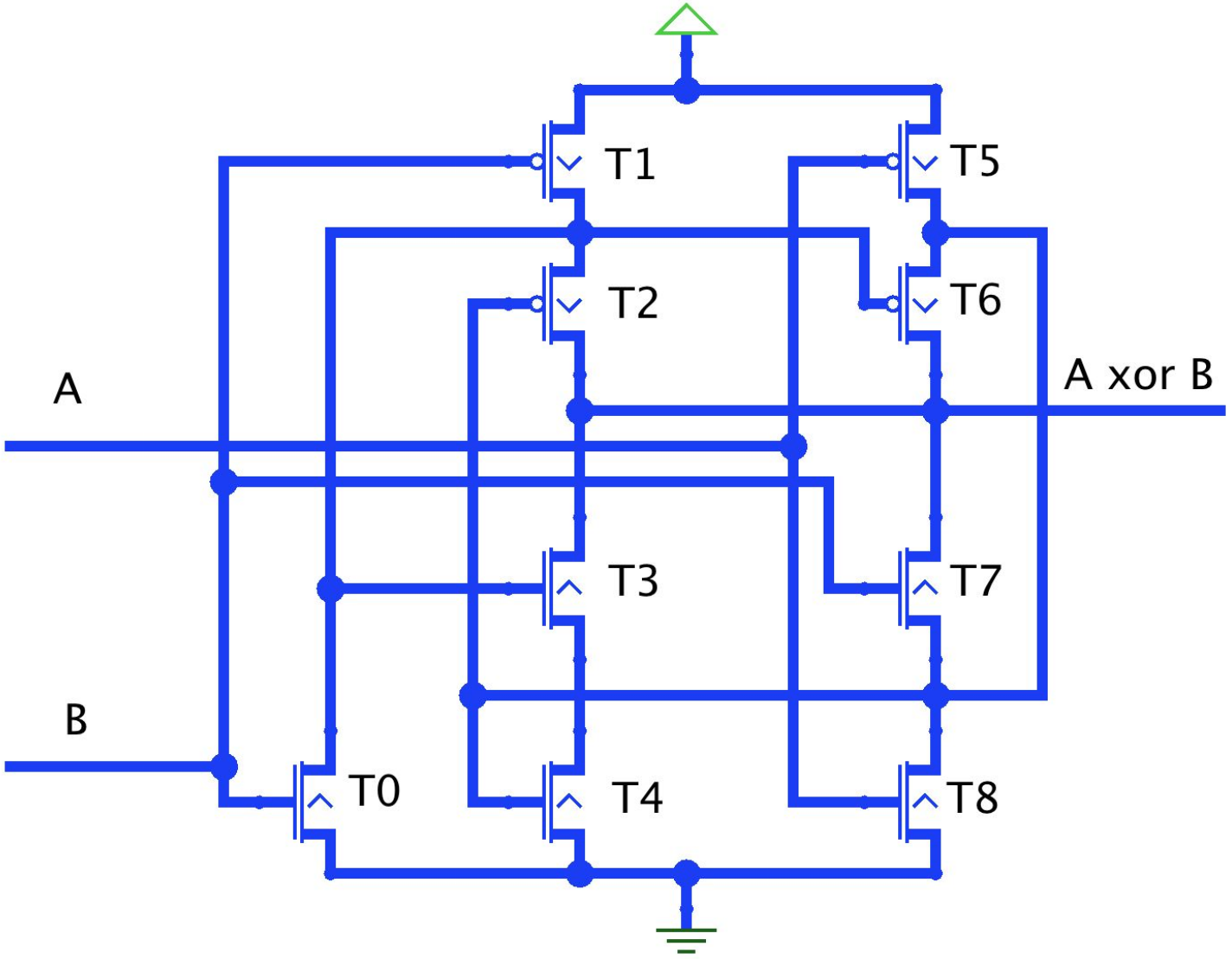
XOR gate optimized on transistor level

- At the core, we have symmetrical circuit which is not equivalent to one of basic gates
- To have output=1, we need one of upper pairs open: (A&B’=1 | A’&B=1)
- To have output=0, we need one of lower pairs open: (A&B=1 | A’&B’=1)
- 12 transistors



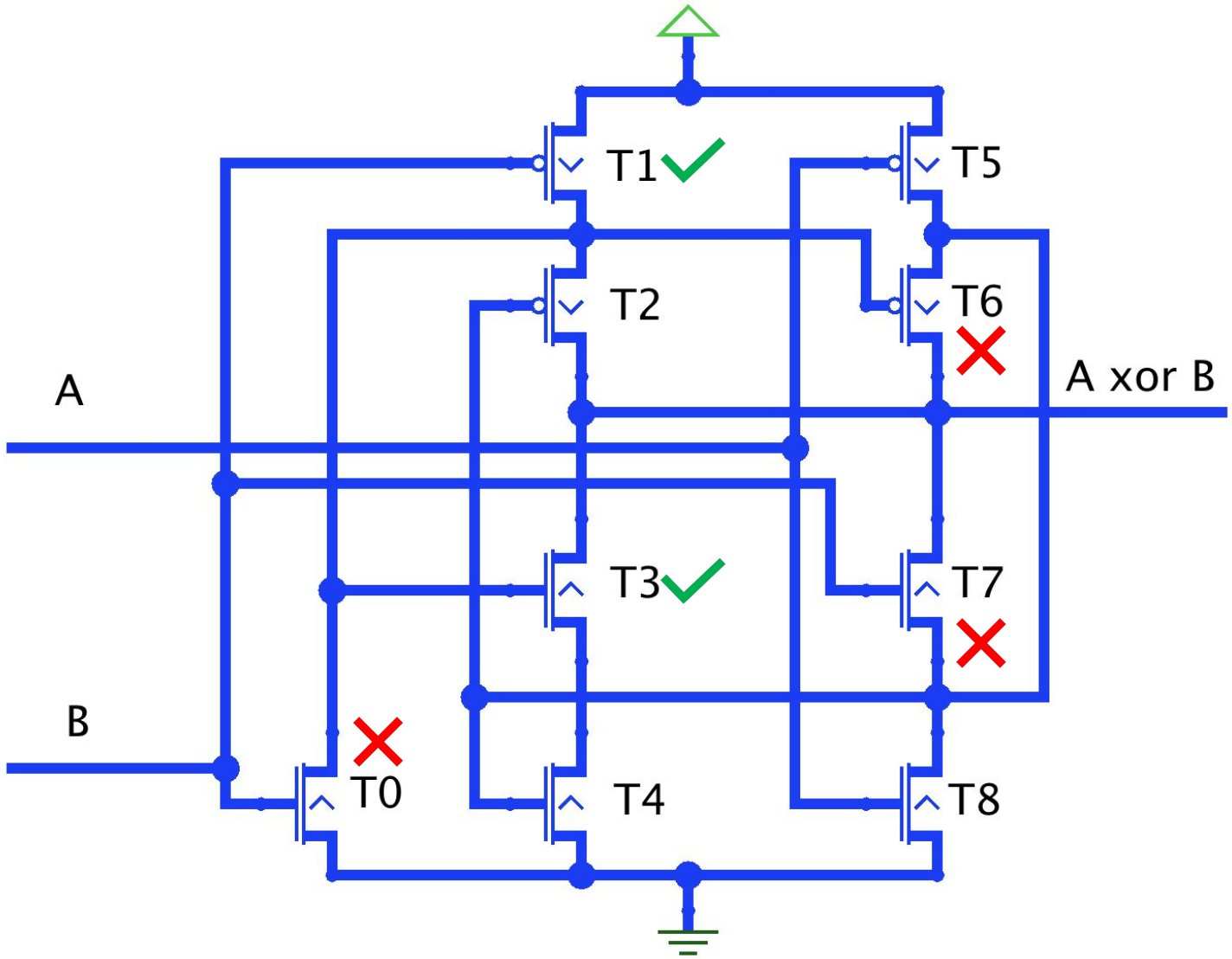
XOR gate optimized: second try

- Much harder to understand

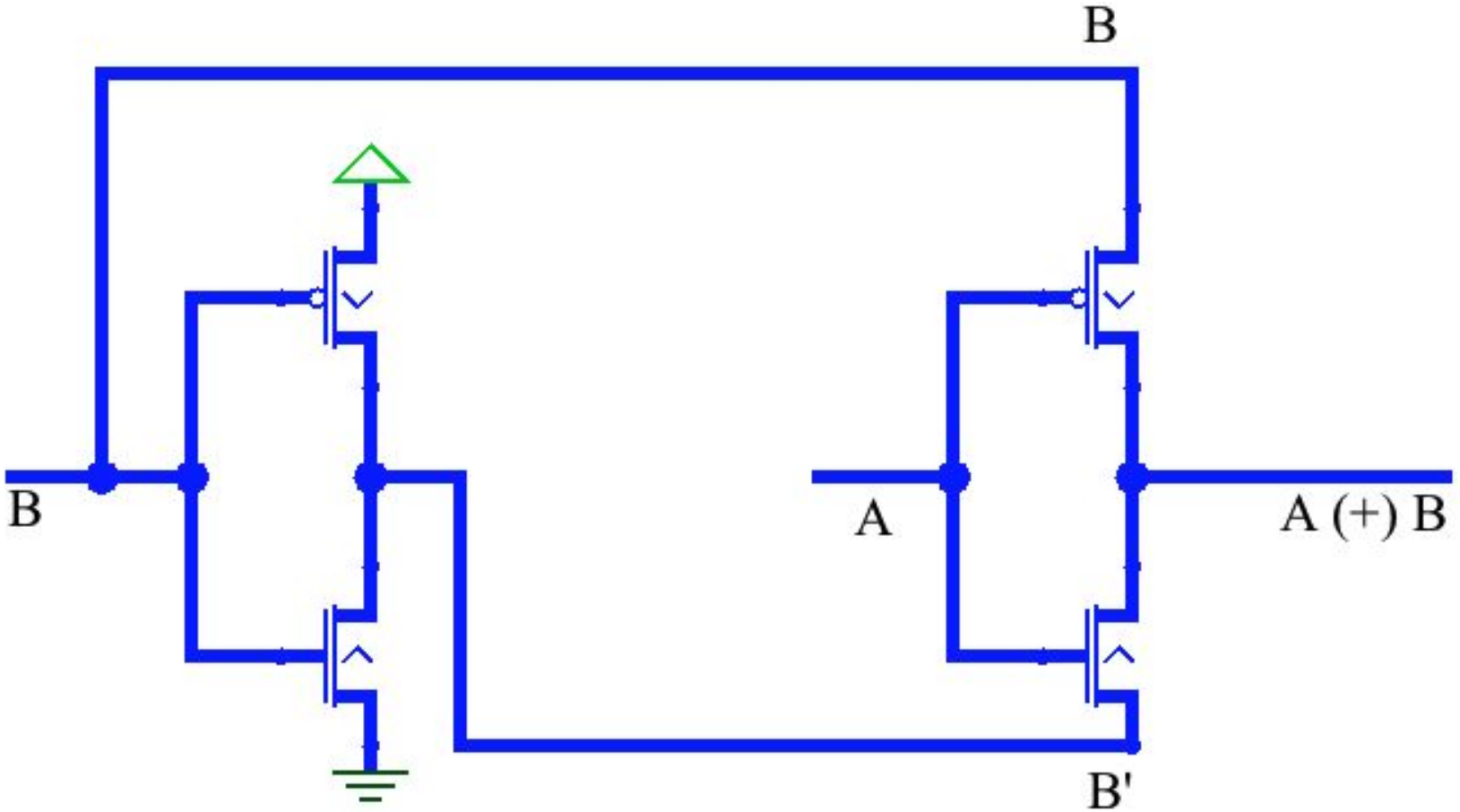


How it works?

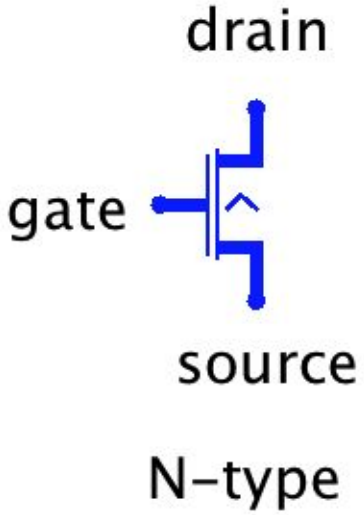
- Consider B=0
- This closes T0 and T7 directly, and opens T1
- Open T1 opens T3 and closes T6
- Transistors T2,4,5,8 form a pair of NOT gates
- Output will be (A⊕0)=A
- Case B=1 is described in tome.pdf

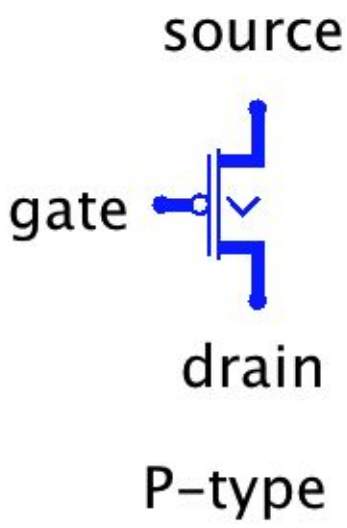


Pass transistor logic (PTL)



Floating signals





N-type truth table

gate	source	drain
0	0	Z
0	1	Z
0	Z	Z
1	0	0
1	1	1
1	Z	Z

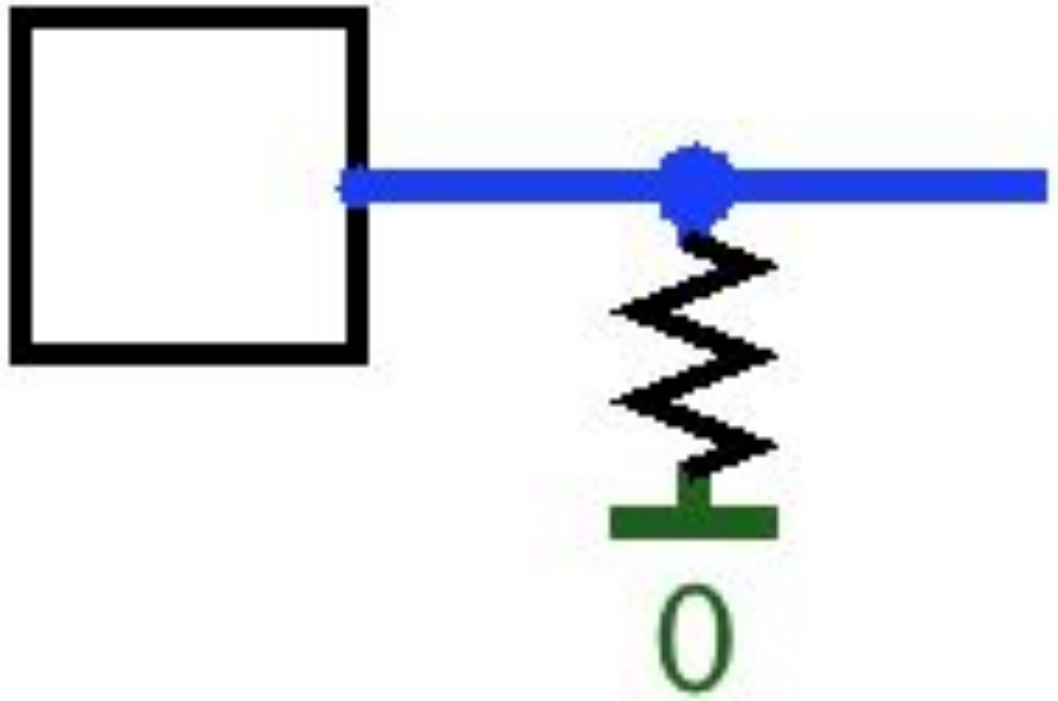
P-type truth table

gate	source	drain
0	0	0
0	1	1
0	Z	Z
1	0	Z
1	1	Z
1	Z	Z

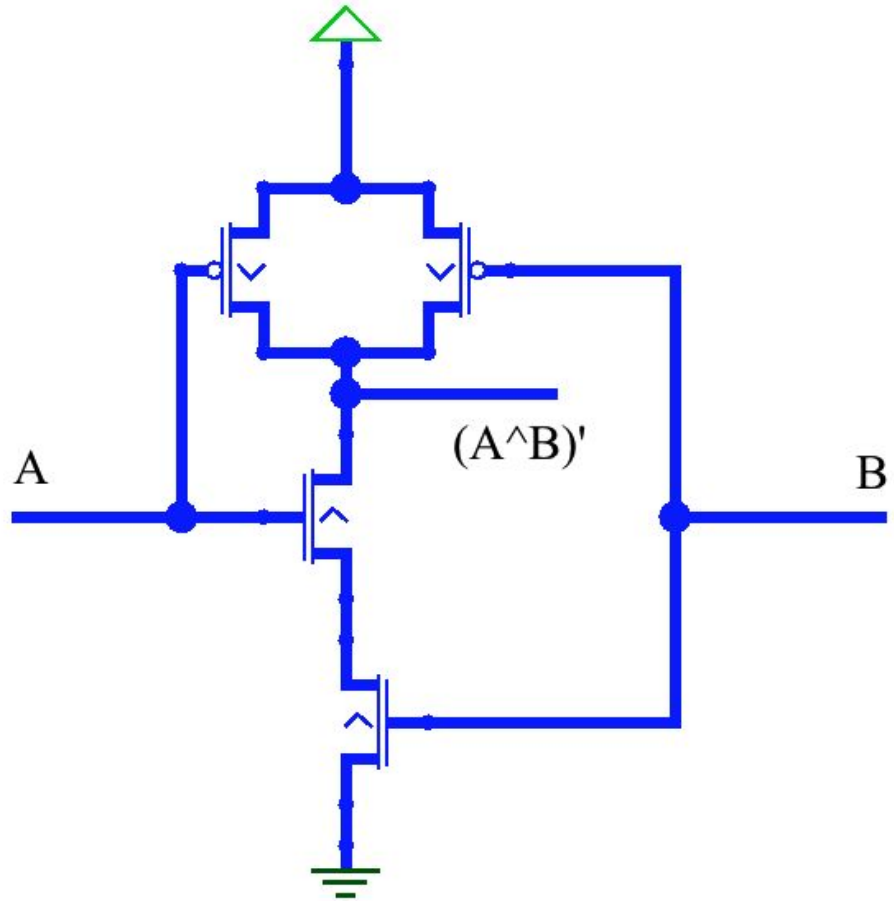
Generally, you should avoid floating input on transistor gates
Also, you should avoid connecting conflicting outputs
But connecting floating output to non-floating one is OK
Actually, NOT gate uses exactly this kind of connection

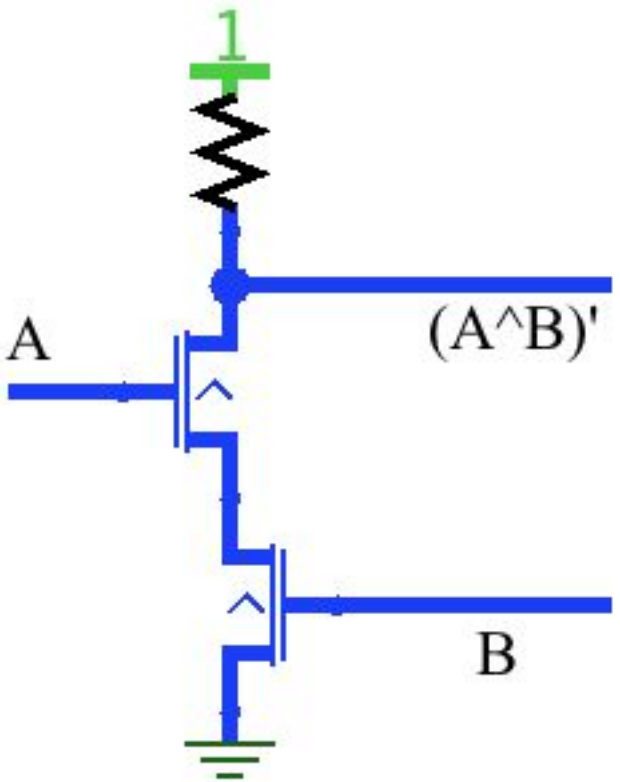
Pull resistor

- Gives sort of default value to circuit output
- I.e. when output floats, pull resistor pulls it to 0
- If we connect it to PWR, it will pull it to 1

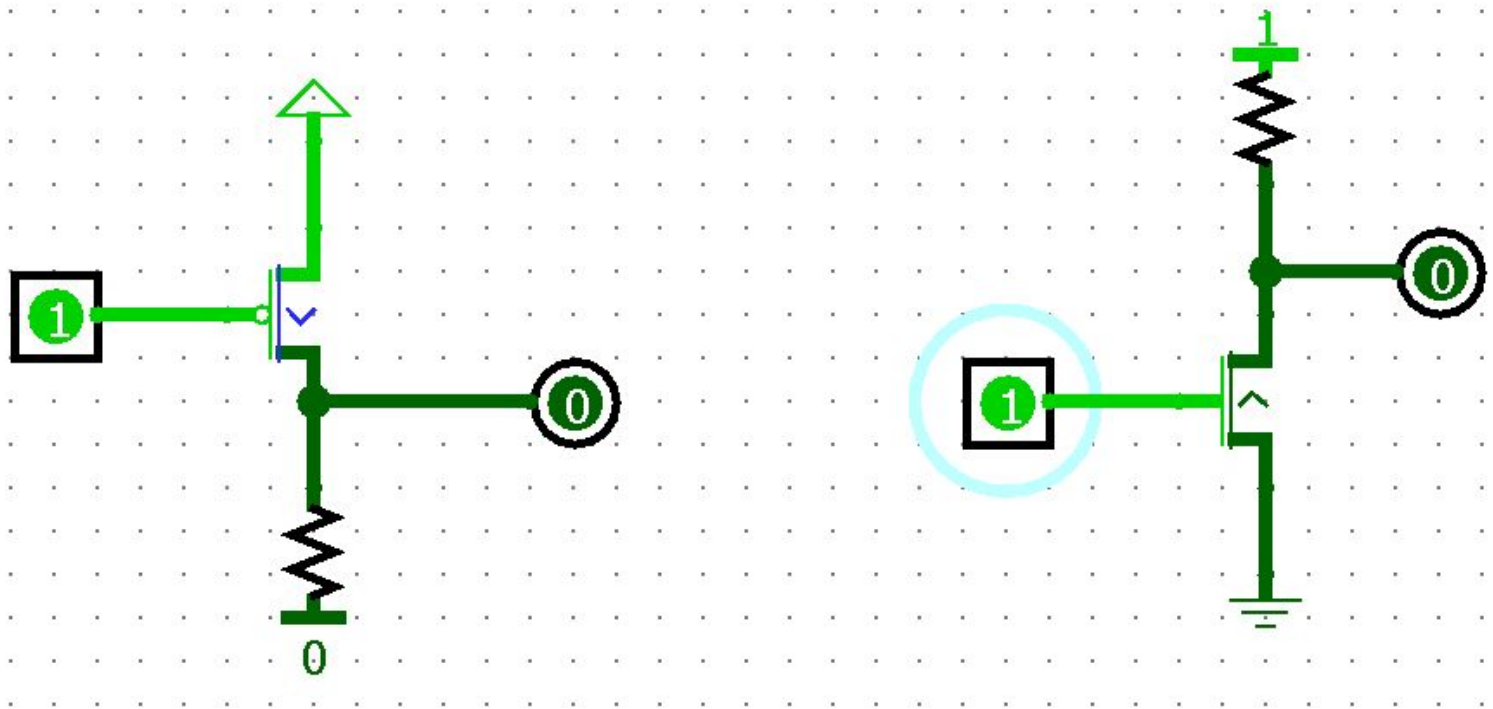


NAND gate using pull resistor





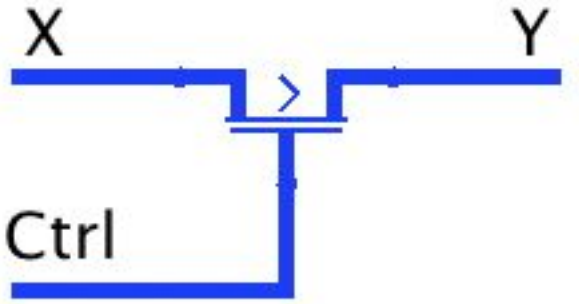
NOT using pull resistor



Why not use pull resistors everywhere?

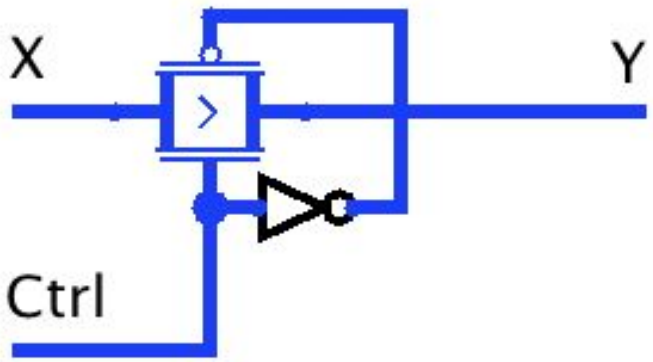
- They are slow
- They consume power

Controlled buffer



This device allows to controllably pass X to Y
Actual buffers are bidirectional (signal and even floating value passes also from Y to X)
But Logisim simulates them as unidirectional

Ctrl	X	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



Smarter implementation known as transmission gate
Less signal degradation