Lecture 4
Sequential units. Registers

Computing platforms, semester 2

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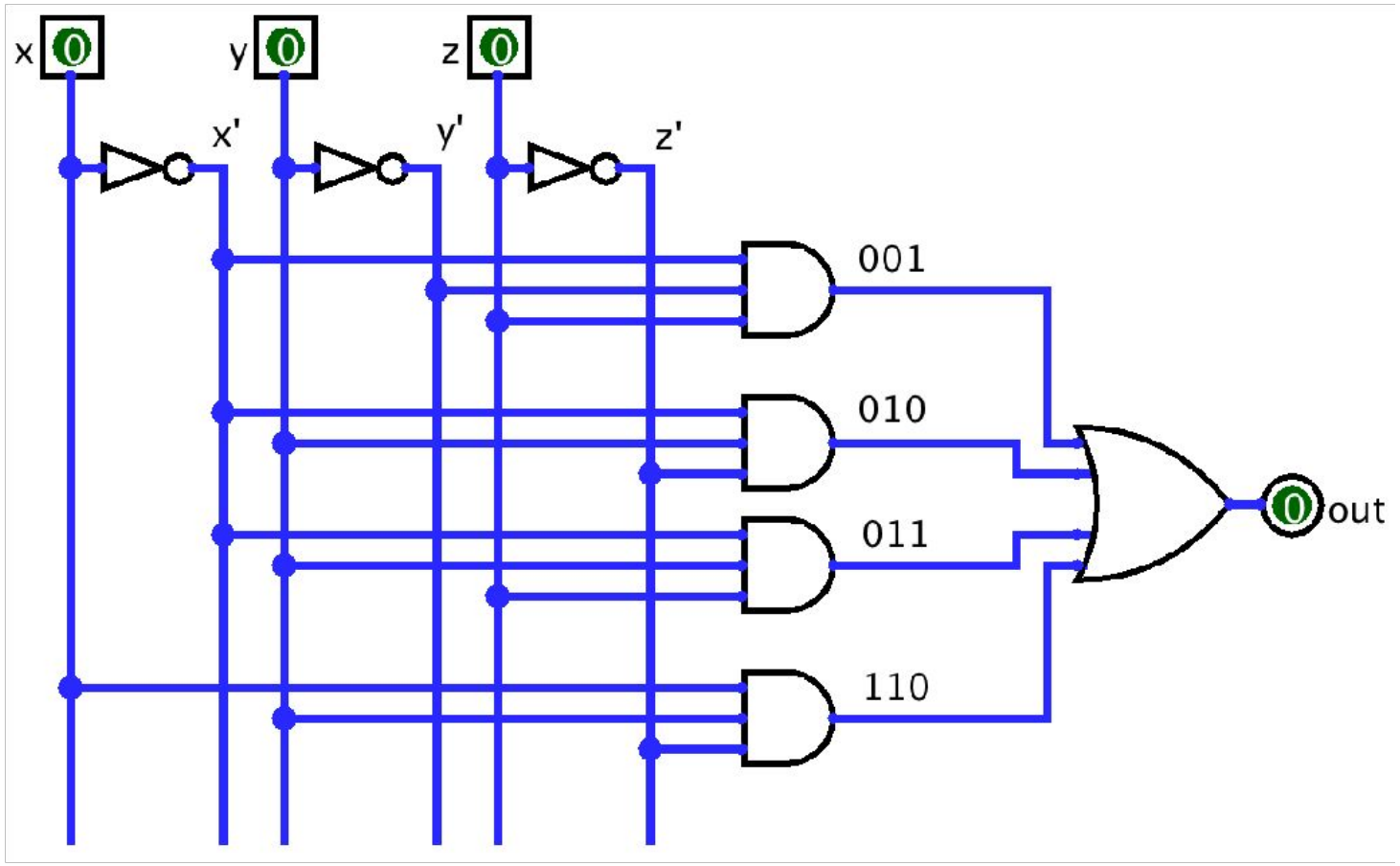
Some terminology

- Combinational units: pure logical functions.
  - Output depends only on input
  - No side effect (except delay)
  - Can be described by single logical expression
- Sequential units: have internal state
  - Output depends not only on the inputs
  - Input can have side-effect (changing internal state)
  - Depend on timing
  - Require triggers, latches and memory

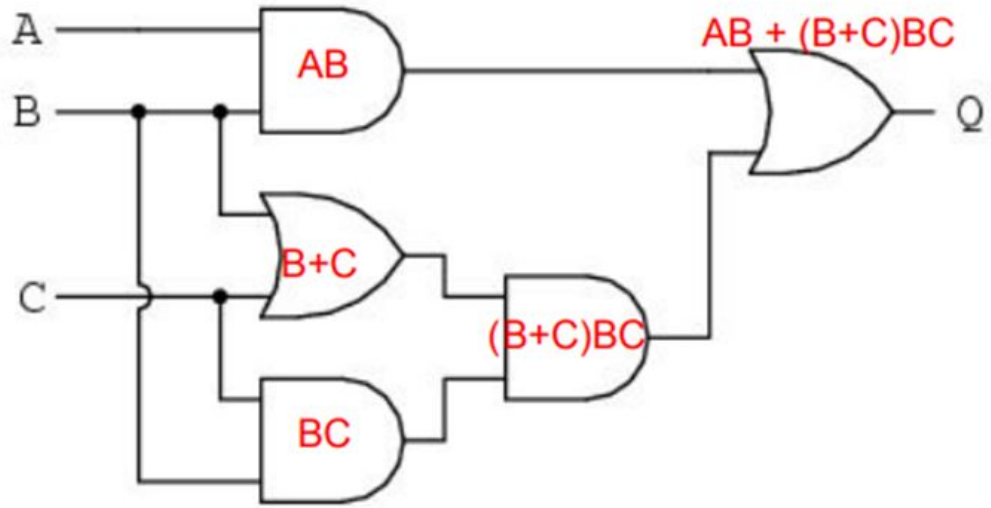
Some final words on combinatory circuits

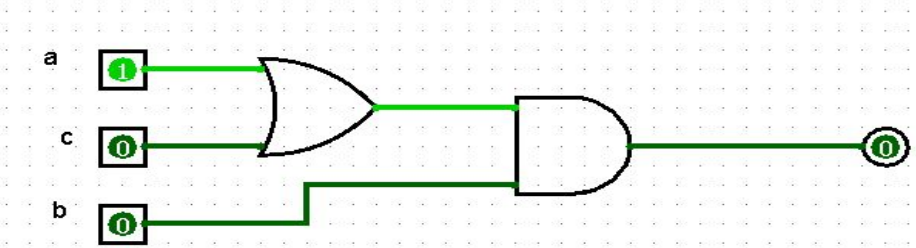
x	y	z	out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



Implementing arbitrary truth table

- Draw input lines. Also add inverted lines
- For every row yielding 1, add AND gate and connect it to corresponding input lines (may be to inverted one)
- Connect outputs of AND gates to OR gate
- This is called minterm approach (normal disjunctive form)
- FPGA design tools do this automatically
- Optimization steps (optional)
  - If table has more rows yielding 1 than 0, build device for inverted table and invert the output
  - Delete unused direct or inverted input lines





Q = AB + (B+C) * BC

By distributing the BC into (B+C) we get:

Q = AB + (BBC + CBC)

Using the multiplicative idempotent law again we know that B*B = B and that C*C=C so we get:

Q = AB + (BC + BC)

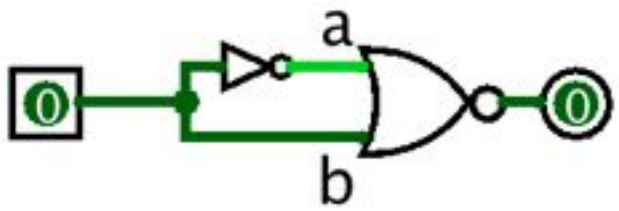
Using the additive idempotent law (B + B = B) we get:

Q = AB + BC

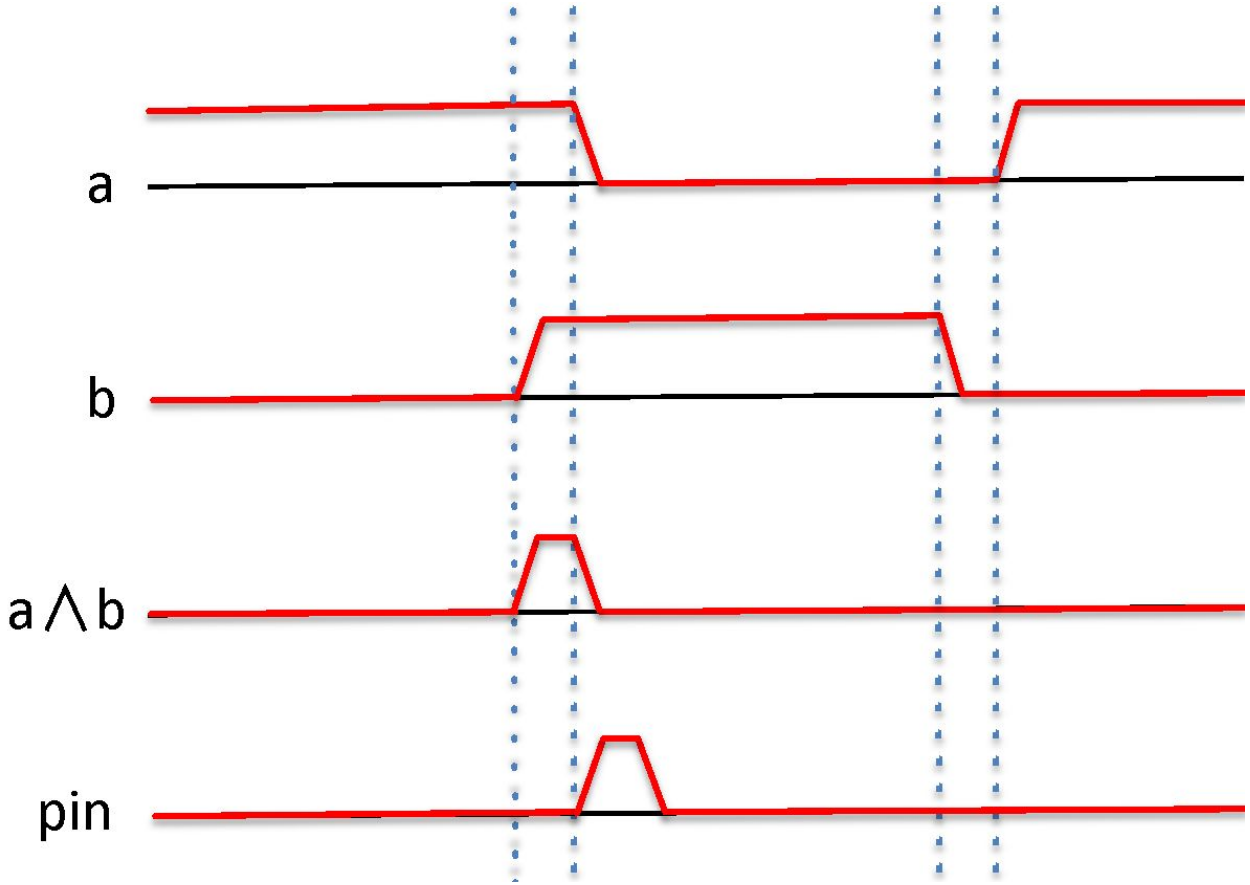
By factoring out the B, we get the final answer of

Q = B(A+C)

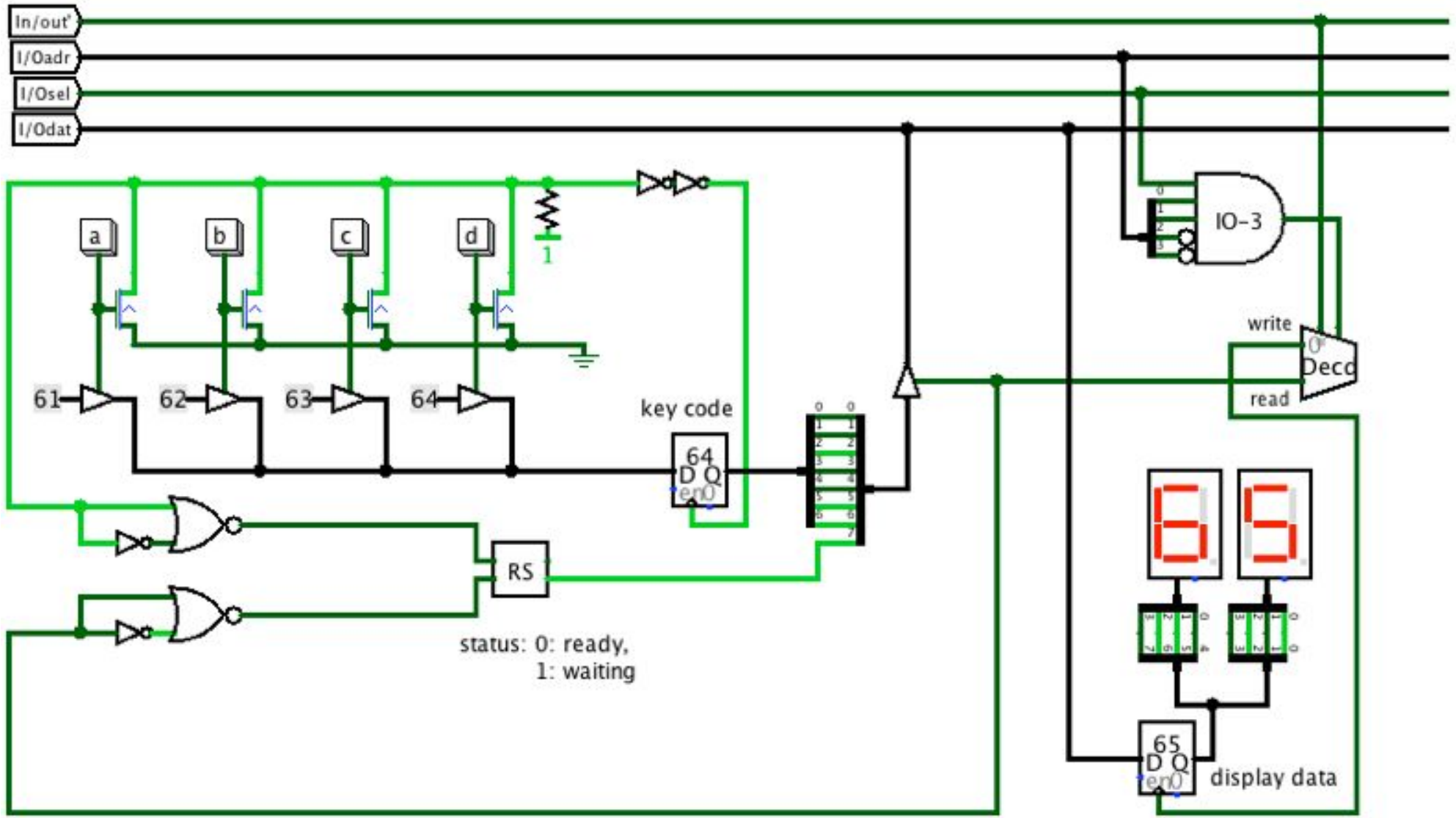
Edge detector



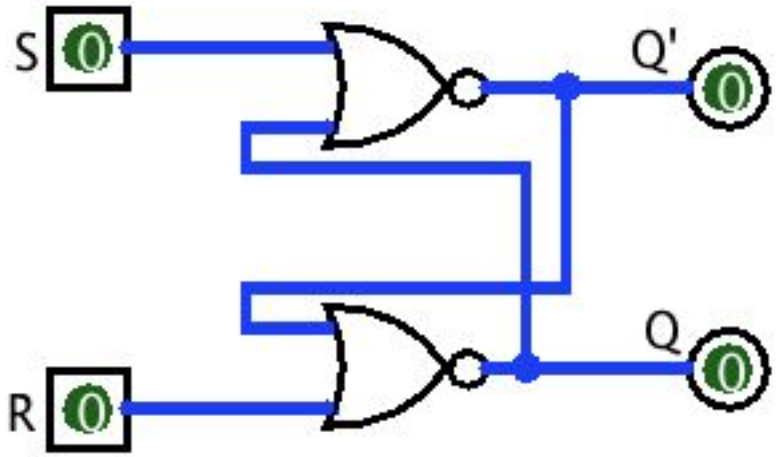
- One of the simplest sequential devices
- Detects input transition from low to high
- Generates pulse when transition occurs



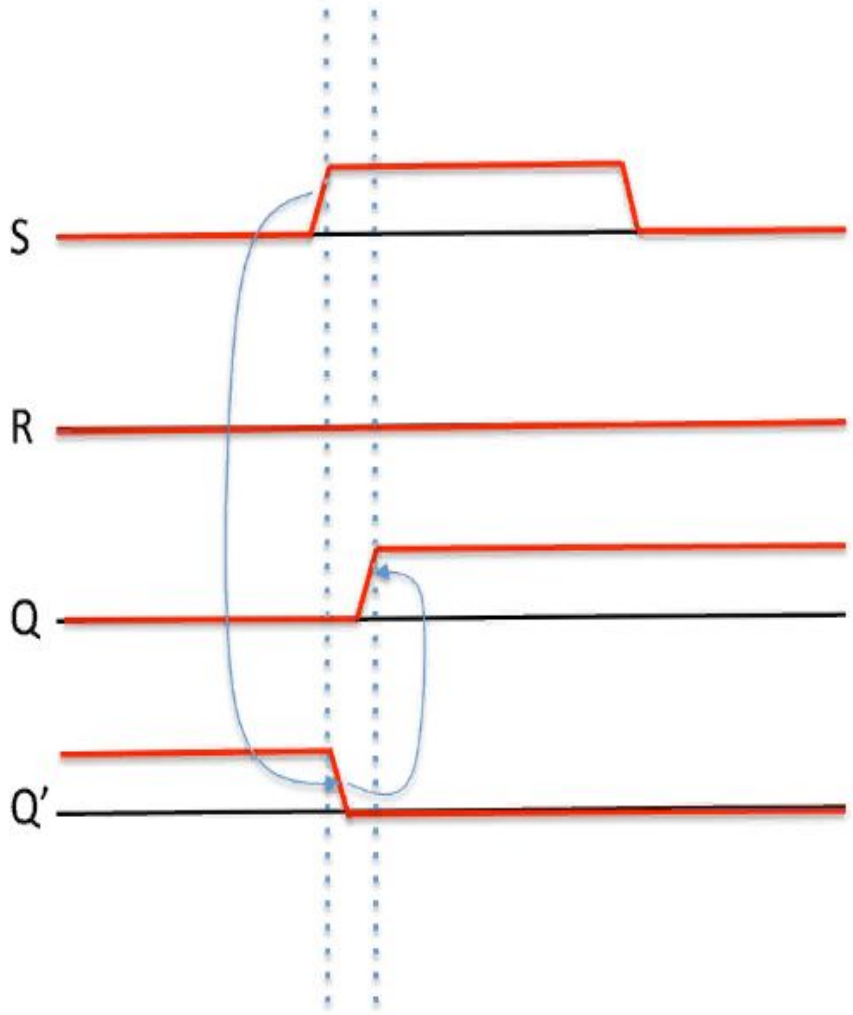
Edge detector



Flip-flop

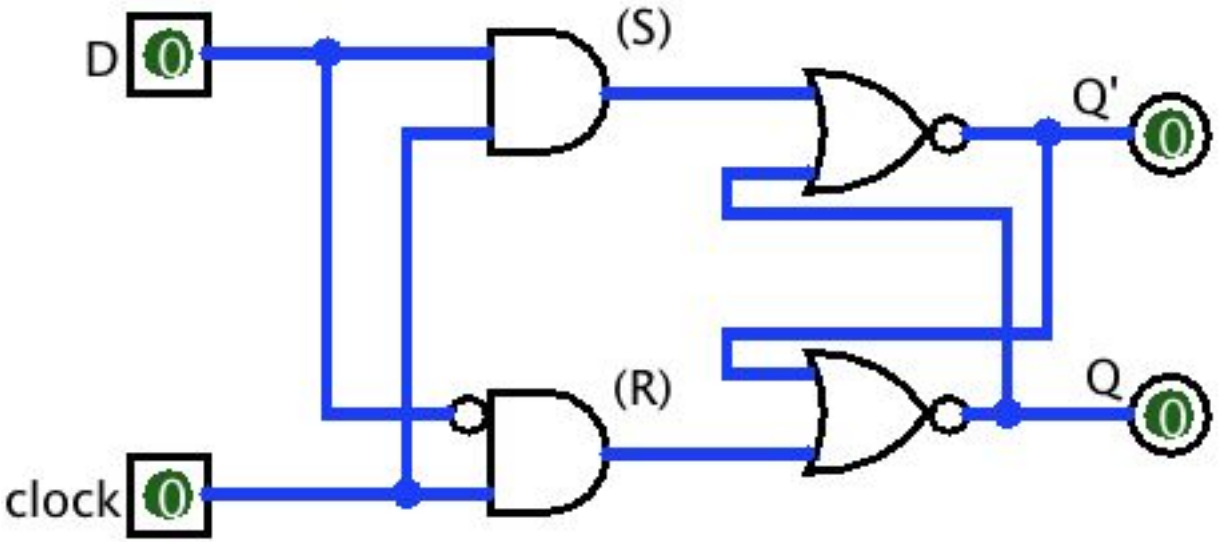


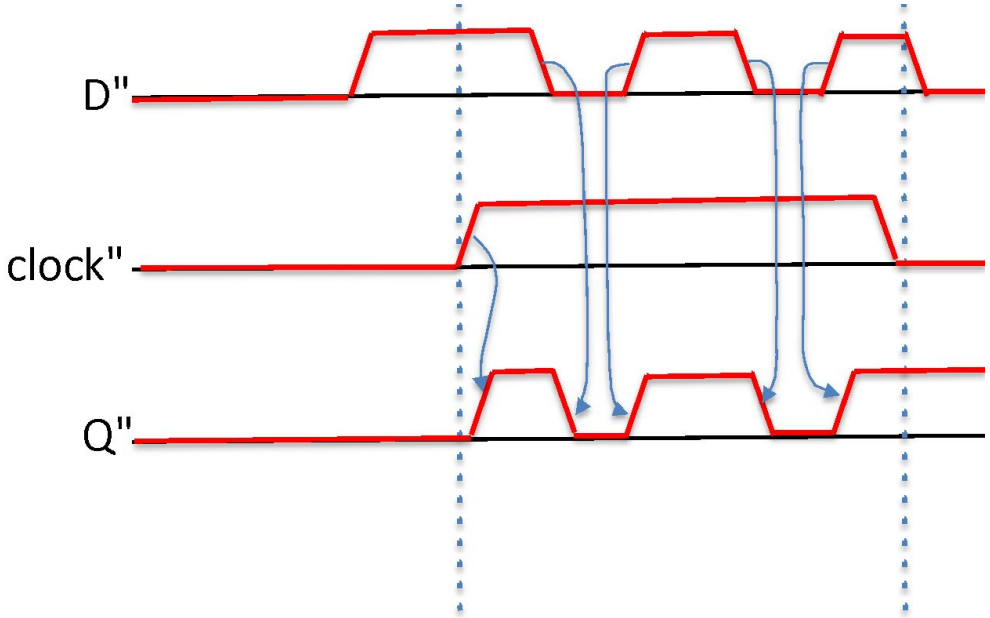
S	R	Q	$\overline{Q}$
0	0	Режим хранения информации	
0	1	0	1
1	0	1	0
1	1	Запрещенное состояние	



- Also known as Set-Reset trigger, RS-trigger, RS-latch, etc
- Detects and remembers change in R and S signals
- Edge-triggered (like edge detector)

D-trigger





- Remembers value of D when clock is high
- When D changes on high clock, we have problem

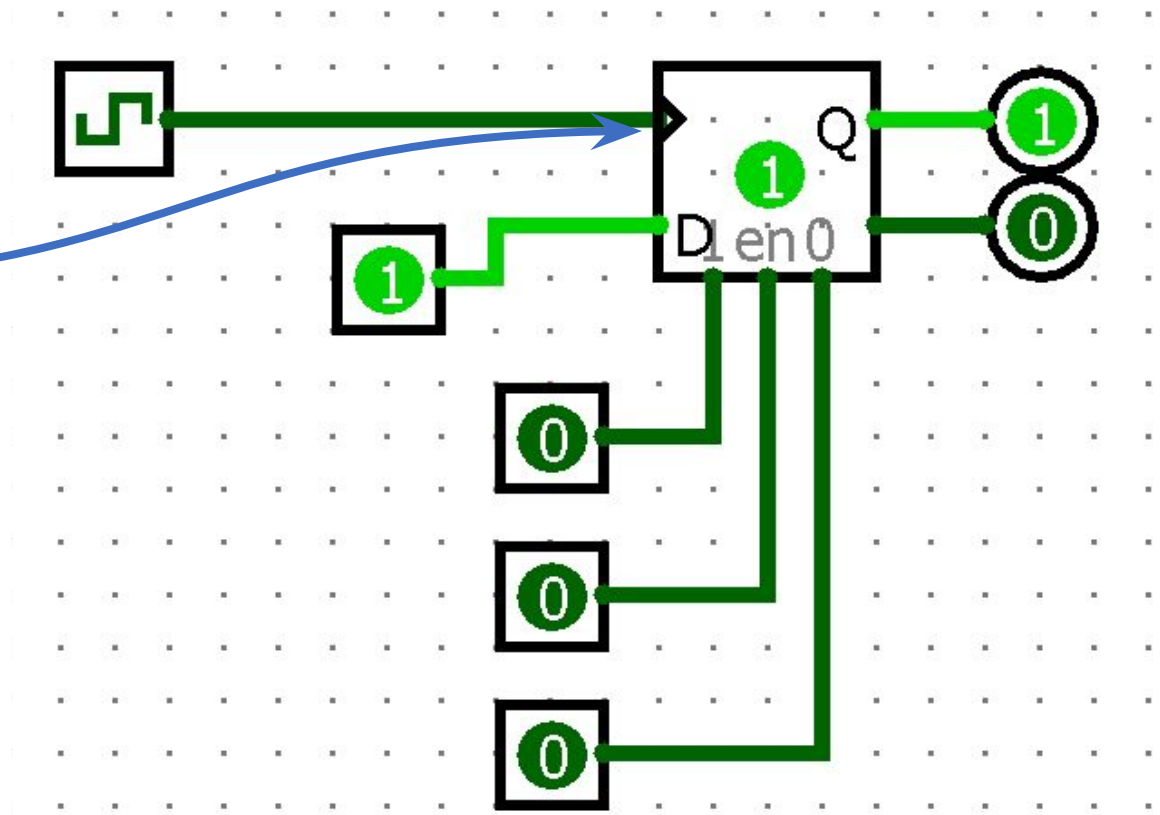
D-trigger in Logisim

Передний фронт;

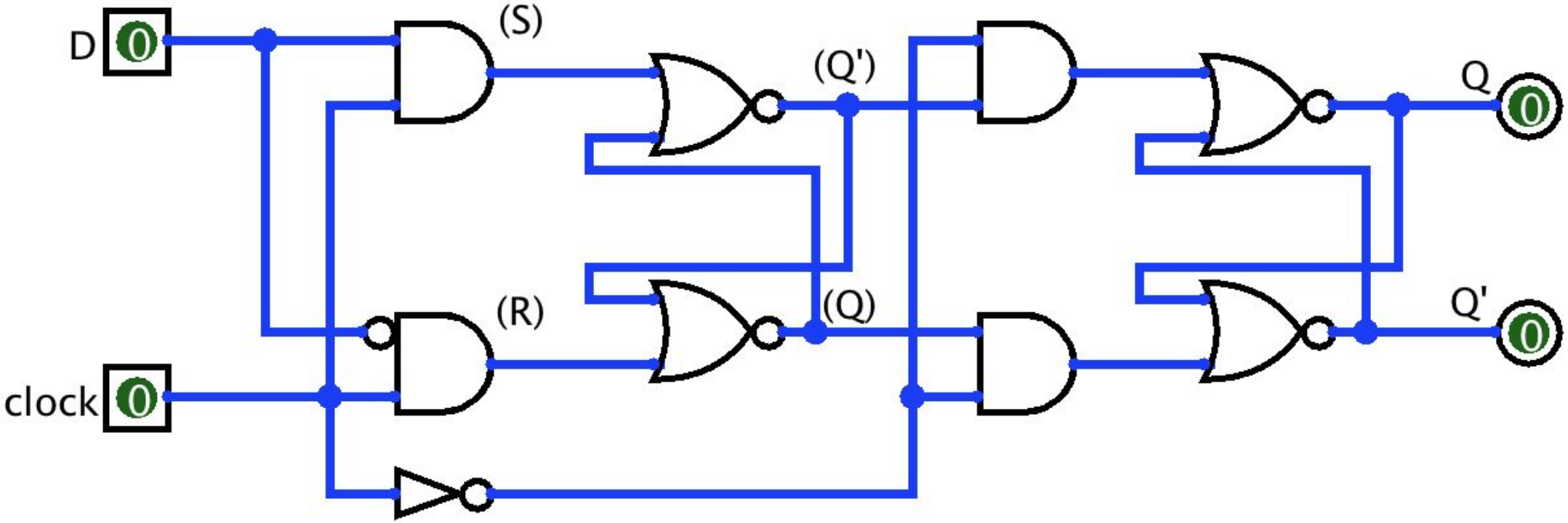
Задний фронт;

Высокий уровень;

Низкий уровень.

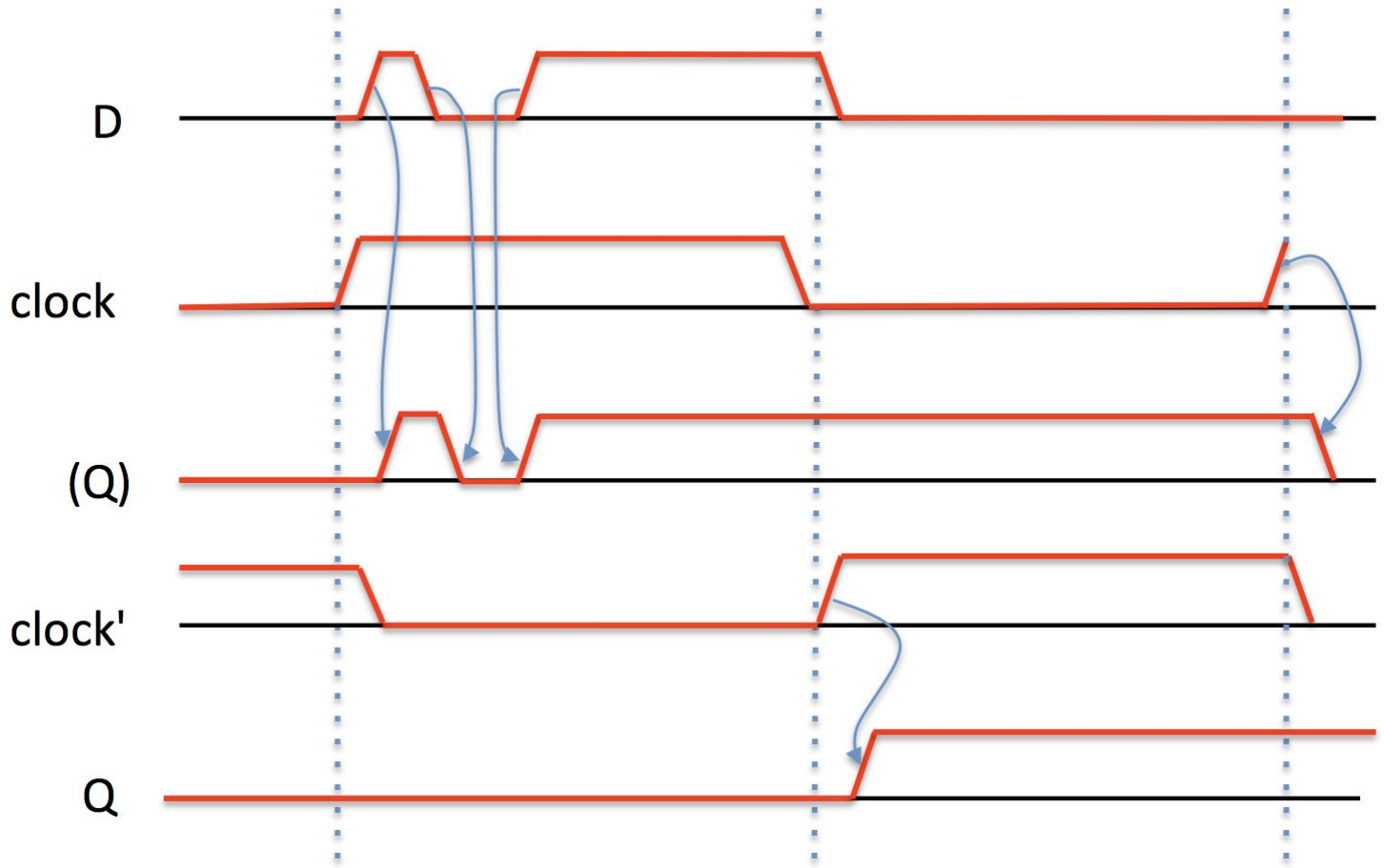


Master-slave latch

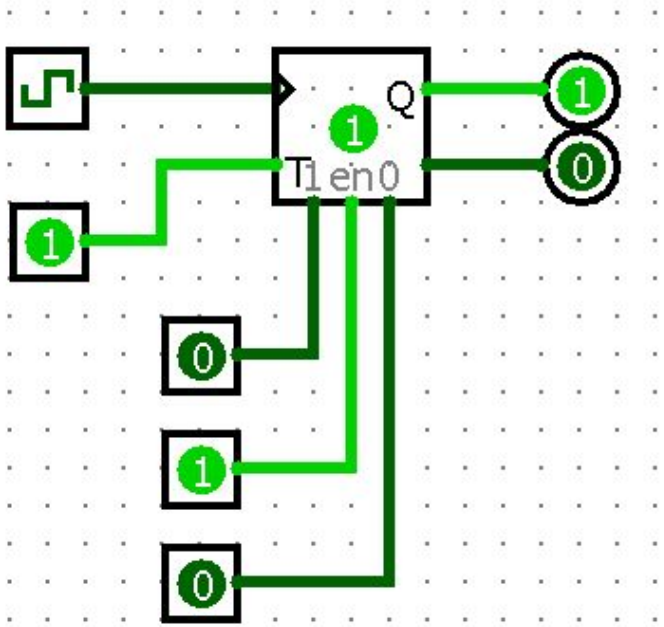


- Two D-triggers connected sequentially, with inverted clock
- First trigger latches D on high clock
- Second trigger latches stable value of (Q) on low clock

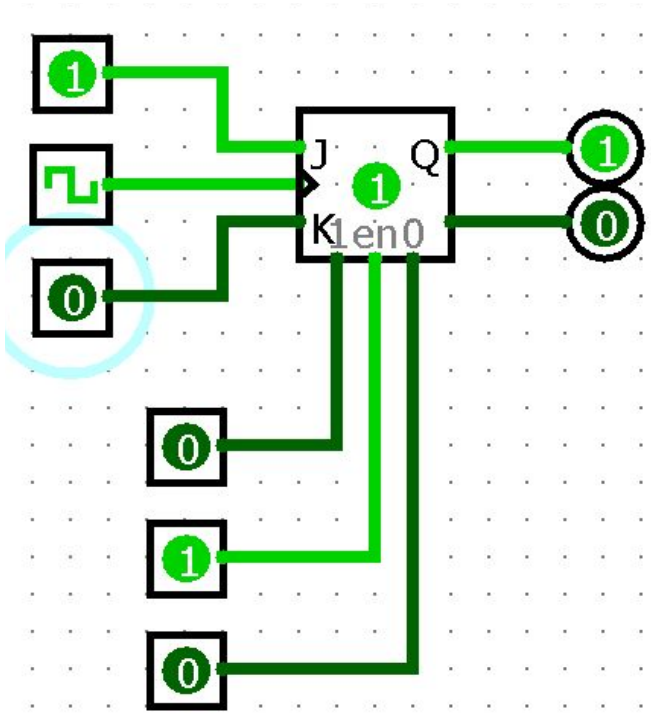
MSL timing diagram



T-trigger



JK-trigger

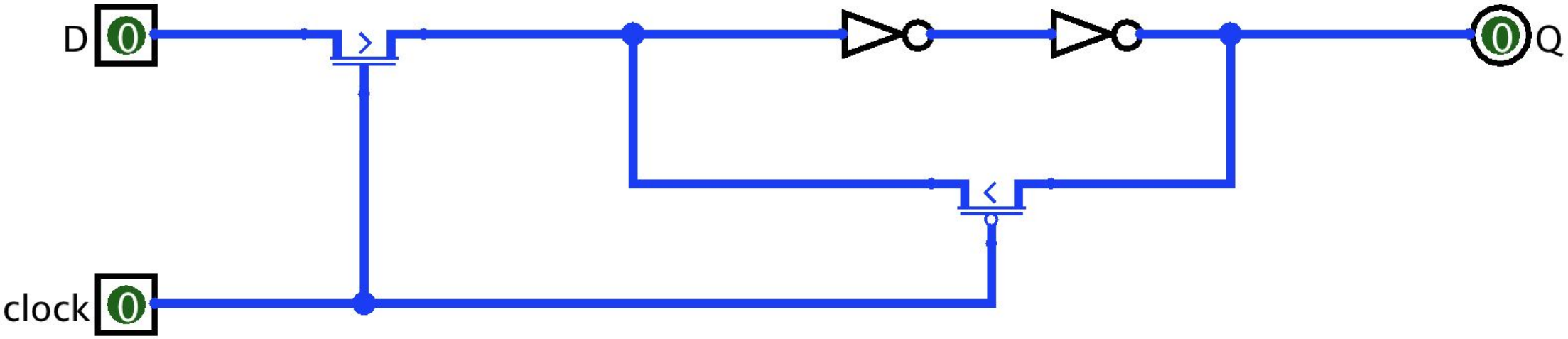


входы			выходы		Режим работы
C	J	K	Q	$\overline{Q}$	
0	x	x	Q	$\overline{Q}$	Хранение
↓	0	0	Q	$\overline{Q}$	
↓	0	1	0	1	Запись 0
↓	1	0	1	0	Запись1
↓	1	1	$\overline{Q}$	Q	Иверсия

Other interesting devices

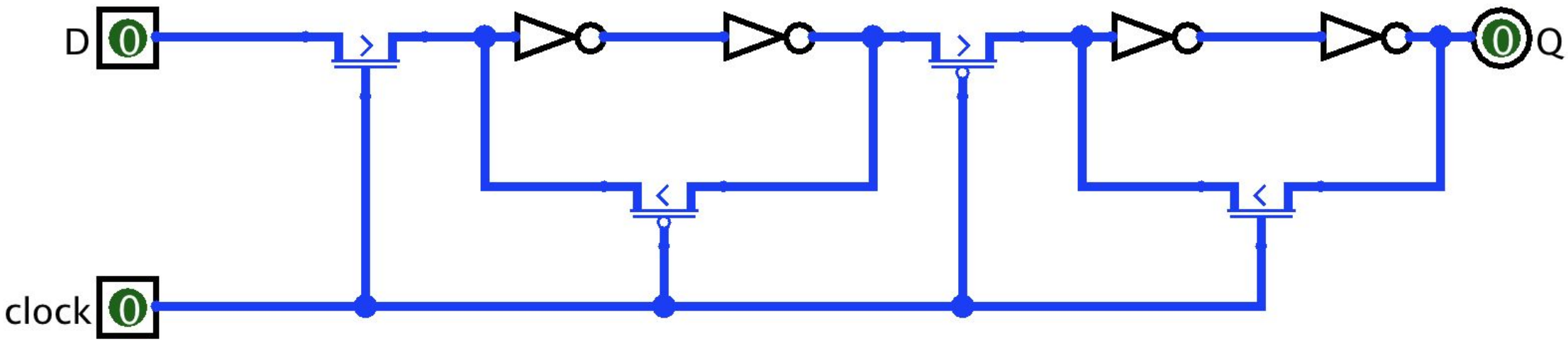
- Edge-triggered D-latch
  http://www.falstad.com/circuit/e-edgedff.html
- JK-trigger http://www.falstad.com/circuit/e-jkff.html
- 4-bit ripple counter built on JK-triggers
  http://www.falstad.com/circuit/e-counter.html
- 4-bit synchronous counter (simplified carry lookahead)
  http://www.falstad.com/circuit/e-synccounter.html
- Decimal (BCD) counter
  http://www.falstad.com/circuit/e-deccounter.html

D-latch using CMOS PTL

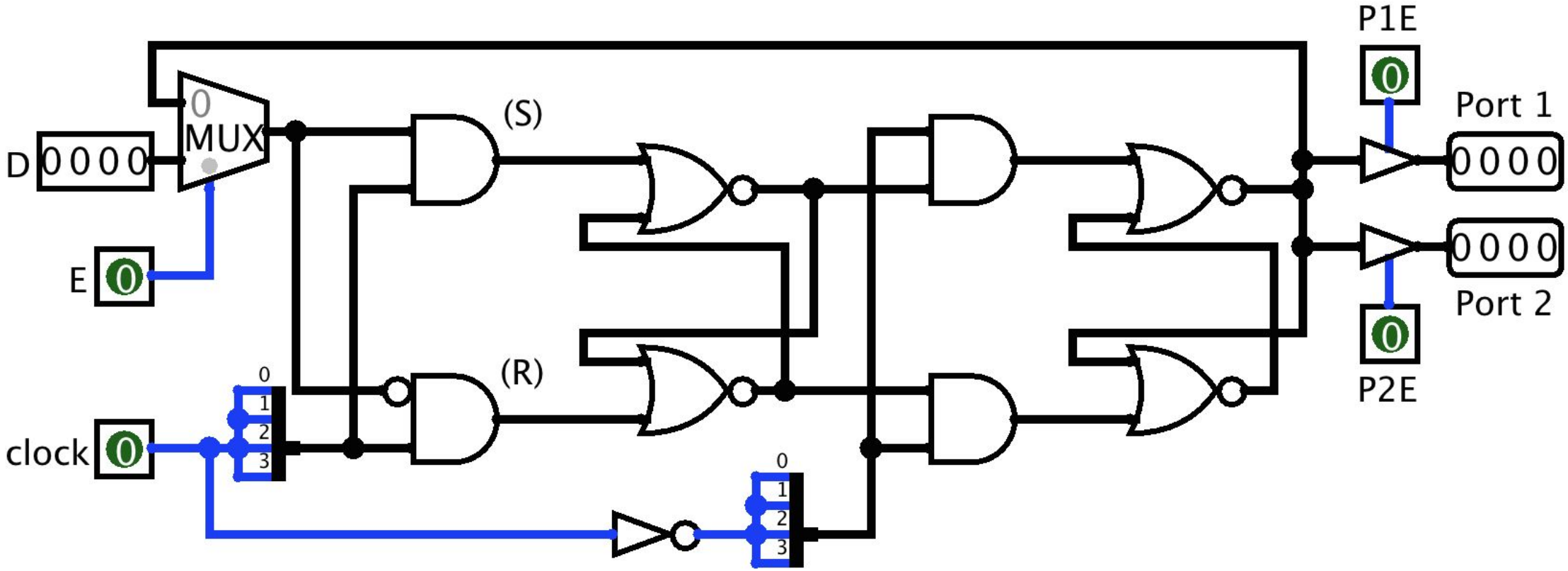


- Six transistors
- The D-latch on logic gates used 22 transistors!

Master-slave latch on PTL



Multiported register

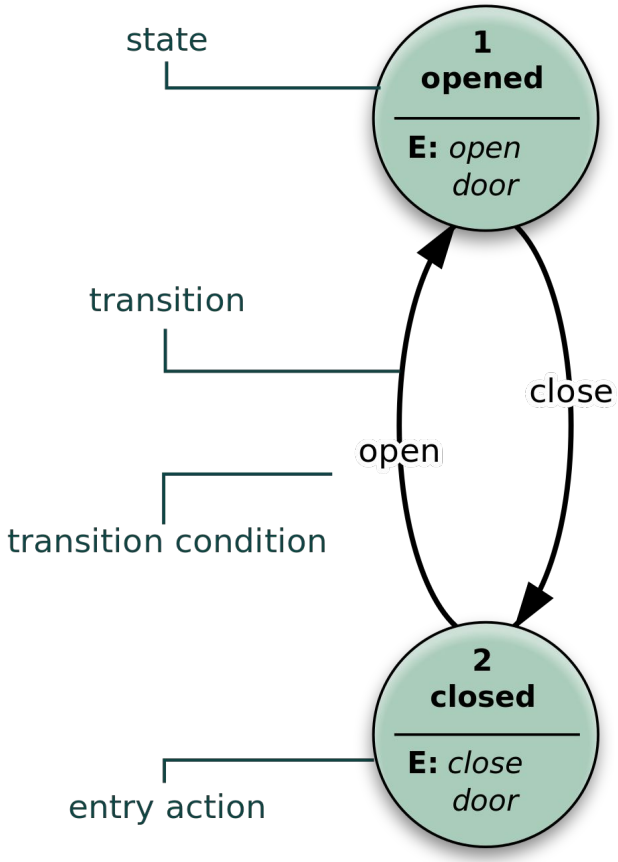


Multiport register features

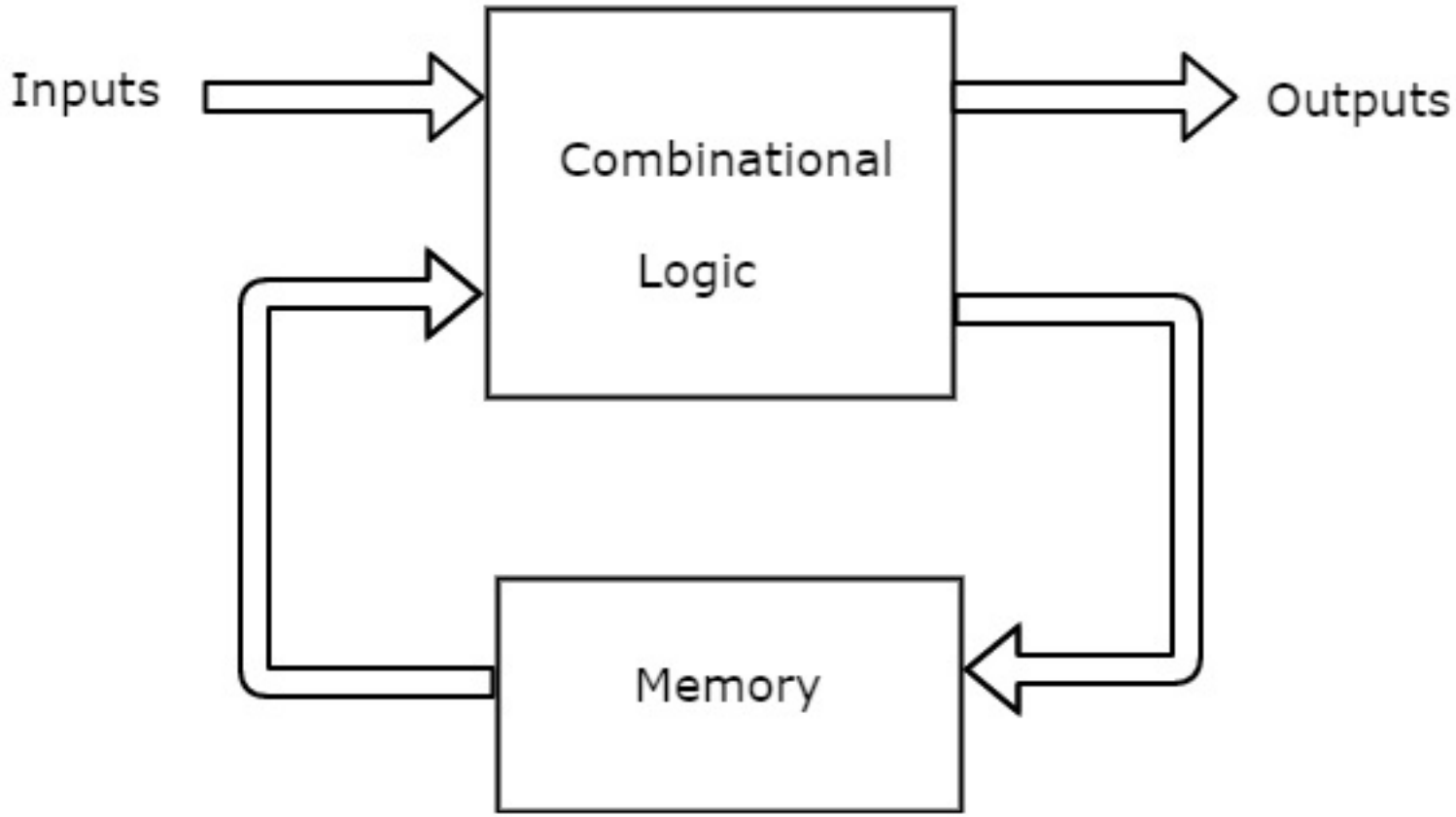
- Multibit storage (4 bit on previous slide)
- Controlled latching. Has clock and Enable signals.
  - In CdM-8, most instructions operate on a single register.
  - Other registers must remain unchanged.
- Multiple three-state outputs
  - In CdM-8, only selected register values are needed on each clock
  - Using three-state outputs, we can attach all registers to a single bus or to several buses

Finite state machine

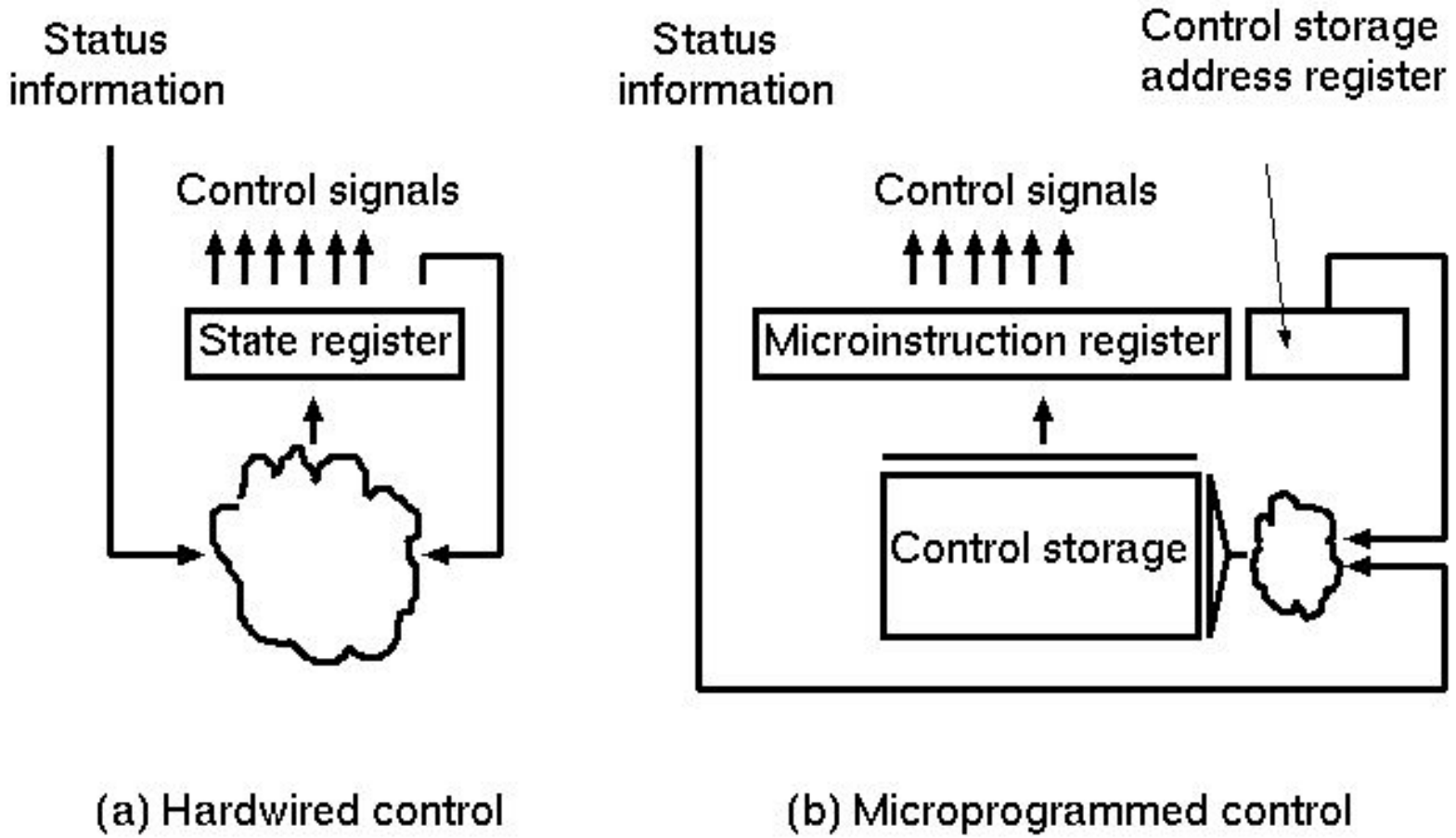
- A formal computation model
- Used in many branches of computing
  - Network protocols
  - Parsers and lexers
  - Event-driven programming
  - Hardware design
  - etc
- Formally, any digital device (including von Neumann computer) is a Finite State Machine
- Can be represented as graph of states and transitions
- Can be directly implemented in hardware



Hardware FSM



One possible next step: microprogramming



(a) Hardwired control

(b) Microprogrammed control

Microprogramming

- Most modern CPU are actually microprogrammed machines
- Many peripherial computer devices (those which do not have it’s own CPU inside) also are implemented as microprogrammed machines or FSM
- But we won’t go into this now