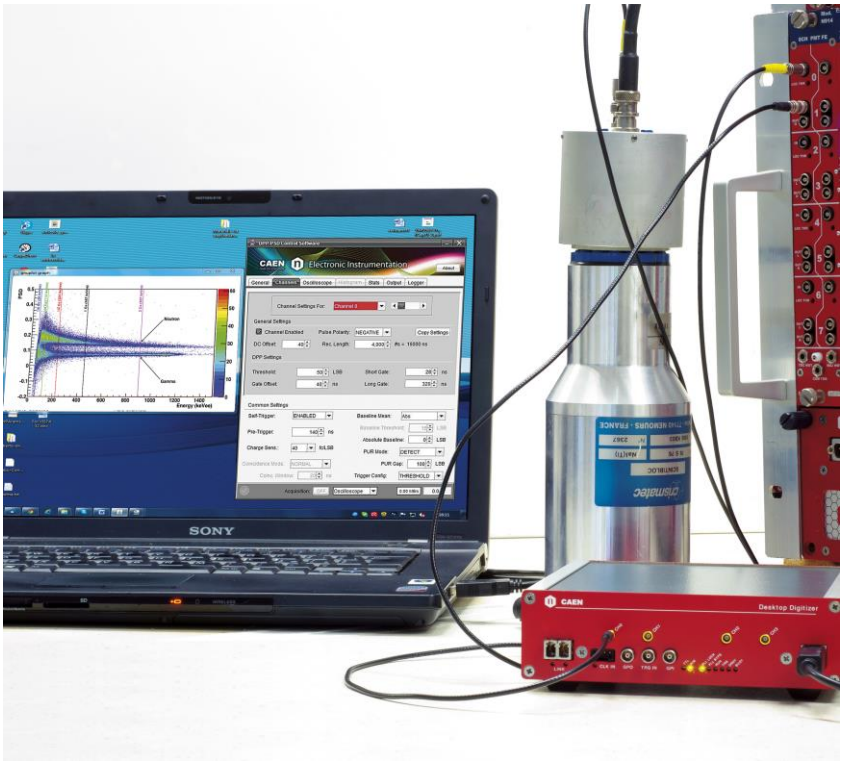
CAEN
Tools for Discovery

Electronic Instrumentation



UM2580

DPSD User Manual

Rev. 3 – 05 June 2013

Purpose of this Manual

This User Manual contains the full description of the Digital Pulse Shape Discrimination for 720 and 751 Digitizer series. The description is compliant with DPP-PSD firmware release **4.1_131.6** for 720 series, DPP-PSD firmware release **4.1_132.6** for 751 series, and DPP-PSD Control Software release **1.2.3**. For future release compatibility check in the firmware and software revision history files.

Change Document Record

Date	Revision	Changes
10 May 2012	00	Initial release
07 June 2012	01	Updated § 6
10 October 2012	02	Document revised to support 751 series
05 June 2013	03	Support to new firmware and software releases. Removed Register Chapter*(*)*.

(*) A new document unifying the registers descriptions of CAEN digitizers is in progress; the user can temporarily refer to the document "DPSD Registers Description" at the DPP-PSD page in the documentation tab .

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
DAQ	Data Acquisition
DPP	Digital Pulse Processing
DPP-CI	DPP for Charge Integration
DPP-PSD	DPP for Pulse Shape Discrimination
DPSD	Digital Pulse Shape Discriminator
MCA	Multi-Channel Analyzer
OS	Operating System
PC	Personal Computer
PMT	Photo Multiplier Tube
QDC	Charge-to-Digital Converter
TDC	Time-to-Digital Converter
USB	Universal Serial Bus

Reference Documents

[RD1] WP2081 - Digital Pulse Processing in Nuclear Physics

[RD2] AN2506 - Digital Gamma Neutron discrimination with Liquid Scintillators

[RD3] GD2827 - How to make coincidences with CAEN digitizers **COMING SOON**

[RD4] UM1935 - CAENDigitizer User & Reference Manual

[RD5] GD2783 – First Installation Guide to Desktop Digitizers & MCA

[RD6] GD2512 - CAENUpgrader QuickStart Guide

[RD7] AN2086 - Synchronization of a multi-board acquisition system with CAEN digitizers

[RD8] UM2784 – CAENDigitizer LabView User & Reference Manual

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1 Introduction

CAEN S.p.A offers a wide range of digitizers to meet different needs of sampling frequency, resolution, form factor, etc. Besides the use of the digitizers as a waveform recorder (oscilloscope mode), the user can upload special versions of the FPGA firmware for the **Digital Pulse Processing** (DPP) algorithms. A digitizer running in DPP mode becomes a multipurpose instrument which replaces most of the traditional modules such as MCAs, QDCs, TDCs, Discriminators, etc. (for more details refer to the DPP overview **[RD1]**). In particular CAEN provides two algorithms for the charge integration of the digitized input pulses at the firmware level:

- the **Digital Pulse Processing** for **Charge Integration** firmware (DPP-CI), single gate compatible to the 720 series digitizers (featuring both the EP1C4 and the EP1C20 Altera FPGA models).
- the **Digital Pulse Processing** for **Pulse Shape Discrimination** firmware (DPP-PSD), dual gate, running only on the 720 series digitizers (12 bit, 250MS/s) with the EP1C20 FPGA, and on the 751 series digitizers (10 bit, 1 GS/s; DES mode not supported). The DPP-PSD firmware allows for charge integration in two different gate widths to discriminate short and long components of the input signal. **Fig. 1.1** shows a typical example of signals from neutrons and gamma, where we can see a difference in the waveform. See **[RD2]** for an example of DPP-PSD application in gamma-neutron discrimination in liquid scintillators**.**

This manual describes in details the DPP-PSD algorithm, suitable for those models summarized in **Tab. 1.1**.

Note: The description of the DPSD system of this Manual is compliant with DPP-PSD firmware release **4.1_131.6** for 720 series, DPP-PSD firmware release **4.1_132.6** for 751 series, and DPP-PSD Control Software release **1.2.3**. For future release compatibility check in the firmware and software revision history files.

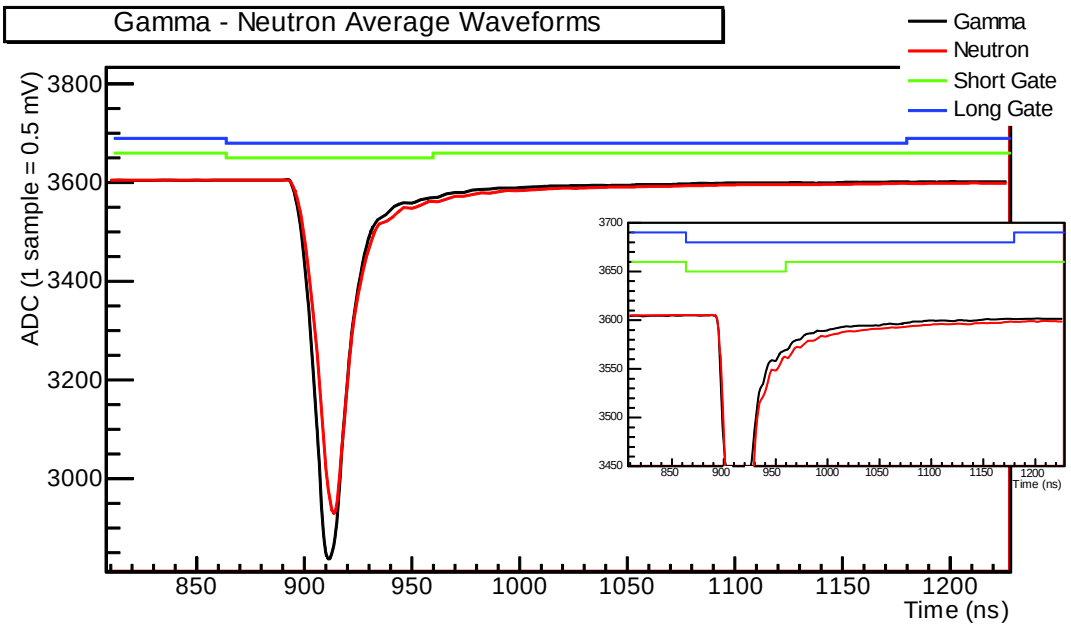


Fig. 1.1: Plot of typical Gamma-Neutron waveforms

Desktop Digitizers(*)	Description	Product Code
DT5720B	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	WDT5720BXAAA
DT5720C	2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	WDT5720CXAAA
DT5720D	4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	WDT5720DXAAA
DT5720E	2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	WDT5720EXAAA
DT5751	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE	WDT5751XAAAA
NIM Digitizers(*)	**Description**	**Product Code**
N6720B	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	WN6720BXAAAA
N6720C	2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	WN6720CXAAAA
N6720D	4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	WN6720DXAAAA
N6720E	2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	WN6720EXAAAA
N6751	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE	WN6751XAAAAA
N6751C	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8 MS/ch, EP3C16, SE	WN6751CXAAAA
VME Digitizers(*)	**Description**	**Product Code**
V1720E	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	WV1720EXAAAA
V1720F	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, DIFF	WV1720FXAAAA
V1720G	8 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	WV1720GXAAAA
V1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE	WV1751XAAAAA
V1751B	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, DIFF	WV1751BXAAAA
V1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8MS/ch, EP3C16, SE	WV1751CXAAAA
VX1720E	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	WVX1720EXAAA
VX1720F	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, DIFF	WVX1720FXAAA
VX1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE	WVX1751XAAAA
VX1751B	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, DIFF	WVX1751BXAAA
VX1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8MS/ch, EP3C16, SE	WVX1751CXAAA
DPP Firmware(*)	**Description**	**Product Code**
DPP-PSD	Digital Pulse Processing for Pulse Shape Discrimination (x720)	WFWDPPNGAA20
DPP-PSD	Digital Pulse Processing for Pulse Shape Discrimination (x751)	WFWDPPNGAA51

Tab. 1.1: Supported CAEN digitizers for DPP-PSD firmware.

(*) For accessories and customizations related to digitizers and for multiple DPP-PSD license packs, refer to the board User Manual or have a look at the board page on CAEN web site: www.caen.it

The Digitizer is a dead-timeless acquisition system, meaning that the analog input signal is continuously converted into a stream of digital samples and on-line processed by the Channel FPGA (AMC). The AMC purpose is to perform the on-line Digital Pulse Processing to implement a Pulse Shape Discrimination MCA (DPP-PSD). A simplified block diagram of the module is shown in **Fig. 1.2**.

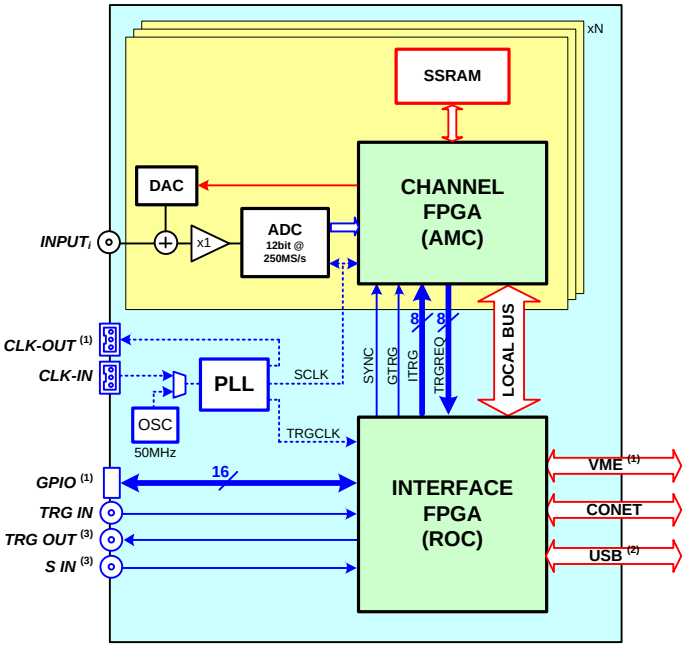


Fig. 1.2: Simplified block diagram of the Digitizer

The **DPP-PSD Firmware** transforms the waveform Digitizer into a spectroscopy acquisition system providing on-line energy (dual gate integrated charge), timing information, and *PSD* (charge of fast and slow components), as well as portions of the waveform for debugging, monitoring and further off-line pulse shape analysis.

The DPSD system also includes the **DPP-PSD Control Software** which allows to set the parameters for the acquisition, to configure the hardware, and to perform the data readout. It allows also to collect the histograms, and to plot and to save the list, the histogram, and the waveforms. Drivers, libraries and demo source codes are also available for those who need either to modify the program for their specific needs or to integrate it into their DAQ programs.

It is also possible to operate with multi-board systems: the front panel clock, the trigger and the general purpose LVDS I/Os connectors (VME only) make easy to synchronize several boards and to run them simultaneously; the advanced trigger logic and the event time stamp allow to implement the coincidences and anti-coincidences between detectors.

The following list summarizes what the user can do with the DPSD:

- calculate the baseline and subtract it from the input signal;
- detect input pulses and generate a local trigger on them;
- calculate the time of arrival of the trigger,
- set two integration gates of different width and position;
- integrate the charges (Q_{short} and Q_{long}) inside those gate windows;
- build the event through a configurable combination of Trigger Time Stamp, Q_{short}, Q_{long}, baseline and raw waveforms (i.e. series of ADC samples belonging to a programmable size acquisition window);
- set PSD threshold (751 series only, under development for 720 series. Not yet managed by the DPP-PSD Control Software GUI);
- detect pile-up conditions (not yet managed by the DPP-PSD Control Software GUI);
- implement coincidences between channels within the same board (**[RD3]**) as well as among channels of different boards through the LVDS I/O connectors and external modules;
- save events (list) into a memory buffer and manage the readout through the Optical Link, USB or VME;
- plot the signal waveforms (oscilloscope mode) and allows to make online adjustments of the acquisition parameters;
- plot 1-D histogram of Q_{long} and time difference of time stamps, as well 2-D scatter plot of the *PSD* parameter (see the definition in the **Principle of Operation** section) vs Q_{long};
- generate output files (for histograms or waveforms) in different formats suitable for other spectroscopy analysis software tools.

2 Principle of Operation

The figure below shows the functional block diagram of the DPP-PSD firmware:

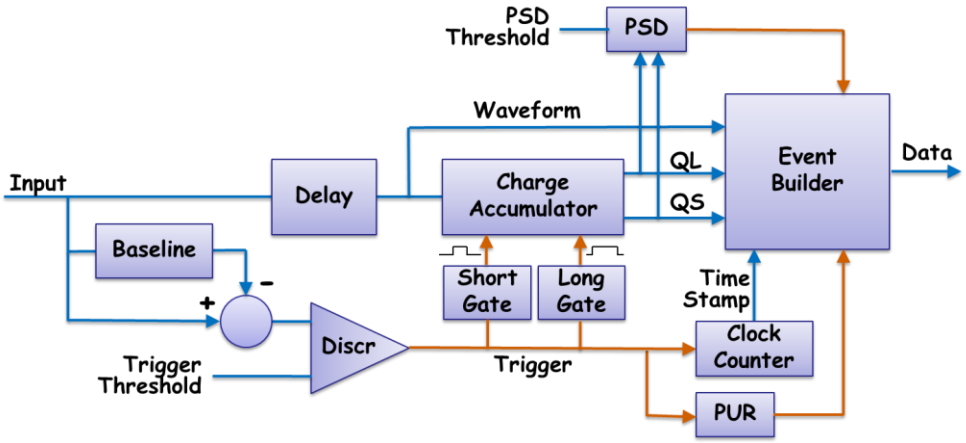


Fig. 2.1: Functional Block Diagram of the DPP-PSD

The aim of the DPP-PSD firmware is to calculate the two charges Q_{short} and Q_{long}, performing a double gate integration of the input pulse. The ratio between the charge of the tail (slow component) and the total charge gives the *PSD* parameter used for the gamma-neutron discrimination:

$$PSD = \frac{Q_{LONG} - Q_{SHORT}}{Q_{LONG}}$$

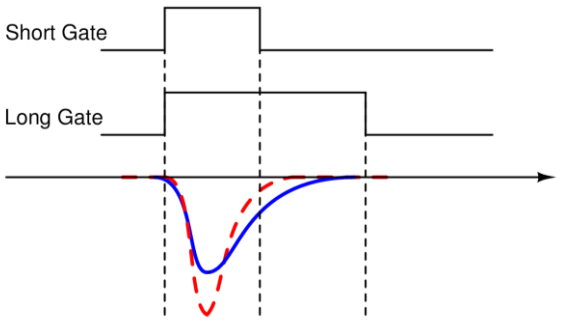


Fig. 2.2: Long and short gate graphic position with respect to a couple of input pulses. The blue pulse has a longer tail than the red one.

The main operations of the DPP-PSD firmware can be summarized as follows:

- the algorithm continuously calculates the *baseline* of the input signal by averaging the samples belonging to a moving window of programmable size (see Sect. **Baseline**). The baseline is subtracted from the input signal, giving *input_sub= input – baseline;*
- the *input_sub* value is compared with the value of the trigger threshold and the trigger fires as soon as the *input_sub* signal crosses the threshold (see **Fig. 2.4**);
- once the trigger fires, the signal is delayed by a programmable number of samples (corresponding to the "pre-trigger" value in ns). In this way the gates for charge integration can start before the trigger (through the "gate offset" value). During the gate the baseline remains frozen to the last averaged value and its value is used as charge integration reference;
- for the whole duration of a programmable "trigger hold-off" value, other trigger signals are inhibited. It is recommended to set a trigger hold-off value compatible with the signal width. The baseline remains frozen for the whole trigger hold-off duration. For 751 series the baseline remains frozen for a longer time;

- the user can set a value of PSD to cut online the events with higher/lower value of PSD. In **Fig. 2.3** is shown an example of neutron-gamma discrimination. Referring to that example, the cut on PSD allows to reject most of the gamma events, allowing to record only neutrons and the small amount of gamma overlapping with the neutrons. The data throughput after the cut reduces significantly. This feature is available for 751 series only, being under development for 720 series. The user must set the FPGA register "PSD_THRESHOLD" (0x1n78 address, where n is the channel number) and bits 27 and 28 of the DPP_CTRL register (0x1n80 address, where n is the channel number) for gamma or neutron cut, respectively;

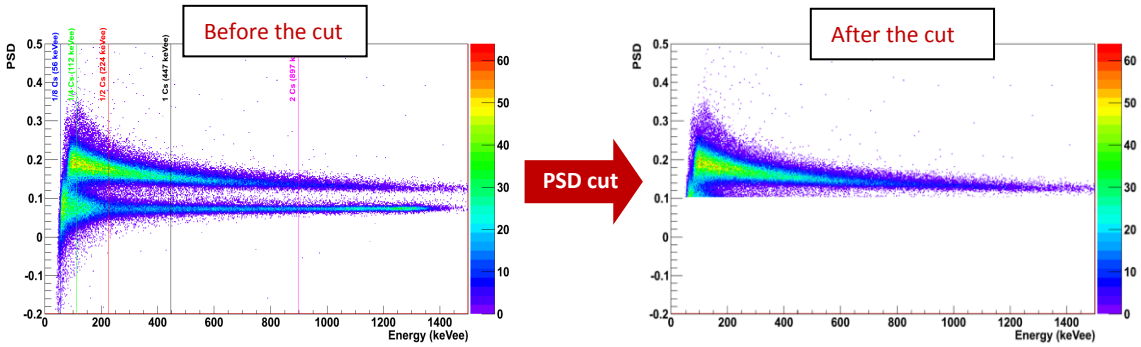


Fig. 2.3: 2D scatter plot of PSD parameter vs Energy in a neutron-gamma application. On the left the 2D plot before the cut, on the right the plot after the cut on PSD.

- the trigger enables the event building, that includes the waveforms (i.e. the raw samples) of the input, the trigger time stamp, the baseline, and the charge integrated within the gates. After that the system gets ready for a new event;
- the event data is saved into a memory buffer. The Control Software automatically optimize both the number of events inside the buffer, and the number of total buffers that the memory is divided in. The user can also choose to set these parameters by hand. If the buffer contains only one event, that buffer becomes immediately available for the readout and the acquisition continues into another buffer. If more events are written in one buffer, only when the buffer is complete those events become available for the readout.

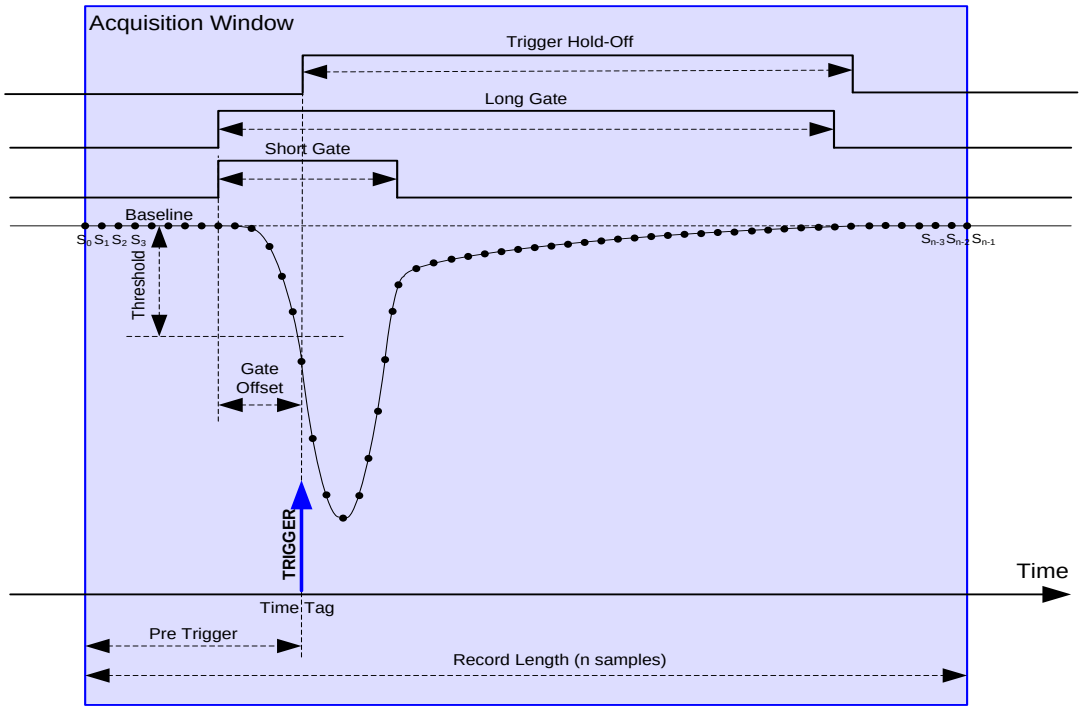


Fig. 2.4: Diagram summarizing the DPSD parameters. The trigger fires as soon as the signal crosses the threshold value. Long Gate, Short Gate, Gate Offset, Pre-Trigger, Trigger Hold-Off, and Record Length are also shown for one acquisition window.

Baseline

The baseline calculation is an important feature of the DPP-PSD Firmware, since its value is used as reference value for the charge integration of the input pulses. Moreover, most of the DPP parameters are related to the baseline values too. This paragraph describes in detail how it works.

The user can choose to set a fixed value for the baseline, or to let the DPP firmware calculate it. In the first case the user must set the value in LSB units, where 1 LSB = 0.48 mV for 720 series, and 1 LSB = 0.97 mV for 751 series. In the latter case, the baseline is dynamically evaluated as the mean value of *N* points inside a moving time window. The user can choose the *N* value among 8, 32, and 128 for 720 series, and 8, 16, 32, 64, 128, 256, and 512 for 751 series. The baseline is then frozen from few clocks before the gates start, to the end of the maximum value between the long gate and the trigger hold-off. For 751 series the freeze lasts some trigger clocks more than that maximum value. After that the baseline restarts again its calculation considering in the mean value also the points before the freeze. This allows to have almost no dead-time due to the baseline calculation.

Fig. 2.5 shows how the baseline calculation and freeze work. The trigger threshold dynamically follows the variation of the baseline.

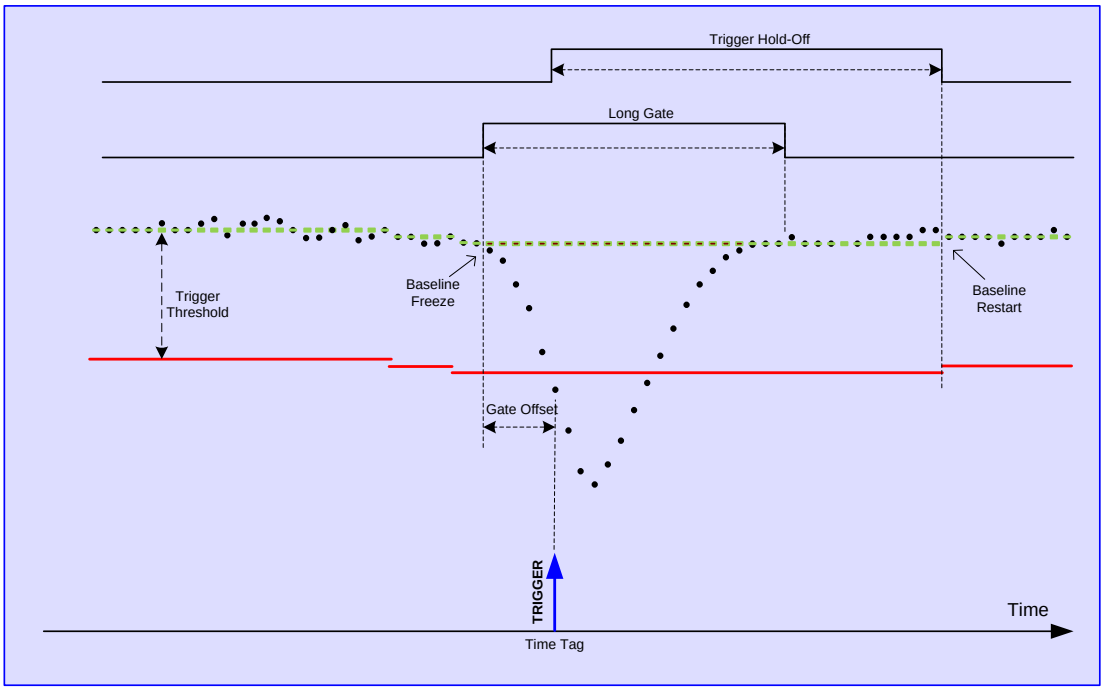


Fig. 2.5: Baseline calculation as managed by the DPP-PSD algorithm

3 Acquisition Modes

The DPSD allows for three main acquisition modes: Oscilloscope, List and Mixed.

1. **Oscilloscope Mode:** this acquisition mode is mainly intended to debug and to set the DPP parameters. For each trigger (internal or external), the digitizer saves a portion of the waveform (i.e. a sequence of samples within the acquisition window) into a local memory buffer. Running in Oscilloscope Mode, the user can view the input signal, the baseline, and other control signals (such as the trigger, the gate, the trigger hold-off, etc…) in the same plot. This makes easier to adjust the parameters for the acquisition. Running in oscilloscope mode implies a very high data throughput, due to the huge amount of samples saved into the board memory and then read out by the DAQ software.
2. **List Mode:** this is the mode where the DPP algorithm is applied runtime by the FPGA on the input signals. Once the parameters are properly set in the Oscilloscope Mode, the acquisition can be switched to the List Mode (histogram mode in the DPP Control Software). The waveform recording is disabled, while time stamp and integrated charge are calculated and saved into the local memory buffer for each triggered pulse. As soon as the list reaches a certain size, it is made available for readout and the acquisition continues in another buffer. This feature assures an acquisition with *no dead time*. Being the size of the event very small (typically few bytes), the throughput is extremely reduced.
3. **Mixed Mode:** in some applications, the simple charge/time stamp information is not enough and it is necessary to save also few samples (as raw waveforms) belonging to a specific region of interest. This is useful in sophisticated pulse shape analyses, as pulse fitting, that cannot be implemented on-line by the FPGA. Another example is when, to increase the timing resolution (4 ns for the x720 module, and , 1 ns for the x751 module) it is required to interpolate the samples around the threshold and evaluate the crossing timing. In all these cases, it is possible to read the charge, the baseline and the time stamp information together with a portion of the waveform, so that the user can retrieve further information and use it off-line, still keeping a reasonable level of throughput bandwidth.

Note: Mixed Mode is not managed by the DPP-PSD Control Software.

4 Memory Organization

Each channel has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers (also called “aggregates”), where each buffer contains a programmable number of events. The event format is programmable as well. The board registers involved are the following:

- BUFF_ORG (*Nb*): defines the total number of buffers (i.e. aggregates) in which the memory is divided ($num.buffers = 2^{Nb}$).
- NEV_AGGREGATE (*Ne*): defines the number of events contained in one aggregate. The maximum allowed value is 1023.
- RECORD_LENGTH (*Ns*): defines the number of samples of the waveform, if enabled (*Ns* = 8 * CUST.SIZE for 720 series, and *Ns* = 12 * CUST.SIZE for 751 series, where CUST.SIZE is the value written in the register).
- CONFIG: defines the acquisition mode and the event data format.

Note: Those who need to write their own DAQ software, must take care to choose the *Ne* value according to the event and buffer size, as explained in the examples in the next section.

For a detailed description, refer to the specific User Manual. Information about the use of these parameters in the CAENDigitizer library can be found in **[RD4]**.

According to the programmed event format, an event can contain a certain number of samples of the waveform, one trigger time stamp, the two charges Q_{short} and Q_{long}, and the baseline.

720 series

The physical memory of a board is made of memory locations, each of 128-bit (16B).

In terms of location occupancy:

Trigger Time Stamp = 1 location;

Waveform (if enabled) = 1 location every 8 samples;

Charges (Q_L and Q_S) and Baseline (BSL) = 1 location.

Fig. 4.1 shows how the data is saved into the physical memory.

Note: Fig. 4.1 refers to the event storage in the physical memory, while the event readout format is shown in the **Event Data Format** section.

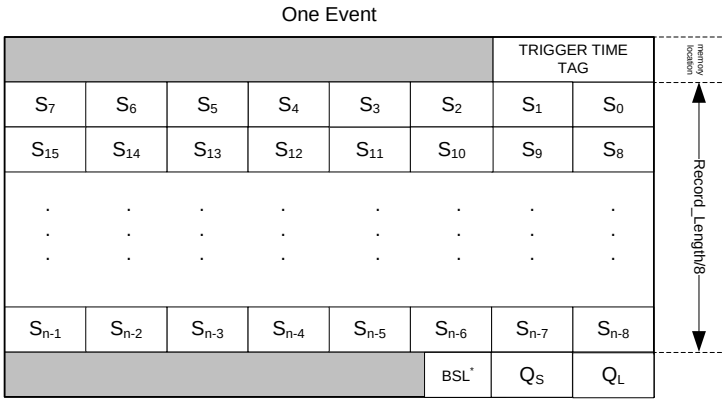


Fig. 4.1: Data organization into the Internal Memory of x720 digitizer

(*)Baseline data is the baseline value frozen with the trigger.

As previously said, the RECORD_LENGTH and the CONFIG settings determine the event size; the user must calculate the number of event per buffer (*Ne*) and the number of buffers (2^{Nb}) accordingly. When the board runs in List Mode, the event memory contains only two locations, one for the Trigger Time Tag and one for the Charge and Baseline. Therefore it is very small and it is suggested to use a big value for *Ne* to make the buffer size as big as at least a few KB. Small buffer size results in low readout bandwidth. The only drawback of setting high values for *Ne* is that the events are not available for the readout until the buffer is complete; hence there is some latency between the arrival of a trigger and the readout of the relevant event data. Conversely, when the board runs in Oscilloscope Mode, especially when the record length is large, it is more convenient to keep *Ne* low (typically 1).

Example1: suppose that the mixed mode is enabled and *Ns* is set to 400 samples:

event size (in locations) = 1(Time_Stamp) + *Ns*/8(Waveform) + 1(Charge_Baseline) = 52 loc.

Suppose to set *Ne* = 60 (number of events per buffer), hence:

buffer_size (in locations) = 52 * 60 = 3120 loc.

Supposing that the memory board is made of 128k loc./ch, the number of buffers will be:

128k/3120 = 42 (buffers).

This value corresponds to the maximum number of buffers that the memory can contain. However, since the programmable value must be a power of two, the user has to choose the closest number smaller than 42 which can be represented as a power of two, that is $2^5 = 32$ (i.e. *Nb* = 5 has to be written in the BUFF_ORG register).

Example2: suppose that the mixed mode is enabled and *Ns* is set to 24 samples:

Event size (in locations) = 1(Time_Stamp) + *Ns*/8(Waveform) + 1(Charge_Baseline) = 5 loc.

Having a small event size, is it convenient to divide the memory into few buffers of bigger size to store a large amount of events.

Suppose to have set *Nb* = 3, so that the number of buffers is 8.

Supposing that the board memory option is made of 64k locations, each buffer consists in 64k/8 = 8k locations and so the resulting number of event per aggregate should be:

Ne = 8k/5 = 1639.

IMPORTANT: in this case, the real number of events stored per aggregate is 1023, due to the register length constraint already mentioned.

751 series

The physical memory of a board is made of memory locations, each of 128-bit (16B)

In terms of location occupancy:

Trigger Time Stamp = 1 location;

Waveform (if enabled) = 1 location every 12 samples;

Charges (Q_L and Q_S) plus Baseline = 1 location.

Therefore, the events size can be easily calculated. **Fig. 4.2** shows how the data are saved into the physical memory.

Note: Fig. 4.2 refers to the event storage in the physical memory, while the event readout format is shown in the **Event Data Format** section.

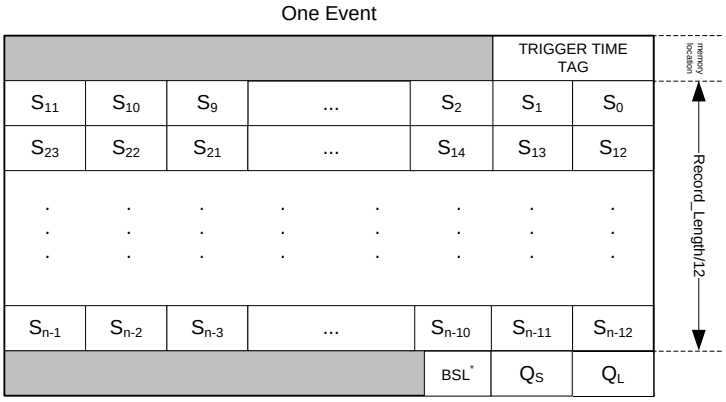


Fig. 4.2: Data organization into the Internal Memory of x751 digitizer
(*)Baseline data is the baseline value frozen with the trigger.

The same relation between the readout bandwidth and *Ne* in the 720 series is valid for the 751 series.

Example: suppose that the mixed mode is enabled and *Ns* = 480 samples:

event size (in locations) = 1(Time_Stamp) + *Ns*/12(Waveform) + 1(Charges_Baseline) = 42.

Suppose to have *Ne* = 30 (number of events per buffer), hence:

buffer_size (in locations) = 42 * 30 = 1260 loc.

Supposing that the board memory is made of 128k loc./ch, the number of buffers will be:

128k/1260 = 102 (buffers).

This value corresponds to the maximum number of buffers that the memory can contain. However, since the programmable value must be a power of two, the user has to choose the closest number smaller than 102 which can be represented as a power of two, that is $2^6 = 64$ (i.e. *Nb* = 6 has to be written in the BUFF_ORG register).

Event Data Format

When the data readout is performed by the Control Software, the data format has the following encoding. Those who need to write their own acquisition software must take care of the following sections.

Channel Aggregate Data Format for 720 series

The Channel Aggregate is composed by the set of *Ne* events, where *Ne* is the programmable number of events contained in one aggregate (see the previous section). The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) for 720 series is shown in **Fig. 4.3**, where:

"CHANNEL AGGREGATE" DATA FORMAT

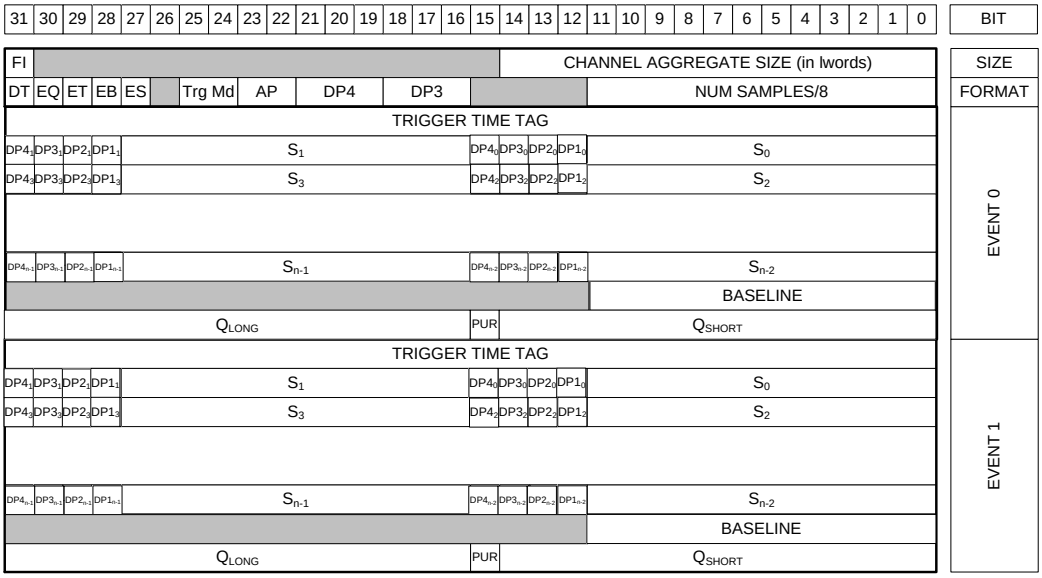


Fig. 4.3: Channel Aggregate Data Format scheme for 720 series

FI: if 1, the second word is the Format Info

DT: Dual trace enabled flag (1 = enabled, 0 = disabled)

EQ: Charge enabled flag

ET: Time Tag enabled flag

EB: Baseline enabled flag

ES: Waveform (samples) enabled flag

Trg Md: Trigger Mode enabled flag

AP: Analog Probe selection (for DPSD this is equal to the "Baseline")

DP3: Digital Virtual Probe 3 selection among:

000 = "External TRG", the external trigger signal when enabled;

001 = "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

010 = "Shaped TRG", this is a logic signal of programmable width coming out together with the trigger. This is useful when you want to send out a trigger signal, and in the coincidence acquisition mode (refer to **[RD3]**);

011 = "TRG Val. Acceptance Win.", the logic signal corresponding to the time window where the coincidence validation is accepted. The validation enable the event to be written into the memory (see **[RD3]**);

100 = "Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = "Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**).

DP4: Digital Virtual Probe 4 selection among:

000 = “Short Gate”;

001 = “Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold;

010 = “TRG Validation”, digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA(refer to **[RD3]**);

011 = “TRG HoldOff”, digital signal corresponding to the Trigger Hold-Off, with the same width set in the Channel Tab for the Trigger Hold-Off parameter;

100 = “Pile Up“, logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = “Coincidence“, logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**).

DPi_m (*i*=1, ...,4; *m*=0, 1, …,n-2): Digital Virtual Probe value *i* for sample *m*

$DP1_m$ is always the “Trigger” probe value

$DP2_m$ is always the “Long Gate” probe value

$DP3_m$ is the value of the probe written in DP3 flag

$DP4_m$ is the value of the probe written in DP4 flag

$S_{m'}$ (*m’*=0, 2, 4, …, n-2): Even Samples of input signal at time *t=m’*. If DT=1, $S_{m'}$ corresponds to the Baseline at time *t=m’+1*

$S_{m''}$ (*m’’*=1, 3, 5, …, n-1): Odd Samples of input signal at time *t=m’’*

$Q_{short/long}$: integrated charge value in the short/long gate

Channel Aggregate Data Format for 751 series

The Channel Aggregate is composed by the set of *Ne* events, where *Ne* is the programmable number of events contained in one aggregate (see the previous section). The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) for series 751 is shown in **Fig. 4.4**, where:

“CHANNEL AGGREGATE” DATA FORMAT

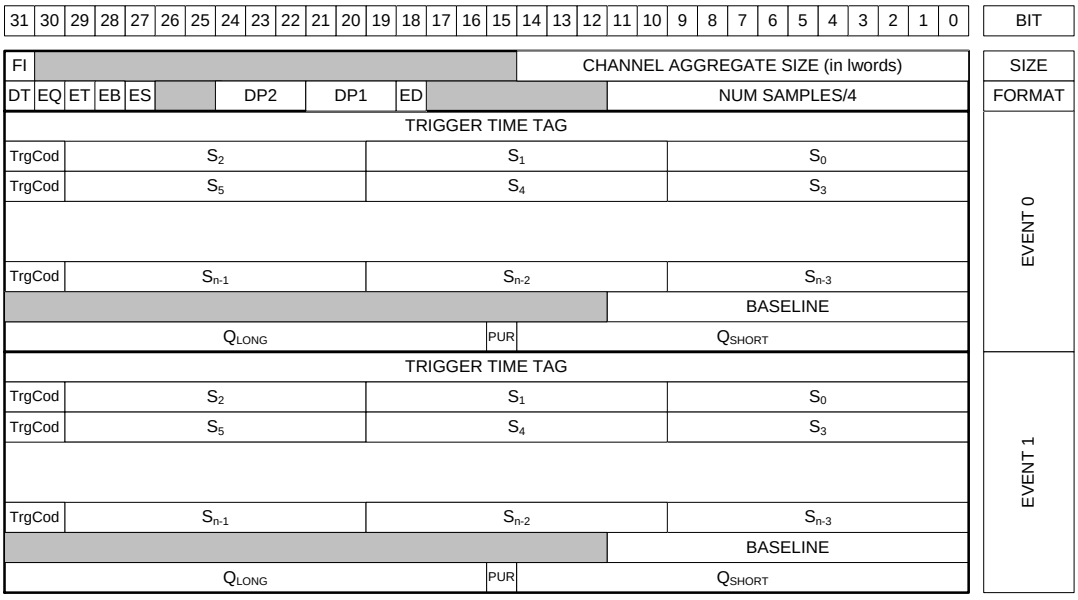


Fig. 4.4: Channel Aggregate Data Format scheme for 751 series

FI: if 1, the second word is the Format Info

DT: Dual trace enabled flag (1 = enabled, 0 = disabled)

EQ: Charge enabled flag

ET: Time Tag enabled flag

EB: Baseline enabled flag

ES: Waveform (samples) enabled flag

DP1: Digital Virtual Probe 1 selection among:

000 = “Long Gate”;

001 = “Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold;

010 = “Shaped TRG”, this is a logic signal of programmable width coming out together with the trigger. This is useful when you want to send out a trigger signal, and in the coincidence acquisition mode (refer to **[RD3]**);

011 = “TRG Val. Acceptance Win.”, the logic signal corresponding to the time window where the coincidence validation is accepted. The validation enable the event to be written into the memory (see **[RD3]**);

100 = “Pile Up“, logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = “Coincidence“, logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**);

DP2: Digital Virtual Probe 2 selection among:

000 = “Short Gate”;

001 = “Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold;

010 = “TRG Validation”, digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA(refer to **[RD3]**);

011 = “TRG HoldOff”, digital signal corresponding to the Trigger Hold-Off, with the same width set in the Channel Tab for the Trigger Hold-Off parameter;

100 = “Pile Up“, logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = “Coincidence“, logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**);

ED: Digital Probe enabled flag. (*)

$S_{m'}$ (m'=0, 2, 4, …, n-2): Even Samples of input signal at time $t=m'$. (*)

$S_{m''}$ (m''=1, 3, 5, …, n-1): Odd Samples of input signal at time $t=m''$. If DT=1, $S_{m''}$ corresponds to the Baseline at time $t=m''-1$. (*)

Trg Cod: encodes on which sample (of the same word) the trigger fired

00 = no trigger

01 = trigger on the first sample S_0

10 = trigger on the second sample S_1

11 = trigger on the third sample S_2

$Q_{short/long}$: integrated charge value in the short/long gate

(*) When ED $\neq$ 0, the analog trace sample is represented into 8 bits, rather than 10 bits. Indeed the last two bits of each samples are reserved for the two digital probes. Conversely, when ED = 0, each analog trace sample is represented into 10 bits.

Board Aggregate Data Format

The Board Aggregate data format is common for both 720 and 751 series.

For each readout request (occurring when at least one channel has available data to be read) the “interface FPGA (ROC)” reads one aggregate from each enabled channel memory. No more than one aggregate per channel is read each time. The sample of Channel Aggregates is the Board Aggregate. If one channel has no data, that channel does not come into the Board Aggregate.

The data format when all 8 channels of a VME have available data is as shown in **Fig. 4.5**, where:

“BOARD AGGREGATE” DATA FORMAT

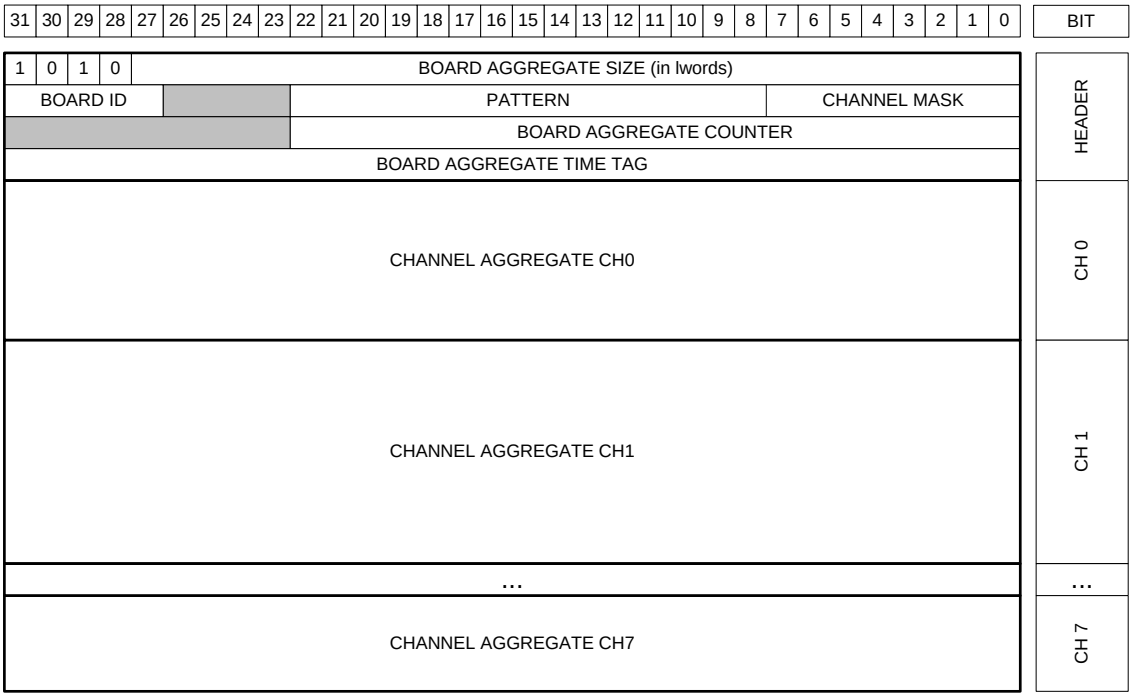


Fig. 4.5: Board Aggregate Data Format scheme

BOARD AGGREGATE SIZE: total size of the aggregate

PATTERN: is the value read from the LVDS I/O (VME only);

CHANNEL MASK: corresponds to those channels participating to the Board Aggregate;

BOARD AGGREGATE COUNTER: counts the board aggregate. It increase with the increase of board aggregates;

BOARD AGGREGATE TIME TAG: is the time of creation of the aggregate (this not corresponds to any physical quantity);

Data Block

The readout of the digitizer is done using the Block Transfer (BLT, refer to **[RD4]**); for each transfer, the board gives a certain number of Board Aggregates, consisting in the Data Block. The maximum number of aggregates that can be transferred in a BLT is defined by the READOUT_BTL_AGGREGATE_NUMBER. In the final readout each Board Aggregate comes successively. In case of n Board Aggregates, the Data Block is as in **Fig. 4.6**.

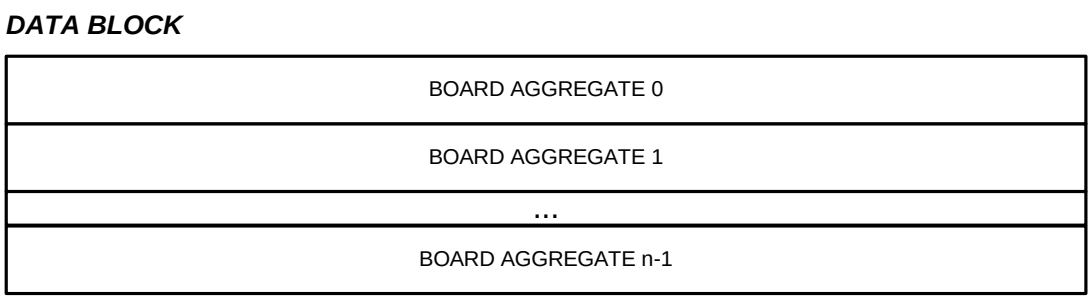


Fig. 4.6: Data Block scheme

5 Getting Started

Scope of the chapter

This chapter is intended to provide the user with a quick guide of the DPP-PSD Control Software, in order to deal with a DPSD System in the practical use. For a demo purpose only we used a gamma source of Cobalt-60. The user can refer to **[RD2]** for a real neutron – gamma discrimination application.

All steps in this chapter are made with the 720 series. The same behaviour can be generalized for the 751 series.

System Overview

CAEN's DPSD System proposed in the chapter consists of the following CAEN products:

- DT5720B, 4-channel 12-bit 250 MS/s Desktop Digitizer.
- DPP-PSD firmware for 720 series, release 4.1_131.6, running on the Digitizer.
- DPP-PSD Control Software, release 1.2.3, running on the host station.

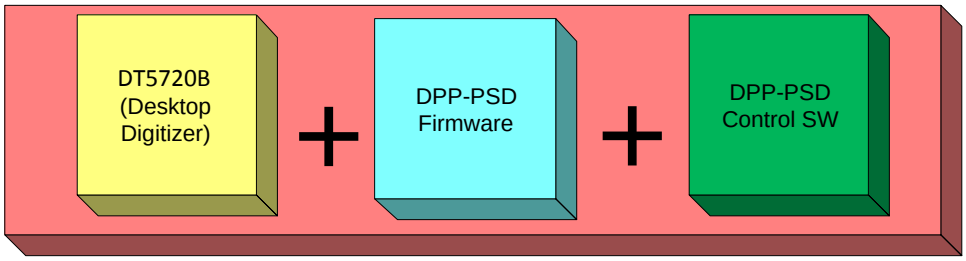


Fig. 5.1: CAEN DPSD System components

Hardware Setup

The DPSD receives on channel 0 of the DT5720B the signal from a NaI(Tl) coupled with a PMT. The CAEN N1470 (a 4-channel, HV Programmable Power Supply board) provides the supply to the detector (V_{bias} = 800 V). A Cobalt-60 (^{60}Co) gamma ray source (counting rate ~ 1 KHz) is used. A computer equipped with a Microsoft Windows 7 Professional 64-bit OS acts as host station. The communication protocol between the computer and the Digitizer is USB (2.0 version).

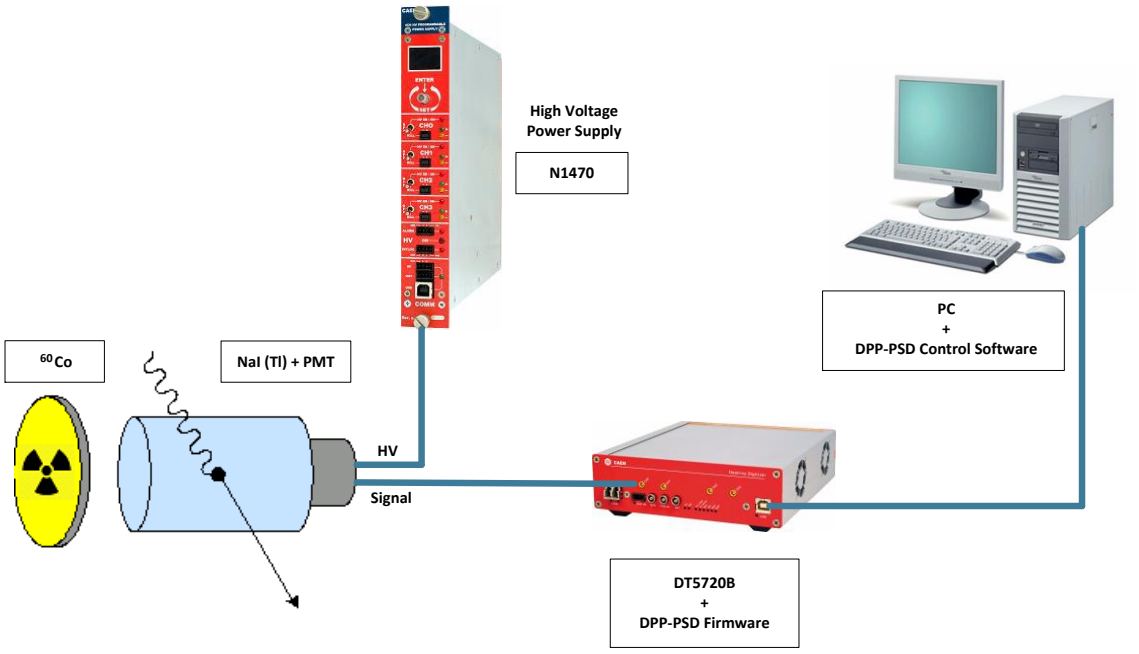


Fig. 5.2: The hardware setup including the DPSD used for the practical application

Drivers and Software

In order to manage the DPHA System, the host station needs either Windows or Linux OS, and the third-party software **Java Runtime** Environment 6 or later (trademark of Oracle, Inc, downloadable from http://www.java.com). Linux users must also take care of proper installation of **gnuplot** graphical tool, as well as of **CAEN Libraries**. The latter can be downloaded from CAEN website (login required before to download).

According to the preferred way of connection to the digitizer, users must also take care of proper installation of USB or optical drivers. In our case we are going to describe the procedure for USB connection.

- ✓ DRIVERS
  - **USB 2.0** CAEN driver.

Note: If you're using a different communication interface (i.e. Optical Link or VME), the related driver is required.

Note: It is recommended to install the driver before to connect the hardware.

Note: Detailed installation steps of CAEN USB drivers for communicating with desktop digitizers are described for several Microsoft Windows OSs in **[RD5]**.

How to install the driver (Windows)

Download the latest release of the **USB driver** for Windows on CAEN website in the 'Software/Firmware' area at the DT5720 page.

Unpack the **driver package**.

Power on the **Digitizer** and **plug** the **USB cable** in a USB port on your computer.

Windows will try to find drivers and, in case of failure (the message "**Device driver software was not successfully installed**" may be displayed), the driver needs to be installed manually:

Go to the system's **Device Manager** through the Control Panel and **check** for the **CAEN DT5xxx USB1.0** unknown device.

Right click and **select Driver software update** in the scrolling menu.

Select the option to **browse my computer for driver software.**

Point to the **driver folder** and finalize the installation.

How to install the driver (Linux)

Download the latest release of the **USB driver** for Linux on CAEN website in the 'Software/Firmware' area at the DT5720 page.

Unpack the **driver package** (tar –zxf CAENUSBDrvB-xxx.tgz).

Go to the driver **folder** (cd CAENUSBDrvB-xxx).

Follow the **instructions** on the **Readme.txt file.**

Type: make

sudo make install

Reboot your machine

- ✓ SOFTWARE
  - **DPP-PSD Control Software** for Windows OS.

    Download the standalone **DPP-PSD Control Software 1.2.3** full installation package on CAEN website in the 'Download' area at the DPP-PSD Control Software page (**login is required before the download**).

    Unpack the **installation package, launch** the **setup file** and **complete** the **Installation wizard.**

  - **DPP-PSD Control Software** for Linux.

    Download the DPP-PSD_ControlSoftware-1.2.3.tar.gz package on CAEN website in the 'Download' area at the DPP-PSD Control Software page (**login is required before the download**).

    Unpack the **installation package** (tar –zxf DPP-PSD_ControlSoftware-1.2.3.tar.gz).

Follow the instruction on **Setup/Linux/Readme.txt**

Type: ./configure

make

sudo make install

Launch the Control Software typing **DPP-PSD_ControlSoftware**

Note: in the Linux environment it is required to first install CAENVME, CAENComm and CAENDigitizer. You can find those libraries in the CAEN web page. In the Windows environment all libraries come within the control software package.

Firmware and Licensing

The DPP-PSD Control Software works with the **DPP-PSD Firmware**.

✓ **How to install the firmware**

Download the **DPP-PSD Firmware** (.cfa) for 720 series on CAEN website in the 'Download' area at the DPP-PSD page.

Download the **CAENUpgrader** software to upload the firmware on your board. The program full installation package for Windows OS is available on CAEN website in the 'Download' area at the CAENUpgrader page.

Unpack the **installation package, launch** the **setup file** and **complete** the **Installation wizard.**

Run the **CAENUpgrader GUI** by one of the following options:

- The **desktop icon** for the program
- The **Quick Launch icon** for the program
- The **.jar file** in the *bin* folder from the installation path on your host

Select '**Upgrade Firmware**' in the '**Available actions**' scroll box menu of the '**Board Upgrade**' tab.

Select the **model** of your board in the '**Board Model**' scroll box menu.

Enter the **.cfa file** in the '**Firmware binary file**' text box by the '**Browse**' button.

Set '**USB**' in the '**Connection Type**' scroll box menu.

Set '**0**' as '**Link number**' setting.

Check '**Standard Page**' in the '**Config Options**'.

Press the '**Upgrade**' button to perform the upload; after few seconds, a pop up message will inform you about the successful upgrade.

Power cycle the **board**.

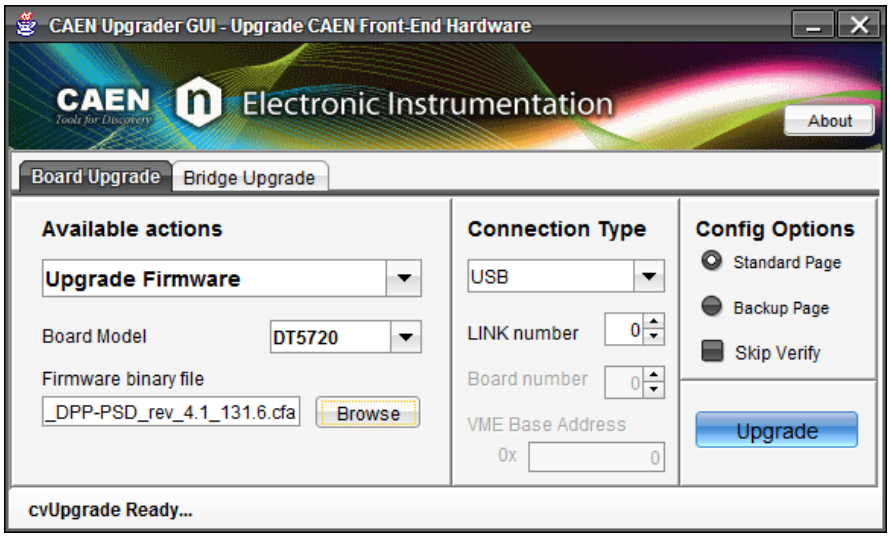


Fig. 5.3: CAENUpgrader settings for DPP-PSD firmware upgrade.

Note that when running the DPP-PSD Control Software, the program checks for the firmware loaded in the target Digitizer. If no license is found, a pop-up warning message shows up and reports the time left before the acquisition is stopped (trial version). In order to unlock the DPP firmware and to use it without any time limitation, you need to purchase a license from CAEN. Refer to **[RD6]** for detailed instructions on how to use CAENUpgrader and the licensing procedure.

Practical Use

The following step-by-step procedure shows how to use the DPP-PSD Control Software (see Chapter **7**) in an application of gamma ray detection, how to set the relevant DPP parameters and plot the signals (Oscilloscope mode), how to display the energy histogram and the 2D-histogram for the Neutron -Gamma discrimination (Histogram mode), and how to save the acquired data.

Check that the whole hardware in your setup is properly connected and powered on.

Note: After typing the value of a parameter in a box menu, press the "**Enter**" key on your keyboard to activate the setting.

1. **Run the software.**

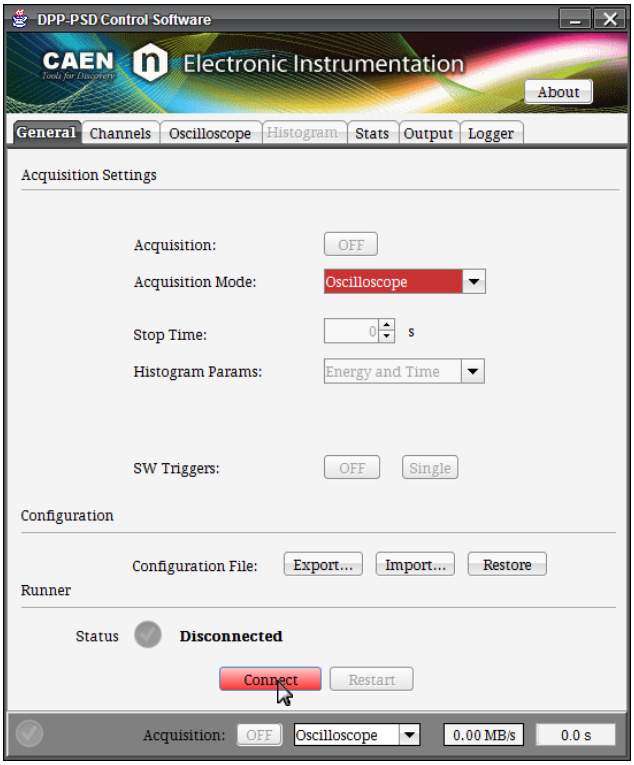
Run the **DPP-PSD Control Software GUI**, according to the options selected in the installation wizard, choosing one of the following options:

- The **Desktop icon** for the program
- The **Quick Launch icon** for the program
- The **.bat file** in the main folder from the installation path on your host

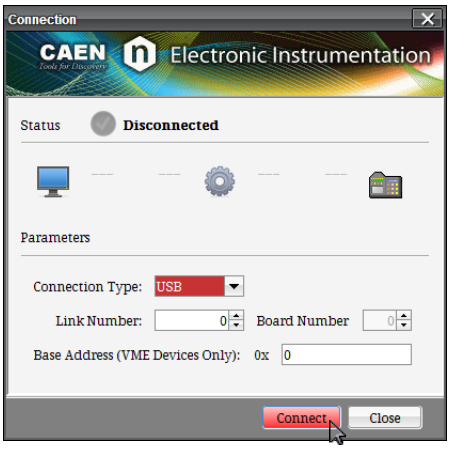
2. Connect to the Digitizer.

Path1: Tab **GENERAL** → Section **RUNNER**

Action1: click the button **CONNECT**. The "**Connection**" window will appear.



Action2: set the connection parameters values. Using a USB communication link with a Desktop digitizer, the correct settings are: **TYPE** = "**USB**", **LINK** = "**0**" and **ADDRESS** = "**0**". **Tab. 5.1** shows the setting values for common communication channels and Digitizers. Further examples are in **Tab. 7.2**.

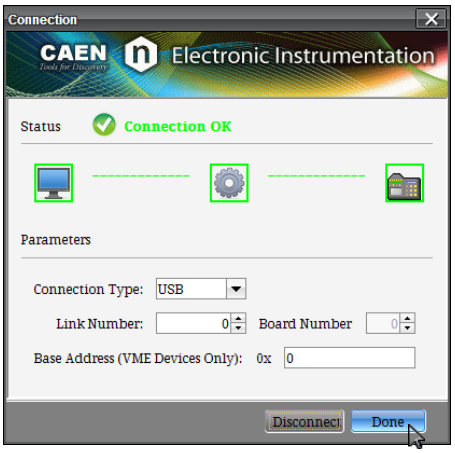


Connection chain	Type	Link	Slave	Address
PC –> **USB** –> DT5720 / N6720	USB	0	0	0
PC –> **USB** –> V1718 –> **VME** –> V1720	USB	0	0	32100000*
PC –> **PCI/PCIe** –> A2818/A3818 –> **CONET** –> DT5720 / N6720	PCI	0	0	0
PC –> **PCI/PCIe** –> A2818/A3818 –> **CONET** –> V1720	PCI	0	0	32100000*

Tab. 5.1: Examples of connection settings

(*)For the correct VME base address to be used, please refer to the Digitizer's User Manual.

Action3: click the button **CONNECT** and verify that the connection Status turns on green (i.e. Connection OK), then click the button **DONE**.

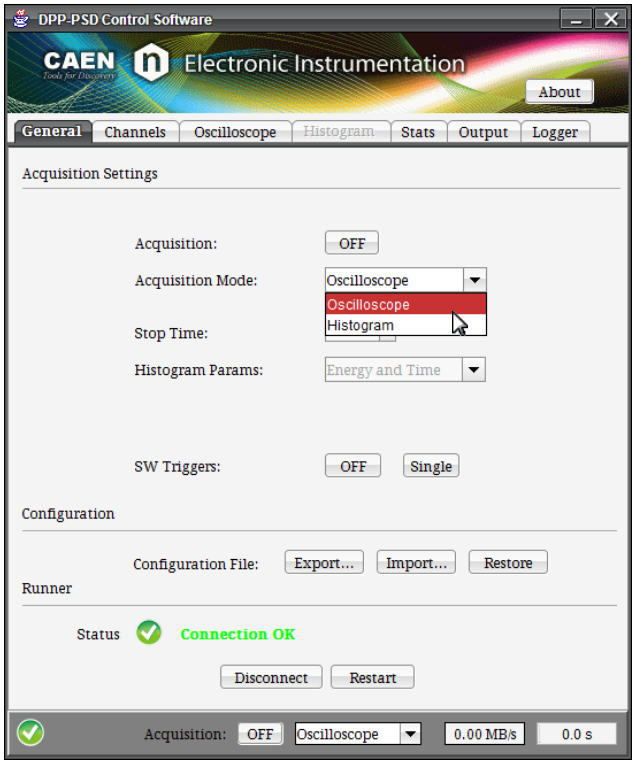


Note: Every time you connect the Control Software to a 751 series digitizer, the latter makes an internal calibration of the ADCs, which is strongly dependent on the ADC temperature itself. For this reason check that the ADC temperature is stable by reading the temperature registers (address 0x1nA8, where n is the channel number). The temperature can take some minutes to level off.

3. Set Oscilloscope mode, enable Channel 0, check signal polarity and start acquisition.

Path1: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: set **ACQUISITION MODE** on "**Oscilloscope**" using the scroll menu box.



Path2: Tab **CHANNELS** → Field **CHANNEL SETTINGS FOR** → Section **GENERAL SETTINGS**

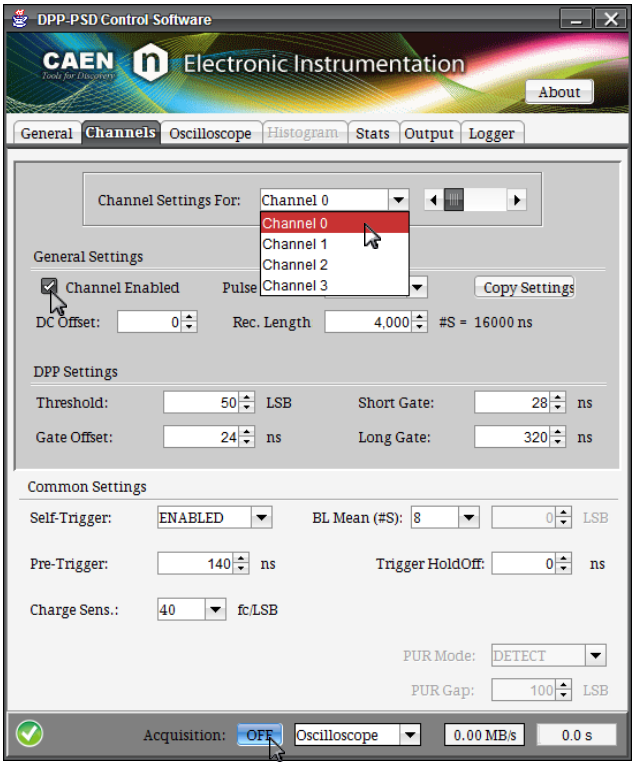
Action1: Select "**Channel 0**" using the scroll menu box or the side bar.

Action2: check "**Channel Enabled**" so that the settings in the tab are active for the selected channel.

Action3: press the **ACQUISITION** button in the deep grey common bar at the bottom of the GUI:

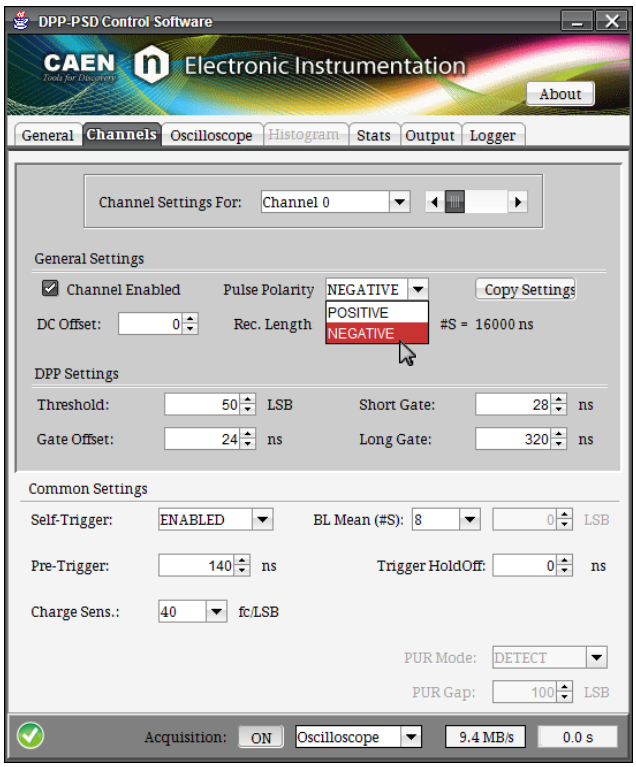
- **OFF** = acquisition is off.
- **ON** = acquisition is on.

Check that the "Run" green LED on the Digitizer's front panel lights on.



Action4: set the **PULSE POLARITY** on "**Negative**", according to the polarity of the input signal from the detector.

Note: The algorithm is internally designed to work with negative pulses. When the analog input pulse is positive, it is necessary to invert it before the DPP algorithms are applied. The option PULSE POLARITY = "Positive" enables the internal inversion of the pulse polarity. Please notice that the inversion is applied to the DPP algorithms only, while it doesn't affect the waveform recording (both plots and output files keep the original pulse polarity).



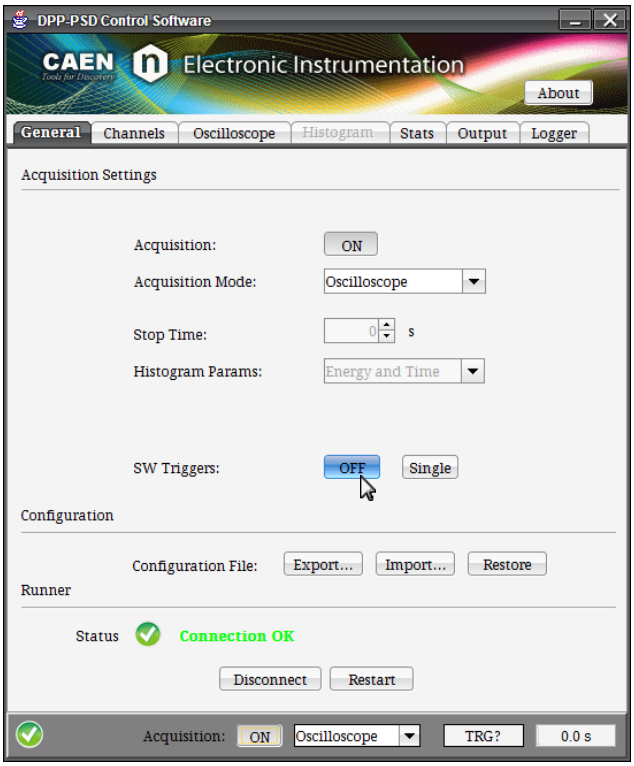
4. **Set the parameters for self-triggering (DC Offset, Baseline, Threshold).**

With the acquisition on, since it is not guaranteed that the channel is properly triggering on the input pulses, the Software Trigger is used to force the acquisition. It is so possible to adjust parameters like the DC Offset, the Baseline and the Threshold in order to enable the Digitizer to self-trigger.

Path1: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: Press the **SOFTWARE TRIGGERS** "**ON/OFF"** button to enable a software trigger to be continuously issued.

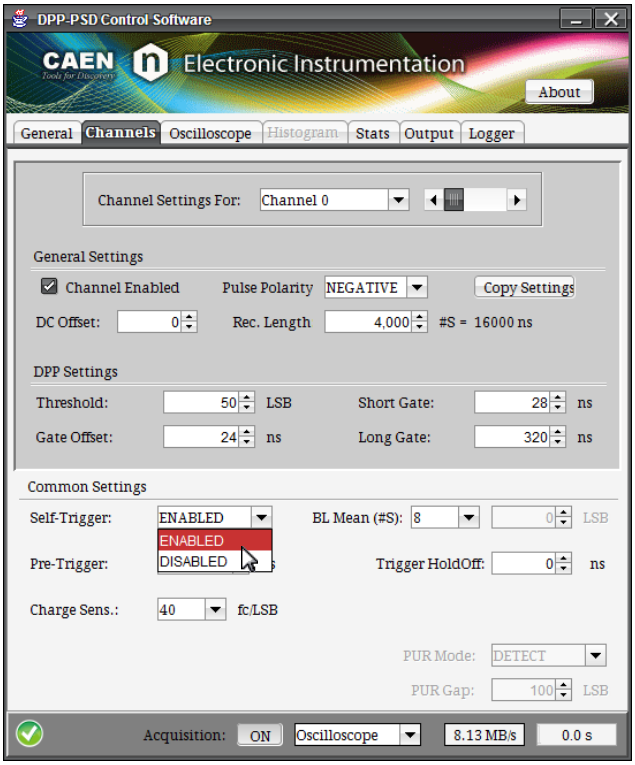
- **OFF** = Software Trigger is disabled.
- **ON** = Software Trigger is enabled.



Make sure that the self-trigger option is enabled. Otherwise, perform the **path2** below.

Path2: Tab **CHANNELS** → Section **COMMON SETTINGS**

Action1: set **SELF-TRIGGER** on "**Enabled**" in the using the scroll menu box.



Now it is worth plotting the input signal to estimate the DC Offset adjustment.

Path3: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

Action1: set "**Channel 0**" in the **CHANNEL** list.

Action2: check the "**Wave**" box as **PLOT MODE**.

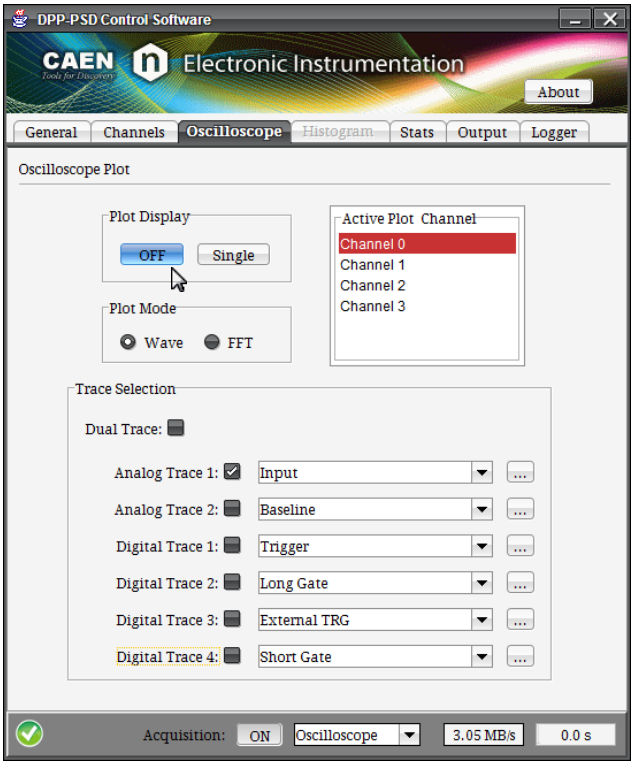
Action3: disable **DUAL TRACE** displaying.

Action4: check **ANALOG TRACE 1** and select "**Input**" in the scroll box. The input pulse from the Detector-PMT system will be plotted.

Action5: disable **ANALOG TRACE 2**, **DIGITAL TRACE 1**, **DIGITAL TRACE 2**, **DIGITAL TRACE 3** and **DIGITAL TRACE 4** (DIGITAL TRACE 4 not present for the 751 series)**.**

Action6: enable the continuous plotting by pressing the **PLOT DISPLAY** "**ON/OFF**" button:

- **OFF** = Plot displaying is off.
- **ON** = Plot displaying is on.



The DC Offset is a DC value added to the input signal at the input stage of the Digitizer to fit the signal dynamic range to the ADC input dynamics.

The DC Offset parameter is expressed in percentage of the Digitizer's ADC input dynamics and ranges between -50 and +50 (%). Theoretically, the value of 0 (DC Offset = "0") means an input pulse DC level set to half of the ADC dynamics (i.e. 2048 counts for the 12-bit and 2 V input range DT5720).The value of "50" (DC Offset = "50") sets the DC level at the lower dynamics limit (i.e. 0 counts), while the value of "-50" (DC Offset = "-50") sets the DC level at the upper dynamics limit (i.e. 4095 counts). The real DC offset adjustment implemented in the DPP-PSD firmware is shown in **Fig. 5.4**: in order to preserve from saturation the input signals near the dynamics boundaries, setting the DC offset to +50 or -50 puts the signal baseline respectively a step up the upper boundary and a step under the lower boundary.

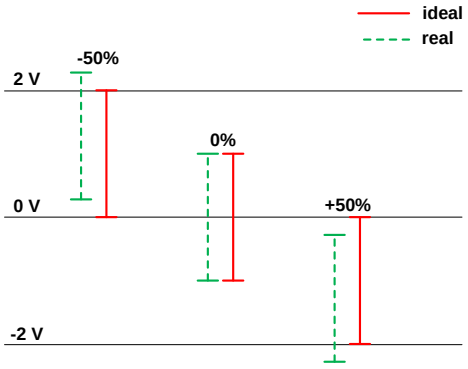


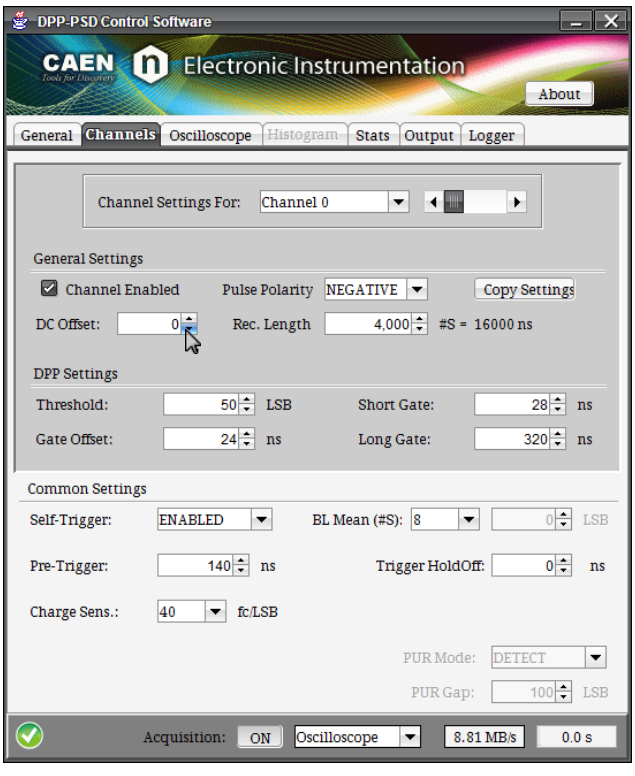
Fig. 5.4: Input signal DC offset adjustment description.

Action7: look at the DC level of the input pulse (DC offset) in your plot to check if an adjustment is needed according to the Digitizer's ADC dynamic range. In the specific case, we chose to set the DC offset around half the dynamics (theoretically 2048 counts).

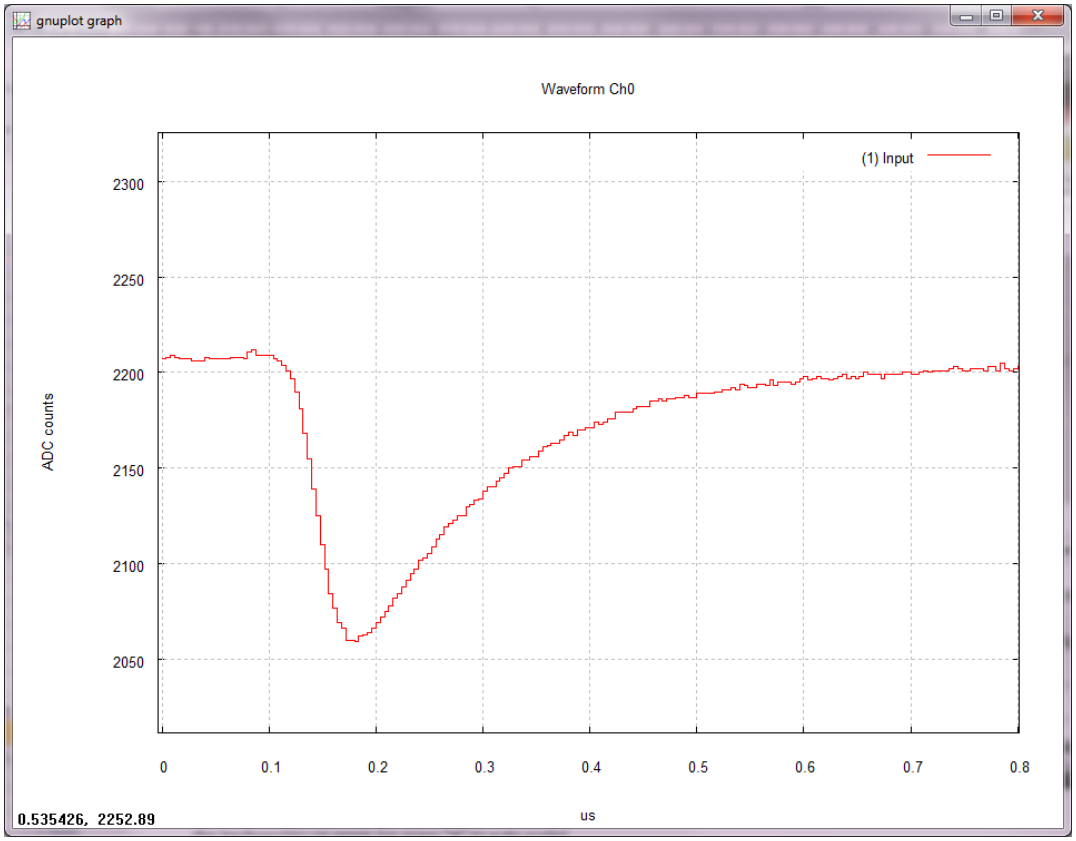
Path4: Tab **CHANNELS** → Section **GENERAL SETTINGS**

Action1: verify that the "**Channel Enabled**" box is checked.

Action2: type or set "**0**" in the **DC OFFSET** box menu.



Action3: check the effect of the previous settings in the plot window.



Note: The plot above has been zoomed. To do that, right click on the plot in a point near the portion of the signal you want to zoom, then release the mouse button, move to a point on the opposite corner and left click. Press "**u**" key on the keyboard to un-zoom (or press "**a**" to auto scale).

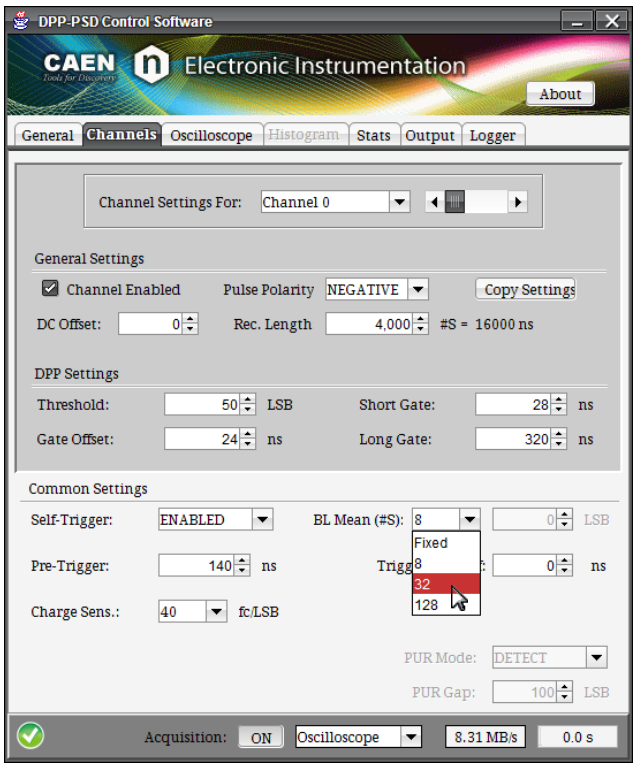
Next step is to set the input signal baseline calculation. Both the Threshold parameter, i.e. the trigger threshold, and the charge integration are referred to the baseline value.

The Control Software provides two options for setting the baseline:

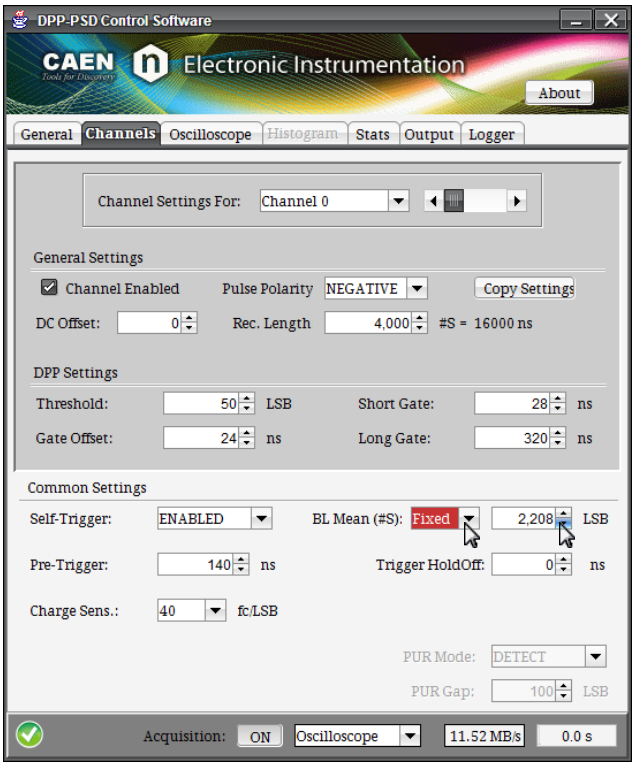
- Baseline mean calculation, where the DPP-PSD algorithm calculates *online* the input signal baseline through a mean filter over a number of samples set by the BASELINE MEAN parameter.
- Absolute baseline, where a fixed baseline value is set by the ABSOLUTE BASELINE parameter.

Path5: Tab **CHANNELS** → Section **COMMON SETTINGS**

Action1: set the **BASELINE MEAN** to "**32**" in the scrolling box menu. Those values correspond to the number of samples used in the baseline calculation.



Action2: set the **BASELINE MEAN** to "**Fixed**" in the scrolling box menu and set the absolute value for the baseline according to the waveform plot.



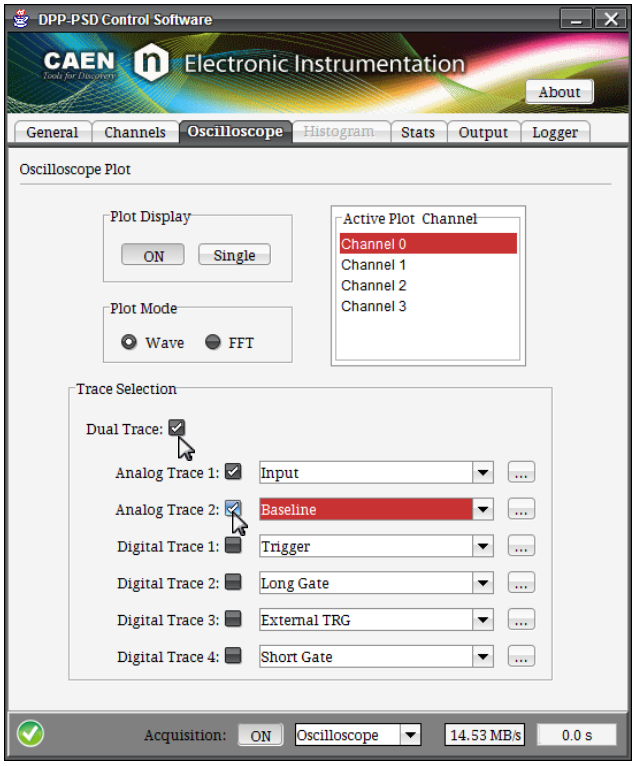
The user must choose either one of the two methods.

The plotting of the input signal and the baseline can help to check the effect of the setting.

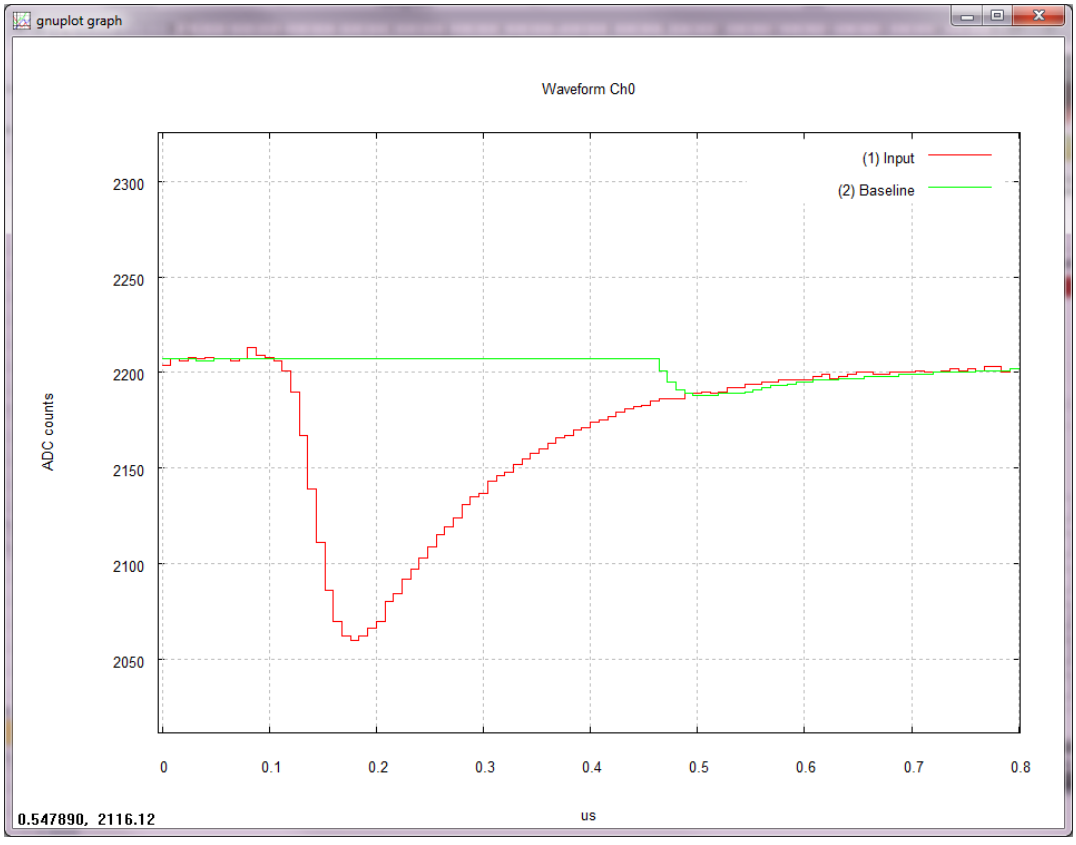
Path6: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

Action1: enable **DUAL TRACE** displaying by clicking the related check box. This allows the second analog trace (ANALOG TRACE 2) to be plotted. When you disable the **DUAL TRACE** setting, the ANALOG TRACE 2 will not be plotted, even if enabled.

Action2: enable **ANALOG TRACE 2** check box and select "**Baseline**" in the scroll menu.



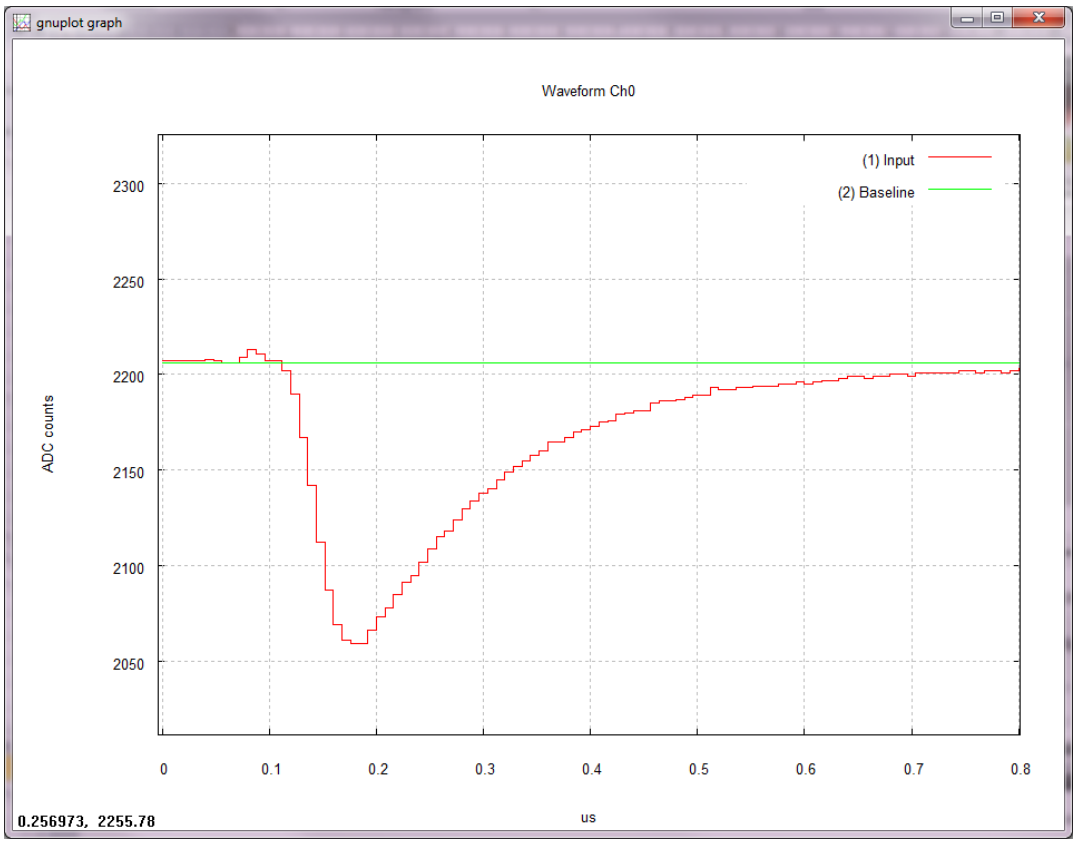
When selecting the automatic baseline calculation the oscilloscope plot will appear as follows:



The baseline remain frozen for the whole duration of the maximum value between the gate and the trigger hold-off parameters. To freeze it for the whole signal width you must adjust the gate and trigger hold-off parameters. Instructions on how to change those parameters are explained in the following steps.

Note: For 751 series, the baseline freeze lasts for a longer time than the greater value between Long Gate and Trigger Hold-off.

When choosing the fixed value for the baseline, the baseline remains frozen for the whole acquisition window, as you can see from the following plot.



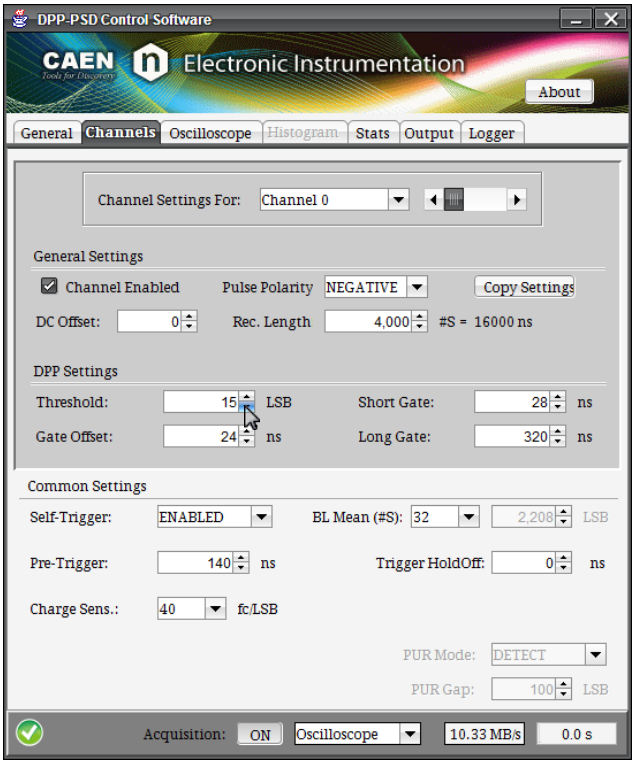
Note: The oscilloscope plots above has been displayed using the auto scale function of *gnuplot* (press "**a**" on your keyboard to activate the auto scale).

We choose the first method, i.e. the automatic baseline calculation. It is now possible to set the trigger threshold. For this purpose, the parameter THRESHOLD is defined as the relative absolute value of the trigger threshold with respect to the baseline.

Once the baseline calculation has been fixed, it is possible to set the trigger threshold. For this purpose, the parameter THRESHOLD is defined as the relative absolute value of the trigger threshold with respect to the baseline value.

Path7: Tab **CHANNELS** → Section1 **DPP SETTINGS** → Section2 **COMMON SETTINGS**

Action1: set a value of **THRESHOLD** in the box menu according to the noise level of the input signal baseline. In our example we fix "**15"** LSB as threshold level.

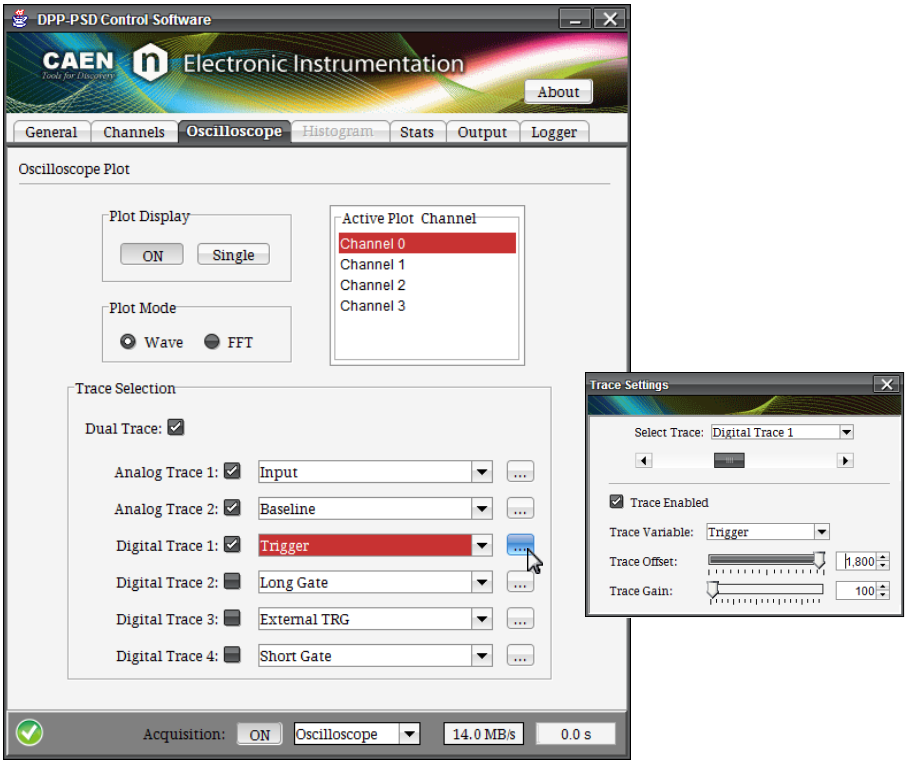


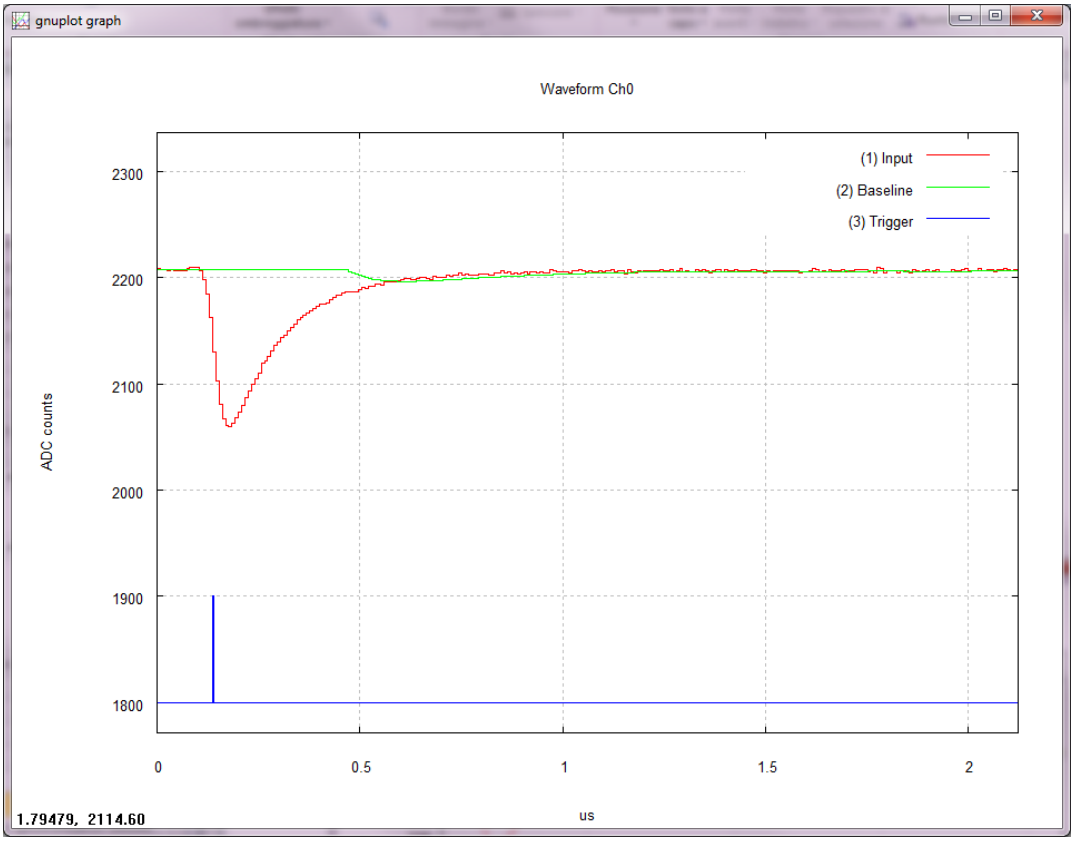
Path8: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: Disable Software Trigger by the "**ON/OFF**" button. You should observe the board going on self-triggering.

Path9: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

Action2: Enable **DIGITAL TRACE 1** and select "**Trigger**". Press the "**…**" button and use the options in the "**Trace Settings**" window to set the proper digital offset and gain to apply to the trace.





You can look at the plot if the trigger is properly issued.

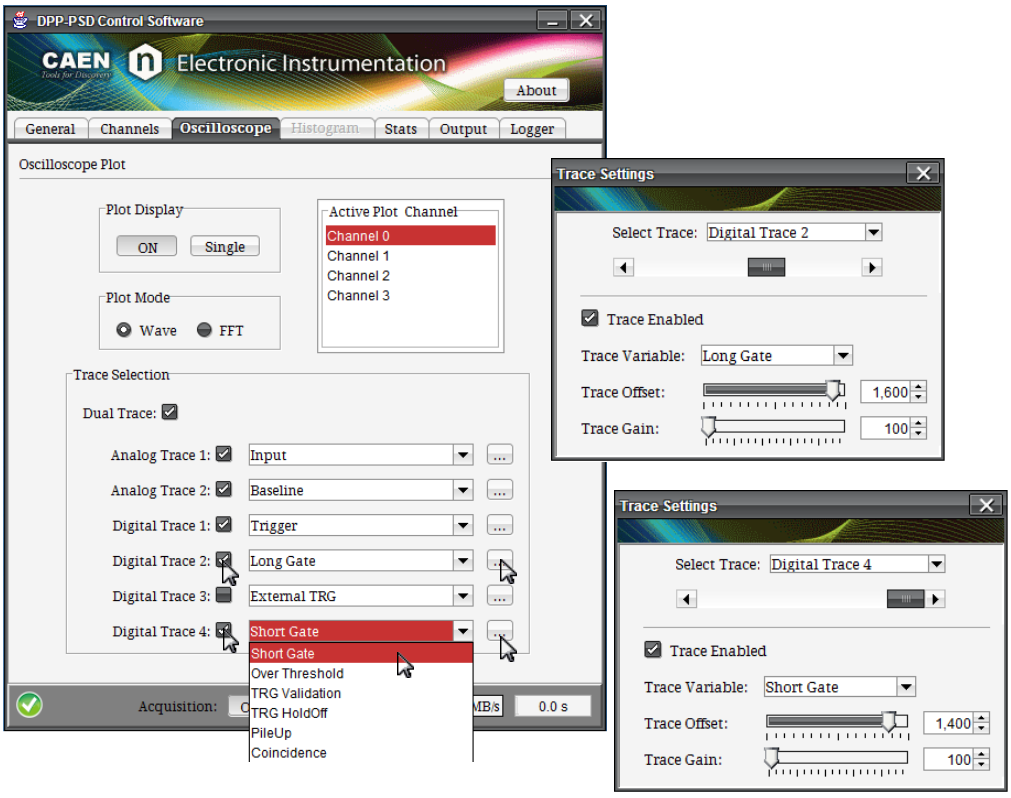
5. Set the parameters for the charge integration (gate offset, short gate, long gate)

Setting the SHORT GATE and the LONG GATE widths enables the firmware to integrate the input pulse and calculate the charges Q_{short} and Q_{long}. We will increase the GATE width to integrate the whole width of the signal [1]. First enable the gate visualization in the oscilloscope plot.

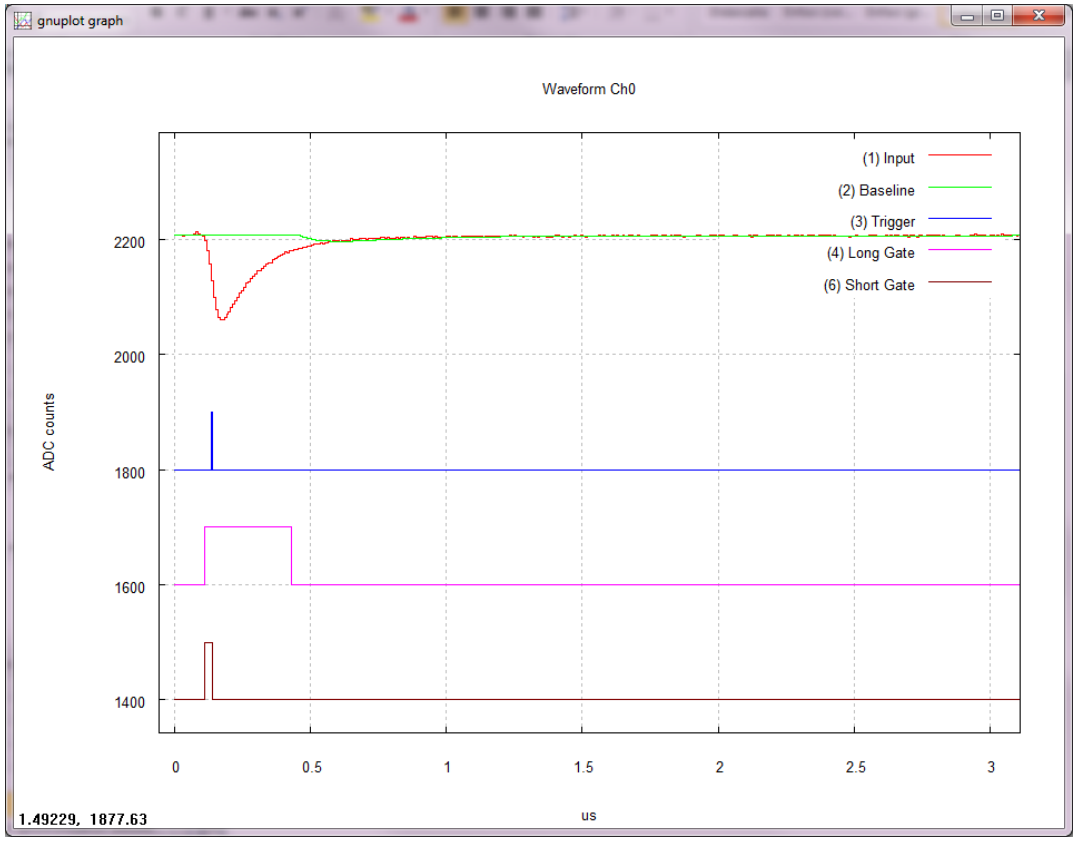
Path1: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

Action1: Enable **DIGITAL TRACE 2**, **"Long Gate"**, and enable **DIGITAL TRACE 4**, selecting "**Short Gate**" (i.e. DIGITAL TRACE 3 in case of 751 series).

With the default values of short and long gate the istogram plot will appear as in Fig.



[1] In **[RD2]**, a configuration of such parameters is reported for a typical Neutron-Gamma discrimination measurement with the BC501-A detector.


gnuplot graph
Waveform Ch0
(1) Input
(2) Baseline
(3) Trigger
(4) Long Gate
(6) Short Gate
ADC counts
2200
2000
1800
1600
1400
0
0.5
1
1.5
2
2.5
3
us
1.49229, 1877.63

Path2: Tab **CHANNELS** → Section **DPP SETTINGS**

Action1: First adjust the **GATE OFFSET** value in the box menu. This value corresponds to the number of ns the gate will start before the trigger. Indeed the input signal is delayed by the "**Pre-Trigger**" value, so that the gate can start before the trigger. Gate Offset and Pre-Trigger must follow the relation:

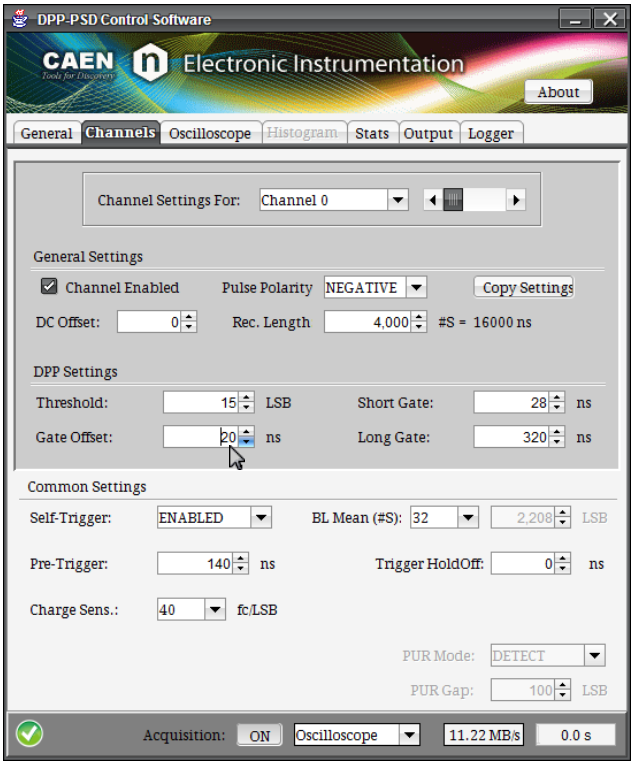
$$Gate - Offset \leq Pre - Trigger - 32ns$$

We set the gate offset value to 20 ns.

For 751 series

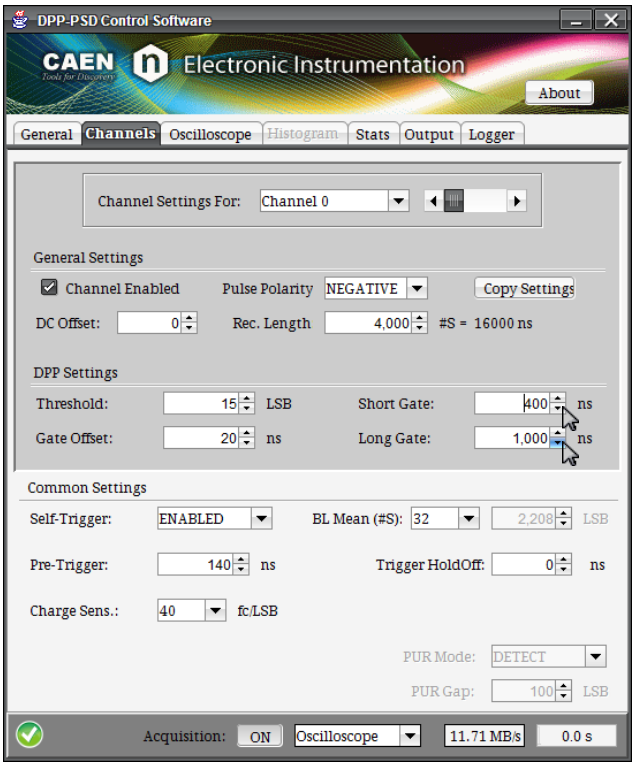
$$Gate\_Offset \leq Pre\_Trigger - 8ns$$

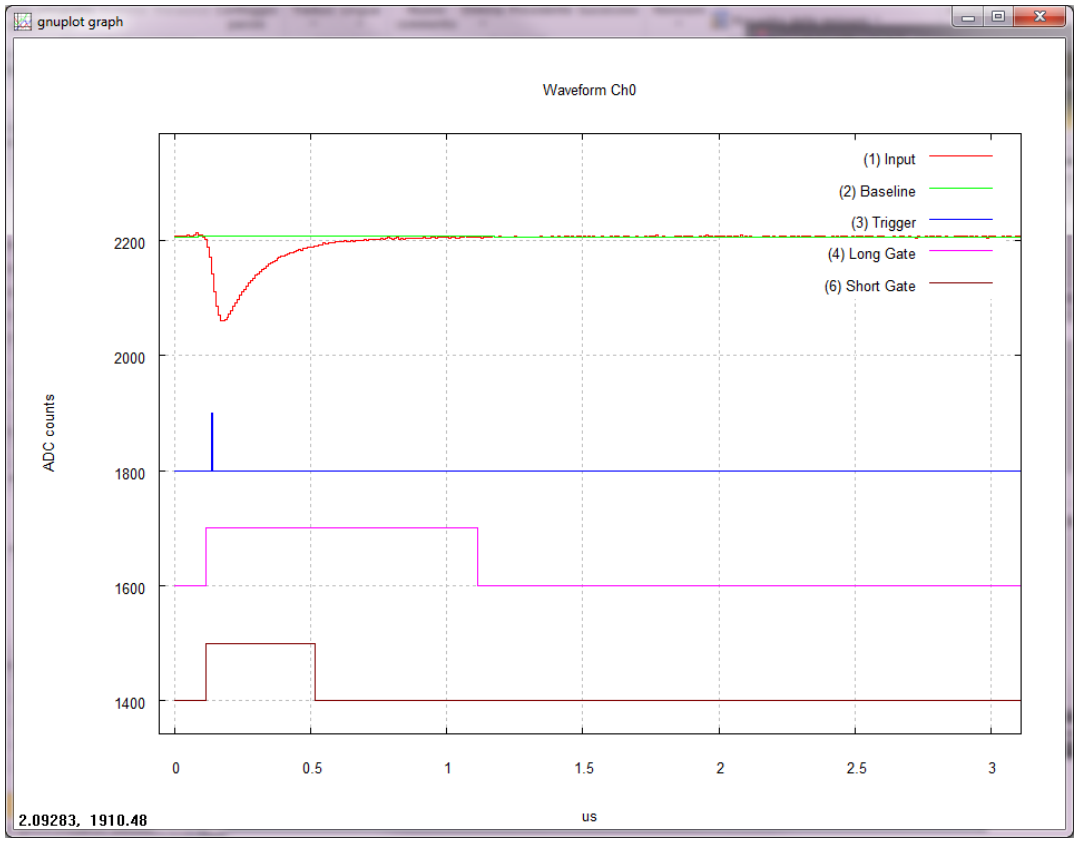
Note: When switching to the histogram mode the Pre-Trigger value is automatically set to the minimum allowed, i.e. Gate-Offset + 32 ns for 720 series, and Gate-Offset + 8 ns for 751 series.



Action2: Set the Short Gate and Long Gate widths to the proper value according to the input signal. In this example we choose 400 ns for the Short Gate and 1000 ns for the Long Gate. The following relation must be satisfied:

$$Gate - Offset \leq Short\_Gate \leq Long\_Gate$$





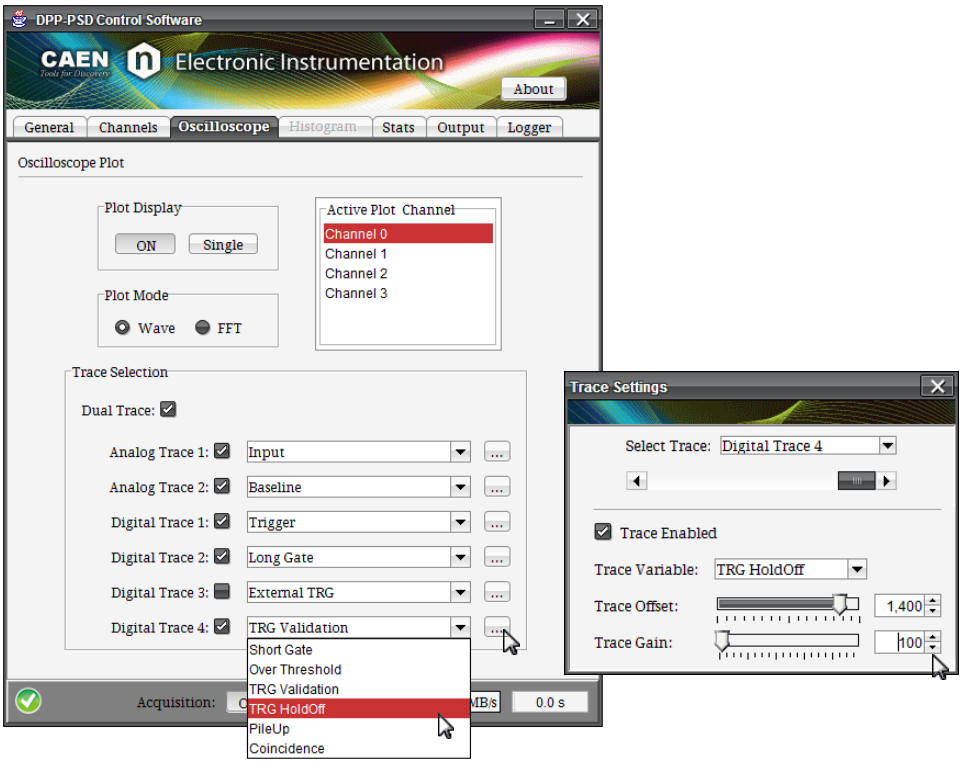
You can see that the baseline is now frozen for the whole signal width.

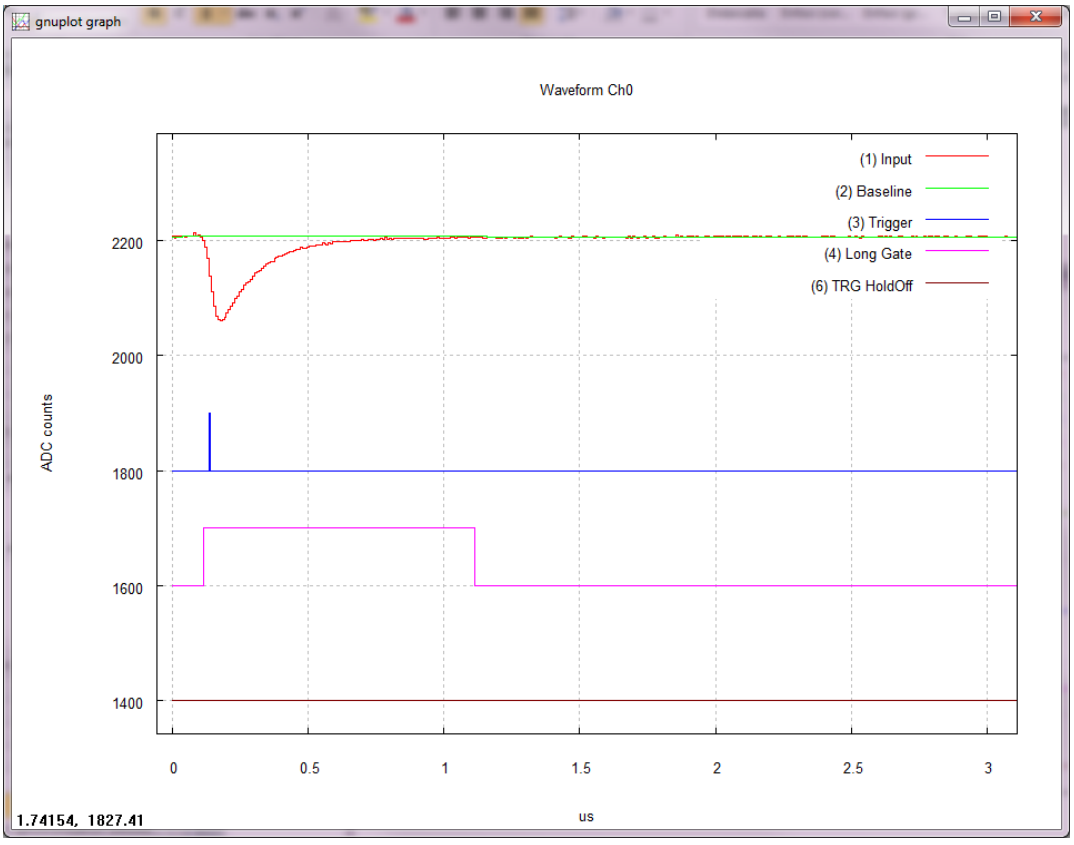
6. Set the Trigger Hold-Off and Pre-Trigger parameters.

The Trigger Hold-Off enables a time window after the trigger, where any other triggers are inhibited. Make sure to set the proper value of the Trigger Hold-Off according to your signal width, especially in case of high frequency signals.

Path1: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

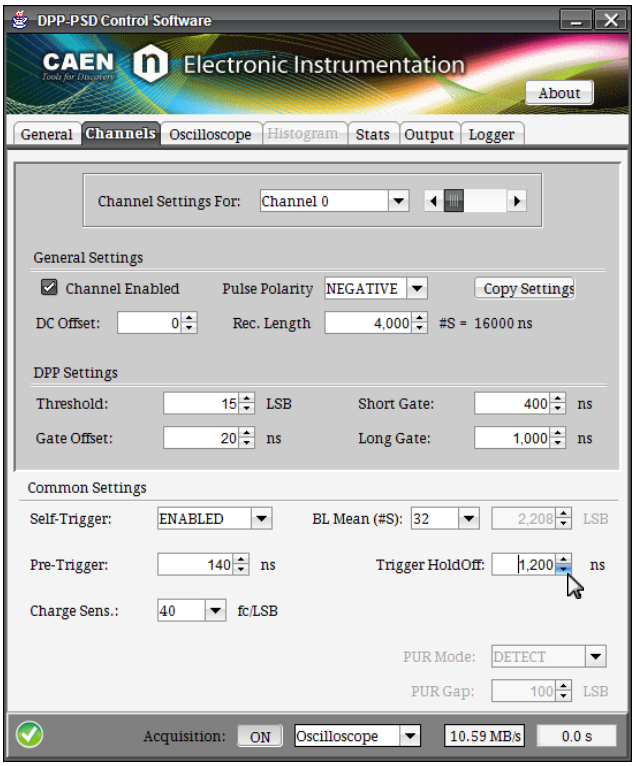
Action1: Enable **DIGITAL TRACE 4**, and select "**TRG HoldOff**" in the menu.

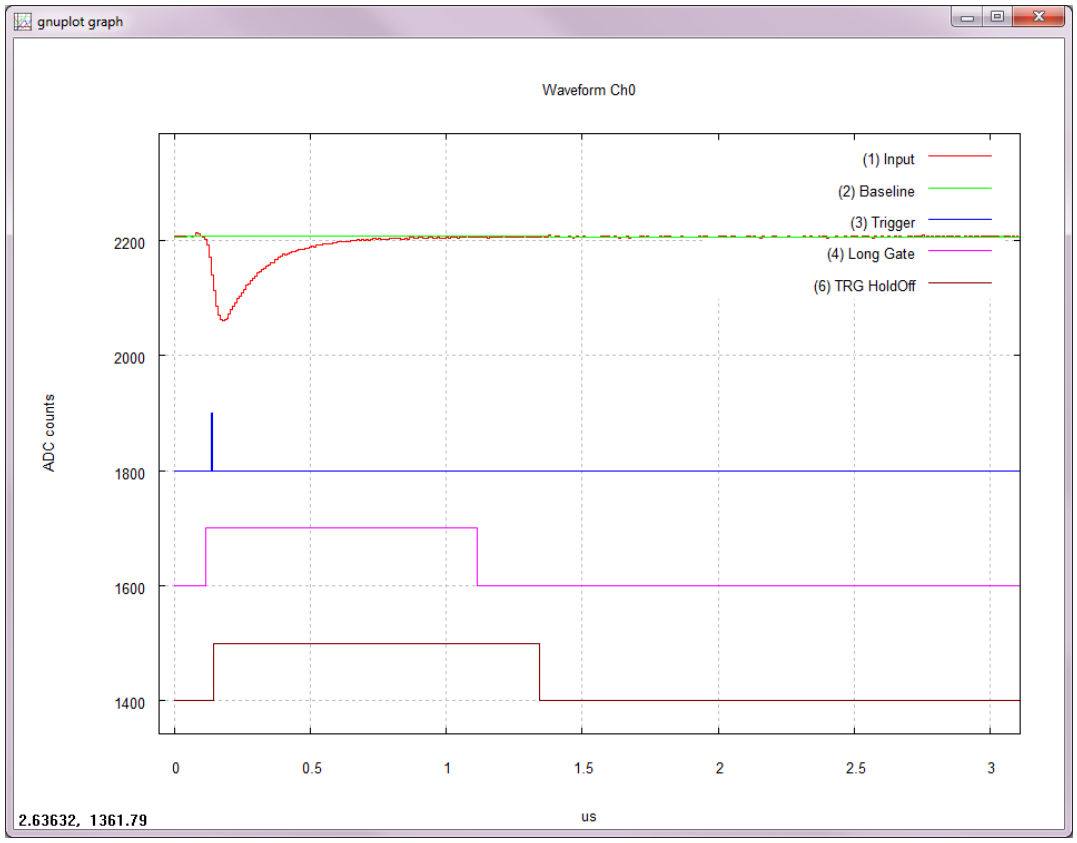




Path2: Tab **CHANNELS** → Section **COMMON SETTINGS**

Action1: Set the **TRIGGER HOLD-OFF** value in the box menu. The Trigger Hold-Off goes in steps of 8 ns. We set the Trigger Hold-Off value to 1200 ns.





Action3: Stop the oscilloscope mode plotting through the **PLOT DISPLAY** "**ON/OFF**" button.

7. Switch to Histogram mode, plot the Energy Spectrum and the 2D-plot of Energy vs PSD.

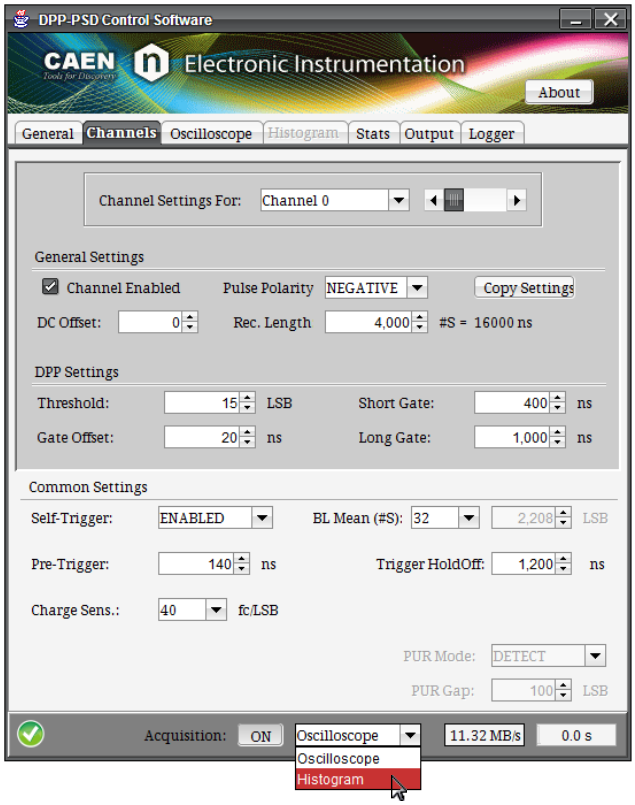
Once the DPP-PSD parameters has been properly set, it is possible to plot the Energy Histogram of the gamma-ray source. For a complete Neutron-Gamma discrimination, the software allows for a 2D-plot of Energy vs PSD . The PSD parameter is calculated as reported in Chapter **2**.

Note: The DPP-PSD Control Software calculates every histogram by post processing the data coming out from the Digitizer (i.e. the list of events being Time Stamp, Q_{short}, Q_{long} and PSD).

Note: In the Oscilloscope acquisition mode it may happens that a lot of data are processed and transmitted, so that the Digitizer memory can go full and some data are lost. You can check it through the red "**BUSY**" LED on the Digitizer front panel. Usually this happens when you have high frequency input signals, and/or the "**RECORD LENGHT**" window is big. Conversely in the Histogram acquisition mode, the overall data throughput of the Digitizer is significantly reduced since only few data are transmitted (Trigger Time Stamp and Charge), and the busy state can disappear.

Path1: Any Tab.

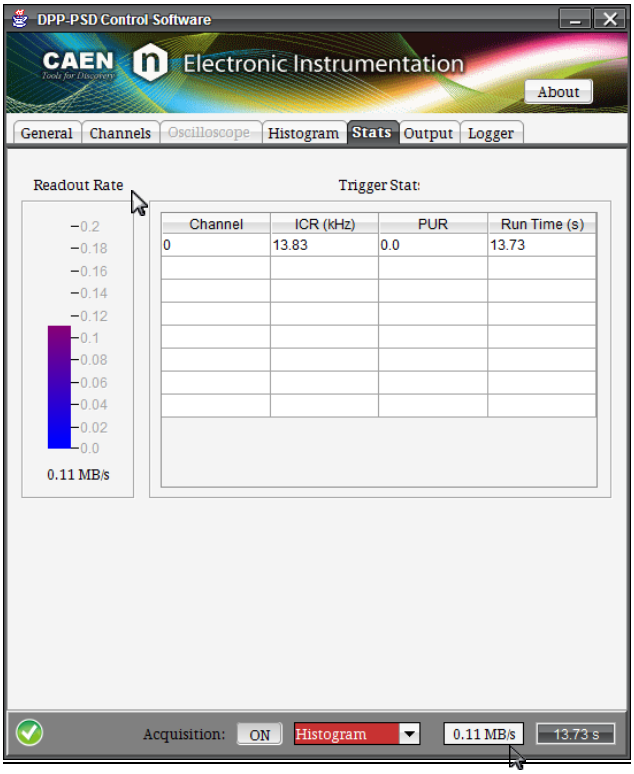
Action1: set **ACQUISITION MODE** on "**Histogram**" using the scroll box menu in the deep grey common bar at the bottom of the GUI.



You can check that the readout rate is significantly reduced

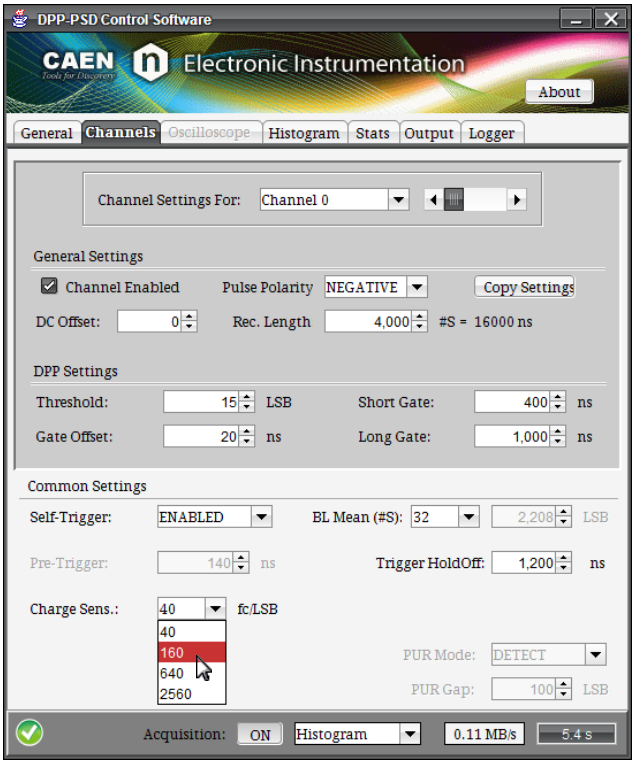
Path2: Tab **STATS**

Action1: check the readout in the left banner of the tab, under **READOUT RATE**. The same parameter is written in the bottom box, common to all tabs.



Path3: Tab **CHANNELS** → Section **COMMONS SETTINGS**

Action1: set **CHARGE SENS** on "**160**" in the box menu. The charge sensitivity allows to rescale the signal charge. This is useful especially when the charge exceeds the full scale range (0xFFFF in 16 bits). In case of saturation only a spike corresponding to the overflow events is visible in the histogram plot.



Path4: Tab **HISTOGRAM** → Section **HISTOGRAM PLOT**

Action1: set "**channel 0**" in the **CHANNELS** list box.

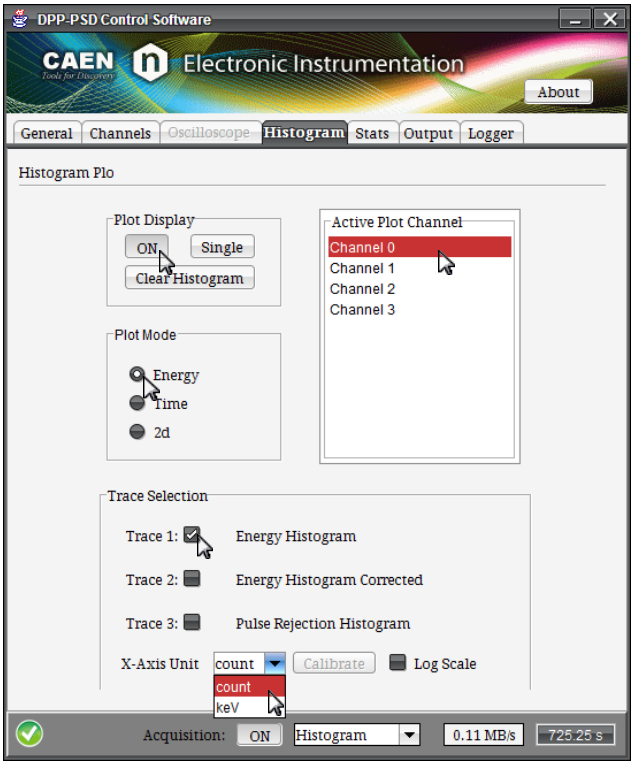
Action2: check "**Energy**" as **PLOT MODE**.

Action3: check "**Energy Histogram**" as **TRACE 1**:

Action4: select "**count**" as **ENERGY X-AXIS**. This means that the X-axis are the bin numbers in ADC counts.

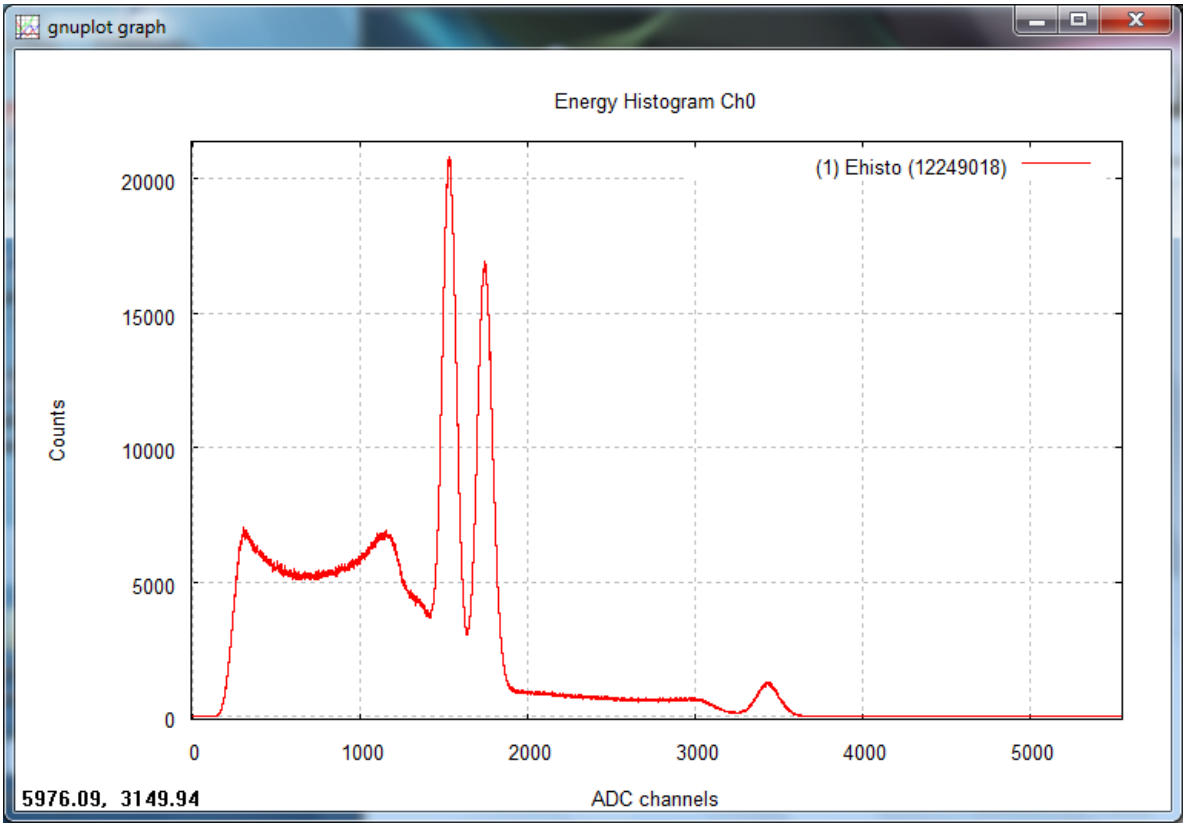
Action5: Press the **ENERGY PLOT** "**ON/OFF**" button to issue the energy histogram continuous plotting.

- **OFF** = Plot displaying is off.
- **ON** = Plot displaying is on.



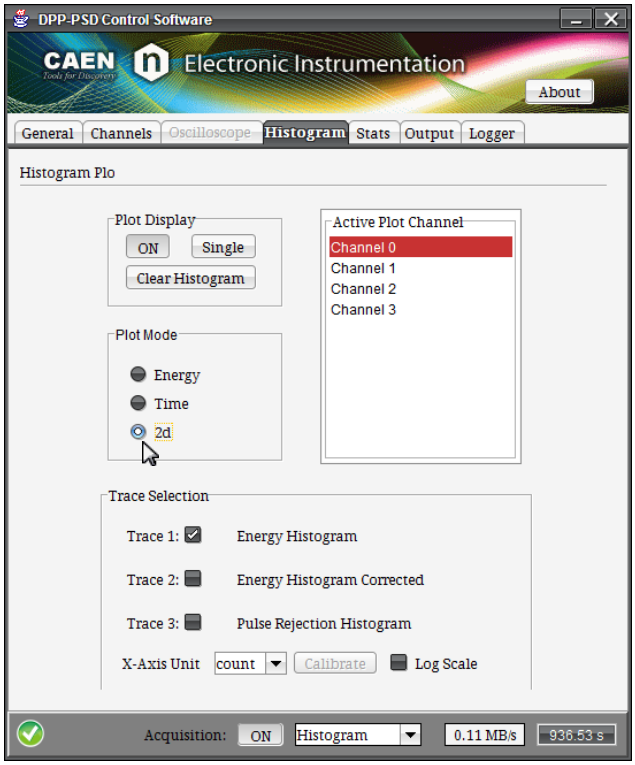
The ^{60}Co energy spectrum shows the typical two relevant peaks which should correspond to 1.33 MeV and 1.17 MeV.

Note: The DPP-PSD Control Software provides only the energy histogram related to Qlong.

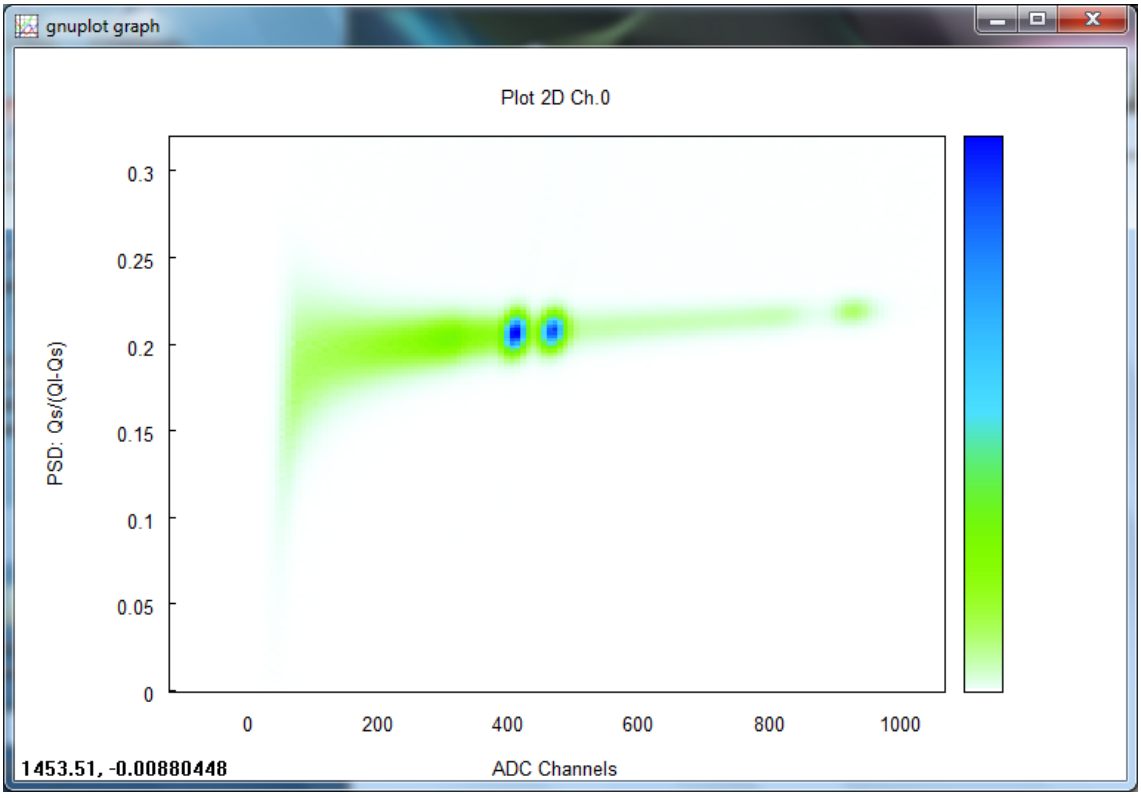


Path3: Tab **HISTOGRAM** → Section **HISTOGRAM PLOT**

Action1: check "**2D**" as **PLOT MODE**.



The 2D-plot is the scatter plot of the PSD parameter (Y-axis) vs the pulse Energy Q_{long} (X-axis). In the following picture we can clearly see the two lobes corresponding to the ^{60}Co peaks



Note: The positive Z-axis (vertical and pointing up) is represented by the chromatic scale on the right. Going to light green to deep blue, the more the colour is deep, the more the correspondent histogram value is high.

In a Neutron-Gamma experiment the 2D scatter plot (**Fig. 5.5**) will show two distinctive areas, one for Neutron (top) and one for gamma (bottom). The discrimination among the two sources is easier if they are well separated and do not overlap. **[RD2]** gives a reference method to quantify the separation of the two areas.

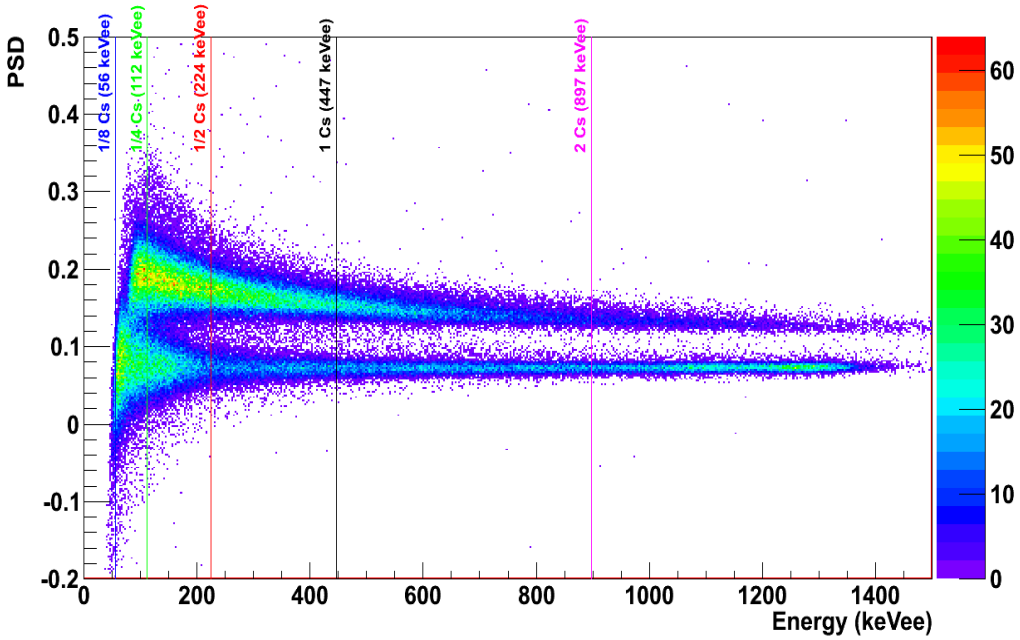


Fig. 5.5: 2D scatter plot of PSD parameter vs Energy in a neutron-gamma application [RD2].

8. Generate the output file and save the Energy Histogram-plot data.

The steps below explain how to save the List file (Time Stamp and Charge) by generating an output file on the host station disk.

Path1: Tab **OUTPUT** → Section1 **OUTPUT**

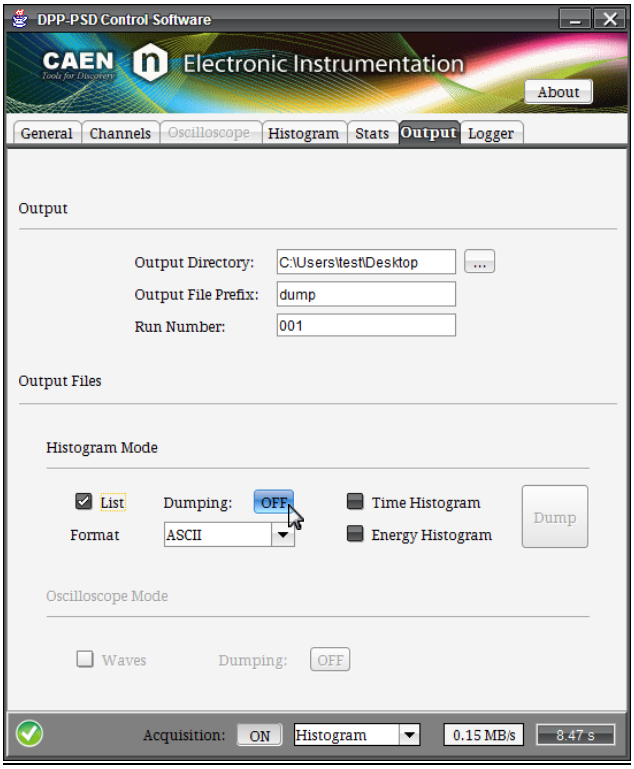
Action1: use the **OUTPUT DIRECTORY** "**…**" button to browse a specific destination folder where to save the output file on the host station; in the example we use the "**Desktop**" folder. If no destination is selected, data will be saved into the user *home* folder.

Action2: in the **OUTPUT FILE PREFIX** text box write the name of the prefix for the output file ("**dump**", in this case) and press "**Enter**" on your keyboard. If no prefix is written by the user, the program generates the output file with a default prefix.

Action3: in the **RUN NUMBER** text box write the run number. This number automatically increase by one unit when you start a new acquisition through the ON/OFF Acquisition button.

Path2: Tab **OUTPUT** → Section2 **OUTPUT FILES**

Action4: click on the **LIST** checkbox, select the data writing format between ASCII and BINARY, and press the **ON/OFF** button to start/stop the output file writing.



Action5: press the **ACQUISITION** "**ON/OFF**" button to start/stop the acquisition session.

Action6: check the file saved in the selected destination folder. The file format for the current acquisition data is: **dump_001_ls_0.dat**, where "**dump**" is the chosen prefix, "**ls**" stands for list, "**001**" is the run number, and "**0**" is the channel number. The file is a 4-column file where the first column is the time stamps of each triggered event, the second is the Q_{short}, the third is the Q_{long}, and the fourth is the PSD. In case of Binary format the PSD is omitted. Binary writing is particularly efficient for high readout throughput.

6 Coincidences and Synchronization

The DPP-PSD firmware allows for coincidences among different channels and synchronization of different boards.

Coincidences

Acquiring coincident events from different channels is a common task in physics. Through the DPP firmware each channel of the digitizer can trigger independently from the others, and generate a "trigger request". All the trigger requests can be sent to the common "ROC FPGA" (see **Fig. 2.1**) for the coincidence evaluation. The ROC can be programmed to look for triggers within a programmable window, through the Individual Trigger Logic (ITL) that can perform the logic operation of AND, OR, or Majority. When the coincidence condition is met, the ROC sends back a "trigger validation" signal, one per channel. The coincidence logic is individual, so that it is possible to program different coincident conditions for each channel.

The trigger validation enables the data saving into the memory buffer. In this way the channel uses its local trigger for the event building (time stamp, gate, etc..) but only those events having the validation are saved into the memory.

More information and detailed instructions on how to make coincidences among channels of the same board can be found in **[RD3]**.

Synchronization among different boards

In cases when multi-board systems are involved in the experiment, it is necessary to synchronize different boards. In this way the user can acquire from N boards with Y channel each, like if they were just one board with (N x Y) channels.

The main issue in the synchronization of a multi-board system is to propagate the sampling clock among the boards. This is made through input/output daisy chain connections among the digitizers. One board has to be chosen to be the "master" board that propagates its own clock to the others. A programmable phase shift can adjust possible delays in the clock propagation. This allows to have both the same ADC sampling clock, and the same time reference for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards is aligned to the same absolute time.

There are several ways to implement the trigger logic. The synchronization tool allows to propagate the trigger to all boards and acquire the events accordingly. Moreover in case of busy state of one or more boards, the acquisition is inhibited for all boards.

Refer to **[RD7]** for more details on how to synchronize CAEN digitizers.

7 Software Interface

Introduction

The DPP-PSD Control Software is an application that manages the communication and the data acquisition from digitizers where the DPP-PSD firmware is installed. The software allows the user to select proper communication and DPP settings. Waveforms and histograms can also be plotted in real time for one channel at a time (as described in the

GUI Description paragraph).

Note: DPP-PSD Control Software is not provided with data analysis features and it is developed to work both with 720 and 751 Digitizer series.

Block Diagram

The DPP-PSD Control Software (**Fig. 7.1**) is made by different parts: there is a user-friendly java *GUI* that allows to easily configure all the relevant parameters for the DPP-PSD acquisition. The GUI directly handles the Acquisition Engine (*DPPRunner*) through run time commands and generates a textual configuration file that contains all the selected parameters values. This file is read by DPPRunner, a C console application that programs the Digitizer according to those parameters. DPPRunner can also start/stop the acquisition and manage the data readout. Data (both as waveforms, and list of time stamps and energies/time) can be plotted using the external plotting tool *gnuplot*, or saved to output files and analyzed offline.

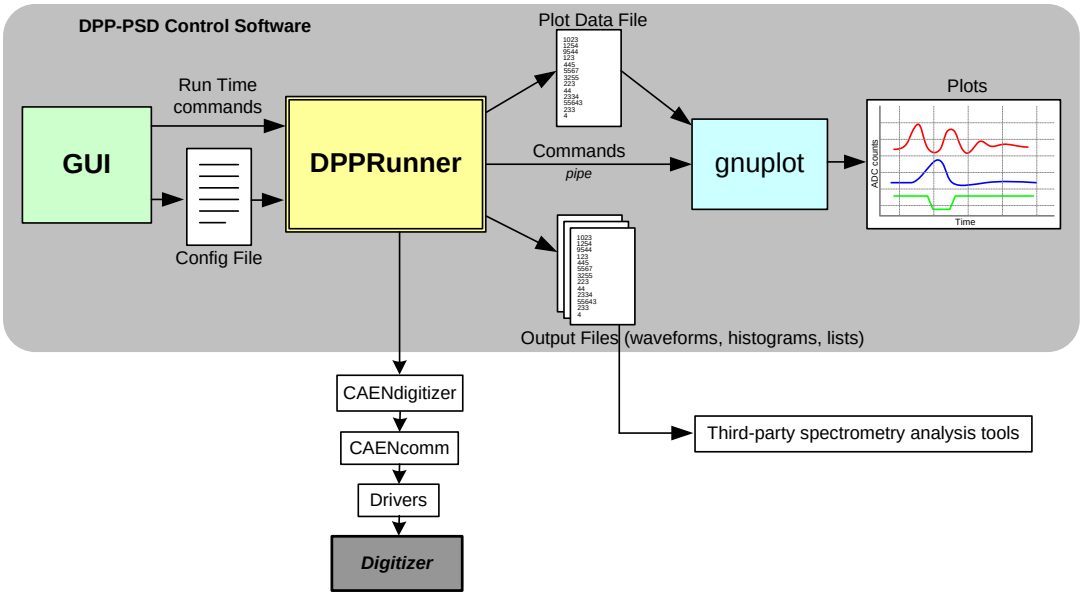


Fig. 7.1: The DPP-PSD Control Software block diagram

Libraries and Driver

CAEN provides the drivers for all the different types of physical communication channels featured by the DPSD, both for Windows and Linux OS:

- **USB 2.0**. The driver installation package is available on CAEN website in the 'Software/Firmware' area at the Digitizer or V1718 page.
- **CONET Optical Link**, managed by the A2818 PCI card or A3818 PCIe card. The driver installation package is available on CAEN website in the 'Software/Firmware' area at the A2818 or A3818 page.

- **VME bus**, accessed by the V1718 and V2718 bridges.

Refer to each board User Manual for driver installation instructions. Concerning the installation of USB drivers in Windows OSs for desktop digitizers, refer also to **[RD5]**.

In addition a set of C and LabView libraries are available:

- **CAENVMELib** is a set of ANSI C functions to program the use and the configuration of the CAEN Bridges V1718/VX1718 (VME-USB2.0 Bridge), V2718/VX2718 (VME-PCI Optical Link Bridge), A2818/A3818 (PCI CONET Controller).

  The CAENVMElib installation package is available on CAEN website in the 'Download' area at the CAENVMELib Library page.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, making the libraries and applications that rely on the CAENComm independent from the physical layer. CAENComm requires CAENVMELib library (access to the VME bus) even when the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.

  The CAENComm installation package is available on CAEN website in the 'Download' area at the CAENComm Library page.

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware, as it happens for the DPP-PSD. The CAENDigitizer library is based on the CAENComm which is based on CAENVMELib, as said above. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

  The CAENDigitizer installation package is available on CAEN website in the 'Download' area at the CAENDigitizer Library page.

Note: For Windows only, all libraries are automatically installed through the standalone DPP-PSD Control Software Setup tool. Linux users have to install them in the order described above.

CAENComm (and so the CAENDigitizer) supports the following communication ways (see also **Fig. 7.2**):

PC → USB → Digitizer DT5720 (DT5751) or N6720 (N6751) - Desktop and NIM models

PC → USB → V1718/VX1718 → VME → Digitizer V1720/(V1751)/VX1720/(VX1751) - VME models

PC → PCI (A2818) → CONET → Digitizer x720 (x751) - All models of the 720 (751) series

PC → PCI (A2818) → CONET → V2718/VX2718 → VME → Digitizer V1720/(V1751)/VX1720/(VX1751) - VME models

PC → PCIe (A3818) → CONET → Digitizer x720 (x751) - All models of the 720 (751) series

PC → PCIe (A3818) → CONET → V2718/VX2718 → VME → Digitizer V1720/(V1751)/VX1720/(VX1751) - VME models

CONET (Chainable Optical NETwork) indicates the CAEN proprietary protocol for communication on Optical Link.

Note: CAENDigitizer library for LabVIEW (only for Windows OS) has been released. CAENDigitizer LabVIEW needs the *labview* subfolder of CAENComm to be installed. Please, refer to **[RD8]** for detailed information.

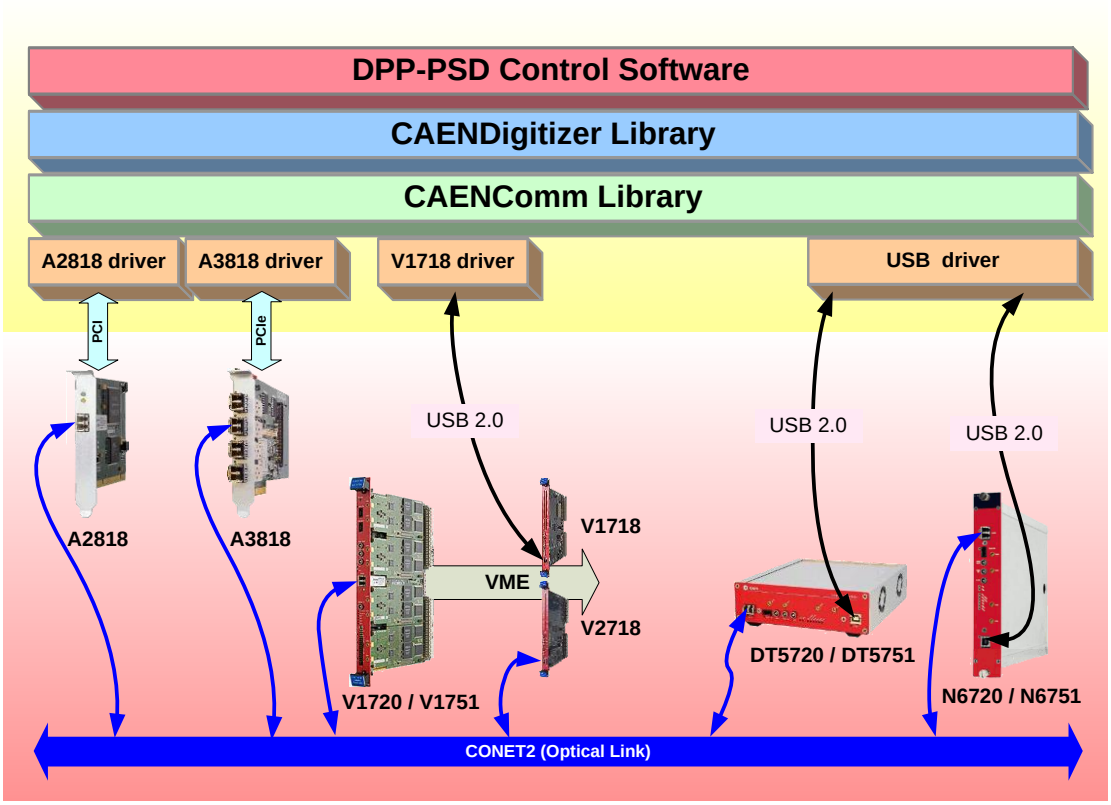


Fig. 7.2: Libraries and drivers required for the DPSD system

Installation

In order to manage with DPHA system, the host station needs either Windows or Linux OS, and the third-party software **Java Runtime** Environment 6 or later (trademark of Oracle, Inc, downloadable from http://www.java.com). Linux users must also take care of proper installation of **gnuplot** graphical tool, as well as of **CAEN Libraries**. The latter can be downloaded from CAEN website (login required before to download).

- **Make sure** that your **hardware** (Digitizer and/or Bridge, or Controller) is **properly installed** (refer to the related User Manual for hardware installation instructions).
- **Make sure** you **have installed** the **driver** for your OS and for the communication to be used. Driver installation packages are downloadable on CAEN website (**login required before to download**) as reported in the **Libraries and Driver** paragraph.

CAEN provides the full installation package for the **DPP-PSD Control Software** in a **standalone version** for **Windows OS**. This version installs all the binary files required to directly use the software (i.e. no need to install the required CAEN libraries in advance). The installation package for **Linux OS** needs other libraries to be installed apart.

- **Download the specific DPP-PSD Control Software installation package** for your OS from CAEN website in the 'Download' area at the DPP-PSD Control Software page (**login required to download**).
- **Extract files** in your host.

For Linux users:

- **Click on the red link** above the DPP-PSD Control Software package to download the required CAEN Libraries.
- **Install the libraries** in the following order:
    1. CAENVMELib
    2. CAENComm
    3. CAENDigitizer

  The **installation instructions** can be found in the **README file** inside each library folder.
- **Install** the **DPP-PSD Control Software** according to the **installation instructions** of the **Setup/Linux/Readme.txt file** inside the program folder. **Launch** the Control Software typing **DPP-PSD_ControlSoftware**

For Windows users

- **Launch** the **DPP-PSD Control Software installer** and complete the Installation Wizard
- **Run** the **DPP-PSD Control Software GUI** by one of the following options:
    1. The **Desktop icon** for the program
    2. The **Quick Launch** icon for the program
    3. The **.bat file** in the main folder from the installation path on your host.

GUI Description

The Graphical User Interface (GUI) is composed of seven (7) Tabs, each one divided in one or more sections. In the different tabs there are all the commands needed to manage the connections, to set the board and the channel parameters, and to control the acquisition.

A **Common Bar** lays at the bottom of the GUI (**Fig. 7.3**), being visible from any active tab. It contains:

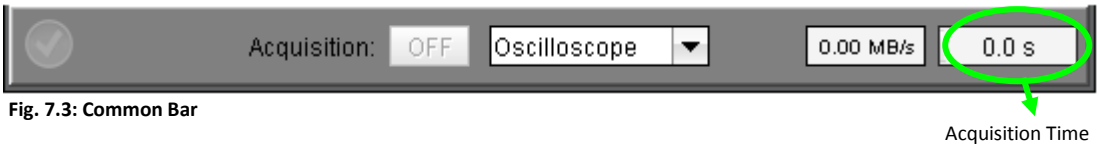


Fig. 7.3: Common Bar

- **"Acquisition" button:** starts and stops the acquisition session.
- **"Acquisition Mode" menu:** sets the *"Oscilloscope"* or the *"Histogram"* acquisition mode.
- **"Readout Rate" box:** displays the data throughput rate during the acquisition.
- **"Time acquisition" box:** displays the time duration (sec) of the acquisition. This works only in the Histogram Mode. The acquisition will automatically stop if a "*non zero*" value is set for the Stop Time parameter.
- **"Connection" icon:** updates itself according to the connection status:

Icon	Status
	Disconnected
	Connection OK
	Connection Error

Tab. 7.1: Table of the Connection icon values.

1. The Tab "General"

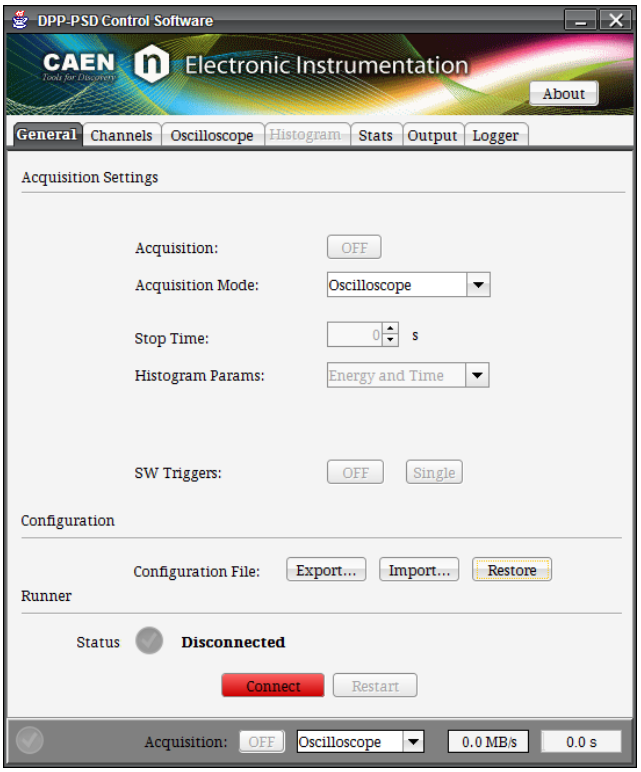


Fig. 7.4: Tab "General"

The **General Tab** is divided into three sections: **Acquisition Settings**, **Configuration,** and **Runner**.

The **Acquisition Settings** section includes:

- **"Acquisition" button:** starts and stops the acquisition:
  - **OFF** = acquisition is off
  - **ON** = acquisition is on

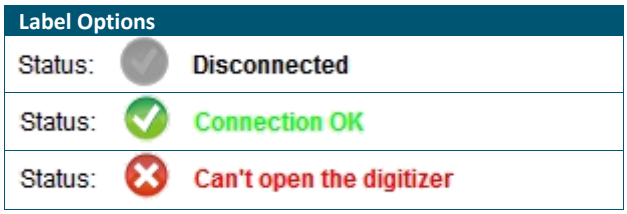
  It is duplicated in the Common Bar.
- **"Acquisition Mode" menu:** selects between the *"Oscilloscope"* mode, where the raw waveforms can be visualized and saved, and the *"Histogram"* mode, where the spectra can be visualized and saved. This command is duplicated in the Common Bar.
- **"Stop Time" box:** sets the value (in seconds) for the Real Time acquisition in Histogram mode. At the end of the fixed time (visualized in the "Acquisition Time" window of the Common Bar) the acquisition is automatically stopped. Set Stop time to *"0"* for an infinite acquisition time.
- **"Histogram Params" menu:** selects the data that the Digitizer provides for the *"Histogram"* acquisition mode (Energy only, Energy and Time).
- **"SW Triggers" buttons:** start/stop a software trigger input from the computer to the board in a continuous ("ON/OFF") or single-shot ("Single") way.

The **Configuration** section includes:

- **"Configuration File" buttons:** store (*"Export"*) and recall (*"Import"*) the configuration of the software and the parameters for the acquisition. The user can so easily manage the different parameters during different acquisitions. *"Restore"* resets online the parameters to their default values.

The **Runner** section shows the status of the connection between the board and the Control Software. It is made of:

- "**Status**" **label**: shows the status of the connection:



  It is duplicated in the Connection window.

- **"Connect" button:** opens the Connection window (**Fig. 7.5**).

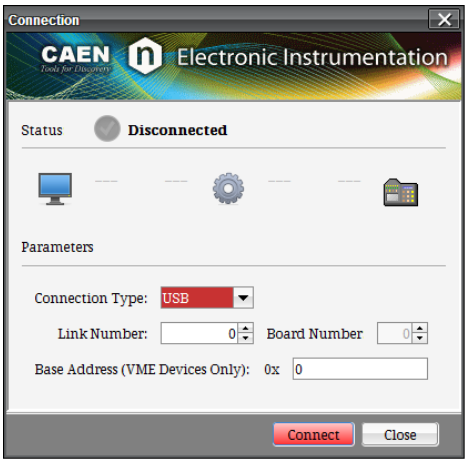


Fig. 7.5: Connection Window

  In this window the connection parameters can be set:

  - **"Connection Type" menu:** selects between *"USB"* or *"OPTLINK"* according to the way the board is connected to the PC.
  - **"Link Number" box:** sets the number of the port used in the connection and is valid for multiple boards connection.
  - **"Board Number" box:** indicates the number of the desired board in a Daisy chain connection between different boards.
  - **"Base Address" box:** for VME boards only, sets the VME base address. Set "0" for direct connection.

  More details about the connection parameters can be found in **[RD1]** and **[RD8]**.

As a reference, in **Tab. 7.2** there are shown some connection examples involving the DPP-PSD supporting boards.

Connection chain	Type	Link	Slave	Address
PC –> **USB** –> DT5720 (DT5751)	USB	0	0	0
PC –> **USB** –> V1718 –> **VME** –> V1720 (V1751)	USB	0	0	32100000*
PC –> **PCI** –> A2818 –> **CONET** –> N6720 (N6751)	PCI	0	0	0
PC –> **PCI** –> A2818 –> **CONET** –> V1720 (V1751)	PCI	0	0	32100000*
PC –> **PCI** –> A2818 –> **CONET** –> V1720 (V1751)**	PCI	0	1	0
PC –> **USB** –> DT5720 (DT5751)***	USB	1	0	0

Tab. 7.2: Examples of connection settings

(*) For the correct VME base address to be used, please refer to the Digitizer's User Manual.
*(**) The VME Digitizer is intended to be part of a Daisy chain (see the examples at the end of **[RD1]**)*
*(***) It is supposed that at least two USB ports are used by the PC to communicate with digitizers (see the examples at the end of **[RD8]**).*

The connection is handled by:

- **"Connect" button:** establishes the connection. A green sign will confirm the correct connection.
- **"Close" button:** closes the connection window.

When a connection is established, in the Runner section the **"Status"** field shows the *"**Connected**"* value.

- **"Restart" button:** restarts the software causing the board to reset and to reprogram with the actual parameters; the communication is unaffected.

Note: Every time you connect the Control Software to a 751 series digitizer, the latter makes an internal calibration of the ADCs, which is strongly dependent on the ADC temperature itself. For this reason check that the ADC temperature is stable by reading the temperature registers (address 0x1nA8, where n is the channel number). The temperature can take some minutes to level off.

2. The Tab "Channels"

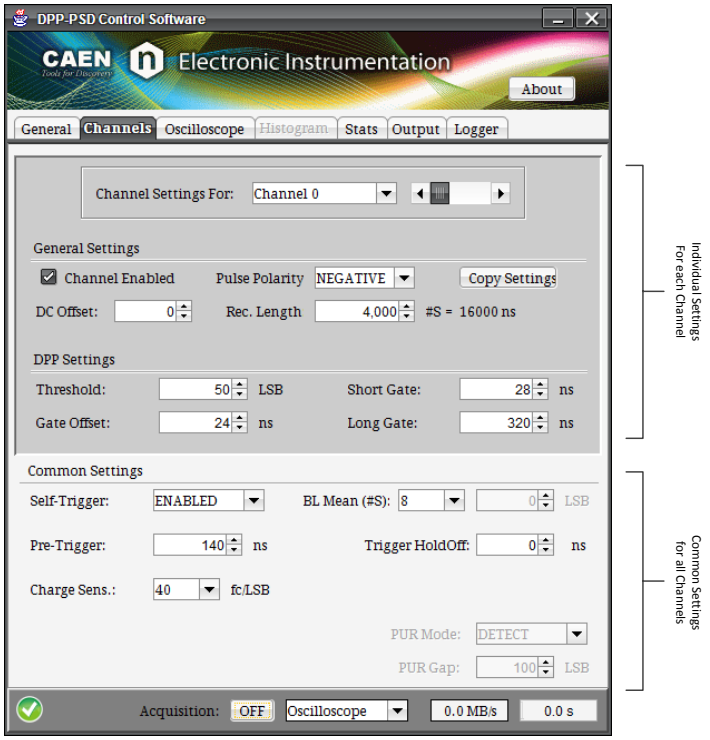


Fig. 7.6: Tab "Channels"

The **Channels Tab** is the core of the DPP-PSD Control Software where it is possible to set all the parameters required by the algorithm.

The tab consists in the **Channel Settings For** field with the sections: **General Settings**, **DPP Settings**, **Common Settings**. Through the **"Channel Settings For" menu** it is possible to select the channel which the parameters are referred to. The channels are selectable either through the drop-down menu or through the slider. Two macro areas can be noticed: the deep grey area for the individual settings of each channel, and the light grey area for the common settings valid for all channels. Once all parameters have been set for the current channel, it is possible to select another channel and a new configuration tab will be available.

The **General Settings** section includes the following commands:

- **"Channel Enabled" checkbox:** enables the selected channel to acquire data.
- **"DC Offset" box:** sets the value of the DC Offset applied to the channel, expressed as the percentage of the Full Scale Range. Allowed values range between -50% (Full negative) and +50% (Full Positive). The DC Offset is a DC value added to the input signal by the input stage of the Digitizer in order to fit the signal dynamic range to the ADC input dynamics. Theoretically, the value of 0 (DC Offset = "0") means that the input pulse DC level

is set at half of the ADC dynamics (e.g. 2048 counts for the 720 series and 512 counts for the 751 series). The value of "50" (DC Offset = "50") sets the DC level at the lower dynamics limit (i.e. 0 counts), while the value of "-50" (DC Offset = "-50") sets the DC level at the upper dynamics boundary (i.e. 4095 counts for the 720 series and 1024 counts for the 751 series). The real DC offset adjustment implemented in the DPP-PSD firmware is shown in **Fig. 7.7**: in order to preserve from saturation the input signals near the dynamics boundaries, setting the DC offset to -50 or +50 puts the signal baseline respectively a step up the upper boundary and a step under the lower boundary.

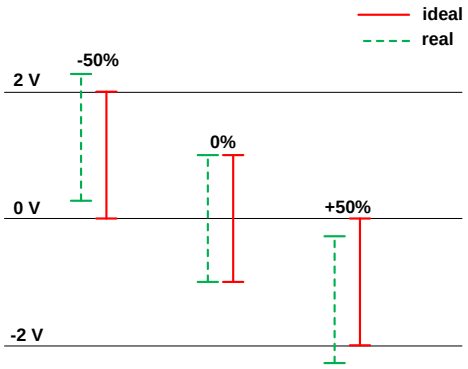


Fig. 7.7: Input signal DC offset adjustment description.

- **"Pulse Polarity" menu:** selects the polarity (NEGATIVE/POSITIVE) of the input signal to be processed by the DPP-PSD algorithm. The algorithm is internally designed to work with negative pulses. When the analog input pulses are positive, it is necessary to invert them before the DPP algorithm is applied; in this case, the option PULSE POLARITY = "Positive" enables the internal inversion of the pulse polarity. Note that the inversion is applied to the DPP algorithms only, while it doesn't affect the waveform recording (both plots and output files keep the original pulse polarity). With negative analog input pulses, use PULSE POLARITY = "Negative".
- **"Record Length" box:** selects the length of the acquisition window expressed in number of points (1 point = 4 ns for the 720 series and 1 ns for the 751 series). This is the number of saved samples of the waveform when the board is running in Oscilloscope Mode.
- **"Copy Settings" button:** copies the general settings of the current channel to other channels.

The **DPP Settings** section includes:

- "**Threshold**" **box:** sets the absolute value of the trigger threshold referred to the input pulse baseline. The value is expressed in LSB. The value in mV for 1 LSB can be calculated according to the board input range. For a digitizer of the 720 series, with 12-bit resolution and input range of 2 Volts, the LSB is:

  $$LSB = 2 / 2^{12} = 0.488 \text{ mV}$$

  While for a 2V input range and 10-bit resolution 751 series, 1LBS = 0.97 mV.
- "**Gate Offset**" **box:** sets the "*pre-gate*" parameter, i.e. the starting position of the long and short gates before the trigger signal. Values are expressed in ns and can vary in steps of clock units (i.e. 4 ns if 720 series, and 1 ns if 751 series).
- "**Short Gate**" **box:** sets the short gate width for the Q_{short} calculation. Values are expressed in ns and can vary in steps of clock units.
- "**Long Gate**" **box:** sets the long gate width for the Q_{long} calculation. Values are expressed in ns and can vary in steps of clock units.

  ⚠ **WARNING:** $Gate\_Offset \leq Short\_Gate \leq Long\_Gate$; this relation must be always true.

The **Common Settings** section includes:

- "**Self-Trigger**" **menu:** ENABLE/DISABLE the DPP *self-trigger* of each channel. When disabled, the DPP algorithm still generates the self-trigger (pulse auto trigger) with the programmed threshold, but the signal is propagated only to the TRG-OUT panel output and it is not used for the acquisition. In these conditions, the

acquisition is activated when an external trigger signal is sent to the TRG-IN panel input or by the combination of the other channel self-triggers.

- "**Pre-Trigger**" **box:** sets the portion of the waveform acquisition window to be saved before the trigger. Its value is expressed in ns. The following relations must be true.

$$Gate - Offset \leq \Pr e - Trigger - 32ns \text{ (for 720 series);}$$

$$Gate - Offset \leq \Pr e - Trigger - 8ns \text{ (for 751 series);}$$

Note: When switching to histogram mode the Pre-Trigger value is automatically set to the minimum allowed, i.e. Gate-Offset + 32 ns for 720 series and Gate-Offset + 8 ns for 751 series.

Note: For 751 series, the firmware allows to set negative values of pre-trigger as well, even if the DPP-PSD Control Software does not manage it. This can be enabled through the PRE_TRG register.

- "**Charge Sens**." **Menu:** sets the *charge sensitivity*, the weight of the LSB for the charge data (16 bit). For instance, if Q = 100 is read and Charge Sens. = 40 fC/LSB, the integrated charge is 4 pC. When the charge pulse exceeds the full scale range (0xFFFF), it is recommended to reduce the sensitivity in order to avoid saturation. The allowed values (fC/LSB) are:

  for the 720 series

  40, 160, 640, 2560;

  for the 751 series

  20, 40, 80, 160, 320, 640.

Note: The charge is integrated inside the FPGA over a 22-bit accumulator; the sensitivity defines the dividing factor (i.e. the right shift) of this accumulator to rescale the energy value before it is saved into the memory buffer.

- "**Baseline Mean**" **menu:** sets the number of samples used by the mean filter to calculate the input pulse baseline. Allowed values are:

  for the 720 series

  "Fixed", 8, 32, 128.

  For the 751 series

  "Fixed", 8, 16, 32 64, 128, 256, 512.

  The "Fixed" option enables the absolute baseline calculation.

- "**Baseline**" **menu:** sets the fixed value (in LSB) of the baseline when the "Fixed" value is selected in the "Baseline Mean" menu.
- **"Trigger Hold-Off" menu**: sets the time width of the trigger hold-off. The trigger hold-off starts with the trigger and corresponds to the time window where any other triggers are inhibited. It is expressed in steps of 8 ns for both 720 and 751 series. Accepted values are:

  0, 8, 16, 24, …, 8184.

- "**PUR Mode**" **menu** and "**PUR Gap**" **box:** (*to be implemented*).

3. The Tab "Oscilloscope"

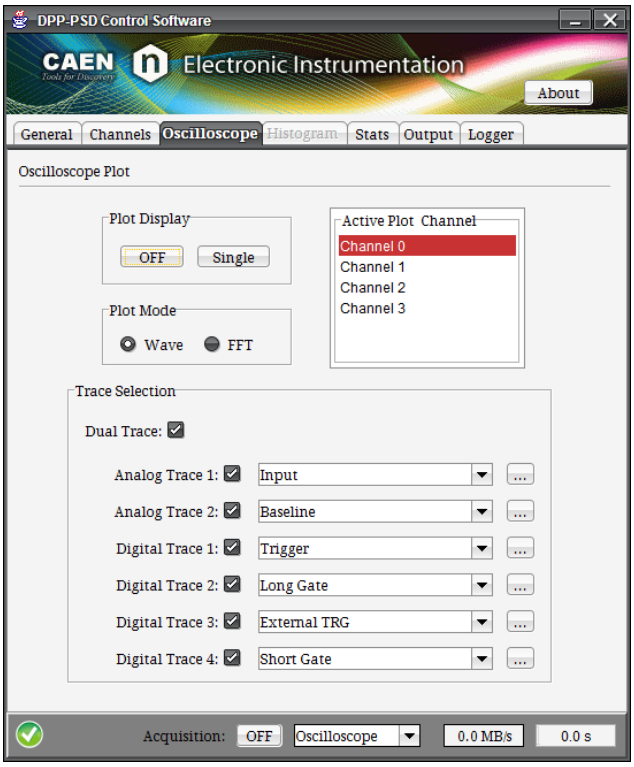


Fig. 7.8: Tab "Oscilloscope"

The **Oscilloscope Tab** consists only of the **Oscilloscope Plot** section, in which all the parameters for the signals visualization are set. A maximum of six (6) traces can be simultaneously displayed for 720 series, and five (5) for 751 series.

The **Oscilloscope Plot** section includes:

- **"Plot Display" buttons:** enable/disable the plot visualization and let the user visualize the waveforms continuously (*"ON/OFF"*) or in single shots (*"Single"*).
- **"Plot Mode" check-cells:** selects if the Waveform (*"Wave"*) or the Fast Fourier Transform (*"FFT"*) has to be visualized. The FFT option uses only the signal in "Analog Trace 1".
- **"Active Plot Channel" menu:** selects the channel whose signals are visualized. Only one channel at a time can be plotted. The selected channel has to be checked in the Channels Tab.
- **"Trace Selection" box** that includes:
    - **"Dual Trace" checkbox:** when enabled the two "Analog traces" are shown in the plot with half number of sampling. This is useful for choosing the right settings of the DPP parameters. When disabled, only the Analog Trace 1 is visualized with full number of samplings.
    - **"Analog Trace 1" menu:** selects the first analog trace to be visualized in the plot, that is the "*input*" pulse.
    - **"Analog Trace 2" menu:** selects the second analog trace to be visualized in the plot, that is the "*baseline*". Analog Trace 2 is not plotted if Dual Trace is disabled.
    - **"Digital Trace 1" menu:** selects the first digital trace to be visualized in the plot, that is the "*trigger*".
    - **"Digital Trace 2" menu:** selects the second digital trace to be visualized in the plot:

      For 720 series:

      "Long *Gate*".

      For 751 series:

      "Long Gate";

"Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

"Shaped TRG", this is a logic signal of programmable width coming out together with the trigger. This is useful when you want to send out a trigger signal, and in the coincidence acquisition mode (refer to **[RD3]**);

"TRG Val. Acceptance Win.", the logic signal corresponding to the time window where the coincidence validation is accepted. The validation enable the event to be written into the memory (see **[RD3]**);

"Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

"Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**);

"None", when both Digital Trace 2 and Digital Trace 3 are set to *None*, the event sample is represented into 10 bits memory location. Otherwise 2 bits are reserved for the Digital Traces 2 and 3, and each sample is represented into 8 bits.

- **"Digital Trace 3" menu:** selects the third digital trace to be plotted:

  For 720 series:

  "External TRG", the external trigger signal when enabled;

  "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

  "Shaped TRG", this is a logic signal of programmable width coming out together with the trigger. This is useful when you want to send out a trigger signal, and in the coincidence acquisition mode (refer to **[RD3]**);

  "TRG Val. Acceptance Win.", the logic signal corresponding to the time window where the coincidence validation is accepted. The validation enable the event to be written into the memory (see **[RD3]**);

  "Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

  "Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**).

  For 751 series:

  "Short Gate";

  "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

  "TRG Validation", digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA(refer to **[RD3]**);

  "TRG HoldOff", digital signal corresponding to the Trigger Hold-Off, with the same width set in the Channel Tab for the Trigger Hold-Off parameter;

  "Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

  "Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**);

  "None", when both Digital Trace 2 and Digital Trace 3 are set to *None*, the event sample is represented into 10 bits memory location. Otherwise 2 bits are reserved for the Digital Traces 2 and 3, and each sample is represented into 8 bits.

- "**Digital Trace 4**" **menu:** selects the fourth digital trace to be plotted (720 series only) among:

  "Short Gate";

  "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

  "TRG Validation", digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA(refer to **[RD3]**);

  "TRG HoldOff", digital signal corresponding to the Trigger Hold-Off, with the same width set in the Channel Tab for the Trigger Hold-Off parameter;

  "Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

  "Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**).

- **"…" button:** opens the Trace Setting window (**Fig. 7.9**) to set the DC offset and the gain of the traces in the Oscilloscope plot. These settings have no effect on the real input signal, but only on the visualization of the Oscilloscope plot. For this reason it is recommended to adjust only the digital traces offset and gain for a correct visualization.

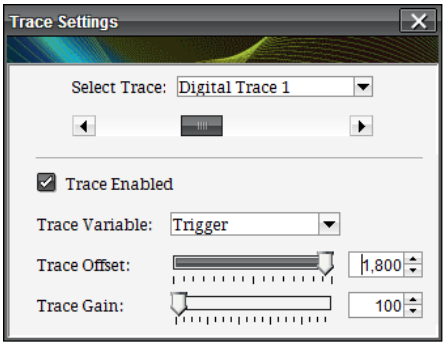


Fig. 7.9: The Trace Settings Window

4. The Tab "Histogram"

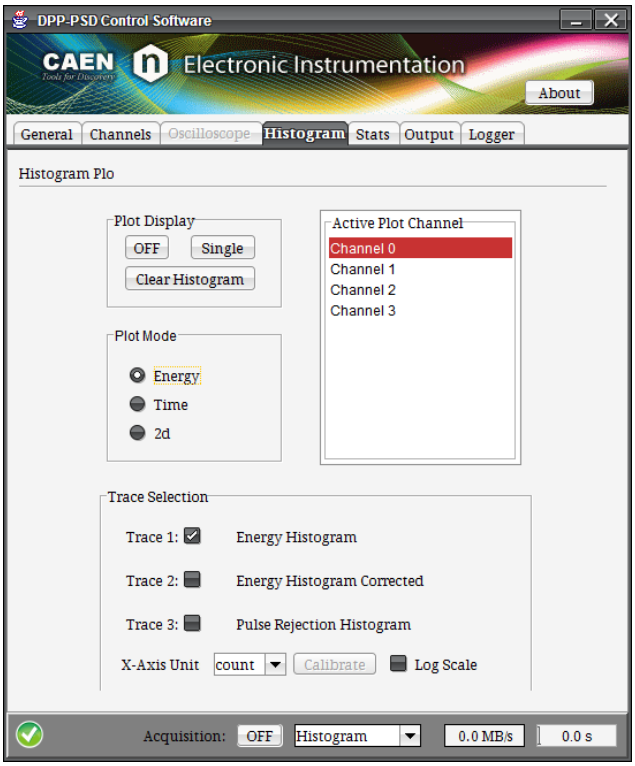


Fig. 7.10: Tab "Histogram"

The **Histogram Tab** contains in the **Histogram Plot** section all functions for plotting the Energy or Time Histograms.

The **Histogram Plot** section includes the following settings:

- **"Plot Display" buttons:** The *"ON/OFF"* button enables/disables the continuous plotting of the histogram. In the OFF position it is possible to update manually the plot by pushing the *"Single"* button. The *"Clear Histogram"* button clears the histogram (i.e. resets the plotting to zero).
- **"Active Plot Channels" menu:** selects the channel whose signals are visualized. Only one channel at a time can be plotted. The selected channel has to be checked in the Tab Channels.
- **"Plot Mode" check cells:** selects if a *"Energy"*, *"Time"* or *"2d"* histogram has to be visualized.
- **"Trace Selection" menu** that includes:

- **"Trace 1":** Energy/Time Histogram when Energy/Time plot mode is enabled. In the Energy Histogram pile-up events are not included. Time Histogram is intended to be the histogram of the time intervals between subsequent triggers;
- **"Trace 2" menu:** for Energy plot mode only, enables/disables the visualization of the Energy Histogram Corrected by adding the redistribution of the pile-up counts (Trace 3) to the Energy Histogram (Trace 1);
- **"Trace 3" menu:** for Energy plot mode only, enables/disables the visualization of the Rejected Pulses Histogram[2]. This is the redistribution of the pile-up counts, within fixed acquisition time windows, with respect to the energy distribution in the same windows;
- **"X-Axis Unit" menu:** for Energy plot mode only, selects the unit of measurement of the Energy x-axis in the histogram between *"ADC Counts"* and *"KeV"*. In order to define a *KeV* scale, the *"Calibrate"* button opens the Energy Calibration window (**Fig. 7.11**) where it is possible to calibrate the spectrum by a dedicated menu: a customized Calibration line can be built here. Different calibration lines are available for the different channels;

Note: The "*KeV*" option affects only the histogram plot, while the histogram x-axis data will be always saved as ADC counts in the Output tab.

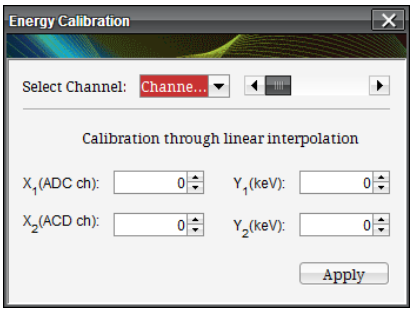


Fig. 7.11: Energy Calibration window

- **"Log Scale" menu:** enables/disables the plot log scale.

[2] Pile up detection is not yet managed by the DPP-PSD Control Software.

5. The Tab “Stats”

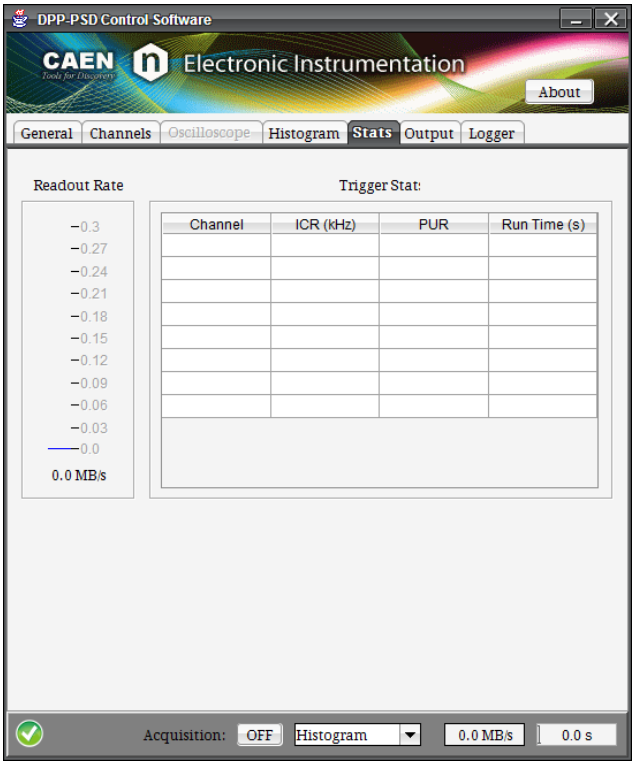


Fig. 7.12: Tab “Stats”

In the **Stats Tab** are summarized most of the important statistic information about every enabled channels. The tab is composed by two sections: **Readout Rate** and **Trigger Stat.**

The **Readout Rate** section hosts:

- **“Readout Rate” display:** shows the data throughput from the board to the computer in MB/s (the same value is visible in the Common Bar).

The **Trigger Stats** section is made by:

“Trigger Stats” table: reports for each enabled channel (*“Channel”*) the real time Incoming Counting Rate (“*ICR”* expressed in kHz), the Pile Up Rejection (“*PUR*” in percentage), and the Run Time (in seconds).

6. The Tab "Output"

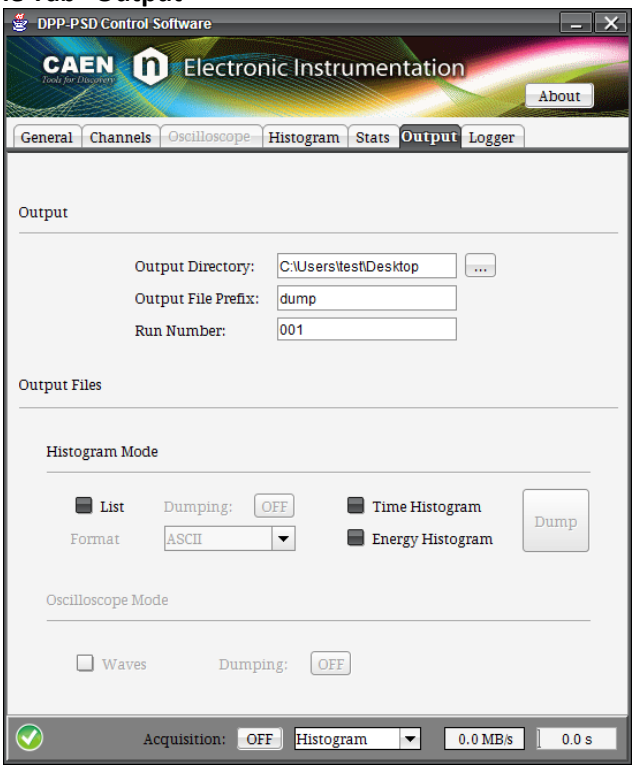


Fig. 7.13: Tab "Output"

In the **Output Tab** there are all the commands to save output files containing spectra, waveforms and lists on a PC. The sections in this tab are **Output** and **Output Files**.

The **Output** section includes the following settings:

- **"Output Directory" box**: contains the destination path for the output files. Directly write the path or inserted it using the "…" button. If no destination is selected, data is saved into the user home folder.
- **"Output File Prefix" box:** contains the prefix for the output file name. If no prefix is chosen, the default one is used.
- **"Run number" box:** contains the run number for the output file. This number automatically increase by one unit when at the start of a new acquisition through the ON/OFF Acquisition button.

  The complete file name will be *Prefix_Run_XY_N.dat,* where:

  XY is "eh" in case of Energy Histogram, "th" in case of Time Histogram, "ls" in case of List and "wf" in case of Waveform, and *N* is the channel number.

Data saving is activated by selecting the options in the **Output Files** section. For the **"Histogram Mode"** there is the possibility to choose among:

- **"List" checkbox:** saves every event in ASCII or BINARY format, according to the list format menu.

  ASCII list format: is a 4-column file where the first column is Trigger Time Tag (in clock units of 4 ns for 720 series and 1 ns for 751 series. Since the Time Stamp is a 32-bit value, there is a roll-over over after 2^{32} * clock_unit ns, i.e. about 17 s for 720 series, and about 4 s for 751 series), the second is the integrated charge Q_{short} (in ADC counts), the third is Q_{long} (in ADC counts), and the fourth is the PSD value (in accordance with the formula in Chapter **2**).

  BINARY list format: the file contains the sequence of the recorded events in the binary format:

  EVENT = |Event|Event|Event|…..|Event|;

  where

  Event = (unsigned 32-bit int) TimeTag|(signed 16-bit) Qlong |(signed 16-bit) Qshort.

Data saving starts/stops by the **DUMPING** "**ON/OFF**" button. Binary writing is particularly efficient for high readout throughput.

- **"Energy Histogram" checkbox:** saves the Energy Histogram data in a 2-column file, where the first column is made of the x-data values (i.e. histogram bins, always ADC counts), and the second is the frequency for each event. Data saving is performed by the **DUMP** button.

Note: The Energy Histogram data refer to Qlong only.

- **"Time Histogram" checkbox:** saves the Time Histogram data in a 2-column file (histogram bins as ADC counts on the first column and frequency values on the second). Data saving is performed by the **DUMP** button.

For the **"Oscilloscope Mode"**, only one option is enabled:

- **"Waves" checkbox:** saves the samples of the digitised waveforms from all the enabled channels. All digital probes that are enabled in the "Oscilloscope Tab" will be saved as well. Data saving starts/stops by the **DUMPING** "**ON/OFF**" button.

Note: Both for *List* and *Waves* dumping, a warning message will appear if you are changing the prefix name while the data saving option is enabled (see **Fig. 7.14**).

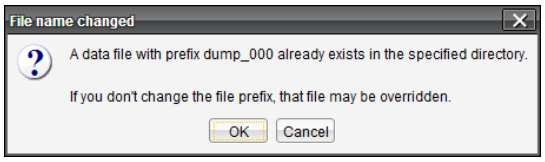


Fig. 7.14: Warning message about data saving .

7. The Tab "Logger"

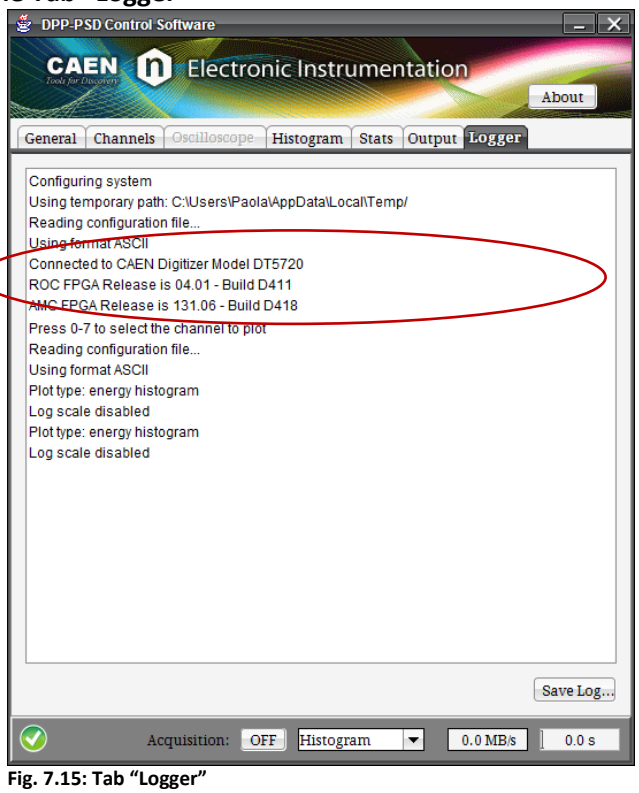


Fig. 7.15: Tab "Logger"

In the **Logger Tab** the user can read board and firmware information (**Fig. 7.15**) and have a direct view of the parameters values and the mode options being set during the current program session. The session log can be saved on disk by using the *"Save Log"* button.

Config File Sintax

The Graphical User Interface (GUI) interacts with the board through a Configuration File which is modified by the GUI itself. Moreover, in the configuration file there are some advanced controls that are not present in the GUI. Acting in the different sections of the Configuration File makes possible to enable/disable/modify these features. In this section there is a brief description of the Configuration File and of the Syntax used.

The Configuration File is a text file called ***DPPRunnerConfig.txt*** generated by the program in a different destination path according to the user.

Here follows some examples of typical paths for different Operating Systems:

Windows: %HomePath%\AppData\Local\DPP-PSD_ControlSoftware\DppRunnerConfig.txt

Where in

- Windows XP: %HomePath% is C:\Documents and Settings\<USER>
- Windows 7: %HomePath% is C:\Users\<USER>

Linux: */home/*<USER>/.DPP-PSD_ControlSoftware/DppRunnerConfig.txt

Note: this is the Configuration file that has to be used for enabling/disabling/modifying the GUI controls.

The safer procedure to modify the Configuration File is:

1. Disconnect the board via GUI
2. Modify the Configuration File
3. Save the Configuration File
4. Connect the board via GUI
5. Start acquisition

The Configuration File is divided in two (2) sections: COMMON and INDIVIDUAL.

Common Settings are listed in the file after the [COMMON] keyword and they are in common to all the channels of the Digitizer.

Individual Settings are the ones related to a single channel of the Digitizer. Each list of individual parameters set for the same channel has to be reported after a [i] keyword, where "i" is the number of the channel section:

```
[0]
ENABLE_INPUT      YES     # setting 1 of channel "0" section
DC_OFFSET         40      # setting 2 of channel "0" section
[1]
ENABLE_INPUT      NO      # setting 1 of channel "1" section
DC_OFFSET         40      # setting 1 of channel "1" section
```

Each parameter not present in the Individual Settings section is intended to assume the value defined in the Common Settings section.

Each command has a description where there are shown the different options to modify it. The commands are textual so it is very easy to modify the different parameters.

Example 1: Enabling the External Trigger with no propagation

Go in the **# EXTERNAL_TRIGGER** section and modify the EXTERNAL TRIGGER line from:

```
EXTERNAL_TRIGGER    DISABLED
```

to

```
EXTERNAL_TRIGGER  ACQUISITION_ONLY
```

In this way the board will be ready to accept an external trigger.

Other commands must be modified with numerical values and, in this case, the units are expressed in the description.

Example 2: Setting the Pre-Trigger value

PRE_TRIGGER: pre trigger size **in number of samples**

options: **1 to 511**

The relative command line will therefore be:

```
PRE_TRIGGER 500
```

In the Configuration File is even possible to manually modify the registers of the board within the Write Register section. For more details about the registers refer to the specific x720 User Manual.

A copy of the Configuration File can be found in the "data" folder of the program and it is called ***DPPRunnerConfigDefault.txt***. This file contains the default values for all parameters and it is read by the GUI when the **Restore** button is pushed.

At the same destination path of the ***DPPRunnerConfig.txt***, another file is generated by the program, that is the ***GuiConfig.txt***: this contains the structure definition of the GUI (not to be modified by the user) and a section with the trace parameters shown in **Fig. 7.9** (Trace Offset and Trace Gain).

Notes on Firmware and Licensing

The DPSD supports the DPP-PSD Firmware for the 720 and the 751 series of CAEN digitizers. When running the DPP-PSD Control Software, the program checks the loaded firmware in the target Digitizer and pops up a warning message if no licensed version is found (**Fig. 7.16**).

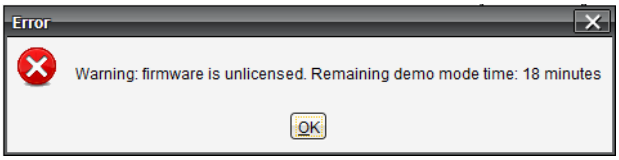


Fig. 7.16: Firmware unlicensed warning message

The DPP-PSD Firmware is unlocked by purchasing a license from CAEN. The licensing procedure is detailed in **[RD1]** and makes use of CAENUpgrader software to finalize the unlocking. This program can also upgrade the DPP-PSD by loading new firmware versions on the digitizer.

Note: Download CAENUpgrader full installation package on CAEN web site at the Digitizer Tools area. Refer to **[RD1]** for detailed information and instructions on how to use it.

8 Specifications

The following tables contain the main specifications about the hardware, the firmware, and the software components of DPSD 720 and 751 series. For more details, please refer to the User Manual of each specific board.

x720 Specifications

PACKAGE		
DT5720B/DT5720C/DT5720D/DT5720E		Desktop module: 154 x 50 x 164 mm³ (WxHxD). Weight: 680 gr
N6720B/N6720C/N6720D/N6720E		1 Unit NIM module
V1720E/VX1720E/V1720F/VX1720F/V1720G		1 Unit wide VME 6U module
Nr. OF INPUT CHANNELS		
DT5720B/DT5720D/N6720B/N6720D		4 channels
DT5720C/DT5720E/N6720C/N6720E		2 channels
V1720E/VX1720E/V1720F/VX1720F/ V1720G		8 channels
ANALOG INPUT		
Dynamic Range	**DT5720B/DT5720C/DT5720D/DT5720E/N6720B/N6720C/N6720D/N6720E/V1720E/VX1720E/V1720G:** 2 Vpp, single ended **V1720F/VX1720F:** 2 Vpp, differential	
Connector Type	**DT5720B/DT5720C/DT5720D/DT5720E/N6720B/N6720C/N6720D/N6720E/V1720E/VX1720E/V1720G:** MCX, Zin=50 Ω (2.25 / 0.5 Vpp), Zin=1 kΩ (10 Vpp) **V1720F/VX1720F:** AMP MODU II, differential, Zin=100 Ω	
DC Offset	**DT5720B/DT5720C/N6720B/N6720C/V1720E/VX1720E/V1720G:** adjustable in the single ended ranges ±1 Vpp	
DIGITAL CONVERSION		
Resolution		12 bit
Sampling Rate		250 MS/s simultaneously on each channels
Bandwidth		125 MHz
ENOB		10.14 (64 kS Buffer)
AMC FPGA		
DT5720B/DT5720C/DT5720D/DT5720E/ N6720B/N6720C/N6720D/N6720E/ V1720E/VX1720E/V1720F/VX1720F/V1720G: Altera Cyclone EP1C20		
I/O PORTS		
TRG-IN		External trigger input: NIM/TTL, Zin=50 Ω. LEMO connector
GPI/S-IN		Programmable input: NIM/TTL, Zin=50 Ω. LEMO connector
GPO/TRG-OUT		Programmable output: NIM/TTL across 50 Ω. LEMO connector
CLK-IN		AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML. AMP MODU II connector, Zdiff=110 Ω
CLK-OUT		Clock output: DC coupled (LVDS), Zdiff = 110 Ω. AMP MODU II connector.
Digital I/Os		N.16 programmable differential LVDS I/O signals, Zdiff_in = 110 Ohm. Four Indipendent signal group 0÷3, 4÷7, 8÷11, 12÷15, In / Out direction control. 34-pin Header Connector
COMMUNICATION INTERFACES		
VME		VME64X compliant; D32 – BLT32 – MBLT64 – CBLT32/64 – 2eVME – 2eSST data modes; Multi Cast Cycles
USB		USB2.0 and USB1.1 compliant; up to 30 MB/s transfer rate
Optical Link		CONET protocol: CAEN proprietary optical link controlled by A2818 PCI or A3818 PCIe cards with a transfer rate up to 100 MB/s. Optical Daisy chain let 8 boards (A2818) up to 32 (A3818) to be managed by a single Controller
TRIGGER		
Trigger Source		**Auto:** each channel can detect the input pulse according to a programmable threshold and generates a trigger on it **Global:** a trigger common to all the channels **Individual:** a trigger related to a specific channel **Software:** a trigger generated by software (acts as global)
Trigger Propagation		Trigger can be propagated out through GPO (in Desktop and NIM modules) or TRG-OUT and LVDS I/Os (in VME modules) to other boards, and it can be feed in through TRG-IN (in all modules) or LVDS I/Os (VME only)

POWER REQUIREMENTS	
DT5720B/DT5720C/DT5720D/DT5720E	Power input: +12 ± 10% Vdc
N6720B/N6720C/N6720D/N6720E	Power consumptions: 2.9 A @ +6 Vdc, 90 mA @ -6 Vdc
V1720E/VX1720E/V1720F/VX1720F/V1720G	Power consumptions: 4.0 A @ +5 Vdc, 0.2 A @ +12 V, 0.2 A @ -12 V

Tab. 8.1: x720 Specifications Table

x751 Specifications

PACKAGE	
DT5751	Desktop module: 154 x 50 x 164 mm³ (WxHxD). Weight: 680 gr
N6751/N6751C	1 Unit NIM module
V1751/V1751B/V1751C/VX1751/ VX1751B/VX1751C	1 Unit wide VME 6U module
Nr. OF INPUT CHANNELS	
DT5751	2/4 channels (4 channels if running the DPP-PSD firmware)
N6751/N6751C	2/4 channels (4 channels if running the DPP-PSD firmware)
V1751/V1751B/V1751C/VX1751/ VX1751B/VX1751C	4/8 channels (8 channels if running the DPP-PSD firmware)
ANALOG INPUT	
Dynamic Range	**DT5751/N6751/N6751C/V1751/V1751C/VX1751/VX1751C:** 1 Vpp, single ended **V1720B/VX1720B:** Vpp, differential
Connector Type	**DT5751/N6751/N6751C/V1751/V1751B/V1751C/VX1751/V1751B/ VX1751C:** MCX, Zin=50 Ω (single ended); AMP MODU II, Zin = 100 Ω (differential)
DC Offset	**DT5751/N6751/N6751C/V1751/V1751C/VX1751/VX1751C:** adjustable in the single ended ranges ±0.5 Vpp
DIGITAL CONVERSION	
Resolution	10 bit
Sampling Rate	1 or 2 GS/s (1 GS/s for digitizers running the DP-PSD firmware)
Bandwidth	500 MHz
ENOB	9.04 (56 kS Buffer)
AMC FPGA	
DT5751/N6751/N6751C/V1751/V1751B/V15ì751C/VX1751/ VX1751B/VX1751C: Altera Cyclone EP3C16	
I/O PORTS	
TRG-IN	External trigger input: NIM/TTL, Zin=50 Ω. LEMO connector
GPI/S-IN	Programmable input: NIM/TTL, Zin=50 Ω. LEMO connector
GPO/TRG-OUT	Programmable output: NIM/TTL across 50 Ω. LEMO connector
CLK-IN	AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML. AMP MODU II connector, Zdiff=110 Ω
CLK-OUT	Clock output: DC coupled (LVDS), Zdiff = 110 Ω. AMP MODU II connector.
Digital I/Os	N.16 programmable differential LVDS I/O signals, Zdiff_in = 110 Ohm. Four Indipendent signal group 0÷3, 4÷7, 8÷11, 12÷15, In / Out direction control. 34-pin Header Connector
COMMUNICATION INTERFACES	
VME	VME64X compliant; D32 – BLT32 – MBLT64 – CBLT32/64 – 2eVME – 2eSST data modes; Multi Cast Cycles
USB	USB2.0 and USB1.1 compliant; up to 30 MB/s transfer rate
Optical Link	CONET protocol: CAEN proprietary optical link controlled by A2818 PCI or A3818 PCIe cards with a transfer rate up to 100 MB/s. Optical Daisy chain let 8 boards (A2818) up to 32 (A3818) to be managed by a single Controller
TRIGGER	
Trigger Source	**Auto:** each channel can detect the input pulse according to a programmable threshold and generates a trigger on it **Global:** a trigger common to all the channels **Individual:** a trigger related to a specific channel **Software:** a trigger generated by software (acts as global)

Trigger Propagation	Trigger can be propagated out through GPO (in Desktop and NIM modules) or TRG-OUT and LVDS I/Os (in VME modules) to other boards, and it can be feed in through TRG-IN (in all modules) or LVDS I/Os (VME only)
POWER REQUIREMENTS	
DT5751	Power input: +12 ± 10% Vdc
N6751/N6751C	-
V1751/V1751B/V1751C/VX1751/ VX1751B/VX1751C	Power consumptions: 6.5 A @ +5 Vdc, 0.2 A @ +12 V, 0.3 A @ -12 V **NOTE:** VME module cannot operate with CAEN crates VME8001/8002 (weak cooling air flow)

Tab. 8.2: x751 Specifications Table

Firmware Specifications

DIGITAL PROCESSING	
Firmware	Digital Pulse Processing for Pulse Shape Discrimination (**DPP-PSD**)
Algorithms	Charge integration (on the short and long component of the input pulses); Time stamp calculation.
Digital controls	**Pulse Polarity Inversion:** allows positive input pulses to be processed by the internal algorithm
	Record Length: • max value 32760 samples (i.e. CUST. SIZE = 4095) for 720 series • max value 786420 samples (i.e. CUST.SIZE = 65535) for 751 series
	Trigger Threshold: • max value 4095 LSB for 720 series • max value 1023 LSB for 751 series
	Gate Offset: • 0 up to Pre-Trigger – 32 ns of reliable range for 720 series • 0 up to 255 ns for 751 series
	Short Gate: Gate Offset value up to Long Gate value of reliable range for the Qshort integration window width
	Long Gate: Qlong integration window width • Short Gate value up to 4095 samples of reliable range for the 720 series • Short Gate value up to 1023 samples of reliable range for the 720 series
	Baseline Mean: • 4 - 8 - 16 - 32 - 64 - 128 allowed values for 720 series • 0 - 8 - 16 - 32 - 64 - 128 - 256 - 512 allowed values for 751 series
	Baseline Threshold: max value 4095 LSB
	Pre-Trigger: • Gate Offset + 16 ns up to 1 us of reliable range for 720 series • -1023 up to +1023 for 751 series (the DPP-PSD Control Software doesn't manage negative values)
	Charge Sensitivity: • 40 - 160 - 640 - 2560 fC/LSB allowed values for 720 series • 20 - 40 - 80 - 160 - 320 - 640 fC/LSB allowed values for 751 series
Pile-up	*To be implemented*
Coincidences	On-line coincidences detection. The board recognizes and saves the events occurring inside a programmable time window.
Dead Time	No dead time due to conversion
ICR	5 Mcps (in List Mode with one channel enabled) or higher
Acquisition Modes	**Oscilloscope:** a portion of waveform (analog and digital signals) is saved into the board memory **List:** only the parameters calculated by the algorithms are saved into the board memory (i.e. charge and time stamp) **Mixed:** charge, time stamp and a reduced portion of waveform is saved in to the board memory **NOTE:** mixed mode is not managed by the DPP-PSD Control Software

Tab. 8.3: Firmware Specifications Table

Software Specifications

SOFTWARE	
Control Interface	**DPP-PSD Control Software** for configuration, acquisition, plotting, saving data
Histograms	Three histograms built by the software: • **Energy histogram:** histogram of the energy (i.e. charge Qlong) distribution • **Time histogram:** histogram of the pulse timing distribution (Δt between pulses) • **2D Plot:** histogram of the counts as function of the pulse Energy and the PSD parameter
Operating Modes	**Oscilloscope Mode:** monitoring of input waveforms and internal filters digital output signals **Histogram Mode:** histogram representation of energy, pulse timing distributions, and energy vs PSD.
PUR Management	*To be implemented*
Coincidence Management	The Control Software manage a file where the user can write all the required coincidence settings.
Plotting	**For 720 series:** up to 6 traces simultaneously selectable per input channel in Oscilloscope Mode, that are 2 analog signals (using Dual Trace option) and 4 digital signals. **For 751 series:** up to 5 traces simultaneously selectable per input channel in Oscilloscope Mode, that are 2 analog signals (using Dual Trace option) and 3 digital signals Energy and Time histogram options, as well as 2D-Plot selectable per input channel in Histogram Mode. **NOTE:** only one channel at a time can be plotted both in Oscilloscope and in Histogram Mode
Saving Options	**Energy histograms** **Lists** (i.e. charges Qshort and Qlong, PSD parameter & time stamp events) **Waveforms** (analog and digital signals) **Time histogram** **2D-Plot (***to be implemented***)**
Libraries	For users who wants to develop their own software, CAEN provides a high-level library to configure the hardware, handle the acquisition and retrieve the acquired data (in form of energy histograms). See **[RD8]**

Tab. 8.4: Software Specifications Table

9 Technical support

CAEN makes available the technical support of its specialists at the e-mail addresses below:

- support.nuclear@caen.it
  (for questions about the hardware)
- support.computing@caen.it
  (for questions about software and libraries)

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